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LHC Project Report 258

RST Digital Algorithm for Controlling the LHC Magnet Current

F. Bordry, H. Thiesen

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The LHC will require a very high precision (a few ppm) in the control of the current (13 kA) in the main superconducting magnets. To achieve this challenging performance, several developments are made at CERN in the domain of DC current transducers, analogue to digital conversion and digital control loops. This paper will focus on the presentation of a robust digital algorithm. Simulation and prototype (2.4 kA) results will be presented.

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RST Digital Algorithm for Controlling the LHC Magnet Current

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Abstract

The LHC will require a very high precision (a few ppm) in the control of the current (13 kA) in the main superconducting magnets. To achieve this challenging performance, several developments are made at CERN in the domain of DC current transducers, analogue to digital conversion and digital control loops. This paper will focus on the presentation of a robust digital algorithm. Simulation and prototype (2.4 kA) results will be presented.

INTRODUCTION

The LHC machine is divided in eight independent sectors [1]. In each sector, individual power converters will power the main dipole and quadrupole (focussing and defocussing) magnets; a total of 24 principal power converters are needed.

Switch-mode techniques will be used for the converters. Due to this technology, the voltage loop of the converters will have a high bandwidth (>1 kHz).

To achieve the required performance for the current loop, digital control was chosen [2]. The basic structure of a digital loop is shown in Fig. 1.

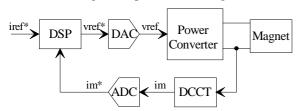


Fig. 1: Power Converter Digital Loop

The developments on the high precision DC transducers (DCCT) and the 20 bits ADC are described in [2] and [3]. In this paper, the digital algorithm to be implemented in the DSP will be described and discussed.

The LHC magnets operate at a maximum current level of 13kA and the electrical circuits have very large time-constants (dipole time-constant is 23'000 seconds and quadrupole time-constant is 450 seconds).

The digital algorithm must handle these large timeconstants and should be robust to the load parameter variations. Furthermore the loop response must be non-overshooting and identical for each magnetic circuit (dynamic and tracking errors). The LHC cycle is shown in Fig 2.

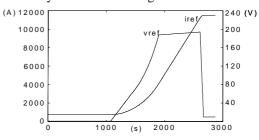
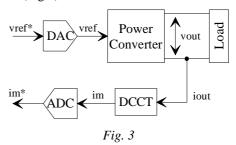


Fig. 2: LHC cycle

SYSTEM MODEL

The system consists of a voltage-regulated power converter (PC) feeding a string of superconducting magnets (Fig 3).



Power converter model

The LHC converters have a soft-switching topology using an intermediate high frequency stage [4].

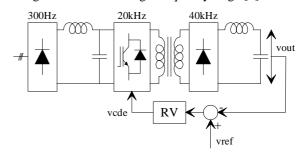


Fig. 4: Power Converter Topology

Due to the high frequency of the intermediate stage, the bandwidth of the voltage loop can be higher than 1kHz. The power converter with the voltage loop can be modelled by a second order system with two complex poles (damping factor between 0.7 and 1) and a natural frequency close to the output passive filter frequency.

$$\frac{Vout(s)}{Vref(s)} = \frac{Gpc}{1 + \frac{2\xi pc}{\omega pc} \cdot s + \frac{s^2}{\omega pc^2}}$$
(1)

with:
$$\begin{cases} 0.7 \le \xi pc \le 1 \\ 2\pi \cdot 1kHz \le \omega pc \le 2\pi \cdot 2kHz \end{cases}$$

Model of the magnet string

The magnet strings consist of several superconducting magnets in series (154 for the main dipoles and 23 for the main quadrupoles). The cables between the converter and the magnet string provide the resistance of the load.

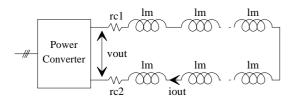


Fig. 5: Magnet string model

The load is a first order system with a high timeconstant and high static gain:

$$\frac{Iout(s)}{Vout(s)} = \frac{\frac{1}{(rc\ 1 + rc\ 2)}}{1 + \frac{\sum lm}{(rc\ 1 + rc\ 2)} \cdot s} = \frac{Gm}{1 + \tau m \cdot s}$$
(2)

with:
$$\begin{cases} 450 \ s \le \tau m \le 23000 \ s \\ 1000 \ \le Gm \ \le 2000 \end{cases}$$

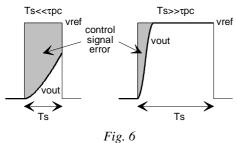
System model for the digital current loop

The system model is:

$$\frac{Im(s)}{Vref(s)} = \frac{Gpc \cdot Gm \cdot G_{DCCT}}{\left(1 + \tau m \cdot s \left(1 + \frac{2\xi pc}{\omega pc} \cdot s + \frac{s^2}{\omega pc^2}\right)\right)}$$
(3)

The current transducer (DCCT) is modelled by a pure gain (TDCCT<<tpc).

Contrary to analogue control, the design of a digital control must take into account the power converter time constant, even if this time-constant is very high in comparison with the load time-constant, since the converter has to transmit accurately the reference voltage. The sampling period (Ts) must be high in comparison with the converter time-constant: $Ts>>\tau pc=1/\omega pc$.



With this hypothesis:

$$\frac{Im(s)}{Vref(s)} = \frac{Gpc \cdot Gm \cdot G_{DCCT}}{1 + \tau m \cdot s} = \frac{G}{1 + \tau m \cdot s}$$
(4)

Then:

$$\frac{Im *}{Vref *} = \frac{G\left(1 - e^{-Ts / \tau m}\right)z^{-1}}{1 - e^{-Ts / \tau m} \cdot z^{-1}}$$
 (5)

Furthermore, due to the high time-constant of the magnet in relation with the sampling period $(\tau m>1000.Ts)$ the equation (5) becomes:

$$\frac{Im *}{Vref *} = \frac{G \cdot Ts / \tau m \cdot z^{-1}}{1 - z^{-1}} = \frac{z^{-1} \cdot B(z^{-1})}{A(z^{-1})}$$
 (6)

With the preceding assumptions, the system (power converter and magnet) can be considered, by the digital control, as a pure integrator (tpc<<Ts<<tm).

DIGITAL ALGORITHM

The general structure of a digital controller can be described by the following discrete equation (tribranched structure known as R-S-T structure) [5]:

$$S(z^{-1})vref*(k) = T(z^{-1})iref*(k)$$

$$-R(z^{-1})im*(k)$$
(7)

where R, S and T are z⁻¹ polynomials.

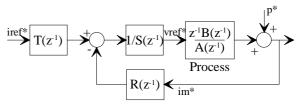


Fig. 7: RST controller

The tracking transfer function is:

$$\frac{Im *}{Iref *} = \frac{z^{-1} \cdot B \cdot T}{A \cdot S + R \cdot B \cdot z^{-1}}$$
 (8)

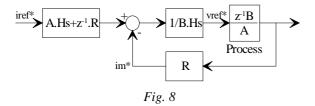
and the regulation transfer function.

$$\frac{Im *}{p *} = \frac{A \cdot S}{A \cdot S + R \cdot B \cdot z^{-1}} \tag{9}$$

The RST controller makes it possible to obtain the desired tracking behaviour (following the reference) independent of the desired regulation behaviour (rejection of a disturbance). This strategy can only be applied to discrete-time models with stable zeroes (known as minimum phase systems). The RST control can be evaluated by the "Tracking and Regulation with Independent Objectives" method (R and S give the regulation behaviour and T gives the tracking behaviour).

In this case:

$$\begin{cases} S = B \cdot Hs \\ T = A \cdot Hs + z^{-l} \cdot R \end{cases}$$
 (10)



Then, the transfer functions become:

$$\frac{Im^*}{Iref^*} = z^{-1} \tag{11}$$

$$\frac{Im^*}{p^*} = \frac{A \cdot Hs}{A \cdot Hs + R \cdot z^{-1}} \tag{12}$$

The regulation dynamics is defined by the R and Hs polynomials. The tracking dynamics is obtained by placing the desired transfer function between the reference and the T polynomial.

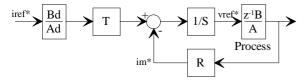


Fig. 9: Tracking and regulation with independent objectives

With some block manipulations, it can be demonstrated that the precedent diagram is equivalent to the diagram shown in Fig 10. That is to say a regulation control with a feed-forward action.

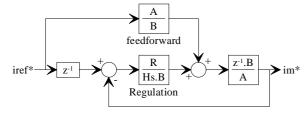


Fig. 10

As already said, this method can only be applied to discrete-time models with stable zeroes. Unstable zeroes may appear as a result of a too small sampling period for continuous-time systems with a difference in degree greater than 2 between the numerator and the denominator of the transfer function (3) [6].

RST CONTROLLER DESIGN

Tracking

To obtain good tracking of the reference (no lagging error, no overshoot), the transfer function that the controller must achieve between the reference iref* and the output im* is:

$$\frac{im*}{iref*} = z^{-1} \tag{13}$$

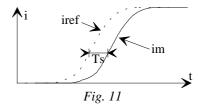
Regulation

According to the LHC cycle, the bandwidth for the closed-loop system is chosen fcl \in [0.1 Hz, 1 Hz]. The regulation is defined by the pole placement with a natural frequency ∞ cl \in [0.628rad/s, 6.28rad/s] and with a damping factor greater than 1. To ensure a zero steady-state error when the reference is constant, the transfer function $1/S(z^{-1})$ must contain an integrator.

Sampling frequency

The sampling frequency for digital control is chosen according to the bandwidth for the closed-loop system fcl. The rule used to choose the sampling frequency in control systems is the following [5]: $fs \in [6 \text{ fcl}, 25 \text{ fcl}]$. A sampling frequency of 20Hz was chosen.

To avoid a lag equal to the sampling period, the reference iref is shifted by one sampling period (-Ts).



SIMULATION

To evaluate the synthesis and the performance of the RST controller, a digital simulation has been performed using MATLAB® software (Fig. 12)

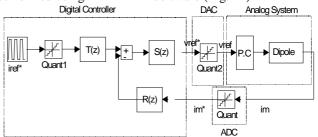


Fig. 12

The converter is modelled by a 2^{nd} order linear transfer function with a static gain Gpc = 40, a damping factor $\xi pc = 0.7$ and a natural frequency $\omega pc = 6280 rad/s$:

$$\frac{Vout(s)}{Vref(s)} = \frac{40}{1 + \frac{2 \cdot 0.7}{6280} \cdot s + \frac{s^2}{6280^2}}$$
 (14)

The model for the other parts is:

- DCCT by a gain: GDCCT = 1
- ADC by a 20bits quantizer
- DAC by a 16bits quantizer
- the load by a resistance (cables) $rm = 0.8 \text{ m}\Omega$ and an inductance (magnet string) Lm = 18H:

$$\frac{Im(s)}{Vout(s)} = \frac{1250}{1 + 23000 \cdot s}$$
 (15)

The RST controller is defined with the following design parameters (fs = 20Hz, ω cl = 6.28rads-1, ξ cl=1):

$$\begin{cases} R(z^{-1}) = 0.54142 - 0.47126 \cdot z^{-1} + 0.00246 \cdot z^{-2} \\ S(z^{-1}) = 0.10078 - 0.08350 \cdot z^{-1} + 0.01731 \cdot z^{-2} \\ T(z^{-1}) = 1 - 1.46104 \cdot z^{-1} + 0.53366 \cdot z^{-2} \end{cases}$$
(16)

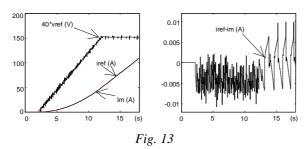


Fig. 13 presents the start of the acceleration phase for the main dipole string for LHC one octant (Lm = 18H, τ m = 23000 s). To test the robustness of the RST controller, parameter errors are introduced (-10% on Lm and +20% on rm). In spite of large parameter errors the current tracking error is less than 1ppm (13 mA).

PROTOTYPE RESULTS

Several tests were performed on a large power converter [2400 A, \pm 100 V] connected to magnets with Lm = 60 mH and rm = 0.1 Ω .

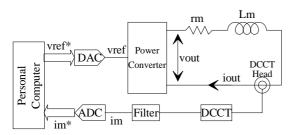


Fig. 14

The converter is a 6-pulse SCR converter with an active filter. The static gain is Gpc = 20 (100 V/5 V), and the bandwidth $\omega pc = 31400 \text{ rads}^{-1} (5 \text{ kHz})$.

A 16 bit ADC was used to acquire the DCCT measurement (resolution: 73 mA = (GDCCT*20V/ 2^{16}); the intrinsic noise was \pm 0.14 A (\pm 2*LSB). A 200 Hz anti-aliasing filter was placed between the DCCT and the acquisition board.

The RST controller was implemented on a standard 150 MHz Pentium PC:

$$\begin{cases} R(z^{-1}) = -0.11003 + 0.71734 \cdot z^{-1} - 0.53469 \cdot z^{-2} \\ S(z^{-1}) = -9.81451 + 1.03170 \cdot z^{-1} - 0.03170 \cdot z^{-2} \end{cases}$$
(17)
$$T(z^{-1}) = 1 + 1.46104 \cdot z^{-1} - 0.53366 \cdot z^{-2}$$

In open loop, the noise on the current measurement has a 50 Hz harmonic of 0.5 A. This is not a problem since the current loop bandwidth is around 1 Hz. The sampling frequency is 20 Hz but the current measurement is over-sampled and digital filters are used.

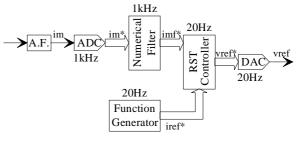
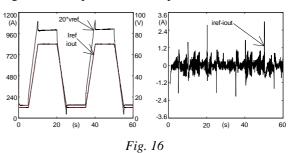
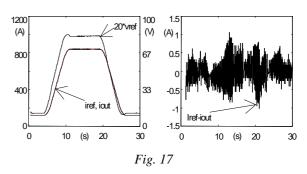


Fig. 15

Fig. 16 and 17 present some experimental results.





The error spikes on the Fig. 16 b are due to the high dv/dt of the reference input to the converter. These spikes disappeared once the discontinuity on *vref*, was removed (Fig. 17 b).

The current error can be seen to be less than the present 0.5 A noise on the measurement system. The output current transducer mainly produces this noise.

CONCLUSION

As a result of the tests completed to date, the digital loop using RST controller seems to fulfil all the performance requirements of the LHC (no overshoot, static or lagging error below 1ppm). The robustness of the algorithm avoids the use of more complex adaptive control.

The next step is to implement these algorithms in a full-scale test with a less noisy current transducer.

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