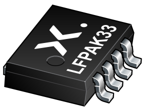


PSMN8R5-40MSD

N-channel 40 V, 8.5 mΩ, standard level MOSFET in LFPAK33 using NextPower-S3 technology

10 February 2020 | Product data sheet

1. General description

60 A, standard level N-channel enhancement mode MOSFET in 175 °C LFPAK33 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high efficiency applications at high switching frequencies.

2. Features and benefits

- Avalanche rated, 100% tested
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low Q_{RR}, Q_G and Q_{GD} for high system efficiency, especially at high switching frequencies
- Low spiking and ringing for low EMI designs
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Brushless DC motor drive
- LED lighting

4. Quick reference data

Table 1. Quick reference data

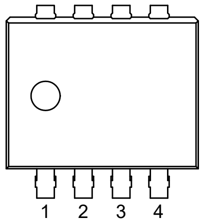
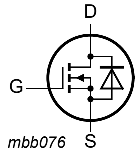
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	60	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	59	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; Fig. 10		-	7.4	8.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 15 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 12; Fig. 13		0.6	2	4	nC
$Q_{G(tot)}$	total gate charge			9	13.4	19	nC

[1] 60A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R5-40MSD	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R5-40MSD	8D5S40

8. Limiting values

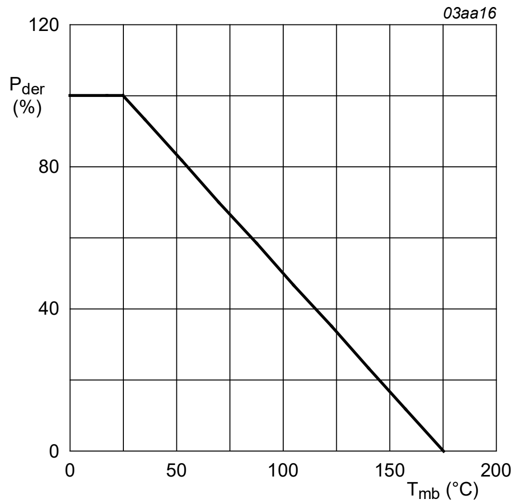
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{DSM}	peak drain-source voltage	t_p ≤ 20 ns; f ≤ 500 kHz; $E_{DS(AL)}$ ≤ 200 nJ; pulsed		-	45	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	59	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	60	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	42	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	239	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	59	A

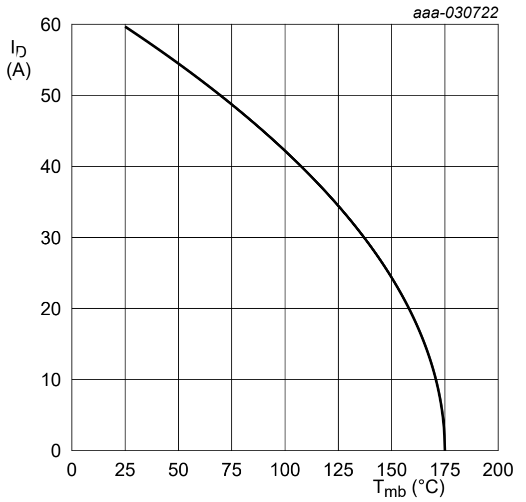
Symbol	Parameter	Conditions		Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	239	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 22 A; $V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 80 µs	[2]	-	46	mJ
		I_D = 15 A; $V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 180 µs	[2]	-	70	mJ

[1] 60A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test



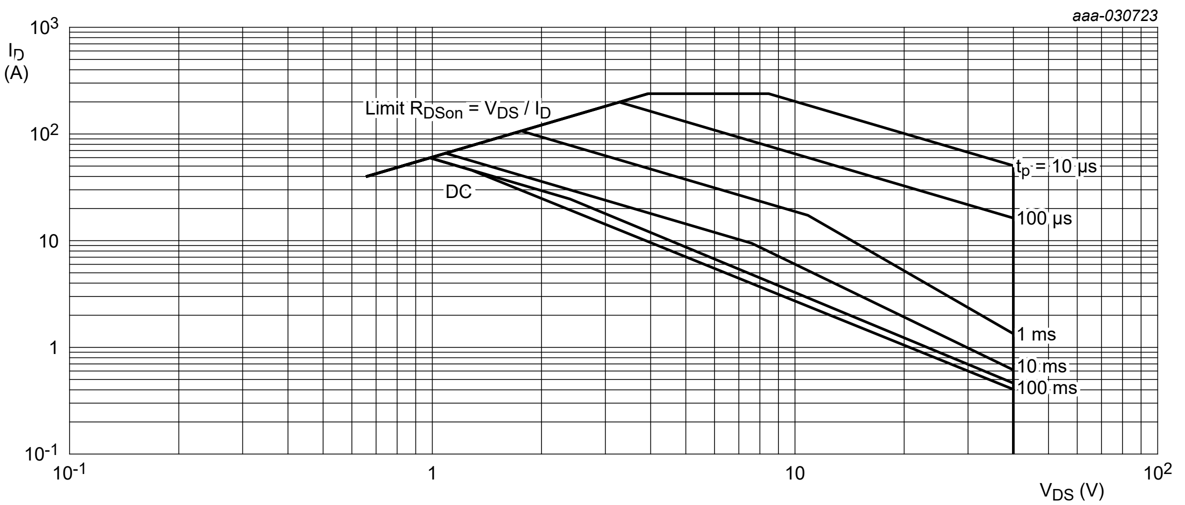
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq$ 10 V
(1) 60A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	2.33	2.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	50	-	K/W
		Fig. 6		-	130	-	K/W

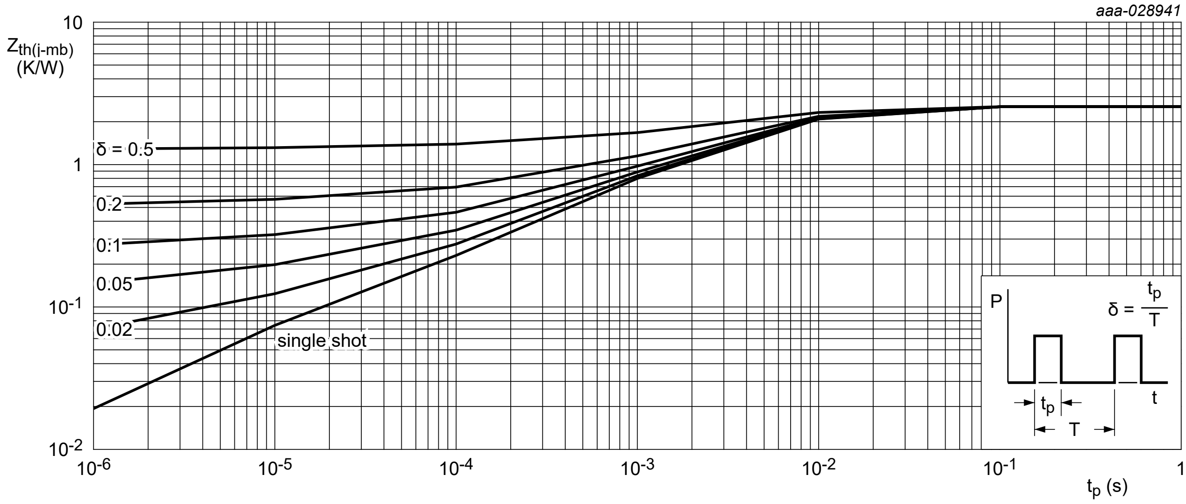
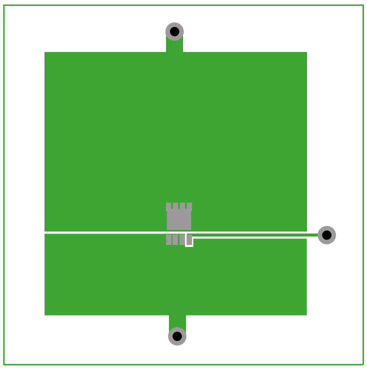
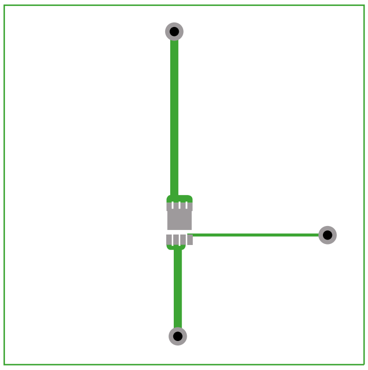


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration



Copper area 25.4 mm x 25.4 mm; 70 µm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 µm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

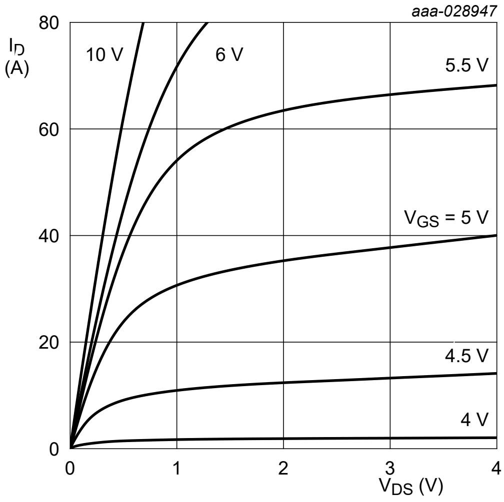
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V

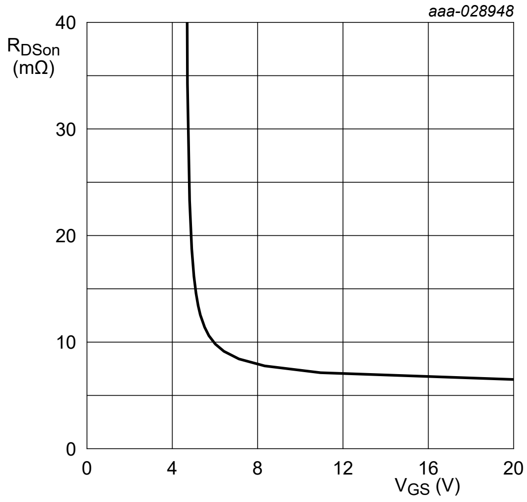
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2.4	3.12	3.6	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-5.9	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	1	µA
		V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125 °C		-	1	-	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; Fig. 10		-	7.4	8.5	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 175 °C; Fig. 11		-	-	16.5	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.3	0.8	2	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 12; Fig. 13		9	13.4	19	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	8.8	-	nC
Q_{GS}	gate-source charge	I_D = 15 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 12; Fig. 13		2.7	4.5	6.8	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			1.7	2.9	4.4	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			1	1.7	2.6	nC
Q_{GD}	gate-drain charge			0.6	2	4	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 15 A; V_{DS} = 20 V; Fig. 12; Fig. 13		-	4.7	-	V
C_{iss}	input capacitance	V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		614	944	1322	pF
C_{oss}	output capacitance			266	409	573	pF
C_{rss}	reverse transfer capacitance			13	44	97	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	5.1	-	ns
t_r	rise time			-	3.2	-	ns
$t_{d(off)}$	turn-off delay time			-	8.9	-	ns
t_f	fall time			-	2.8	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz; T_j = 25 °C		-	12	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.85	1	V
t_{rr}	reverse recovery time	I_S = 15 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 16		-	22	-	ns
Q_r	recovered charge		[1]	-	15	-	nC
t_a	reverse recovery rise time			-	14	-	ns
t_b	reverse recovery fall time			-	8.5	-	ns

[1] includes capacitive recovery



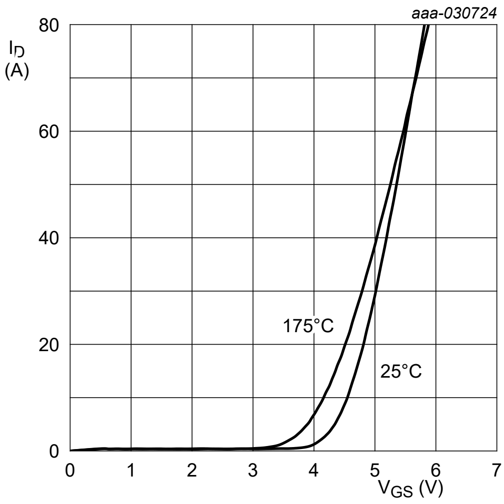
T_j = 25 °C

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values



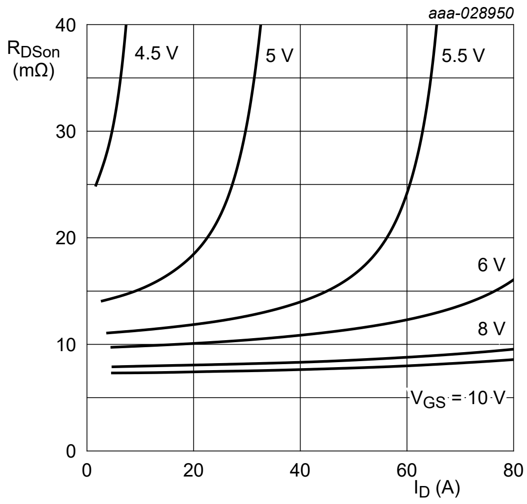
T_j = 25 °C; I_D = 15 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



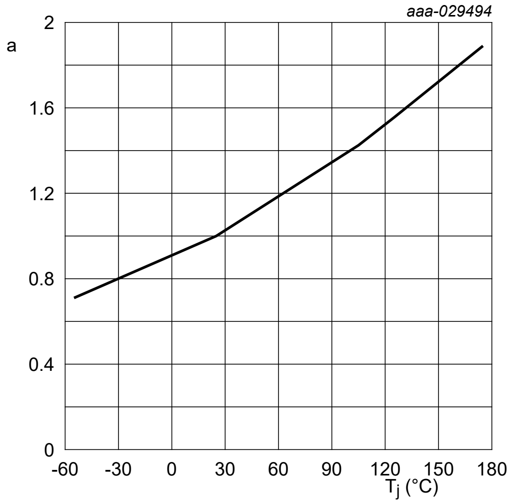
V_{DS} = 8 V

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



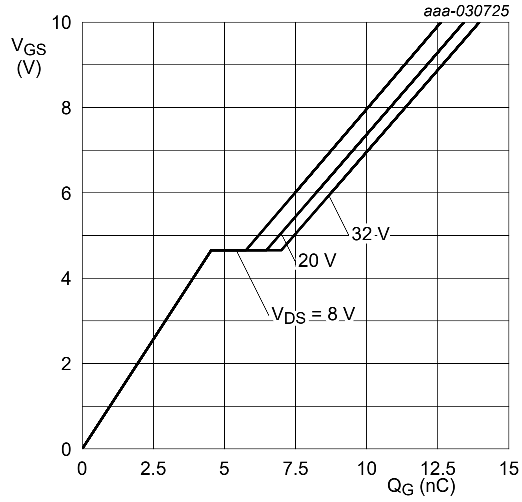
T_j = 25 °C

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 15 A

Fig. 12. Gate-source voltage as a function of gate charge; typical values

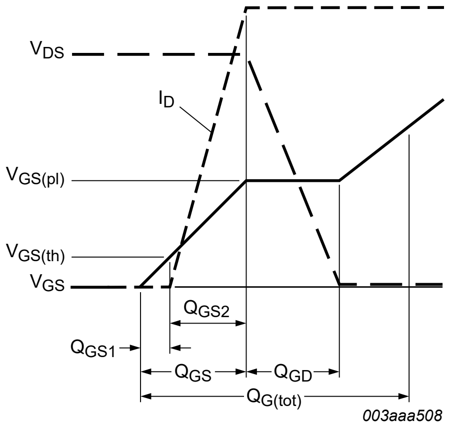
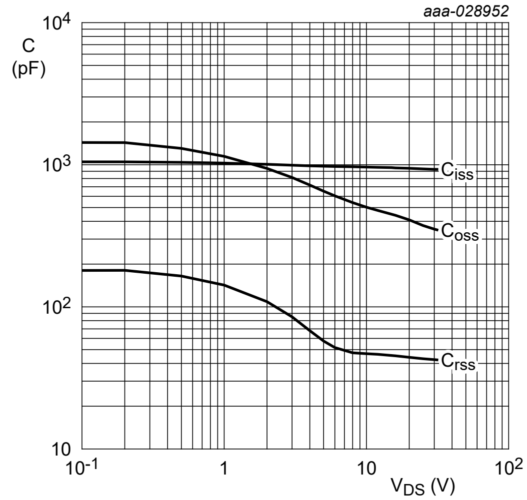
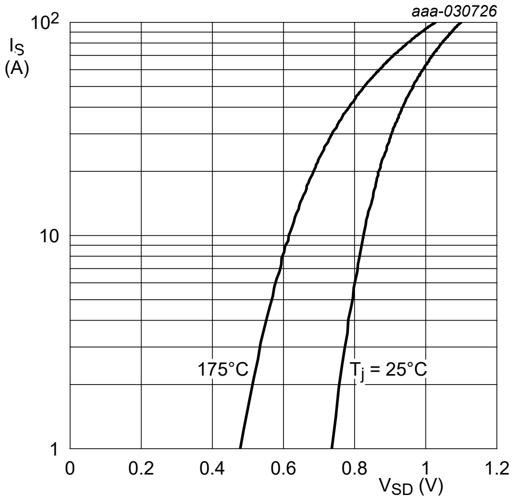


Fig. 13. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

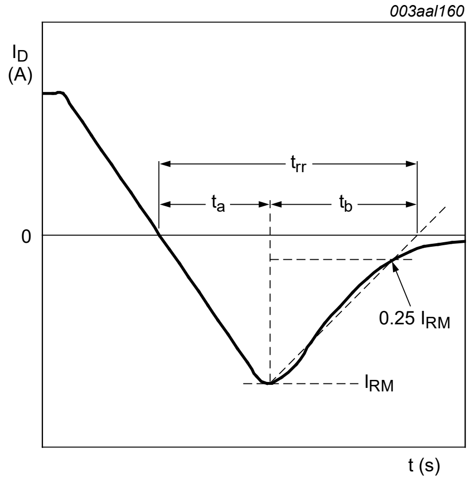
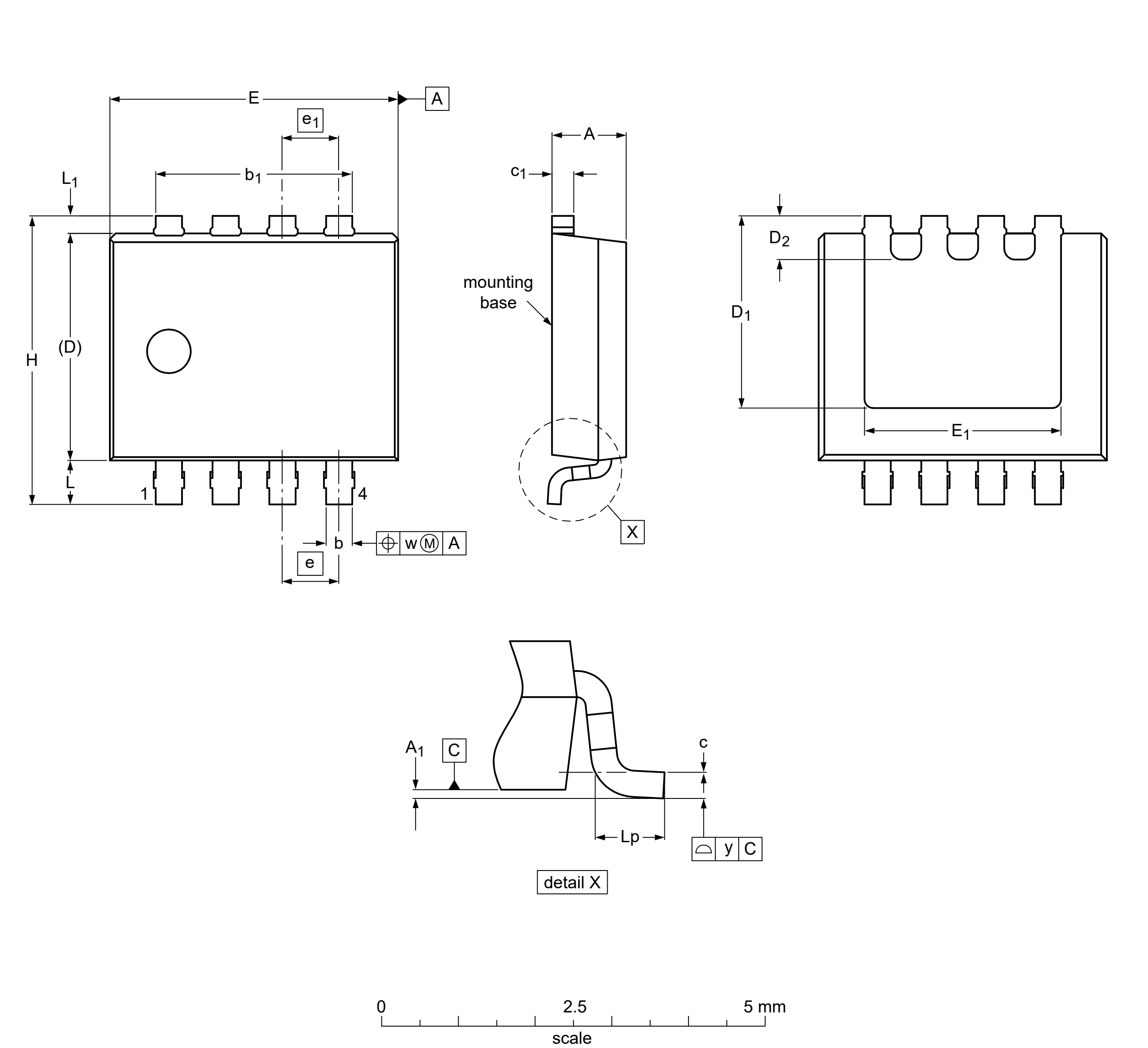


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit(1)		A	A_1	b(1)	b_1(1)	c	c_1	D ref	D_1	D_2	E(1)	E_1	e	e_1	H	L	L_1	L_p	w	y
	max	0.90	0.10	0.35	2.4	0.20	0.30		2.35		3.40	2.45			3.40	0.65	0.25	0.50		
mm	nom							2.60		0.50			0.65	0.65					0.20	0.10
	min	0.80	0.00	0.25	2.2	0.10	0.20		1.90		3.20	2.00			3.20	0.45	0.13	0.30		

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~14-04-25~~ 16-08-09

Fig. 17. Package outline LFPAK33 (SOT1210)

12. Soldering

Footprint information for reflow soldering of LFPAK33 package **SOT1210**

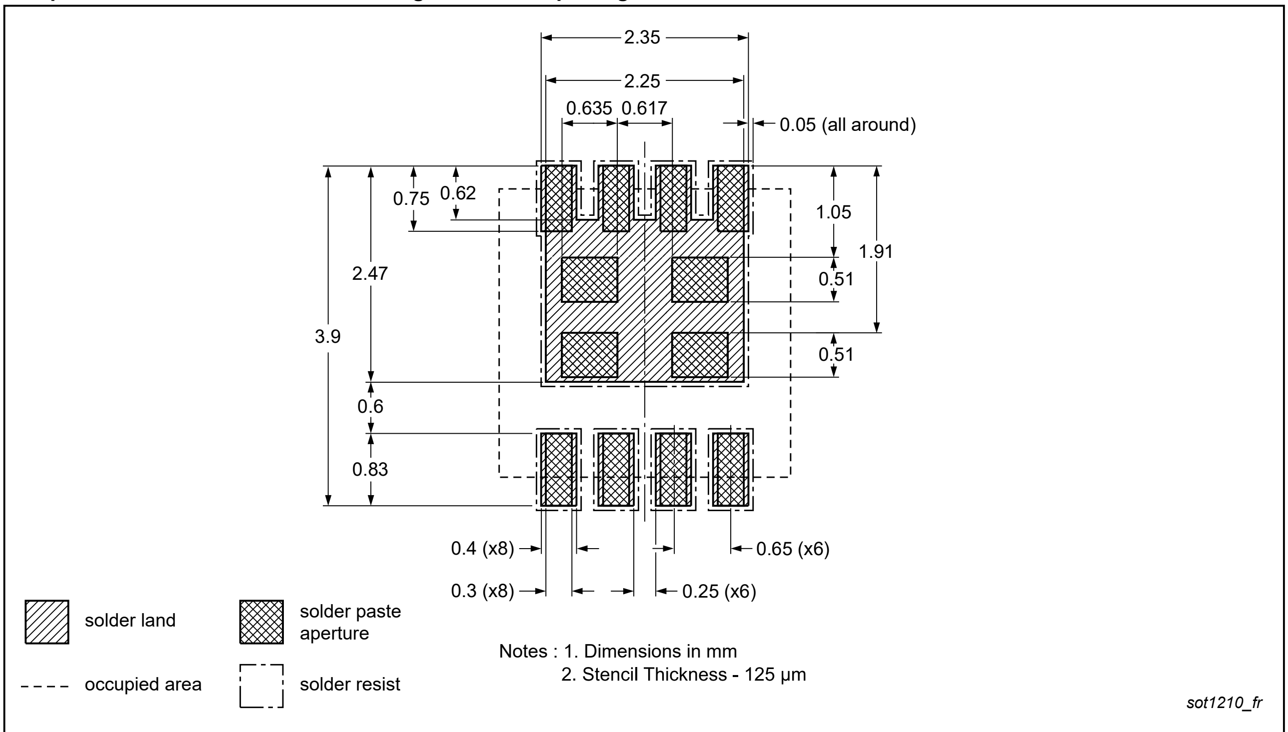


Fig. 18. Reflow soldering footprint for LFPAK33 (SOT1210)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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Date of release: 10 February 2020