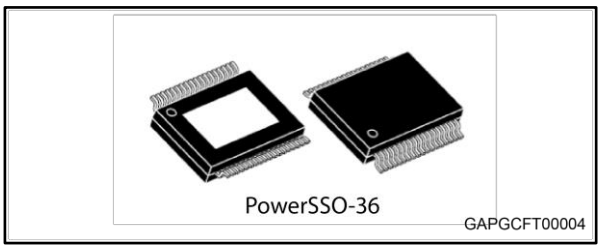
VND7004AY

Double channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	4 mΩ
Current limitation (typ)	I_{LIMH}	100 A
Standby current (max)	I_{STBY}	0.5 µA

- AEC-Q100 qualified
- General
  - Double channel smart high-side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery with self switch of the PowerMOS
  - Electrostatic discharge protection

Applications

Specially intended for Automotive smart power distribution, glow plugs, heating systems, DC motors, relay replacement and high power resistive and inductive actuators.

Description

The device is a double channel high-side driver manufactured using ST proprietary VIPower® M0-7 technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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1 Block diagram and pin description

Figure 1: Block diagram

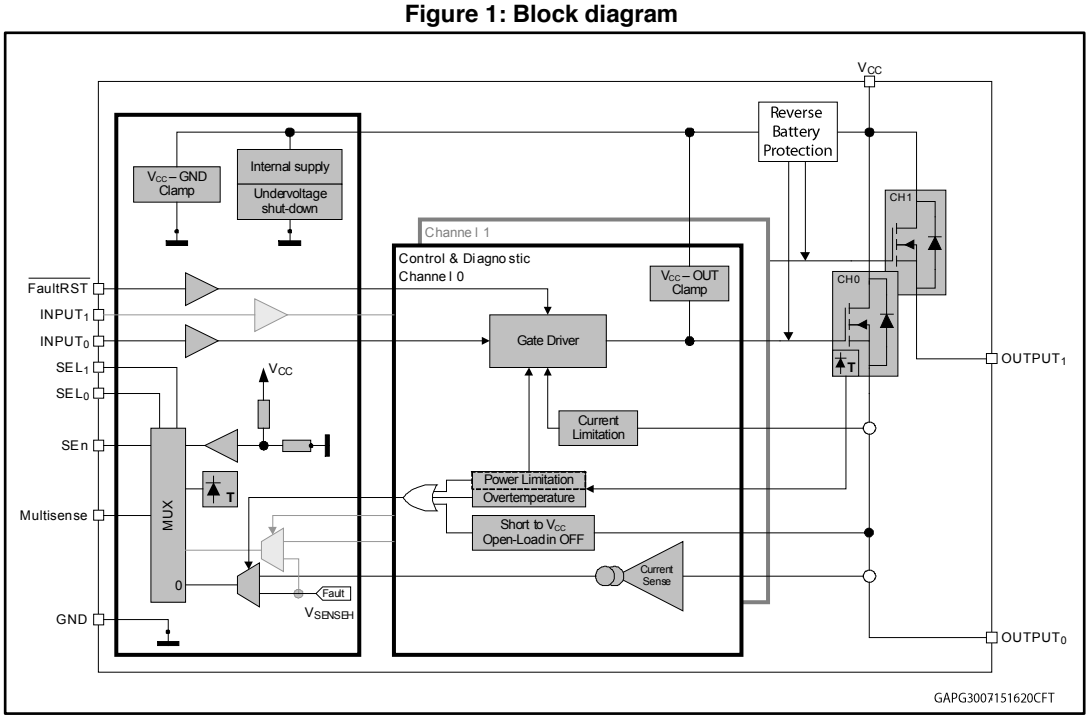


Table 1: Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1}$	Power output.
GND	Ground connection.
$INPUT_{0,1}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer.
$\overline{\text{FaultRST}}$	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode

Figure 2: Configuration diagram (top view)

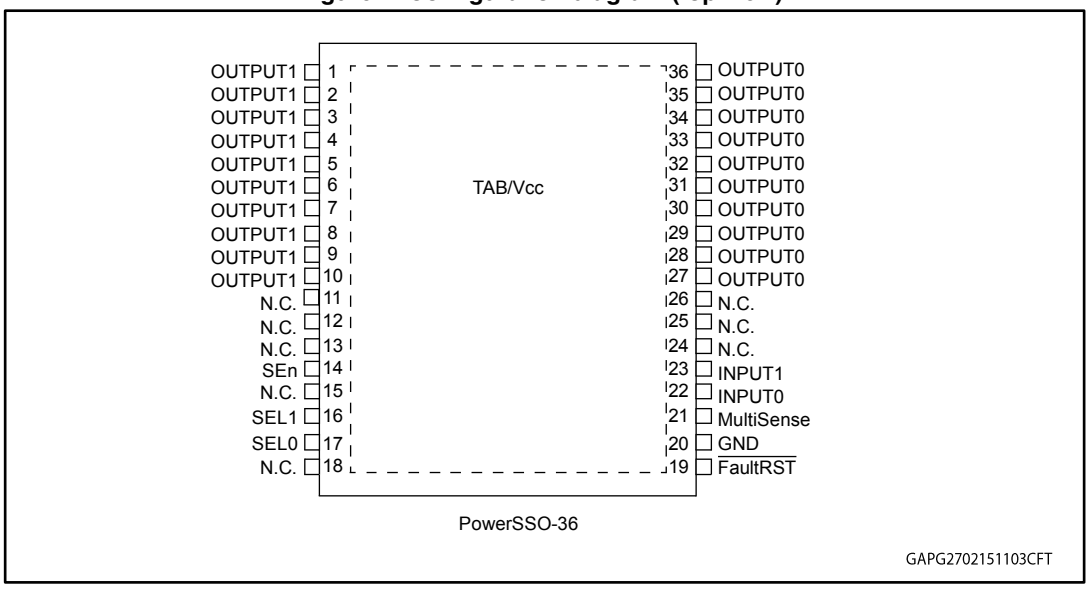


Table 2: Suggested connections for unused and not connected pins

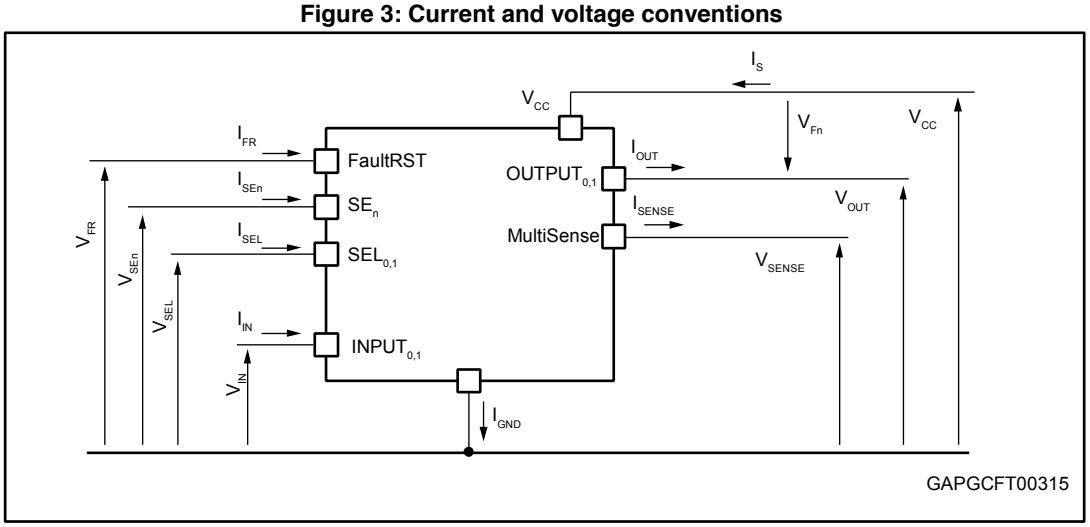
Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X (1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor

Notes:

(1)X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$V_F = V_{OUT} - V_{CC}$ when $V_{OUT} > V_{CC}$ and INPUT = LOW.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO 7637-2:2004 Pulse 5b level IV clamped to 40 V; R_L = 4 Ω)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1}$ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	65	
I_{IN}	$INPUT_{0,1}$ DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V

Symbol	Parameter	Value	Unit
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	-20	
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150 °C)	103	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) • $INPUT_{0,1}$ • MultiSense • SEn, $SEL_{0,1}$, FaultRST • $OUTPUT_{0,1}$ • V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (1)	3.4	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(2)	50.6	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(3)	15.8	

Notes:

(1)One channel ON.

(2)Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

(3)Device mounted on four-layers 2s2p PCB

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	V
$V_{USDReset}$	Undervoltage shutdown reset				5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
R_{ON}	On-state resistance(1)	I_{OUT} = 15 A; T_j = 25°C		4		mΩ
		I_{OUT} = 15 A; T_j = 150°C			8	
		I_{OUT} = 15 A; V_{CC} = 4 V; T_j = 25°C			6	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON_REV}	On-state resistance in reverse battery	I_{OUT} = -15 A; V_{CC} = -13 V; T_j = 25°C		4		mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	V
I_{STBY}	Supply current in standby at V_{CC} = 13 V(2)	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C (3)			1.9	
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			15	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN0} = 5 V; V_{IN1} = 5 V; I_{OUT0} = 0 A; I_{OUT1} = 0 A		6	12	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN0} = 5 V; V_{IN1} = 5 V; $I_{OUT0,1}$ = 15 A			12	mA
$I_{L(off)}$	Off-state output current (2)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		7.5	
V_F	Output - V_{CC} diode voltage	I_{OUT} = -15 A; T_j = 150°C			0.7	V

Notes:

(1)For each channel

(2)PowerMOS leakage included.

(3)Parameter specified by design; not subjected to production test.

Table 6: Switching

V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)}$ (1)	Turn-on delay time	R_L = 0.87 Ω	60	110	195	µs
$t_{d(off)}$ (1)	Turn-off delay time		50	100	160	
$(dV_{OUT}/dt)_{on}$ (1)	Turn-on voltage slope	R_L = 0.87 Ω	0.05	0.21	0.35	V/µs
$(dV_{OUT}/dt)_{off}$ (1)	Turn-off voltage slope		0.05	0.21	0.35	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 0.87 Ω	—	2.3	3.7 (2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 0.87 Ω	—	2.5	4.5 (2)	mJ
t_{SKEW} (1)	Differential pulse skew (t_{PHL} - t_{PLH})	R_L = 0.87 Ω	-110	-45	20	µs

Notes:

(1)See *Figure 4: "Switching time and Pulse skew"*.

(2)Parameter guaranteed by design and characterization; not subjected to production test.

Table 7: Logic inputs

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$INPUT_{0,1}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{\text{FaultRST}}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 8: Protections

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	70	100	140	A
		4 V < V_{CC} < 18 V(1)				
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		33		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(1)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40°C; V_{CC} = 13 V		60		K
t_{LATCH_RST}	Fault reset time for output unlatch	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{IN} = 5 V; $V_{SEL0,1}$ = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40°C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V

Notes:

(1)Parameter guaranteed by design and characterization; not subjected to production test.

Table 9: MultiSense

$7\ V < V_{CC} < 18\ V$; $-40°C < T_j < 150°C$						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
Current sense characteristics						
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 3.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	1500	14200	31500	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 3.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-30		30	%
K_{GP}	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	7990	13900	21050	
dK_{GP}/K_{GP} (1)(2)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	9580	13850	19020	
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-7		7	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 45 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	11470	13800	15840	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 45 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V	0		0.5	µA
		MultiSense disabled: -1 V < V_{SENSE} < 5 V (1)	-0.5		0.5	
		MultiSense enabled: V_{SEn} = 5 V; All channels ON; I_{OUTX} = 0 A; Ch_X diagnostic selected; • E.g. Ch_0: V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; I_{OUT1} = 15 A	0		120	
		MultiSense enabled: V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected: • E.g. Ch_0: V_{IN0} = 0 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT1} = 15 A	0		2	

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OUT_MSD}(1)	Output Voltage for MultiSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ; • E.g. Ch_0: V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 15 A		5		V
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 kΩ; V_{SEn} = 5 V; V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 45 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	65			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 7: "TDSTKON"*)	V_{SEn} = 5 V; Ch_X ON to OFF transition; Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN0} = 0 V; V_{IN1} = 0 V; V_{FR} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT (1)	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function (3)		$V_{SENSE\_VCC} = V_{CC} / 4$				
Fault diagnostic feedback (see *Table 10: "Truth table"*)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ; • E.g: Ch_0 in open load V_{IN0} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see *Figure 5: "MultiSense timings (current sense mode)"*) (4)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 0.87 Ω			60	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 0.87 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 0.87 Ω		170	400	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 0.87 Ω			200	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 0.87 Ω		50	250	µs
MultiSense timings (chip temperature sense mode - see *Figure 6: "Multisense timings (chip temperature and VCC sense mode)"*) [4]						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see *Figure 6: "Multisense timings (chip temperature and VCC sense mode)"*) [4]						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (Multiplexer transition times) [4]						
t_{D_XtoY}	MultiSense transition delay from Ch_X to Ch_Y	V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 0 A; I_{OUT1} = 15 A; R_{SENSE} = 1 kΩ			20	µs
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT0} = 1.5 A; R_{SENSE} = 1 kΩ			60	µs

$7\ V < V_{CC} < 18\ V$; $-40°C < T_j < 150°C$						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT0} = 1.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT1} = 15A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT1} = 15 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVSENSEH}$	MultiSense transition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	V_{IN0} = 5 V; V_{IN1} = 0 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 3 A; V_{OUT1} = 15 V; R_{SENSE} = 1 kΩ			20	µs

Notes:

(1)Parameter guaranteed by design and characterization; not subjected to production test.

(2)All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

(3)V_{CC} sensing and T_C sensing are referred to GND potential.

(4)Transition delay are measured up to +/- 10% of final conditions.

Figure 4: Switching time and Pulse skew

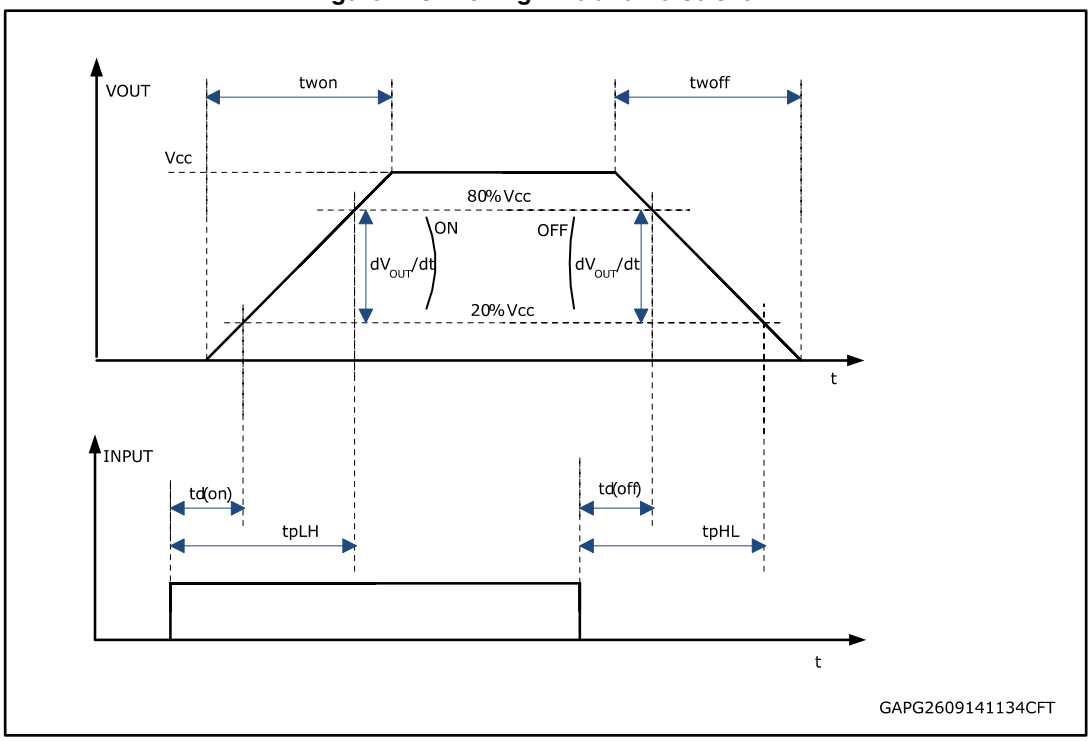


Figure 5: MultiSense timings (current sense mode)

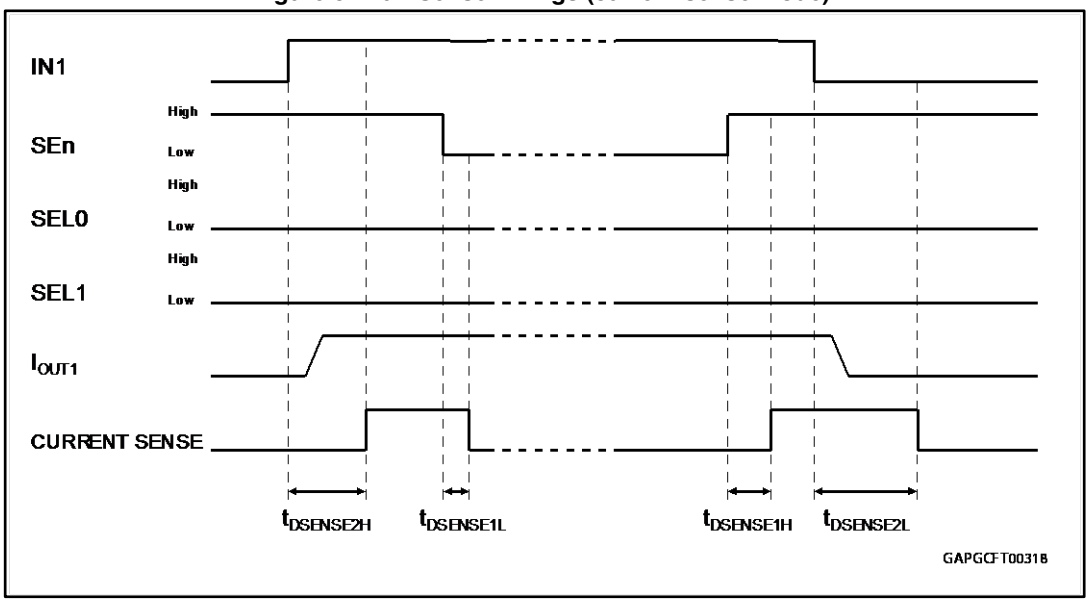


Figure 6: Multisense timings (chip temperature and VCC sense mode)

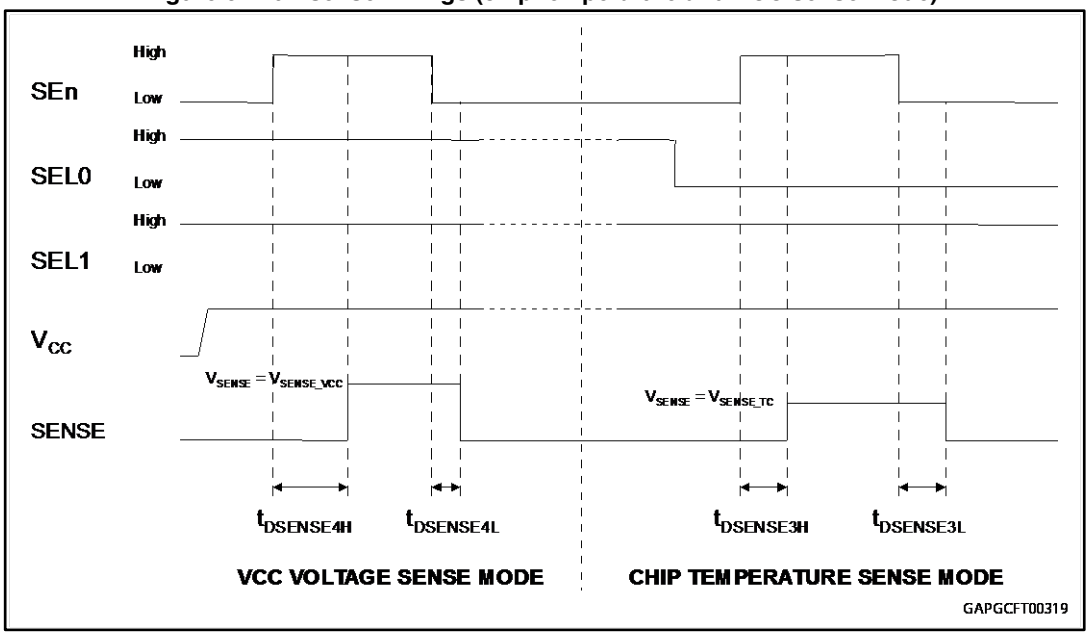


Figure 7: TDSTKON

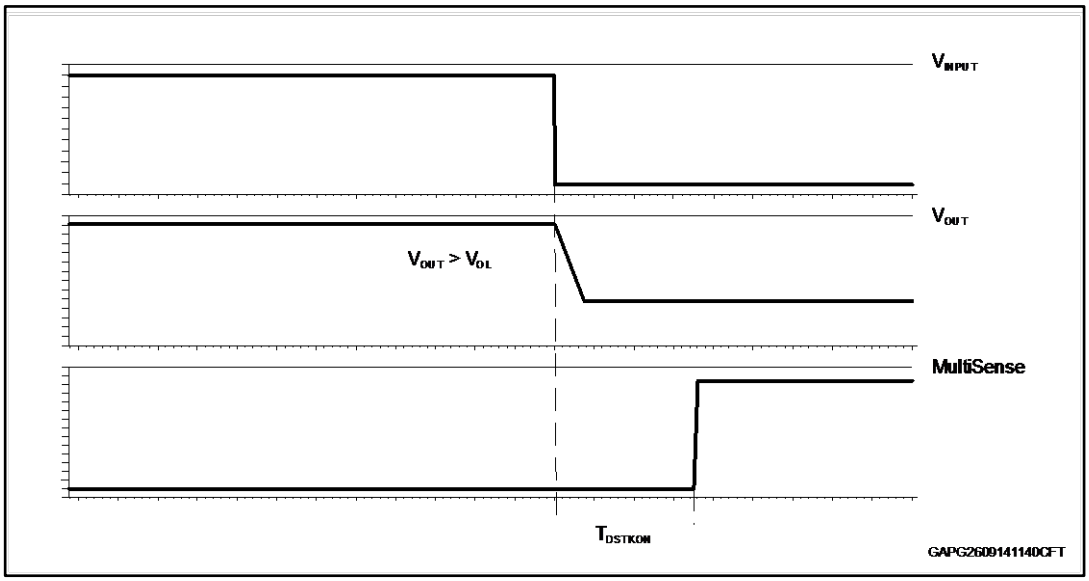


Table 10: Truth table

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150 °C	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Outputs configured for auto-restart
		H	H			H	See (1)	Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Output cycles with temperature hysteresis
		H	H			L	See (1)	Output latches-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See (1)		H	See (1)	
	Open-load	L	X			H	See (1)	External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See (1)		< 0 V	See (1)	

Notes:

(1)Refer to *Table 11: "MultiSense multiplexer addressing"*

Table 11: MultiSense multiplexer addressing

SEn	SEL_1	SEL_0	MUX channel	MultiSense output			
				Normal mode	Overload	OFF-state diag. (1)	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	Channel 1 diagnostic	I_{SENSE} = 1/K * I_{OUT1}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	L	T_{CHIP} Sense	V_{SENSE} = V_{SENSE_TC}			
H	H	H	V_{CC} Sense	V_{SENSE} = V_{SENSE_VCC}			

Notes:

(1)In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.

Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0.

Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

2.4 Waveforms

Figure 8: Latch functionality - behavior in hard short circuit condition (TAMB << TTSD)

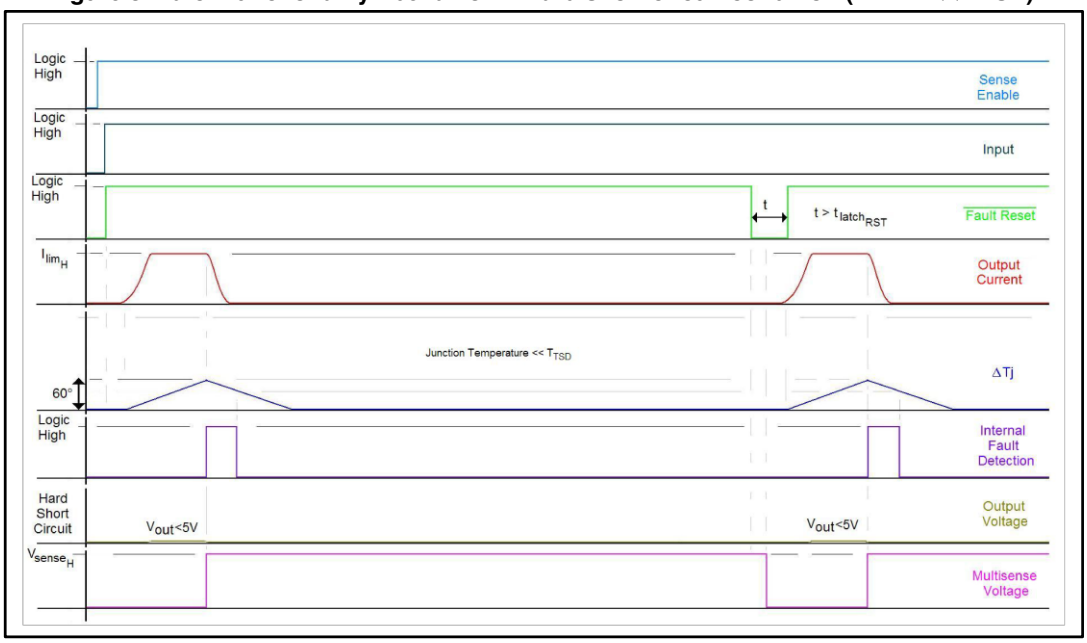


Figure 9: Latch functionality - behavior in hard short circuit condition

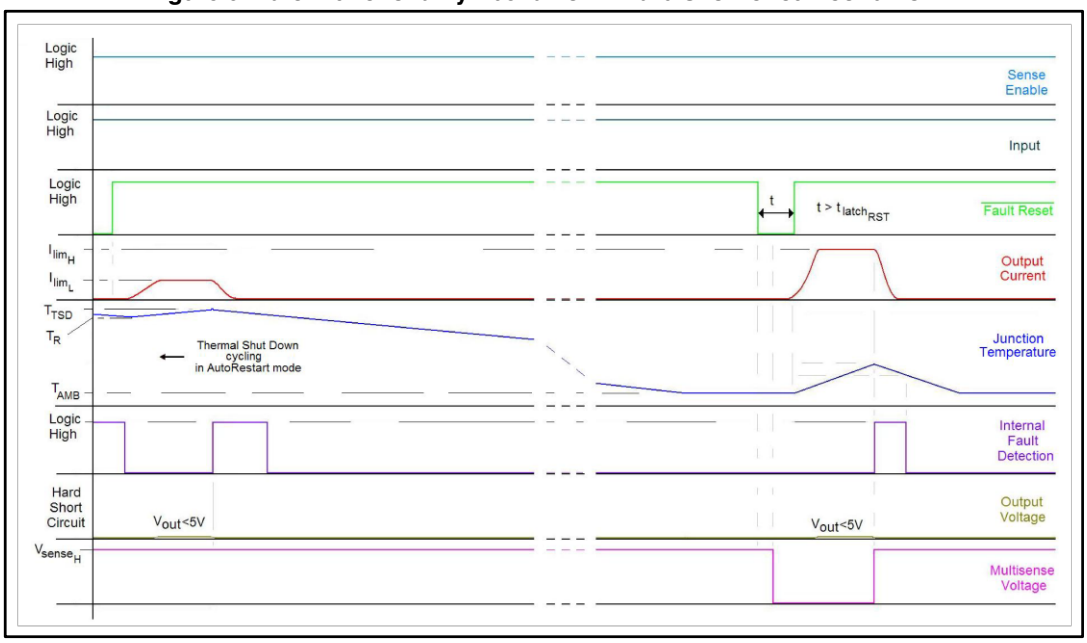


Figure 10: Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

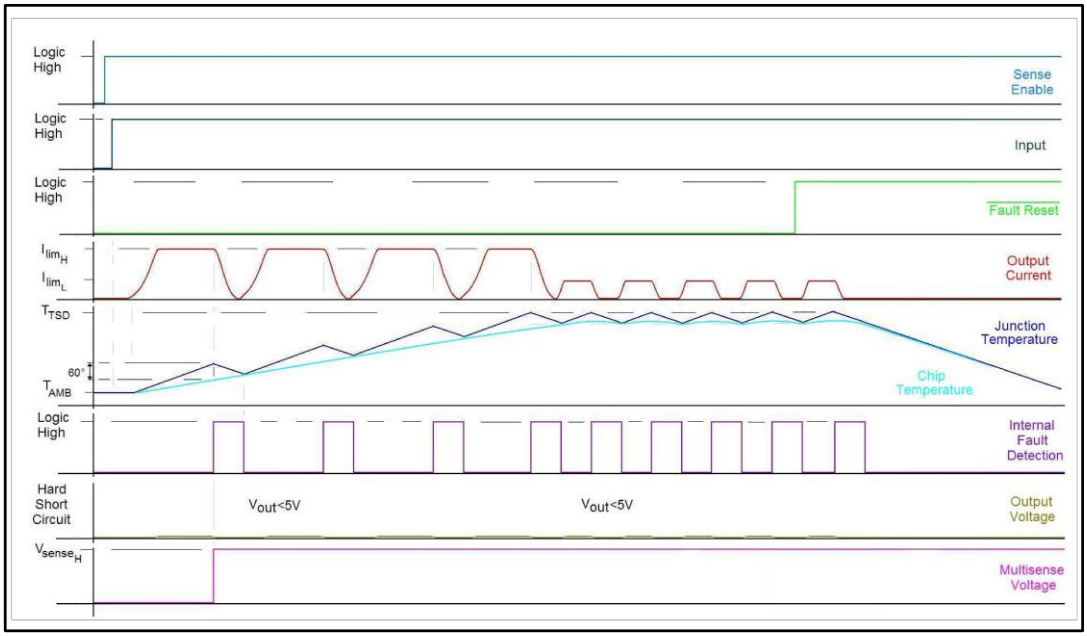


Figure 11: Standby mode activation

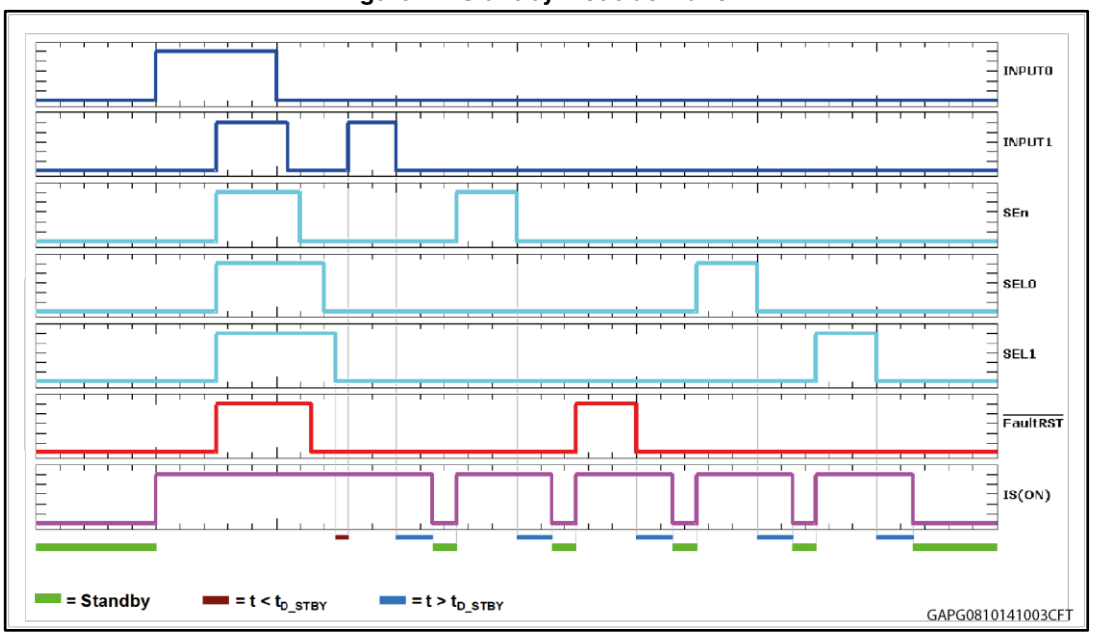
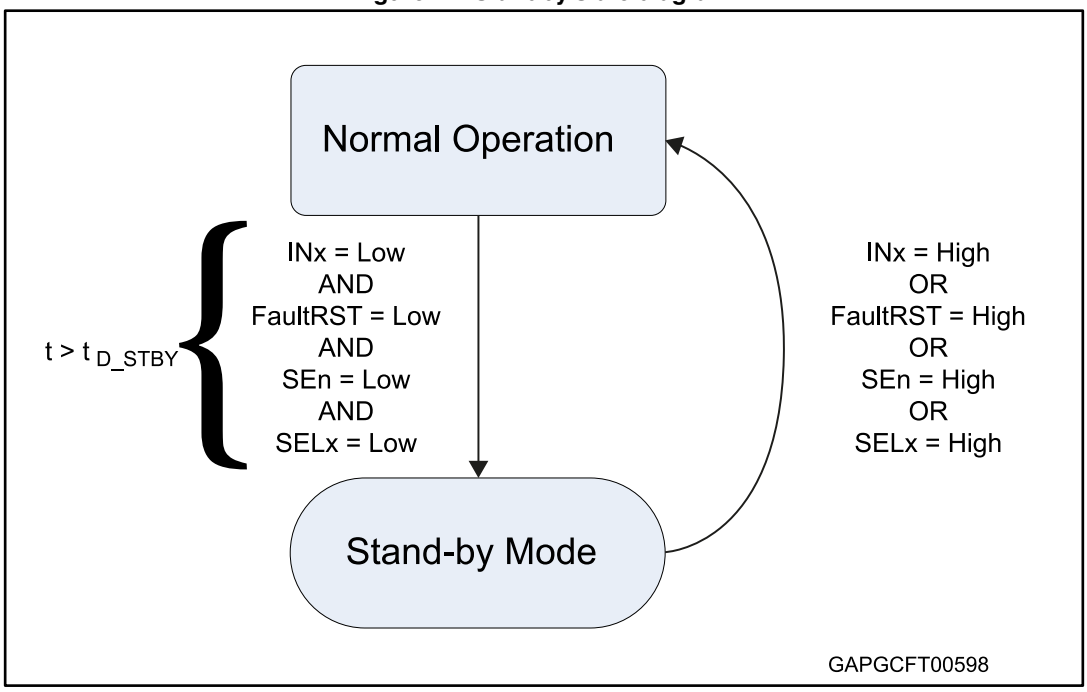


Figure 12: Standby state diagram



2.5 Electrical characteristics curves

Figure 13: OFF-state output current

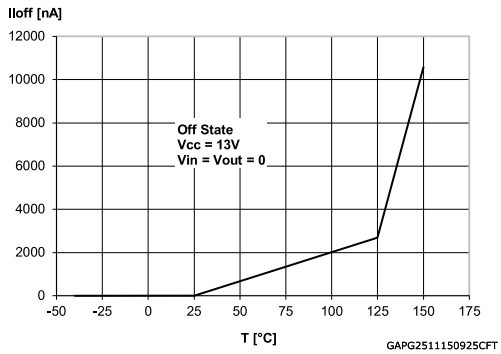


Figure 14: Standby current

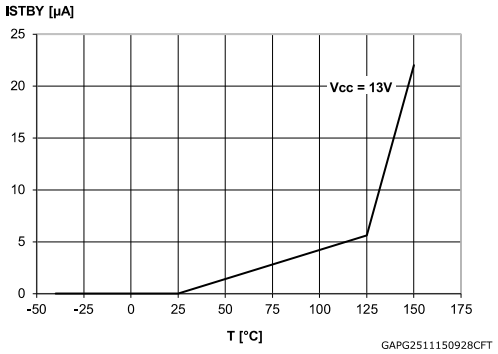


Figure 15: IGND(ON) vs. Iout

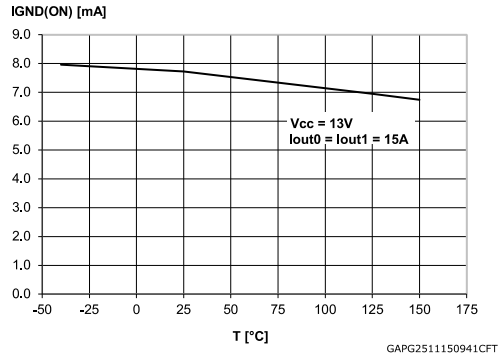


Figure 16: Logic Input high level voltage

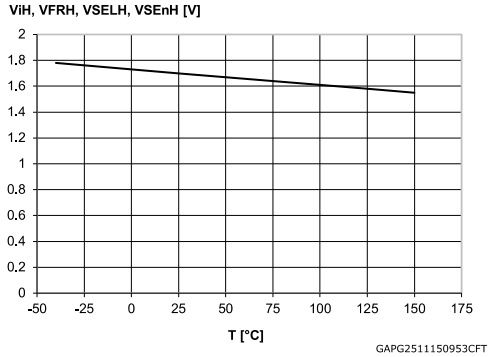


Figure 17: Logic Input low level voltage

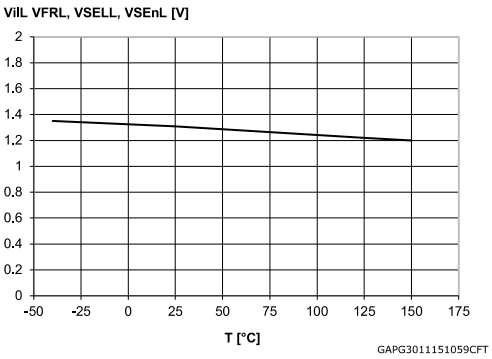


Figure 18: High level logic input current

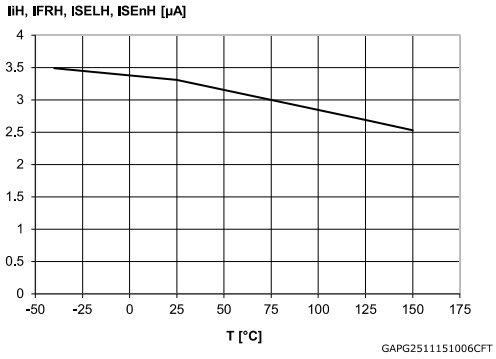


Figure 19: Low level logic input current

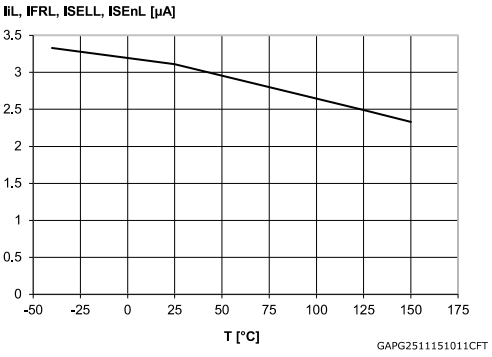


Figure 20: Logic Input hysteresis voltage

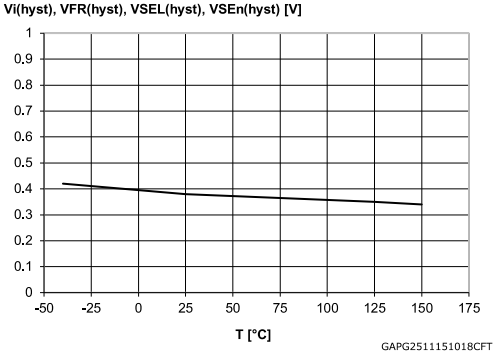


Figure 21: FaultRST Input clamp voltage

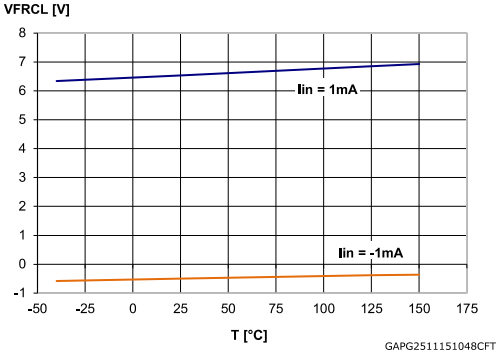


Figure 22: Undervoltage shutdown

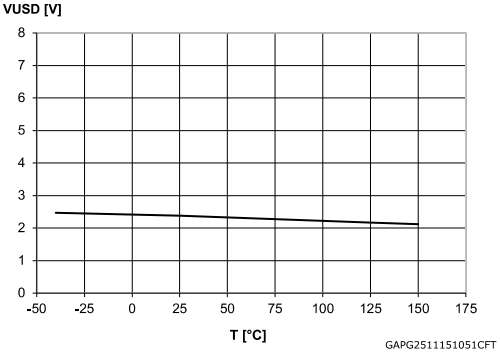


Figure 23: On-state resistance vs. Tcase

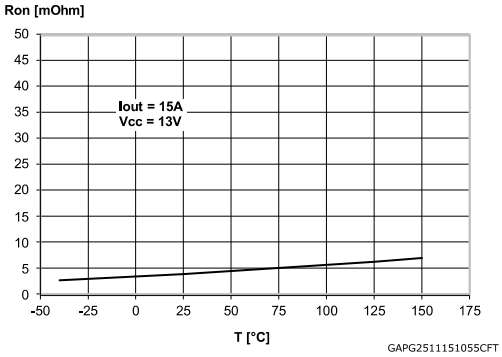


Figure 24: On-state resistance vs. VCC

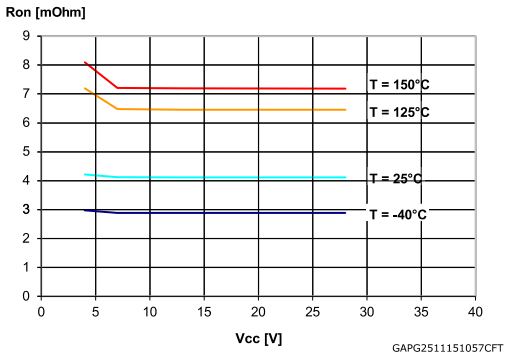


Figure 25: Turn-on voltage slope

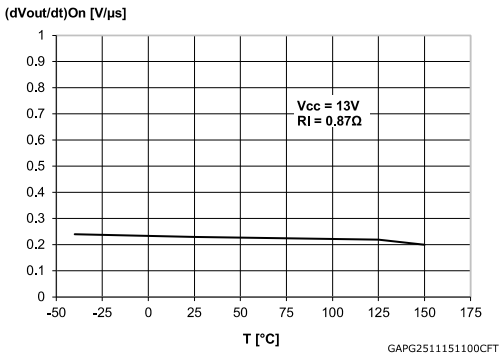


Figure 26: Turn-off voltage slope

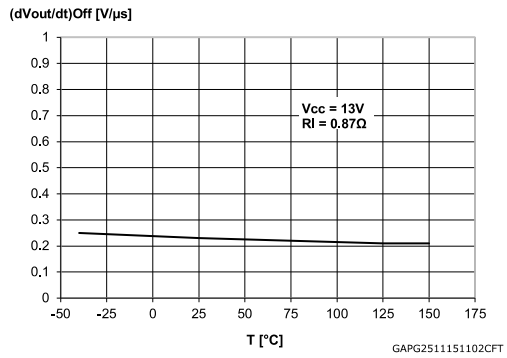


Figure 27: Won vs. Tcase

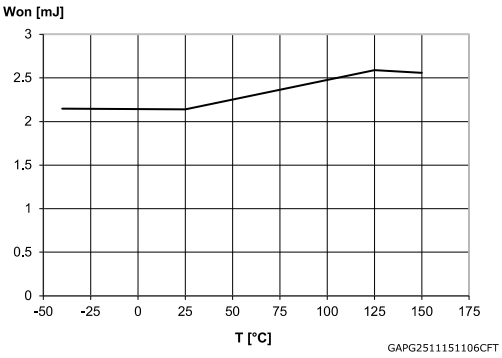


Figure 28: Woff vs. Tcase

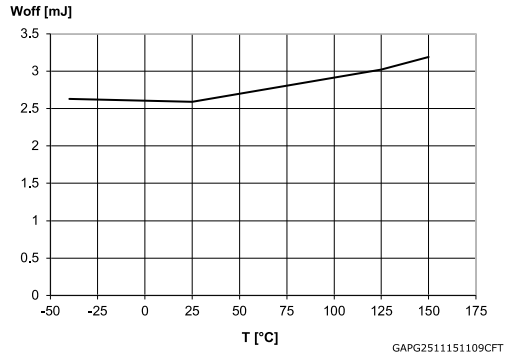


Figure 29: OFF-state open-load voltage detection threshold

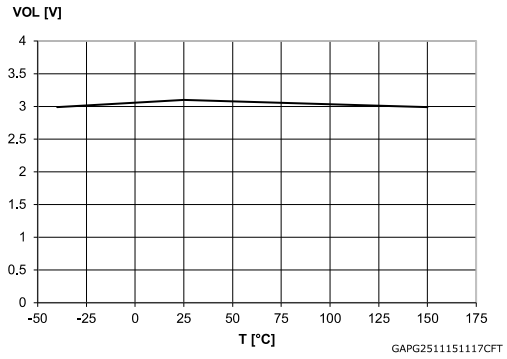


Figure 30: Vsense clamp vs. Tcase

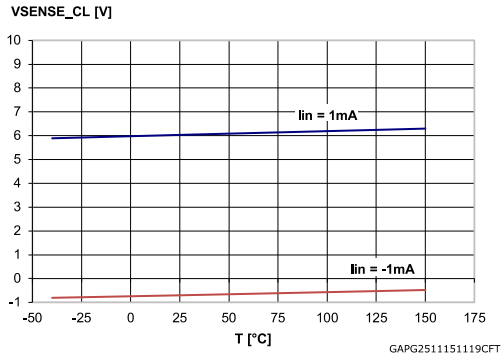
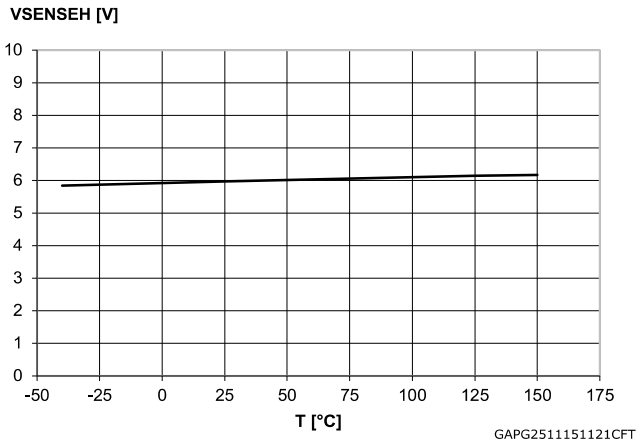


Figure 31: Vsenseh vs. Tcase



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of 60 K. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_{RS} (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

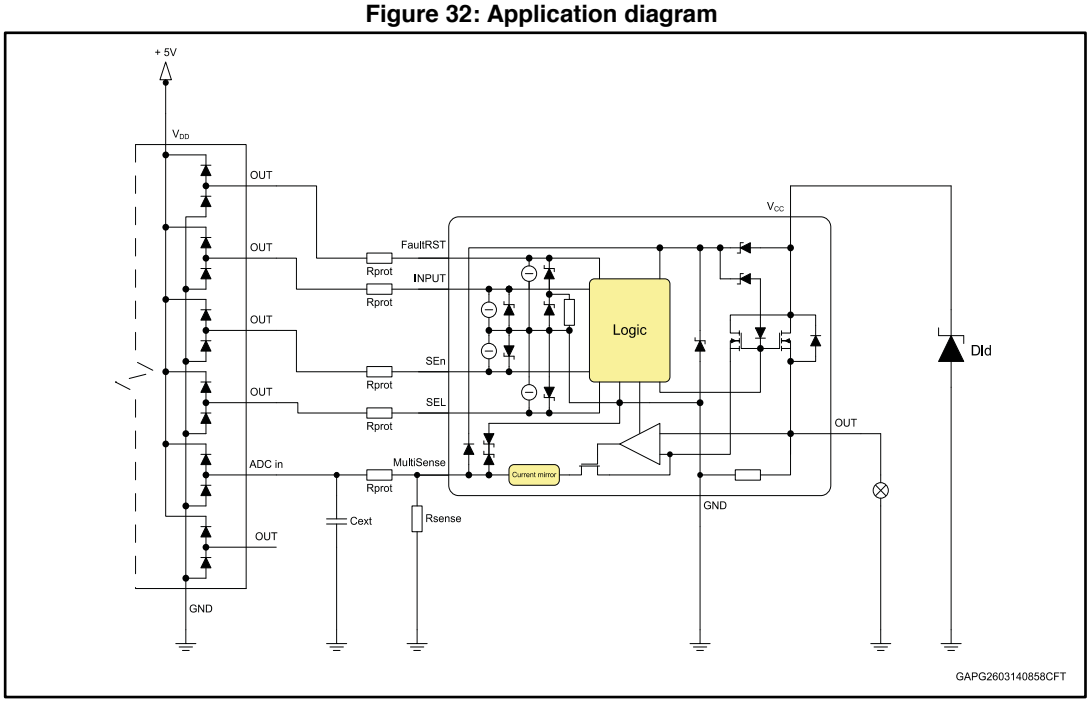
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

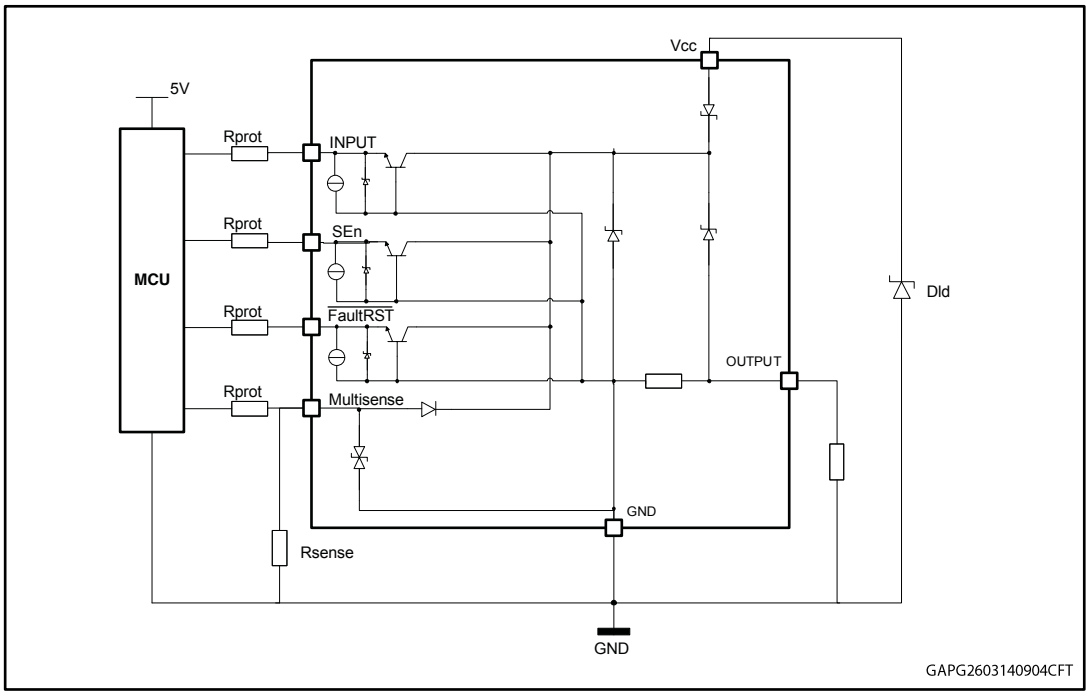
4 Application information

Figure 32: Application diagram



4.1 GND protection network against reverse battery

Figure 33: Simplified internal structure



The device does not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures.

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode, thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 12: "ISO 7637-2 - electrical transient conduction along supply line"*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 12: ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4 (2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B (3)		40 V	5 pulse	1 min		400 ms, 2 Ω

Notes:

(1)U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

(2)Test pulse from ISO 7637-2:2004(E).

(3)With 40 V external suppressor referred to ground (-40°C < T_j < 150 °C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq 20$ mA; $V_{OH\mu C} \geq 4.5$ V

7.5 kΩ ≤ R_{prot} ≤ 140 kΩ.

Recommended values: R_{prot} = 15 kΩ

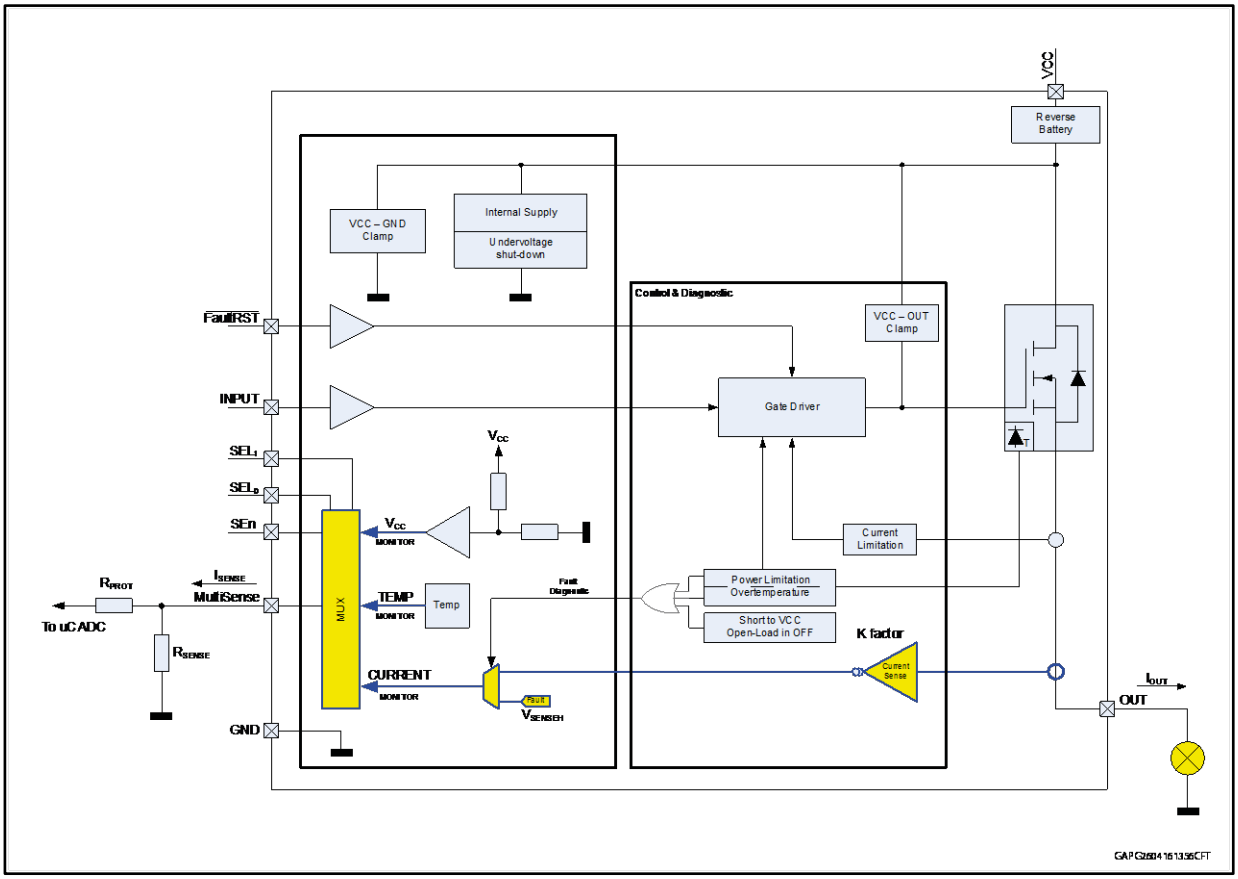
4.4 Multisense - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- V_{CC} monitor: voltage propotional to V_{CC}
- T_{CASE}: voltage propotional to chip temperature

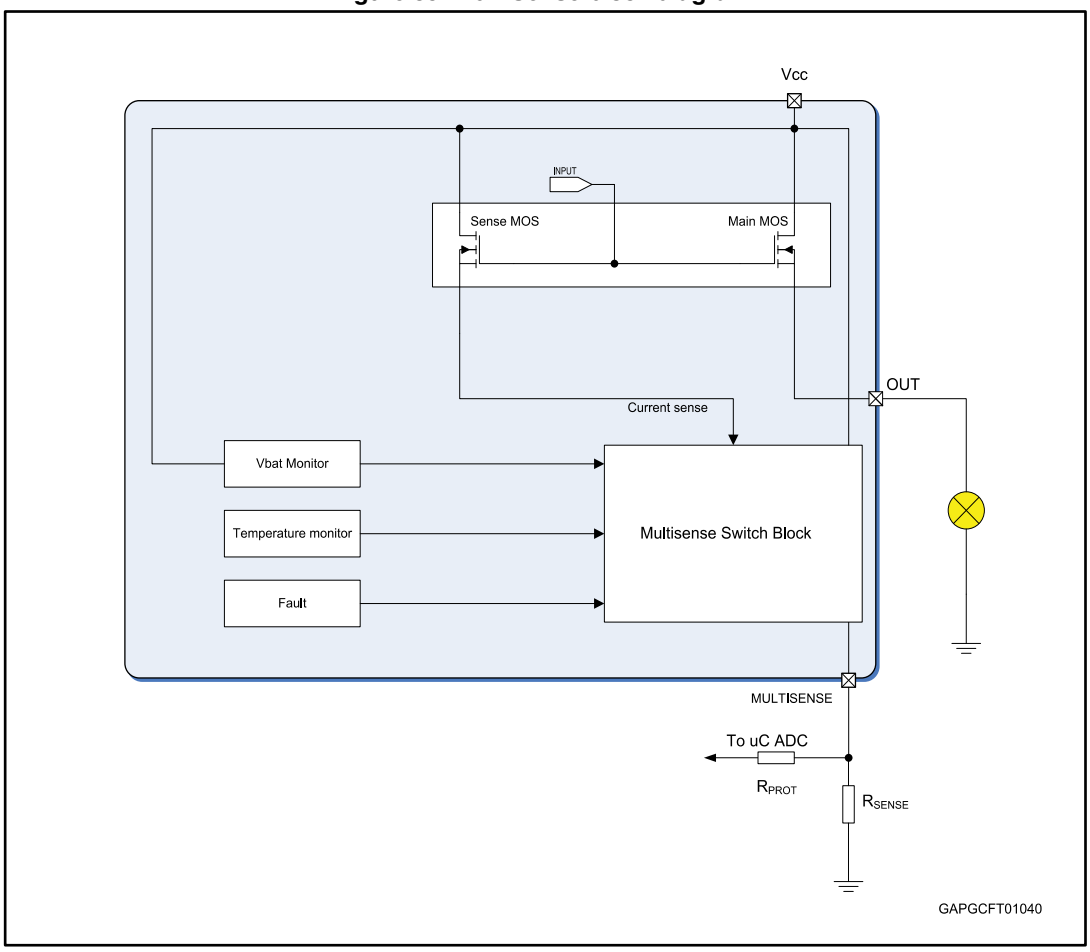
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *MultiSense multiplexer addressing Table*.

Figure 34: MultiSense and diagnostic – block diagram



4.4.1 Principle of Multisense signal generation

Figure 35: MultiSense block diagram



Current monitor

When current mode is selected via MultiSense, this output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on R_{SENSE} resistor
- I_{SENSE} is the current provided from MultiSense pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the MultiSense pin which is switched to a “current limited” voltage source, V_{SENSEH}.

In any case, the current sourced by the MultiSense in this condition is limited to I_{SENSEH}.

The typical behavior in case of overload or hard short circuit is shown in *Waveforms section*.

Figure 36: Analogue HSD – open-load detection in off-state

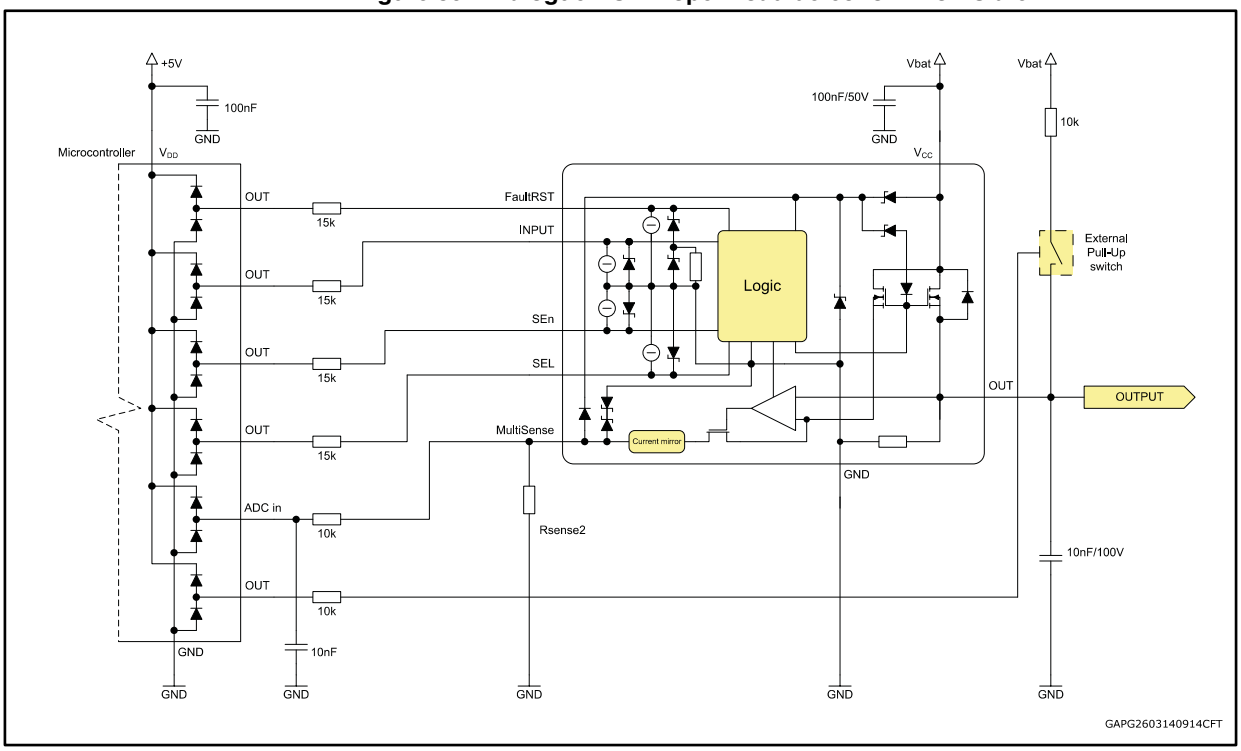


Figure 37: Open-load / short to VCC condition

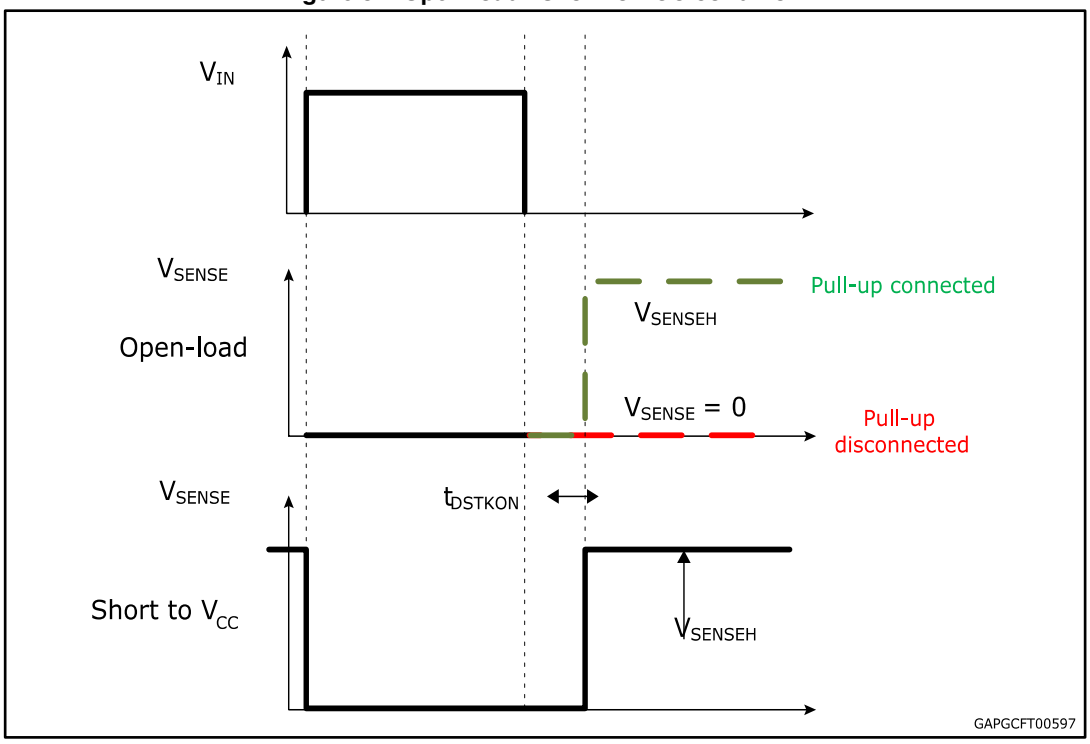


Table 13: MultiSense pin levels in off-state

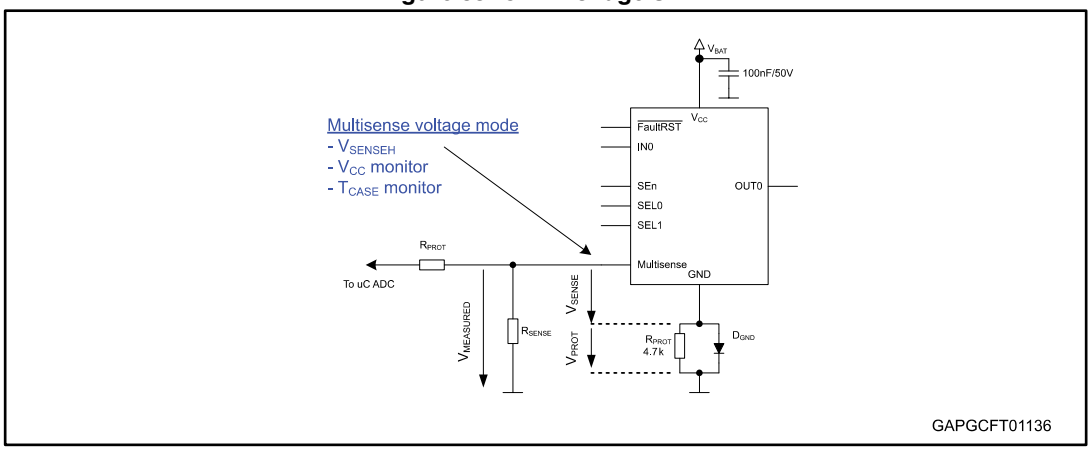
Condition	Output	MultiSense	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 TCASE and VCC monitor

In this case, MultiSense output operates in voltage mode and output level is referred to device GND. Care must be taken in case a GND network protection is used, because a voltage shift is generated between the device GND and the microcontroller input GND reference.

Figure 38: "GND voltage shift" shows the link between $V_{MEASURED}$ and the real V_{SENSE} signal.

Figure 38: GND voltage shift



V_{CC} monitor

Battery monitoring channel provides V_{SENSE} = V_{CC} / 8.

Case temperature monitor

Case temperature monitor is capable of providing information about the actual device temperature. Since a diode is used for temperature sensing, the following equation describes the link between temperature and output V_{SENSE} level:

$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$

where dV_{SENSE_TC} / dT ~ typically -5.5 mV/K (for temperature range (-40 °C to 150 °C)).

4.4.3 Short to VCC and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

Equation

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

5 Package and PCB thermal data

5.1 PowerSSO-36 thermal data

Figure 39: PowerSSO-36 PC board

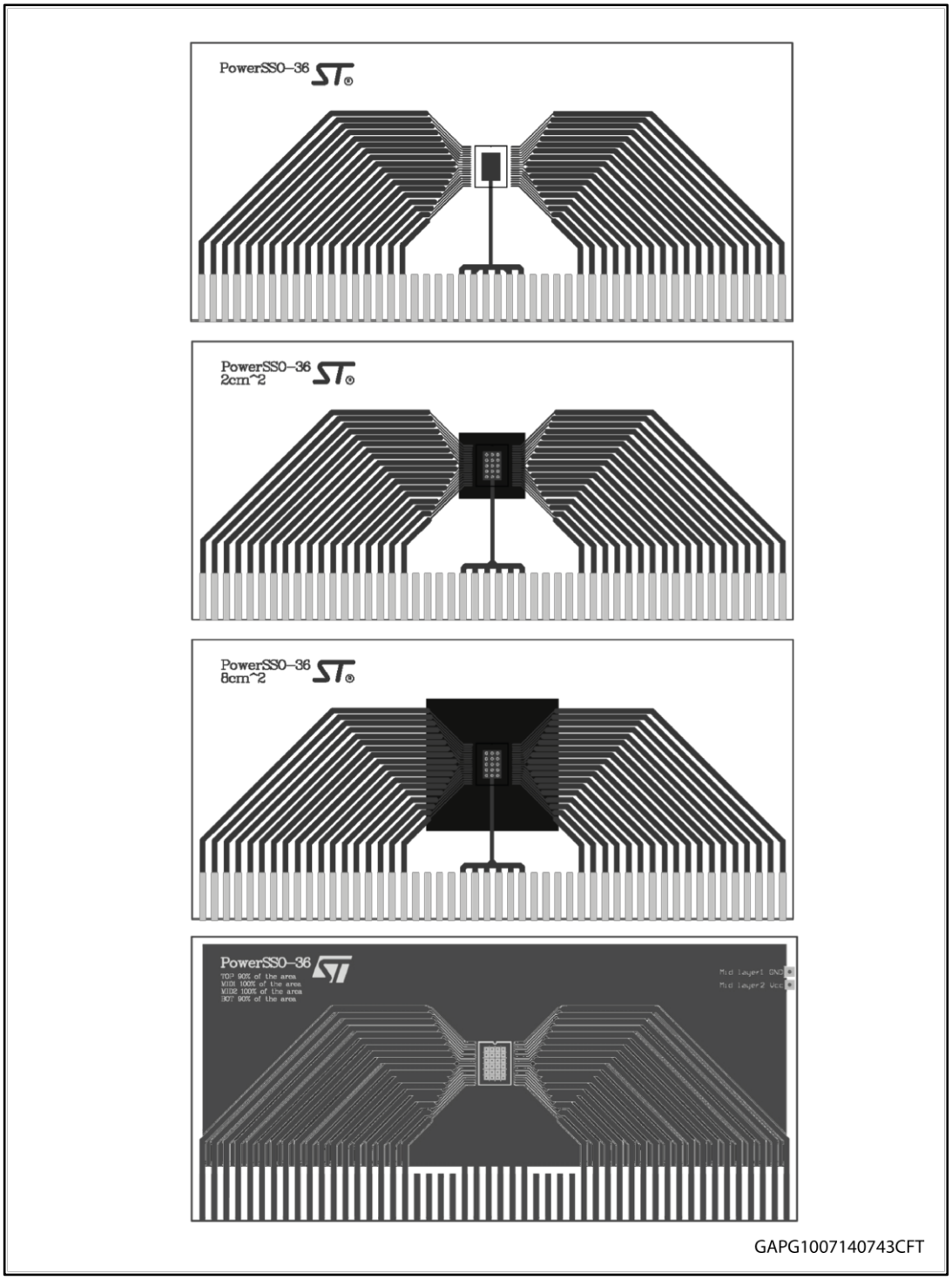


Table 14: PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	4.1 mm x 6.5 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 40: Rthj-amb vs PCB copper area in open box free air conditions

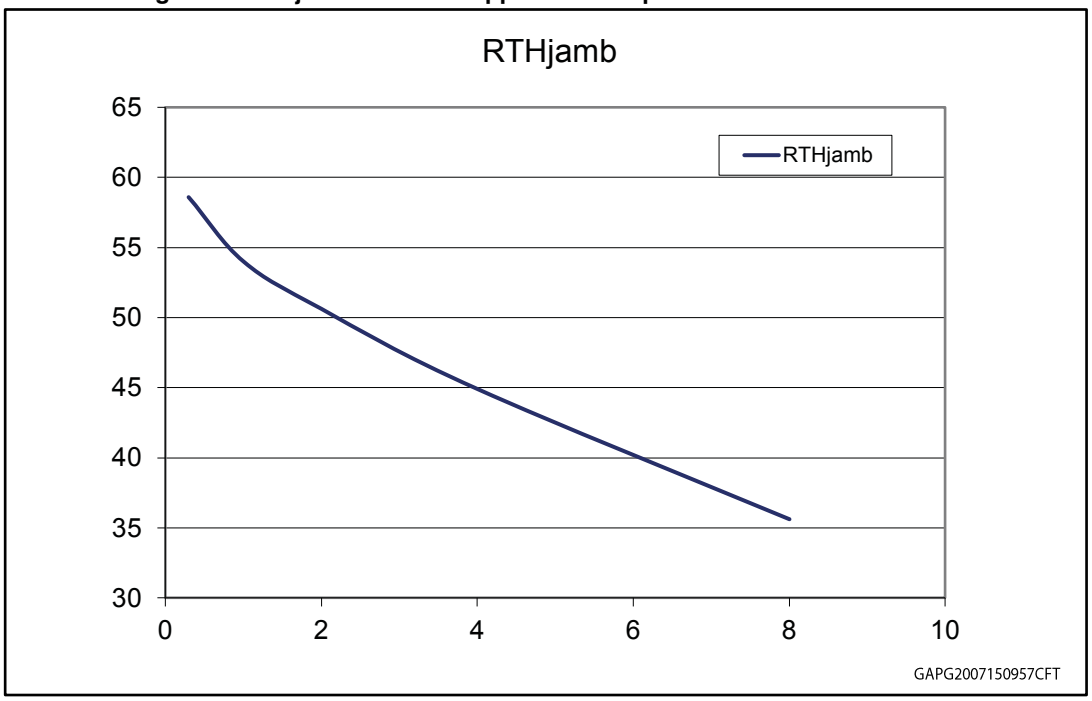
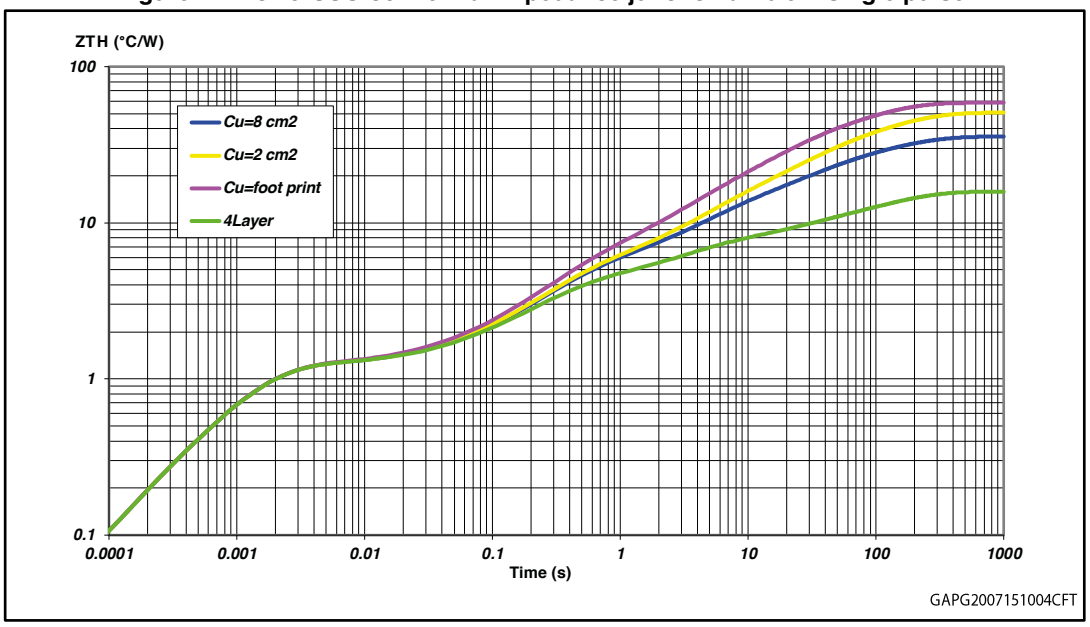


Figure 41: PowerSSO-36 thermal impedance junction ambient single pulse

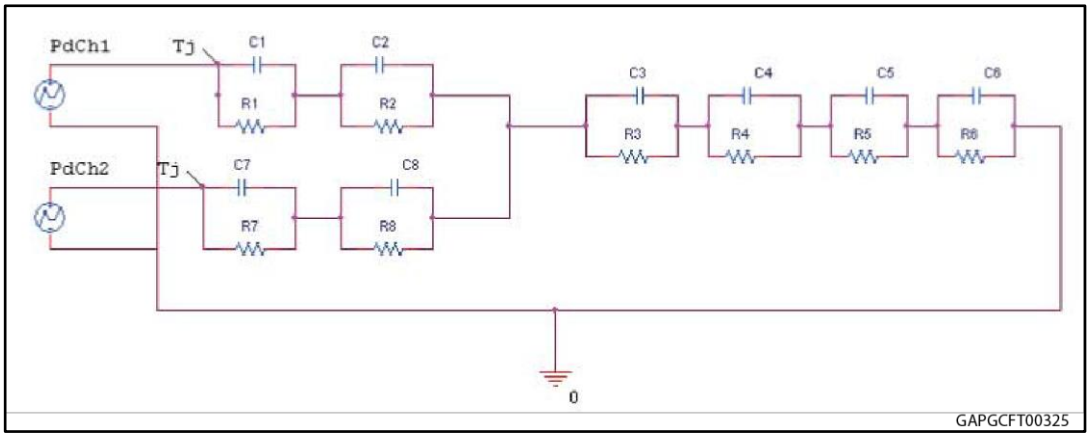


Equation: pulse calculation formula

$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_P/T$

Figure 42: Thermal fitting model for PowerSSO-36



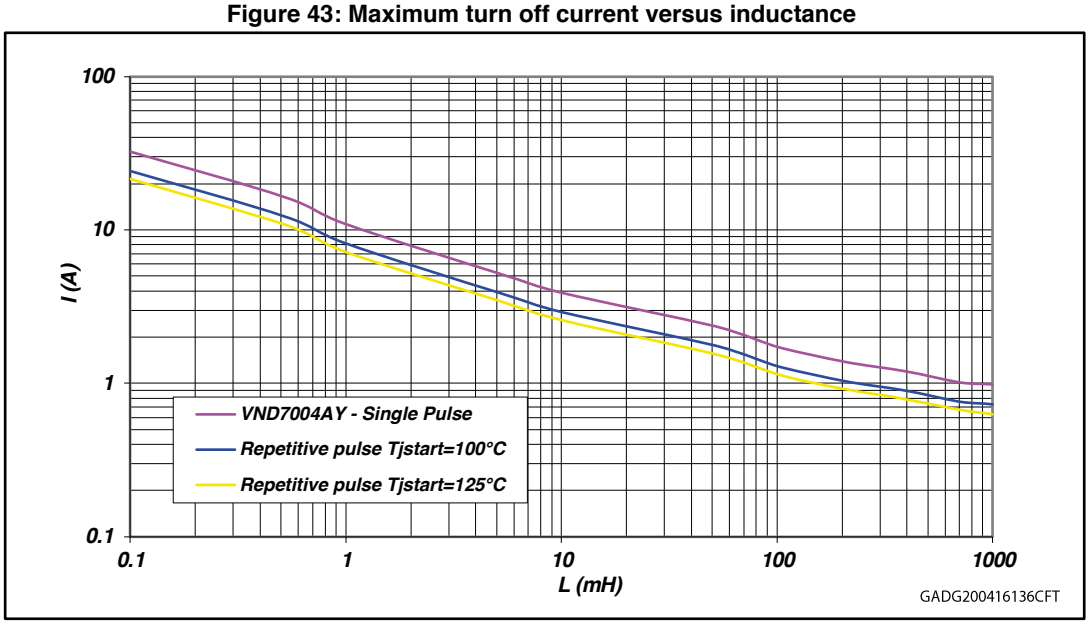
The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15: Thermal parameters

Area/island (cm2)	FP	2	8	4L
R1 = R7 (°C/W)	0.01			
R2 = R8 (°C/W)	1.2			
R3 (°C/W)	3.4	3.4	3.4	2.6
R4 (°C/W)	6	6	6	3
R5 (°C/W)	18	14	10	2
R6 (°C/W)	30	26	15	7
C1 = C7 (W·s/°C)	0.0005			
C2 = C8 (W·s/°C)	0.001			
C3 (W·s/°C)	0.1			
C4 (W·s/°C)	0.5	0.8	0.8	1
C5 (W·s/°C)	1	2	3	10
C6 (W·s/°C)	3	5	9	18

6 Maximum demagnetization energy (VCC = 16 V)

Figure 43: Maximum turn off current versus inductance



Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 PowerSSO-36 package information

Figure 44: PowerSSO-36 package outline

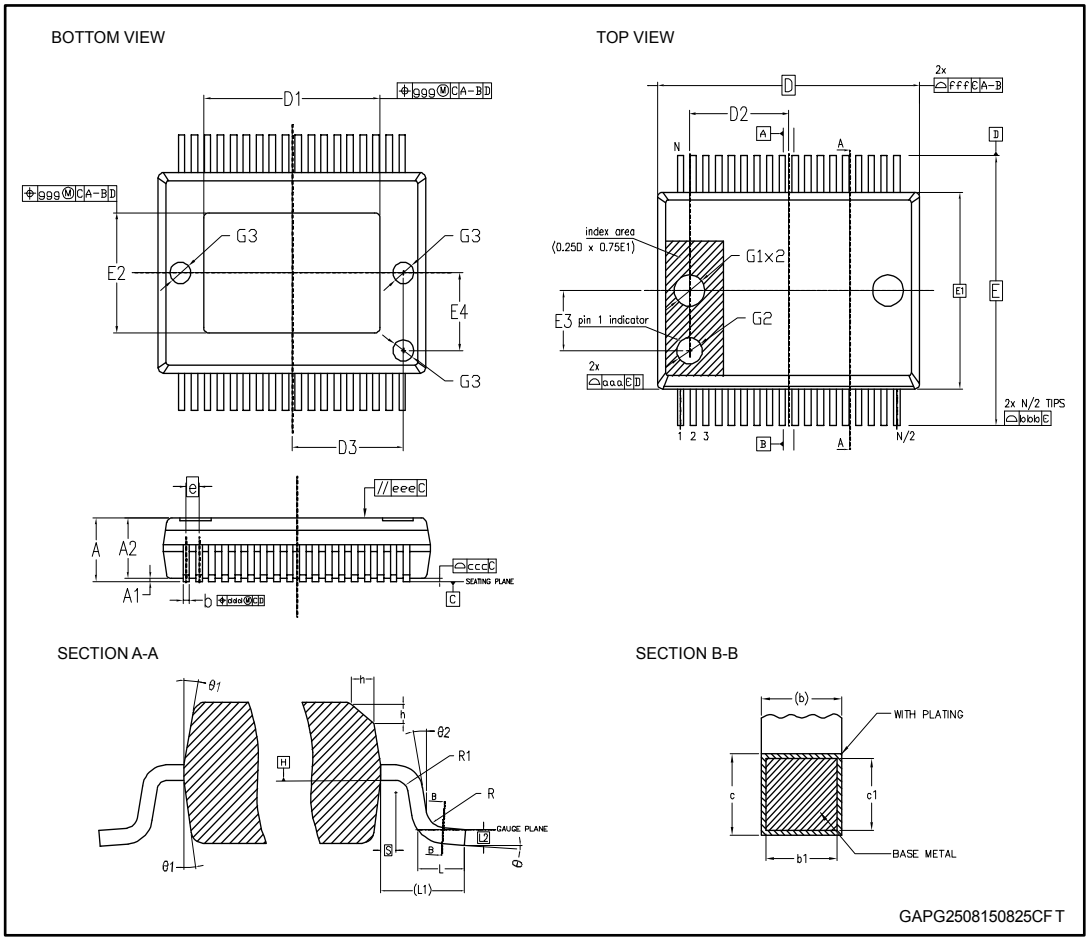


Table 16: PowerSSO-36 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	5°		10°
Θ2	0°		
A	2.15		2.45
A1	0.00		0.10

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A2	2.15		2.35
b	0.18		0.32
b1	0.13	0.25	0.30
c	0.23		0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	6.90		7.50
D2		3.65	
D3		4.30	
e	0.50 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.30		5.20
E3		2.30	
E4		2.90	
G1		1.20	
G2		1.00	
G3		0.80	
h	0.30		0.40
L	0.55	0.70	0.85
L1	1.40 REF		
L2	0.25 BSC		
N	36		
R	0.30		
R1	0.20		
S	0.25		
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
eee	0.10		
fff	0.20		
ggg	0.15		

7.2 PowerSSO-36 packing information

Figure 45: PowerSSO-36 reel 13"

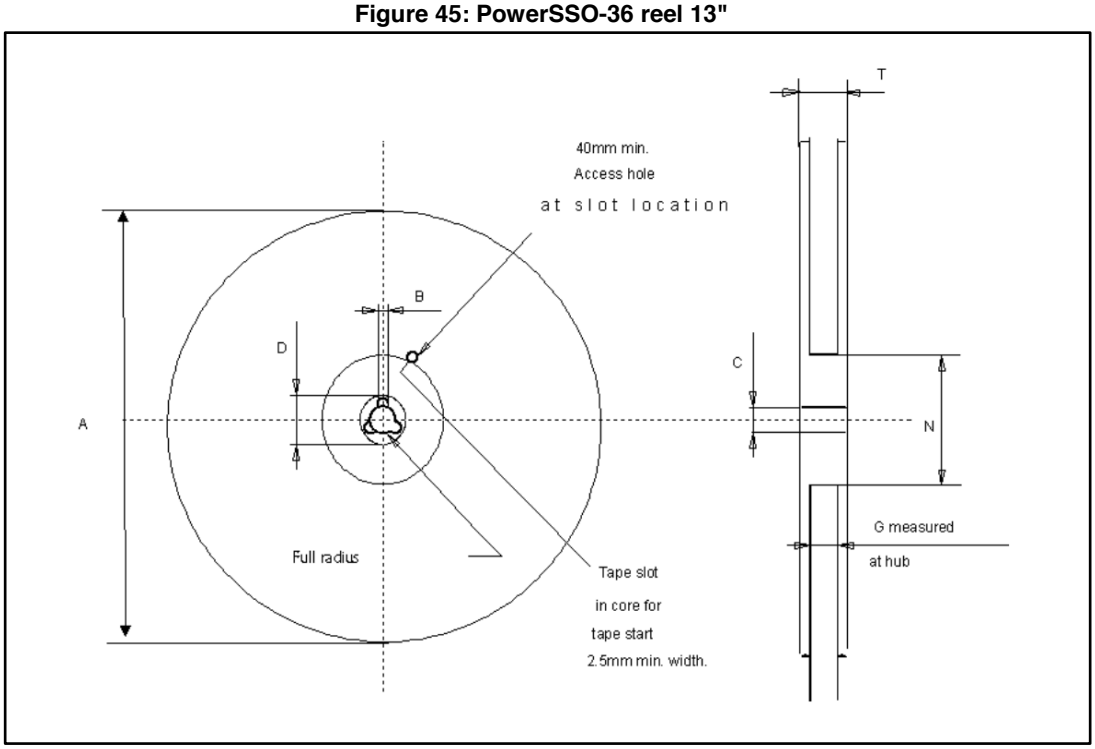


Table 17: Reel dimensions

Description	Value[1]
Base quantity	1000
Bulk quantity	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

Notes:

(1)All dimensions are in mm.

Figure 46: PowerSSO-36 carrier tape

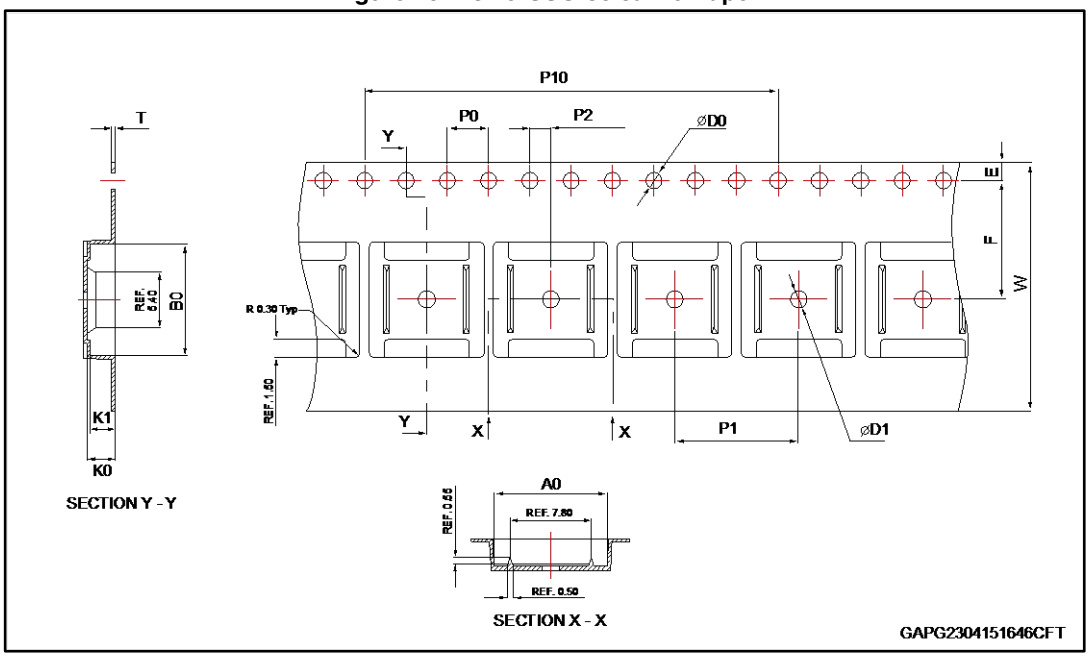


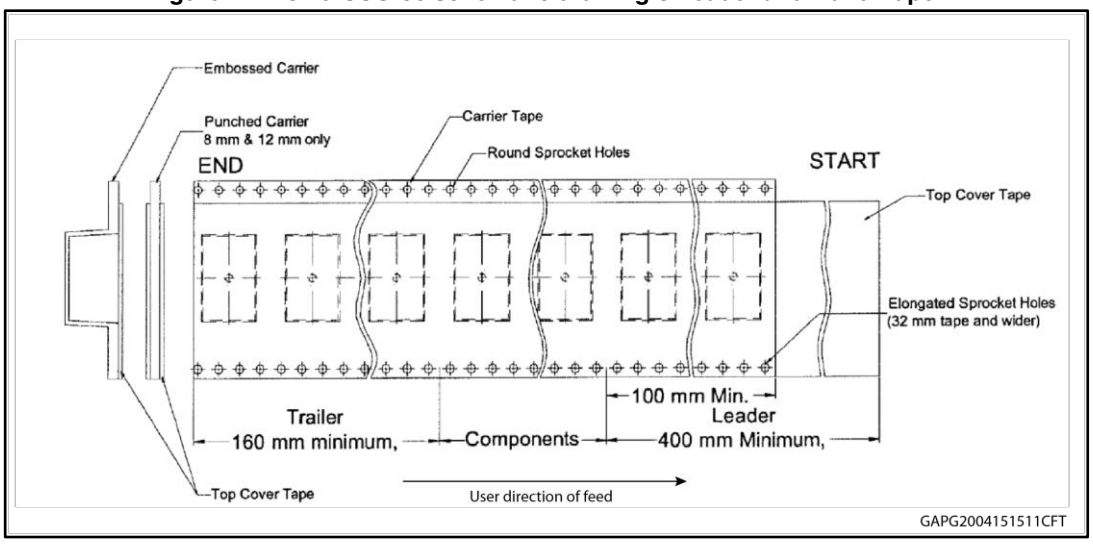
Table 18: PowerSSO-36 carrier tape dimensions

Description	Value[(1)]
A_0	10.90 ± 0.10
B_0	10.80 ± 0.10
K_0	2.75 ± 0.10
K_1	2.45 ± 0.10
D_0	1.50 (+0.10 / -0)
D_1	1.60 ± 0.10
P_0	4.00 ± 0.10
P_1	12.00 ± 0.10
P_2	2.00 ± 0.10
P_{10}	40.00 ± 0.20
E	1.75 ± 0.10
F	11.50 ± 0.10
W	24.00 ± 0.30
T	0.30 ± 0.05

Notes:

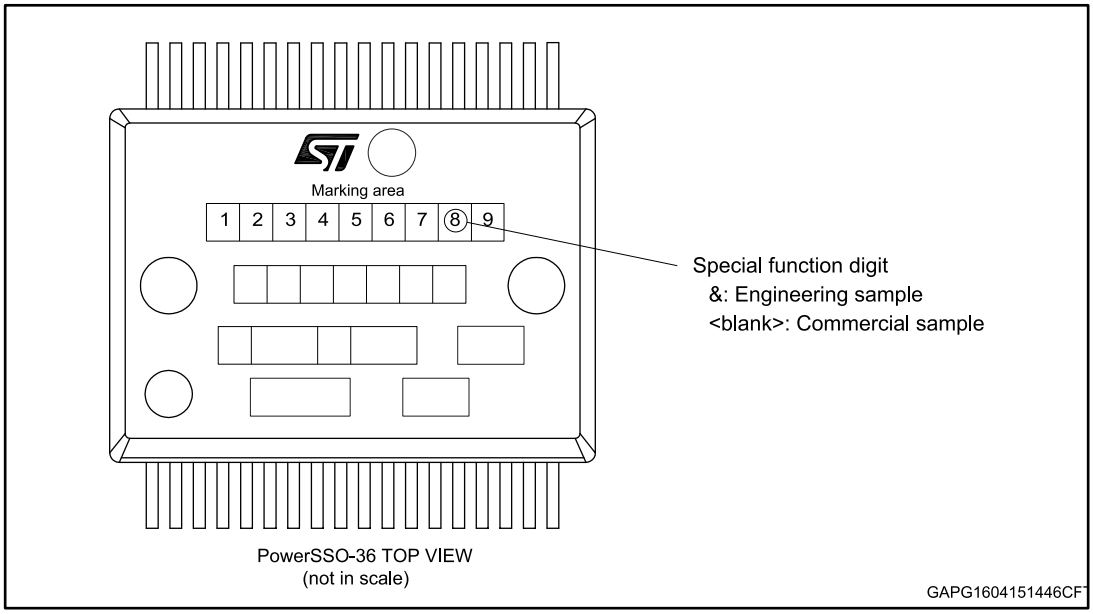
(1)All dimensions are in mm.

Figure 47: PowerSSO-36 schematic drawing of leader and trailer tape



7.3 PowerSSO-36 marking information

Figure 48: PowerSSO-36 marking information



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8 Order codes

Table 19: Device summary

Package	Order codes
	Tape and reel
PowerSSO-36	VND7004AYTR

9 Revision history

Table 20: Document revision history

Date	Revision	Changes
23-Apr-2015	1	Initial release.
20-Jul-2015	2	*Table 3: "Absolute maximum ratings"*: • $-I_{OUT}$: updated value Updated *Table 4: "Thermal data"* and *Table 6: "Switching"* *Table 8: "Protections"*: • T_R, T_{HYST}: added note *Table 9: "MultiSense"*: • K_0, dK_0/K_0: removed rows • K_x, dK_x/K_x, I_{OUT_SAT}: updated values Added *Section 5: "Package and PCB thermal data"*
30-Jul-2015	3	Updated *Figure 1: "Block diagram"* Updated *Table 1: "Pin functions"* *Table 3: "Absolute maximum ratings"*: • I_{SENSE}: updated parameter and value • E_{MAX}: updated parameter *Table 5: "Power section"*: • R_{ON_REV}: updated value *Table 9: "MultiSense"*: • V_{SENSE_CL}, V_{SENSE_TC}, V_{SENSE_VCC}: updated test conditions Removed following tables: • Table: Electrical transient requirements (part 1) • Table: Electrical transient requirements (part 2) • Table: Electrical transient requirements (part 3) Added *Section 4: "Application information"*
02-Dec-2015	4	*Table 5: "Power section"*: • I_{STBY}, $I_{L(off)}$: updated values Updated *Table 6: "Switching"* *Table 9: "MultiSense"*: • K_x, $t_{DSENSE2H}$: updated values Added *Section 2.5: "Electrical characteristics curves"*
27-Jan-2016	5	*Table 9: "MultiSense"*: • I_{SENSE0}: updated value

Date	Revision	Changes
20-Apr-2016	6	Updated Features list *Table 3: "Absolute maximum ratings"*: • E_{MAX}: updated value *Table 9: "MultiSense"*: • dK_x/K_x, I_{SENSE_SAT}, I_{OUT_SAT}: added note Added *Section 6: "Maximum demagnetization energy (VCC = 16 V)"*
26-Apr-2016	7	Updated *Figure 1: "Block diagram"* and *Figure 34: "MultiSense and diagnostic – block diagram"*
15-Jul-2016	8	Updated *Figure 45: "PowerSSO-36 reel 13""*and *Table 17: "Reel dimensions"*
02-Nov-2016	9	Updated Applications section

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