Architecture Development and Implementation of a Synchrophasor-based Real-time oscillation damping Control System

Eldrich Rebello
Department of Electrical Engineering and Automation
Aalto University
Espoo, Finland
Email: eldrich.rebello@aalto.fi

Homer Simpson
Kungliga Tekniska högskolan
Stockholm, Sweden
Email: luigiv@kth.se
tre

Md. Shoaib Almas
Kungliga Tekniska högskolan
Stockholm, Sweden
Email: msalmas@kth.se

***Abstract*—Low-frequency, electromechanically induced, inter-area oscillations are posing an increasing threat to the stability of the modern, interconnected power grid. Wide Area Monitoring, Protection and Control (WAMPAC) systems based on wide-area measurements such as synchrophasor (C37.118) data can be deployed to address the inter-area oscillation problem. This work develops a hardware prototype of a synchrophasor-based oscillation damping control system. A Compact Reconfigurable Input Output (cRIO) controller from National Instruments is used to develop the real-time prototype. This paper presents the design process followed for the development of the software architecture. The three step process followed viz. design proposal, design refinement and finally attempted implementation is detailed. The goals of the design, the challenges faced and the refinements necessary are also presented. The design implemented is tested and validated on OPAL RT's eMEGASIM real-time simulation platform and a brief discussion of the results is also included.**

I. Introduction

The goal of this paper is to document the architecture development process and challenges faced in the real-time implementation of Ängquist and Gama's [2] Phasor Power Oscillation (Phasor POD) algorithm. The developed prototype is termed a Wide Area Power Oscillation Damper [1] (WAPOD). For purposes of comparison, the real-time SIMULINK implementation of the Phasor POD algorithm by Almas and Vanfretti [9] is used as a benchmark. The performance of the hardware prototype developed will be tested and compared to the performance of this implementation of the algorithm. The two-area four-machine model developed by Klein, Rogers and Kundur [3] is used as a test-case and is modified to fit the requirements of this work. A Hardware-in-the-loop setup is constructed around the eMEGASIM real-time simulator from OPAL-RT [10] with the two-area model running in real-time and a synchrophasor-based Phasor-POD algorithm running on a cRIO (Figure 1).

[1]Historically, damping stabilizers have been termed WAPOD where the P represents a measurement of active power through the line. Active power here would be used as a controller input signal. Although this term is not accurate when other quantities are used as control inputs or feedback signals, the term is used here to maintain consistency with existing literature.

A. Background

The growth of power system interconnections between previously unconnected areas has given rise to the phenomenon of inter-area oscillations. These are low frequency (0.1-2 Hz.) oscillations where the generators of one synchronous area oscillate against those of another area. Damping for these oscillations is generally poor and if they are allowed to grow, they can lead to disconnection of the ties or a collapse of the power system. A famous example of the latter was the August 1996 blackout of the WSCC system in the USA [**?**]. Although the purpose of system interconnection was to increase stability, the present situation of the power system incorporates renewable energy sources and power trading corridors, both of which impact system stability.

B. Previous Experiences

Modern solutions to this problem involve using Power System Stabilisers (PSS) with locally available signals. These are effective at damping intra-area modes with good observability but may not be as effective at damping inter-area modes [7] [8]. A theoretical analysis of the advantages of using wide-area signals as a damping input is presented in [15]. Field-test experiences with WAPOD controllers from Norway and China are presented in [4] and [5] respectively.

C. Paper Outline

This paper is organised as follows.
II presents this and that.
III presents

II. Background

A. Phasor POD Algorithm

The Phaso-POD algorithm was developed by Ängquist and Gama [2] and forms the core of this work. The algorithm was selected due to its wide applicability and the fact that it does not depend on network topology. Typical model-linearisation based damping algorithms rely on intensive calculations and

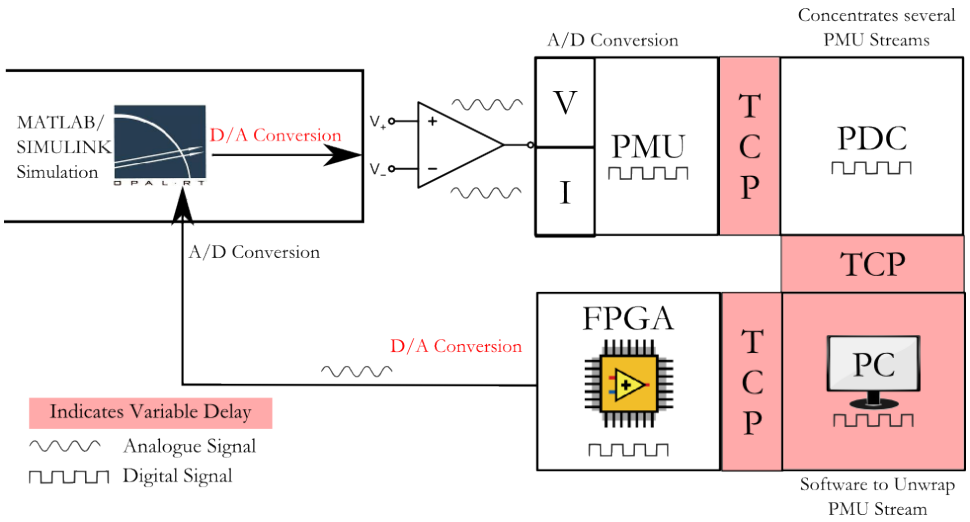

Fig. 1. General Outline for data flow with digital and analogue components indicated

are typically valid for a particular network operating point. The Phasor-POD algorithm only requires knowledge of the inter-area oscillation frequency, which is generally known from system studies or can be determined from synchrophasor measurements. In the two-area network used here, the inter-area oscillation frequency is known to be 0.64Hz. Consider Equation 1 which is a representation of a general signal $s(t)$, as an average valued component and an oscillating component.

$$s(t) = s_{avg} + \mathrm{Re}\left\{\vec{s}_{ph} \cdot e^{j^{wt}}\right\} \tag{1}$$

$\vec{s}_{ph}$ is a complex phasor, rotating at the frequency ω [2]. The Phasor-POD algorithm uses the known oscillation frequency to set up a co-orindate system rotating at this frequency and continuously extracts a phasor representing the magnitude of oscillation [2]. This extracted signal can subsequently be used as a modulating input to a controllable device such as a FACTS device or a generator's AVR system. The implementation of the algorithm used here is based on Almas and Vanfretti's Simulink implementation [9] and uses three inputs : the search frequency, ω_{cs1}, the sampling time T_s, the phase correction $alpha$ in addition to a signal scaling factor.

B. Hardware and Software Used

Real-Time Controller: The real-time implementation of the Phasor-POD algorithm in this work is based on the Compact Reconfigurable Input Output (cRIO) from National Instruments. The cRIO 9081 [16] is used for the implementation of the algorithm. It has an onboard Field Programmable Gate Array (FPGA) in addition to a 1.06 GHz. Intel Celeron processor for real-time control applications [16].

Phasor Measurement Units: The inputs to the real-time controller would come from a C37.118-compliant synchrophasor data stream. Measurement data for this stream would be generated by two PMU's which monitor three-phase currents and voltages at different points on the power network. In this work, two cRIO9076 real-time controllers [17] were deployed as PMU's.

Real-Time Simulator: The eMEGASIM real-time simulator from OPAL RT [6] was used for simulating the two-area network in real-time. This simulator allowed for hardware-in-the-loop tests to be carried out using its analogue input and output terminals. Voltage and current signals were extracted from the simulator's analogue outputs and fed to analogue amplifiers. These amplified signals were then wired to the current and voltage inputs of PMU's. Similarly, the damping signal generated by the Phasor-POD algorithm was then wired back to the simulator's analogue input terminals for use in the simulation. Figure 1 presents the entire signal path including the external, closed-loop control.

Software: The test-case network model used here was based on a SIMULINK demo available with SimPowerSystems. This was modified to include an average-valued SVC model, identical to that used in [9]. The SIMULINK model was modified and prepared for real-time simulation. Software code for the cRIO was written using LabView's Real-Time modules. OPAL RT's eMEGASIM platform uses MATLAB code and SIMULINK models. Software development was done on a workstation computer. Code was loaded on the various devices (cRIO contollers, RT Simulator) over a TCP network.

III. Architecture Development Process

Before beginning the development process, a software development methodology was adopted with the aim of streamlining the process. **(Why this method and not others??)**

The approach followed here is based on the Waterfall method detailed in [11]. The approach broadly includes the four steps from [11] viz.

1) Initial Investigation
2) Requirements Definition
3) Architecture Design
4) Coding and Implementation

The linear waterfall method was modified to be iterative so as to account for various constraints and to also account for revisions in the initial definition caused by these constraints. This iterative process is illustrated in Figure 2.

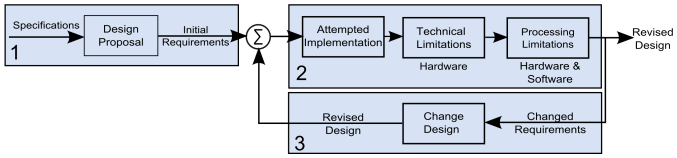

Fig. 2. Iterative Revision Flow Diagram

Several reasons were behind the choice of an iterative design approach. Chief among them was the cRIO hardware itself. As an implementation on this hardware had not been attempted earlier, the limitations of the hardware were unknown. Based on the limitations faced during an implementation attempt, the design and features incorporated would be revised to fit within the limitations of the hardware.

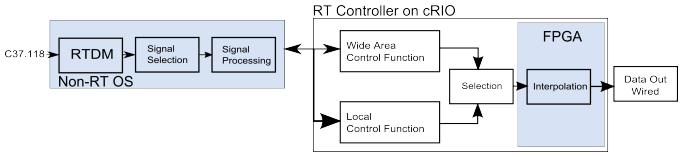

Fig. 3. Iterative Revision Flow Diagram

A. Constraints

Before defining requirements at each stage of the software implementation, the possible constraints at each stage of the test set-up were considered. The test set-up shown in Figure 1 is used to illustrate the constraints faced.

Differing Loop Rates: The power system simulation running on the real-time simulator was run at a loop rate of 50μs. This meant that the simulator would generate new values for currents and voltages every 50μs. and would also expect data from the HIL system every 50μs. The constraint here was the data reporting rate of the PMU's used which was a maximum of 50 samples per second or one sample every 20ms. This was much slower that the 50μs. loop rate of the real-time simulator. A solution would be required for this.

FPGA Accuracy: Something about this here.

IV. Architecture Implementation and Refinement

Figure 2 shows the three stage design process with design proposal, implementation and revision. To begin with, only the controller specifications were available. These were used to draft a design proposal. An implementation attempt was made using this draft proposal. When the additional limits imposed by the software and hardware platforms were included, some goals of the original code would have to revised. With these limitations, the original design was modified to generate a revised design. An attempt was then made to implement this revised design. If further limitations were encountered, the design was further modified. This iterative process was repeated till a working implementation was reached.

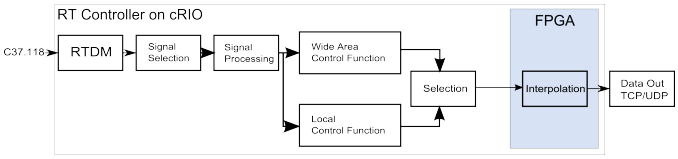

Fig. 4. Initial Software Architecture

1) Initial Design: Initially, the goal was to keep the controller (the cRIO) independent of any other devices. Such a controller would be able to receive synchrophasor data (in the C37.118 format) directly over the communication network (ethernet) and extract measurement data. The architecture block diagram is shown in Figure 4. This controller was completely autonomous, with automated signal selection and processing. This design would be able to compute observability indices for the different input signals and then automatically select the one with the highest observability of a particular mode. This design also incorporated two control functions, a wide area control function and a local control function. The wide area control function selected for implementation was the phasor-based oscillation damping control algorithm [2]. The local control function would use locally available data and implement the control function in a manner similar to a Power System Stabiliser (PSS). Automatic switching between the two functions was also considered. If the signal to noise ratio in the wide area signal deteriorated or if the signal delay became prohibitively high, the controller would switch to the local signal or a back-up wide area signal automatically. The principal consideration in this design was the limited resources available on the FPGA and the complexity of the algorithms to be implemented. This required implementation of all algorithms and computation sections on the RT section of the cRIO. In addition, the RT controller chosen has tremendous flexibility as algorithms are implemented using software, rather than hardware as on the FPGA. The RT controller also has more storage space available to implement algorithms. The trade-off was computation speed.

This design was faced with a problem of differing loop rates. The real-time simulator runs at a 50μs time step. The RT controller on the cRIO is not capable of matching this speed. The fastest that it could run was 1ms. Data would thus

be generated faster than the RT controller was able to process. The second problem was producing control output at the rate expected by the real-time simulator. The speed constraint of the RT controller meant that it would not be possible to use it (the RT controller) to generate this control signal. To address this issue, this architecture envisaged using the FPGA to perform interpolation between successive data points. The FPGA would run at a loop rate of 50 microseconds, to match the real-time simulator. The region between successive data points would be interpolated using a suitable interpolation algorithm. Data generated by the FPGA would be sent over the communication network back to the real-time simulator for use in the simulation.

This design was changed due to limitations of different components. One, no software was available to receive a synchrophasor stream and extract measurement data on the RT controller. This process had to be performed on a desktop computer running a real-time data mediator [19] and LabVIEW. Once measurement data from the synchrophasor stream was available, it could be streamed to the real-time controller over the TCP/IP network.

Two, data generated by the FPGA could not be sent to the real-time simulator directly over the communication network. Though theoretically possible using a FIFO[2] buffer, further work is required. Also, for each succesive data point received by the real-time controller, the FPGA would generate 400, interpolated data points. Synchronising the process of generating the control signal and using the generated data on the real-time simulator will be a complex task.

Three, the process of data interpolation on the FPGA is complex. To achieve results better than with a simple linear interpolation, a history of past data points is required. This process is in itself complex and also introduces further delay. However, it is simpler than implementing the damping control algorithm on the FPGA. At this stage, FPGA limitations were the principal factor behind chosing to implement the Phasor-POD algorithm on the RT controller.

Four, an algorithm for automated signal selection based on observability indices had not been developed. In principle, this too, is possible and can be implemented on the real-time controller in the future when such an algorithm is developed and verified to work. The Phasor POD algorithm input paramaters also change depending on the input used. An approach to determine these parameters iteratively or calculate them from input data is required. This only adds to the complexity.

2) Development and Revision: With the limitations of the initial architecture in mind, it was revised. In this architecture, the process of extracting data from the synchrophasor stream was shifted to a workstation computer. The process of signal selection and signal processing was also moved to this computer. Once data was available, it would be sent to the RT controller, over a communication network. The damping control was kept on the RT controller with the FPGA performing the interpolation required to match the read-interval of the real-time simulator. Besides the damping control algorithm, a local control function was maintained on the RT controller. This revision is shown in Figure 5.

Here, the complexity of implementing an interpolation algorithm on the FPGA was examined in detail. An implementation was also attempted. It was determined that a simple linear interpolation algorithm would not be sufficiently accurate. Further, the FPGA output was limited by the speed of the RT controller as new data would only be available after a minimum of 1ms at the least (if the RT controller were to run at its maximum speed).

An implementation of the damping control algorithm on the RT controller was also tested. The fastest execution speed that could be achieved was in excess of 25ms. This was slower than the reporting rate of the PMUs.

Communication between the cRIO and the RT simulator using TCP/IP was also abandoned. Output values of the FPGA were instead hardwired to the real-time simulator's analogue inputs.

3) Final Implementation: At this stage, the damping control algorithm was moved to the FPGA with the RT controller being used only for network communication and data monitoring. The RT controller would only receive measurement data continuously over the network. Phasor POD algorithm parameters and monitoring data would be sent periodically. The local control function was also discarded as it was found to reduce the response speed of the RT controller. If needed and if space permits, the local control function can be implemented on the FPGA. The FPGA is suited to tasks that are repetitive in nature and has a fast and predictable response time. The desired 50μs. data rate could also be maintained as the FPGA was capable of response times of this order. The problem of differing data and loop rates was sloved by implementing a basic sample-and-hold algorithm on the FPGA. Data would still be received from the RT controller every 20 ms. but the output would be held constant till the next data point was received and proceses. With the Phasor POD algorithm implemented on the FPGA, resource utilization stood at 78%. Space was still available if further functions need to be implemented on the FPGA. As with the previous design, the process of extracting data from the synchrophasor stream was done on a workstation computer. Signal selection and processing was also done on this computer. This (Figure 6) was the final architecture as implemented.

[2]First In First Out

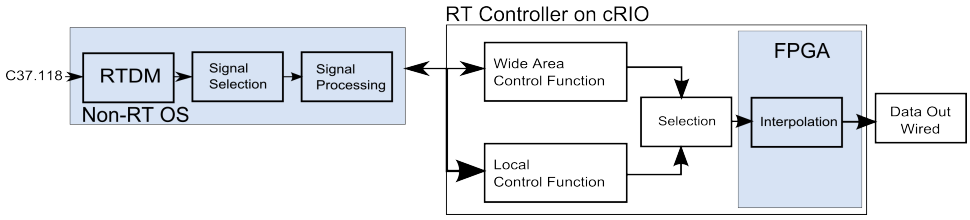

Fig. 5. Revised Architecture

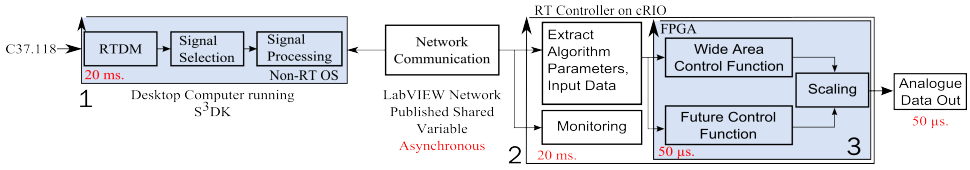

Fig. 6. Final Controller Architecture as Implemented

V. Hardware-in-the-Loop Test

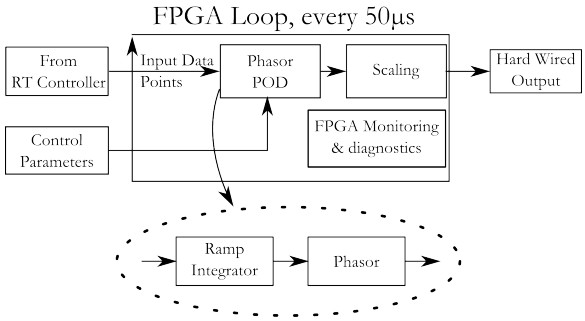

Fig. 7. Architecture Refinement Schematic

VI. Conclusion

The conclusion goes here.

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