

Reviewer Response

1. The figures could have a better graphic quality, though.

Response : Figures have been replaced with higher quality, embedded PDF's. Architecture development figures have been grouped into a single figure and the quality improved. Only the oscilloscope image remains as a bitmapped file for obvious reasons.

2. However, due to the simulation environment constraints, particularly the required 50us rate, design decisions were directly impacted.

Response : The 50 μ s response rate was not the only limitation in this particular design. Though it did influence the final architecture implementation, it was one among many contributing factors.

3. Thinking in a real world application, it should be shown what the rate of the output signal should be. This information, requirement, should be expected to be known and informed in the paper, so that the simulation environment could replicate more correctly the real conditions, whenever possible. Or at least to point out that.

Response : Addressed, with a footnote on Page 3 that reads : In a real-life application, the controller output may not have this constraint. However, the subsequent control system must sample the WAPOD controller's output at a rate faster than the PMU reporting rate.

Explanation : The 50 μ s sampling rate was a constraint imposed by the real-time simulator. Real-world control systems are not expected to have such a high sampling rate.

3. Last but not least, Software Architecture doesn't seem to be appropriate in this context. There is a solution that involves software & hardware. The development process and design decisions were detailed. High level component view diagrams were presented, but that alone does not necessarily configure a Software Architecture. Other detailed and more elaborated diagrams would be expected from a software engineering perspective. In this regard, I would suggest to just quit the term Software Architecture from the title.

Response. Title Changed to *PMU-based Real-Time Damping Control System Software and Hardware Architecture Synthesis and Evaluation*

Thank you for taking the time to read through this paper and, most importantly, for your constructive feedback. We hope you are satisfied with the changes we have made.

Regards,
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