Experimental Framework for Testing Synchrophasor-based Damping Control Systems

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***Abstract*—Wide-Area Power Oscillation Damping (WAPOD) controllers using IEEE C37.118 data have been proposed, developed and deployed in the field and are showing promise. This paper details the development, construction and implementation of a real-time, Hardware-in-the-loop (HIL) test set-up for such a controller. The set-up is based around the eMEGASIM real-time simulator from OPAL-RT. A general purpose, phasor-based control algorithm is implemented on a Compact Reconfigurable Input/Output (cRIO) controller from National Instruments. The complete, closed-loop set-up, the hardware used and the reasons for design choices are also documented. Since this test-set-up uses IEEE C37.118 data over a TCP/IP network, the complete data path is examined. A test-case HIL test with the designed controller is also presented and the results are examined.**

I. Introduction

A. Motivation

Instances such as the Northeast blackout of August 2003 and the August 1996 Western North America (WECC) [1] blackout have been significant events on large, interconnected power systems. Both can be attributed, in part, to low frequency, electromechanically induced, inter-area oscillations [1]. These oscillations involve the generators of one synchronous area oscillating against the generators of another area and are typically between 0.1-2Hz in frequency. The fact that these modes are poorly damped [2] presents a danger to power systems with interconnections used for purposes such as power trading. Inter-area oscillations are also a threat to the stability of grids with significant generation coming from renewable energy sources.

B. Previous Experiences

The phenomenon of intra-area oscillations is well documented and has modern solutions such as Power System Stabilisers (PSS) exist and are in use. A PSS uses locally available signals and might not be very effective at damping inter-area modes with poor local observability [4] [3]. Wide-area control systems as implemented in Norway [2] and China [5] have extended the control system of an existing device to receive and use synchrophasor (IEEE C37.118) data.

C. Contributions

The goal of this paper is to document the details of the design and construction of a real-time test set-up for a wide-area control system. Ängquist and Gama's [6] Phasor Power Oscillation (Phasor POD) algorithm was implemented on a Compact Reconfigurable Input-Output controller (cRIO) [11] from National Instruments which is then tested with a inputs from a two-area model [9] running in real-time. The entire physical test set-up is examined together with constrainsts of the present implementation. The results from one HIL experiment are also presented. This setup can serve as a starting point for future HIL tests that involve real-time, synchrophasor-based controllers.

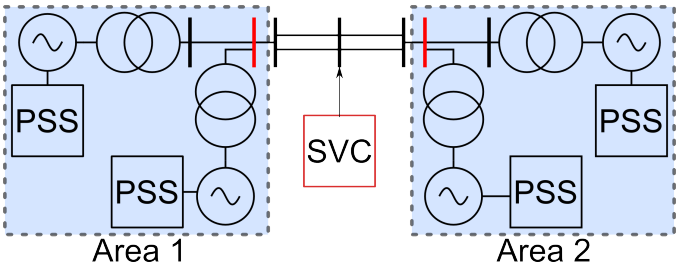

Fig. 1. Two-area model including SVC

II. Background

A. Two-Area Model & Phasor POD

The Phasor-POD algorithm essentially separates an input signal into average-valued and oscillating components [6]. The oscillating component, when suitably phase-shifted can act as a damping input to a controllable device. This algorithm has been demonstrated to work with a two-area model (see Figure 1) where it acts as a modulating input to a flexible AC transmission system (FACTS) device [8]. The SIMULINK implementation of the Phasor-POD algorithm as presented in [8] was re-written in LabView and deployed on a cRIO9081.

B. Controller Architecture

Figure 2 details the three-layer controller architecture as implemented. The two-area model runs in real-time on the OPAL-RT simulator. Phasor Measurement Units (PMUs) are connected to the analogue outputs of the real-time simulator. The synchrophasor data stream that these PMUs generate is parsed on a desktop computer (Label 1 in Figure 2). This data is then sent over a TCP/IP network to the cRIO running the control algorithm. The Phasor-POD algorithm is implemented

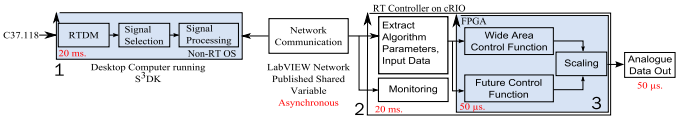

Fig. 2. Three layer controller architecture as implemented

on the cRIO's FPGA which generates an analogue damping signal.

C. SmarTS Lab

All the hardware and software detailed in this work is available in the SmarTS Lab at KTH, Stockholm. For full details of the lab, all its equipment and capabilities, the reader is referred to [14]. This work only presents the hardware that form part of the HIL test described here and only touches upon their capabilities.

III. Hardware & Test Setup

Figure 4 presents the data path and a simplified outline of the entire HIL test conducted. This setup was arrived at after several changes to the design necessitated by limitations of the hardware and software. These are covered in the next section.

1) OPAL-RT Simulator: The eMEGASIM real-time simulator from OPAL-RT [10] was the core of the HIL test. The simulator ran the two-area SIMULINK model in real-time and allowed for interfacing hardware with the model through its analogue input and output terminals. Details of these terminals are below.

- **Analogue Outputs** : Number: 32 (+/-16V and +/-10mA)
- **Analogue Inputs** : Number: 128 (+/-100V and +/-10mA)

The simulator would calcualate and update values for all variables in the two-area model every 50μs. This time step was selected to allow for the assumption of linearity of power system parameters. Updated values would be written to the analoge outputs and input values read at the analouge inputs every 50μs. The SIMULINK model was developed and edited on a workstation computer and the same computer was used to monitor output from the simulator while the model was running.

Fig. 3. cRIO9081 showing NI9225, three-channel, analogue voltage input module and seven empty add-on module slots

2) cRIO Real-Time Controllers: Two different cRIO models were used in this particuar HIL test. One model, the cRIO9081, was used to run the Phasor-POD algorithm in real-time. Two cRIO9076s were deployed as PMUs. Figure 3 shows the cRIO9081 with an analogue voltage input add-on module connected. The data generated by the Phasor-POD algorithm was sent as an analogue signal back to the real-time simulator.

PMUs: Two cRIO9076s were used as PMUs, each with a four-channel, analogue voltage input module and a three-channel, analogue current input module. The inputs to the PMUs were three-phase currents and voltages and a GPS signal for time-sync. PMU software from National Instruments was run on both. The synchrophasor stream from each PMU was sent to a Phasor Data Concentrator (PDC). Each generated a C37.118 synchrophasor data stream which was sent over a TCP/IP network. The reporting rate of the PMUs was 20ms meaning that new measurements were available every 20ms. Though it was possible to generate synchrophasor data from the real-time simulator, the option of using analogue signals was chosen as it mimicked a real-world scenario.

Real-Time Phasor-POD Algorithm: The FPGA of a cRIO9081was used to run the Phasor-POD algorithm in real-time. Though the cRIO9081 has a real-time controller in addition to the FPGA, the latter was chosen to run the Phasor-POD algorithm. This was because the FPGA runs at 400Mhz and is thus capable of a determinsitic response time in the order of nanoseconds. The loop rate chosen was 50μs so that the data output rate of the FPGA was identical to the read rate on the real-time simulator's input.

3) Analogue Signal Amplifiers: The SMRT1 Single Phase Relay Tester [15] from Megger was used as an analogue signal amplifier. Each individual amplifier had a single current and single voltage input. To drive the inputs of two PMUs, six amplifier units were required. The inputs to the amplifiers were the low-level analogue signals extracted from the real-time simulator. The outputs of the amplifiers were wired to the analogue input modules of the PMUs. Table I lists the ratios used.

TABLE I
AMPLIFIER INPUTS AND OUTPUTS

	Input, from simulator	**Amplified Output**
Voltage	$\pm 10V$	$\pm 100V$
Current	$\pm 20mA$	$\pm 1A$

4) Phasor Data Concentrator: The Phasor Data Concentrator (PDC) consisted of a network connected desktop computer running PDC software from SEL. The PDC was used to allow for data from multiple synchrophasor streams to be manipulated and used.

IV. Hardware Design Choices

V. Hardware-in-the-Loop Test

A setup identical to that outlined in Figure 4 was constructed and used to verify the working of the hardware WAPOD. The hardware implementation of the POD algorithm was verified to be able to keep the system stable in steady state. It was also tested with small perturbations applied at one generator to excite the inter-area mode and was verified to

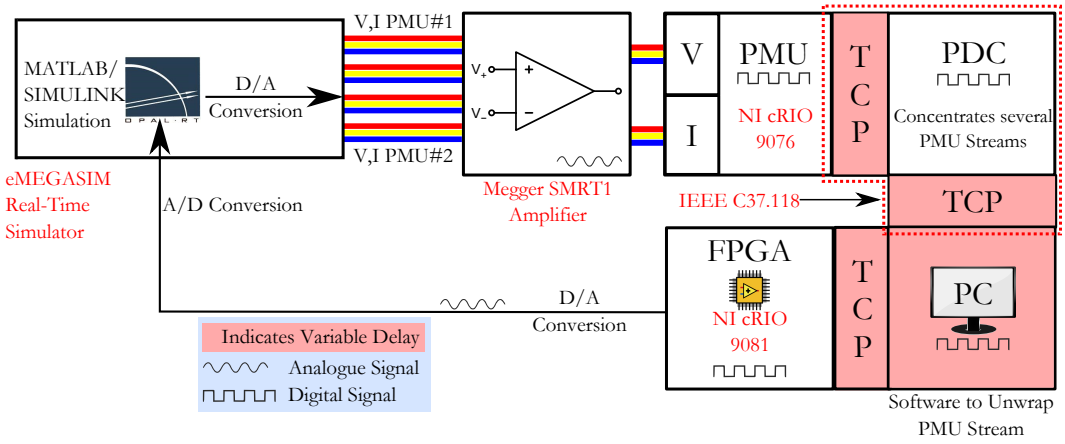

Fig. 4. Data path in HIL test. Hardware used is indicated in red text.

work satisfactorily. Figure **??** shows the performance of the controller with two different inputs,active power and voltage angle difference. It is immediately evident that using the voltage angle difference provides better performance.

REFERENCES

[1] North American Electric Reliability Council *Review of selected 1996 Electric System Disturbances in North America,* August 2002. Available Online: http://www.nerc.com/pa/rrm/ea/System\%20Disturbance\%20Reports20DL/1996SystemDisturbance.pdf

[2] K. Uhlen, L. Vanfretti, M.M. De Oliveira, A.B. Leirbukt,V. H. Aarstrand and J. O. Gjerde *Wide-Area Power Oscillation Damper implementation and testing in the Norwegian transmission network* in Power and Energy Society General Meeting, 2012 IEEE pp. 1-7

[3] M. E. Aboul-Ela, A. A. Sallam, J. D. McCalley and A. A. Fouad, *Damping Controller Design for Power System Oscillations Using Global Signals*, IEEE trans. on Power Systems, Vol. 11, No. 2, May 1996, pp. 767-773

[4] L. Vanfretti, Y. Chompoobutrgool, and J.H. Chow, *Chapter 10: Inter-Area Mode Analysis for Large Power Systems using Synchrophasor Data*, Book Chapter, in Coherency and Model Reduction of Large Power Systems, Joe H. Chow (Ed.), Springer, 2013.

[5] Li Peng and Wu Xiaochen and Lu Chao and Shi Jinghai and Hu Jiong and He Jingbo and Zhao Yong and Aidong Xu *Implementation of CSG's Wide-Area Damping Control System: Overview and experience* in Power Systems Conference and Exposition, 2009. PSCE '09. IEEE/PES pp. 1-9

[6] L. Ängquist and C. Gama *Damping Algorithm based on Phasor Estimation* in Power Engineering Society Winter Meeting, 2001. IEEE, Volume 3, pp. 1160 - 1165

[7] M.Crow, M. Gibbard, A. Messina, J. Pierre, J. Sanchez-Gasca, D. Trudnowski, D. Vowles *Identification of Electromechanical Modes in Power Systems* IEEE Task Force Report, Special Publication TP462, June2012.

[8] M. Shoaib Almas and L. Vanfretti, *Implementation of Conventional PSS and Phasor Based POD for Power Stabilizing Controls for Real-Time Simulation*, IEEE IES IECON14, 29 Oct-1 Nov, 2014, Dallas, USA.

[9] M. Klein, J. G. Rogers and P. Kundur *A fundamental study of inter-area oscillations in Power Systems* IEEE Trans, PWRS, no. 6, pp. 914-921, 1991.

[10] eMEGAsim PowerGrid Real-Time Digital Hardware in the Loop Simulator Opal RT, [Online]. Available: http://www.opal-rt.com/

[11] *Operating Instructions and Specifications Compact RIO NI cRIO-9075/9076 & NI cRIO-9081/9082*, National Instruments, Available Online at http://www.ni.com/

[12] M. Paolone, A. Borghetti, C. A. Nucci, *A Synchrophasor Estimation Algorithm for the Monitoring of Active Distribution Networks in Steady State and Transient Conditions*, Proc. of the 17th Power Systems Computation Conference (PSCC 2011), Stockholm, Sweden, Aug. 22-26, 2011

[13] Kamwa I. (Hydro-Quebec) "Performance of Three PSS for Interarea Oscillations" Available Online at : http://www.mathworks.se/help/physmod/sps/examples_v2/performance-of-three-pss-for-interarea-oscillations.html

[14] M.S. Almas, M. Baudette, L. Vanfretti, S. Lovlund and J.O. Gjerde "*Synchrophasor network, laboratory and software applications developed in the STRONg^{2}rid project*," PES General Meeting, Conference Exposition, July 2014 IEEE pp 1 - 5

[15] SMRT1 Single Phase Relay Test System Data Sheet, Available Online http://www.megger.com/common/documents/SMRT1_DS_en_V10.pdf Retreived 22.12.2014, 2014 © Megger

[16] L. Vanfretti, V.H. Aarstrand, M. Shoaib Almas, V. S. Perić and J.O Gjerde *A Software Development Toolkit for Real-Time Synchrophasor Applications*, IEEE PES Grenoble PowerTech, 2013