Experimental Framework for Testing Synchrophasor-based Damping Control Systems

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***Abstract*—Wide-Area Power Oscillation Damping (WAPOD) controllers using IEEE C37.118 data have been proposed, developed and deployed in the field. This paper details the development, construction and implementation of a real-time, Hardware-in-the-loop test set-up for such a controller. The set-up is based around the eMEGASIM real-time simulator from OPAL-RT. A general purpose, phasor-based control algorithm is implemented on a Compact Reconfigurable Input/Output (cRIO) controller from National Instruments. The complete, closed-loop set-up, the hardware used and the reasons for design choices are also documented. Since this test-set-up uses IEEE C37.118 data over a TCP/IP network, the complete data path is examined. A test-case HIL test with the designed controller is also presented and the results are examined.**

I. Introduction

A. Motivation

Instances such as the Northeast blackout of August 2003 and the August 1996 Western North America (WECC) [1] blackout have been significant events on large, interconnected power systems. Both can be attributed, in part, to low frequency, electromechanically induced, inter-area oscillations [1]. These oscillations involve the generators of one synchronous area oscillating against the generators of another area and are typically between 0.1-2Hz in frequency. The fact that these modes are poorly damped presents a danger to power systems with interconnections used for purposes such as power trading. Inter-area oscillations are also a threat to the stability of grids with significant generation coming from renewable energy sources.

B. Previous Experiences

The phenomenon of intra-area oscillations is well documented and has modern solutions such as Power System Stabilisers (PSS) exist and are in use. A PSS uses locally available signals and might not be very effective at damping inter-area modes with poor local observability [4] [3]. Wide-area control systems as implemented in Norway [2] and China [5] have extended the control system of an existing device to receive and use synchrophasor (IEEE C37.118) data.

C. Contributions

The goal of this paper is to document the details of the design and construction of a real-time test set-up for a wide-area control system.

II. Architecture Development Process

The software development approach followed here is based on the Waterfall method detailed in [15]. The linear waterfall method was modified to be iterative to account for various constraints and to also account for revisions in the initial definition caused by these constraints. This iterative process is illustrated in Figure **??**, sub-figure 1 and is realised for the specific application here, as illustrated in Figure **??**, sub-figure 2.

A. Constraints

III. Architecture Implementation and Refinement

Figure **??**, sub-figure 1 shows the three-stage design process with design proposal, implementation and revision. To begin with, the controller specifications were used to draft a design proposal. An implementation attempt was made using this draft proposal. When the additional limits imposed by the software and hardware platforms were included, some goals of the original implementation needed to be revised. With these limitations, the original design was modified to generate a revised design. An attempt was then made to implement this revised design. As further limitations were encountered, the design was further modified. This iterative process was repeated till a working implementation was reached.

1) Initial Design Proposal: Initially, an autonomous, independent controller was envisaged. Such a controller would be able to receive IEEE C37.118 synchrophasor data directly over the communication network and extract measurement data (Figure **??**, sub-figure 2). This design also incorporated two control functions, a wide area control function and a local control function. The wide area control function was the Phasor POD [6]. The local control function would use locally available data in a manner similar to a Power System Stabiliser (PSS). Automatic switching between the two functions and automated input signal selection was also considered. If the signal to noise ratio in the wide area signal deteriorated or if the signal delay became prohibitively high, the controller would automatically switch to the local signal or another wide-area signal. The principal consideration in this design was the limited resources available on the FPGA and the complexity of the algorithms to be implemented. This required implementation of all algorithms and computation sections on

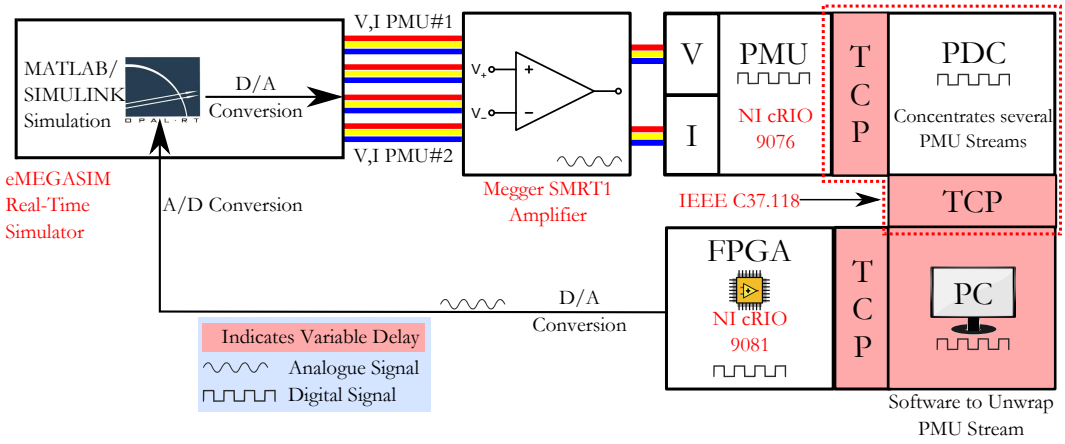

Fig. 1. Data path in HIL test. Hardware used is indicated in red text.

the RT section of the cRIO with the FPGA being used for interpolation only.

2) Development and Revision: With the limitations of the initial architecture in mind, the architecture was refined. The process of extracting data from the synchrophasor stream was shifted to a workstation computer along with the processes of signal selection and processing. Once data was available, it was sent to the RT controller, over the network. The damping control was kept on the RT controller with the FPGA performing the interpolation required to match the read-interval of the real-time simulator. Besides the damping control algorithm, a local control function was included on the RT controller. This revision is shown in Figure **??**, sub-figure 3. Here, the complexity of implementing an interpolation algorithm on the FPGA was examined in detail. An implementation was also attempted. It was determined that a simple linear interpolation algorithm would not be sufficiently accurate. An implementation of the damping control algorithm on the RT controller was also tested. The fastest loop rate that could be achieved was always in excess of 25ms. This was slower than the reporting rate of the PMUs. Communication between the cRIO and the RT simulator using TCP/IP was also abandoned. Analogue output signals of the FPGA were instead hard-wired to the real-time simulator's analogue inputs.

3) Final Implementation: At this stage, the damping control algorithm was moved to the FPGA with the RT controller being used only for network communication and data monitoring. The Phasor POD algorithm parameters and monitoring data would be sent over the network to the RT section of the controller. The local control function was also discarded. The desired 50μs. data output rate could also be maintained as the FPGA was capable of response times of this order. The problem of differing data and loop rates was solved by implementing a basic sample-and-hold algorithm on the FPGA. With the Phasor POD algorithm implemented on the FPGA, resource utilization stood at 78%. As with the previous design, the process of extracting data from the synchrophasor stream was done on a workstation computer. This (Figure **??**) was the final architecture as implemented.

IV. Hardware-in-the-Loop Test

A setup identical to that outlined in Figure **??** was constructed and used to verify the working of the hardware WAPOD. The hardware implementation of the POD algorithm was verified to be able to keep the system stable in steady state. It was also tested with small perturbations applied at one generator to excite the inter-area mode and was verified to work satisfactorily. Figure **??** shows the performance of the controller with two different inputs,active power and voltage angle difference. It is immediately evident that using the voltage angle difference provides better performance.

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