DISCUSSION MEET
8:30 P

Abstract

One sentence approach
Power oscillation damping ?
WAMS (PMUs) for damping ?
Hardware prototype of POD based on phasor based power oscillation damping algorithm & deployed in NI-cRIO.
RT-HIL approach to evaluate performance of developed controller using emegasim Opal-RT & its interface with real PMUs (hardware). Challenges, limitations & lesson learnt are discussed.

INTRODUCTION

Paper presents NI-cRIO based POD. PMU data set ovailable. Detailed Simulink model Kundur. Executed in RT. Interfaced with hardware PMUs. Phasor based POD algorithm deployed in cRIO. cRIO provide signal to FACTs and/or AVR.

Section II – Background

Section III – Software + Hardware architecture + RT-HIL execution + model used + SVC model

Section IV – Results with AVR / FACTS

Section V – Challenges, lesson learnt, discussion, future work

Section VI – Conclusion

Background

One sentance - small signal stability issue + comments from Luigi + Discussion of lead-lag based controllers.

→ Requirement for modularity, fast prototyping, phasor POD with equation & figure

Section III HIW SIW Configuration

First = Model Kunder + Model SVC figures + Scenarios

Second = POD Algorithm in cRIO (Labview)

Third = Realization in HIW

Fourth = Complete Testbench (cRIO + Opal) picture

Section IV

Results

(i) SVC / FACTS

Figure 1 = different PMU inputs + Oscillo scope

Table 1 = overshoot, damping, settling time etc

(ii) AVR

Figure 2 = PMU inputs

Table 2 = overshoot etc

Section V

- Challenges
  - i) delay (You need network figure) OPNET etc
  - ii) Noise SNR, SNID
  - iii) Loop Rates Figure Page 40 Thesis
  - iv) solution of loop rates

Paragraph for future work

(i) Adoptive /optimal signal selection
(ii) Opnet System in loop (delays)
(iii) ABB ECS RT-HIL

Conclusion

- cRIO POD
- tested thoroughly
- possible improvements
- stepping stone for future research

References

- No appendix
- No modifications