

# Real-Time Implementation of Synchrophasor-based Wide-Area Power Oscillation Damping Control System

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**Abstract**—The modern power grid is increasingly being used under operating conditions of increasing stress for which it was not designed. The increasing penetration levels of variable energy sources such as wind present significant power grid stability issues. One of these stability issues is the phenomenon of low frequency, electro-mechanically induced, inter-area oscillations. Simulations have demonstrated the potential of Wide Area Measurement Signals (WAMS) -based Power Oscillation Damping (POD) in achieving improved electromechanical mode damping compared to traditional, local signal based, Power System Stabilizers (PSS). This paper takes an established Phasor-based oscillation damping method and combines it with modern PMU technology to implement a hardware prototype of a real-time oscillation damping control system using remote PMU signals sent over a communications network. The developed prototype is tested in a real-time Hardware-in-the-loop approach in conjunction with the Klein-Rogers-Kundur two-area four-machine test system and is demonstrated to have applications independent of the controlled device.

**Keywords**—*IEEEtran, journal, synchrophasor, PMU, damping control, Wide Area measurement and control*

## I. INTRODUCTION

THE goal of this paper is to demonstrate both the potential and flexibility in oscillation damping controller design that is provided by using synchrophasors. The Phasor Power Oscillation Damping algorithm originally developed by Ångquist and Gama [1] is run on a National Instruments Compact Reconfigurable Input / Output (cRIO) real-time controller. A slightly modified, SIMULINK model of the four-machine, two-area network developed by Klein-Rogers and Kundur [2] is run on the eMEGASIM [3] platform from OPAL RT. This allows interfacing an externally generated control signal with the simulated model in real-time. A HIL<sup>1</sup> test is set up to verify the performance of the hardware implementation of the Phasor POD algorithm. The flexibility of the developed controller is also demonstrated by extracting various data from the synchrophasor input and using each as a damping input to the controller. That the controller can have

multiple applications is demonstrated by testing it with two different controlled devices; a generator AVR and a FACTS device excitation system. A brief analysis of the performance of each input is also presented.

Section II presents a brief background of the work together with the hardware and software architectures implemented.

## II. BACKGROUND

As modern power systems grow in size, both in terms of power transfer capacity and geographic spread, they are increasingly being used for purposes that the power system was not designed for. Examples of these ‘new’ uses include conditions of increasing stress such as power trading between countries. These interconnections, which link synchronous generators, often separated by vast physical distances, create conditions where small disturbances can excite oscillations that may or may not settle. When the generators of one area oscillate at a low frequency (typically 0.2–2.5Hz) against the generators of another interconnected, but distinct area, ‘inter-area’ oscillations may start.

Although the purpose of system interconnection was to increase stability, the present situation of the power system incorporates renewable energy sources and power trading corridors, both of which impact system stability. More modern solutions to the problems of inter area and intra oscillations use Power System Stabilizers (PSS) [4]. While a PSS provides excellent damping to intra area modes with good local observability, its performance with intra-area modes may not be satisfactory [5].

### A. Previous Experiences

One important reason for choosing the Phasor-POD algorithm for real-time implementation was the fact that the algorithm uses few inputs and is independent of network configuration and topology. The only algorithm parameter that is network-dependent is the oscillation frequency and this is usually known from system studies. Compared to conventional, linearisation-based controllers, the adoption of phasor-based controllers has not been high mainly due to the fact that such controllers tend to be highly non-linear and thus difficult to model in simulation studies [16].

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<sup>1</sup>Hardware-in-the-loop

### B. Hardware Architecture

The Wide Area Power Oscillation Damper (WAPOD)<sup>2</sup> prototype developed here uses commercially available micro-controller hardware and is based entirely on PMU measurements received over a TCP/IP network. The Phasor-POD algorithm [1] will be implemented on a general purpose micro-controller and will be run in real-time. The inputs to the controller will come from one or multiple PMU's, each monitoring data at different points in the power system. The power system model used in this paper is the two-area four-machine model, originally proposed by Klein, Rogers and Kundur [2]. To prove the real-world applicability of the developed controller, all tests are carried out in real-time, with conditions such as noise and network transport delay present.

All real-time simulations here are performed on OPAL RT's eMEGASIM [7] real-time simulation platform. SIMULINK models are executed in real-time and are interfaced with externally generated signals. Current and voltage signals from different points on the simulated network are extracted, amplified and then supplied as the input to two PMU's. Two cRIO-9076 [13] devices are used as PMU's. The synchrophasor data stream from these devices is streamed over a TCP/IP network to a Phasor Data Concentrator which produces a time-aligned output stream. This stream is then accessed, via a TCP/IP network, on a PC running LabVIEW which extracts raw measurement data. This extracted data is streamed over the network to a cRIO-9081 which runs the Phasors-POD algorithm in real-time. The FPGA on the cRIO-9081 [12] generates a damping signal which is then wired to the real-time simulator for use in the SIMULINK model.

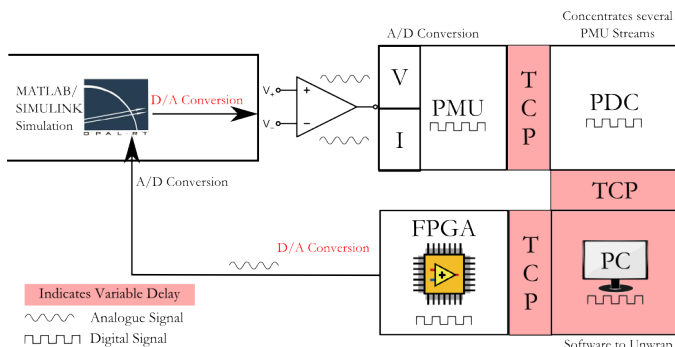


Fig. 1. Hardware Outline

Vanfretti et. al. describe the details of the equipment used here in [9]. It is important to note that the data flow in Figure 1 involves both D/A and A/D conversions. Also, since no synchronisation is used for these conversions, it is

<sup>2</sup>Historically, damping stabilizers have been termed WAPOD where the P represents a measurement of active power through the line. Active power here would be used as a controller input signal. Although this term is not accurate when other quantities are used as control inputs or feedback signals, the term is used here to maintain consistency with existing literature.

important that the sample rates or loop rates of each section be integer multiples of each other. This will prevent data value errors. The issue of different loop rates is covered in Section VI-C.

### C. Software Architecture

The two-area four-machine model used here is available in SIMULINK's SimPowerSystems and can be accessed by typing `power_PSS` as a MATLAB command. The SIMULINK implementation of the Phasor-POD algorithm was developed by Almas and Vanfretti [6]. The Phasor-POD algorithm essentially separates an input signal into an average valued and an oscillating component. The oscillating component when suitably phase-shifted can be used as a supplementary damping input to a generator's AVR or the excitation system of a FACTS device.

LabVIEW's Real Time and FPGA modules were used to write the code for the respective sections of the cRIO. Also, since no synchrophasor data-extraction software was capable of running independently on the RT controller, the process of extracting raw measurement data from the synchrophasor data stream was performed on a desktop computer. The software used for this was identical to that in [15] and would run on a workstation computer, extract data from the PMU stream and send this extracted data to a LabVIEW program running on the same computer [15].

#### D. Real-Time Implementation of Phasor-POD Algorithm

The hardware implementation of the POD was based on the Compact Reconfigurable Input / Output (cRIO) 9081 [12] from National Instruments. This controller is equipped with an on-board Field Programmable Gate Array (FPGA) running at 400MHz in addition to an independent real-time controller. The real-time implementation of the Phasor-POD algorithm was based on the SIMULINK implementation by Almas & Vanfretti [6] and its goal was the replicate the behaviour of the SIMULINK implementation as closely as possible. The algorithm accepts three inputs; the search frequency,  $\omega_{cs1}$ , the sampling time  $T_s$ , the phase correction  $\alpha$  and a signal scaling factor. It takes advantage of the fact that the oscillation frequency for a given network configuration is usually known, which in this case is the 0.64Hz inter-area mode. Using this known frequency value, a co-ordinate system, rotating at this known frequency, is set up where the oscillating component is continuously extracted as a phasor [1].

A three-layer, modular code architecture, based on an available template [14] was selected for implementation. An outline of the architecture is shown in Figure 2 and each of the three layers are outlined below.

- Core FPGA Software : Interacts with hardware terminals for I/O and runs Phasor-POD algorithm

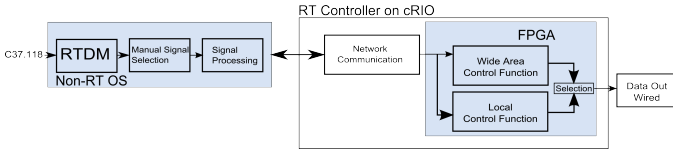


Fig. 2. RT Controller Architecture

- Real Time (RT) Software : Manages network communication to remote terminal and also generates performance monitoring data
- Remote Interface: Runs on workstation computer: Used to update algorithm parameters and monitor data & performance. This layer is non deterministic.

The Phasor-POD algorithm could be implemented on either the real-time section of the cRIO or the FPGA but was implemented on the FPGA. This decision was made keeping in mind the computational resources and response speed needed to match the step size of the real-time simulator. The complexity of the code meant that the cRIO's real-time controller would not be able to complete an iteration of the algorithm in the required  $50\mu\text{s}$  response time. The real-time section of the cRIO handles network communication. Its primary purpose is to receive measurement data that the workstation computer extracts and to stream this data to the Phasor-POD algorithm running on the FPGA. The real-time controller also handles commands coming from the user interface running on the workstation computer. It also monitors the output of the FPGA, sends data to the user interface for monitoring, periodically logs input and output data and handles error conditions.

The remote interface runs in LabVIEW on a conventional Windows® based computer. The Phasor-POD algorithm can be controlled from this interface. Also, the algorithm parameters can be set and modified. Since the operating system here is not real-time but is multi-tasking, the execution speed depends on the processor load and is not deterministic. Statnett's Synchrophasor Software Development Kit ( $S^3DK$ ) was used to unwrap the PMU streams coming from the PDC and extract phasor measurements [15]. This allowed for data to be extracted and used directly in the LabVIEW environment. Since the PMU reporting rate was 50 messages a second, new data was available every 20ms. The loop rate used by the  $S^3DK$  was hence 20ms. The selection of an input for the controller and the computations required are performed here. For example, if active power is to be used as a POD input, voltage and current values must be multiplied to obtain the active power. If the voltage angle difference is to be used as an input, the required calculations are performed in this VI.

### III. SETUP PREPARATION

The nature of the Phasor-POD algorithm is generic enough to allow it to be used as a modulating input to a variety of controlled devices. Two examples are illustrated in this work,

one, as a generator AVR modulating input and the other as a modulating input to the excitation system of a FACTS device (here, an SVC<sup>3</sup>). Figure 4 illustrates both these uses along with the two-area network outline. Note that both possibilities are not implemented simultaneously.

#### A. Two-Area Model Preparation - Generator AVR

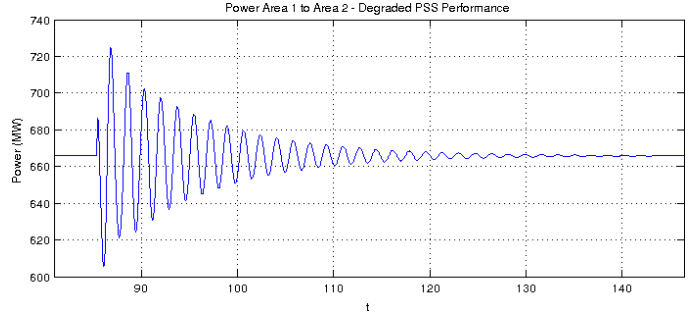


Fig. 3. Degraded performance with PSS

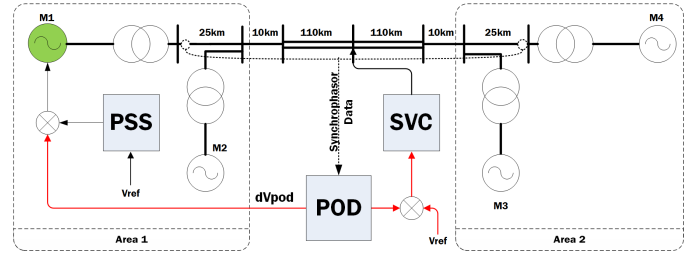


Fig. 4. Modified Two-Area Four-Machine network

The two-area network [2] is known to be unstable without external damping control. The difference between the rotational inertias of two of the machines, in an otherwise symmetric network gives rise to the 0.64Hz inter-area mode. The SIMULINK model used here implements damping control using a supplementary signal generated from a PSS and applied to the excitation system of each of the machines to achieve steady-state stability and also to damp out the inter-area mode. This model was modified to have a damping control system only at Machine M1 in Area-1 (see Figure 4). All other machines have their PSS's disconnected. This configuration was verified to be able to both achieve stability and to be able to restore the system to stability after the application (and subsequent clearing) of an 8 cycle, three-phase to ground fault. The original model uses a PSS tuned to achieve maximum damping, given the operating conditions. To demonstrate a potential application scenario for the developed POD prototype, the performance of the PSS is degraded so that it is still able to provide damping but takes substantially longer (Figure 3). This figure shows the system response to a 200ms perturbation in the voltage reference of machine M1. Note that under the action of the sole PSS at machine M1,

<sup>3</sup>Static VAR Compensator

the inter-area mode is damped and the system is restored to stability. This mimics a real-world situation where an already installed PSS whose performance has degraded over time due to changing network conditions or poor tuning.

### B. Two-Area Model Preparation - FACTS Device

The second application in Figure 4 is to use the WAPOD output as a modulating input to an SVC's excitation system. The two-area model was prepared for simulation in the same way as in the previous case except that the PSS at each machine was included. The SVC model used was an average valued model, identical to that used in [6]. The SVC was connected at the mid-point of the two area network. As proved by Chow and Larsen in [10], this is the point where voltage swings will be the greatest and also where the SVC can be most effective at damping power swings. As before, two parallel and identical implementations of the Phasor-POD algorithm were used, one implemented in SIMULINK and the other on the cRIO. Either could be switched in at a given time. It is important to note here that when the hardware-POD algorithm was switched in, the PSS's at each of the four machines were disconnected, leaving the SVC as the sole control and damping device in the network. The ability of the SVC to keep the network stable and also to restore it to stability was verified with an off-line simulation using the Phasor-POD implemented in SIMULINK. Also, the performance of the PSS's were not degraded as the Phasor-POD algorithm would not be running in parallel with them.

### C. Real-Time Simulation

The modified network in each case was grouped into sub-systems and prepared for simulation in RT-LAB. The simulation time step chosen was  $50\mu\text{s}$ . Outputs and inputs of the real-time simulator would be updated every  $50\mu\text{s}$ . Current and voltage measurements were taken from the points marked in Figure 4 and were extracted from the analogue outputs of the real-time simulator. The damping signal  $dV_{pod}$  in Figure 4 was generated at two points; one in the real-time simulation itself using a Simulink implementation of the Phasor POD algorithm and one externally on the cRIO. Both signals were generated simultaneously and either one could be switched in for use in the simulation.

## IV. TESTING & RESULTS

Testing the operation of the hardware prototype involved using the HIL<sup>4</sup> setup outlined in Figure 1 and verifying whether steady state stability could be maintained in the simulated two-area network. Once this was demonstrated, the inter-area mode was excited by changing the voltage reference  $V_{ref}$  of Machine M1. The oscillations caused by this disturbance would then be damped out by the PSS in tandem with the Phasor POD algorithm. The POD algorithm implemented in SIMULINK uses the locally available active power measurements as input.

In the case of the Generator PSS, this is the active power measured at the terminals of the generator. In the case of the SVC, the active power at the mid-point of the interconnecting line (also the point of connection of the SVC) is used as an input. The WAPOD prototype is also able to use this same signal as input in each case but can also exploit other data contained in the synchrophasor data stream.

### A. SVC Excitation Supplementary Input

Figure 5 illustrates the response of the hardware controller to a small disturbance at machine M1. This disturbance is a 5% change for 200ms in the reference voltage of the AVR. This is sufficient to excite the inter-area mode. The best damping performance is achieved using voltage angle difference as a damping input to the Phasor-POD algorithm. This supports the theoretical results predicted by Chompoobutrgool and Vanfretti in [11]. A frequency analysis of each of these responses shows that the dominant mode in each response is the 0.64Hz inter-area mode. This is evident in Figure 6, which presents the magnitude spectrum of the controller response with voltage angle as input.

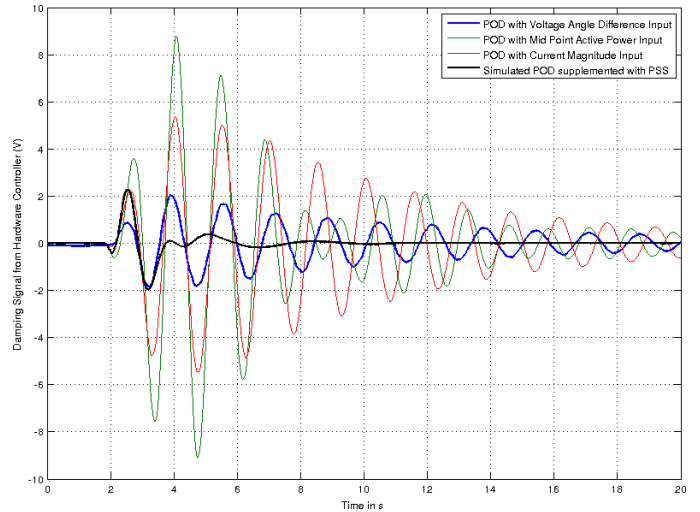


Fig. 5. Controller Response Comparison : Supplementary SVC Excitation Input

All data presented in Figure 5 was captured in the real-time simulator. Data was also recorded at other points such as at the PDC but these have a lower resolution and are not presented here. As further proof of the results presented in this work, the output of the hardware controller is captured directly and presented on an oscilloscope (Figure 7).

### B. Generator Excitation Supplementary Input

The controller response to a small disturbance when operating in tandem with a degraded PSS is shown in Figure 8. It is evident that the combination of the WAPOD and the PSS is significantly better than the PSS alone in every case. It can also be noted that the shape of the response shows a significant deviation from that in Figure 5, where the dominant

<sup>4</sup>Hardware in the Loop

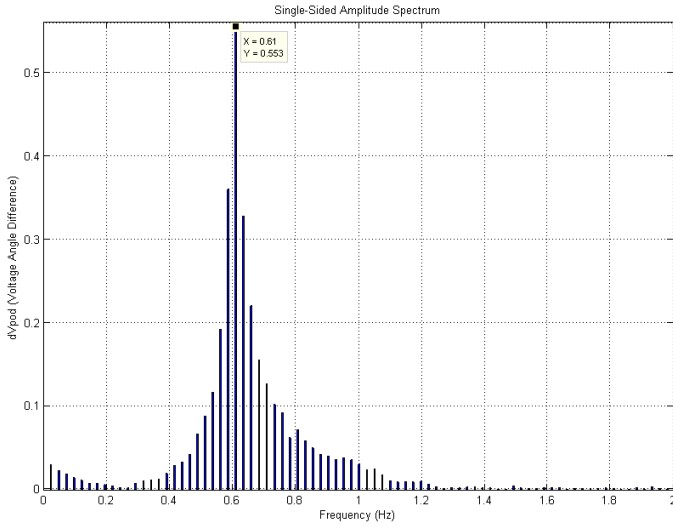


Fig. 6. Controller Response Comparison : Supplementary SVC Excitation Input

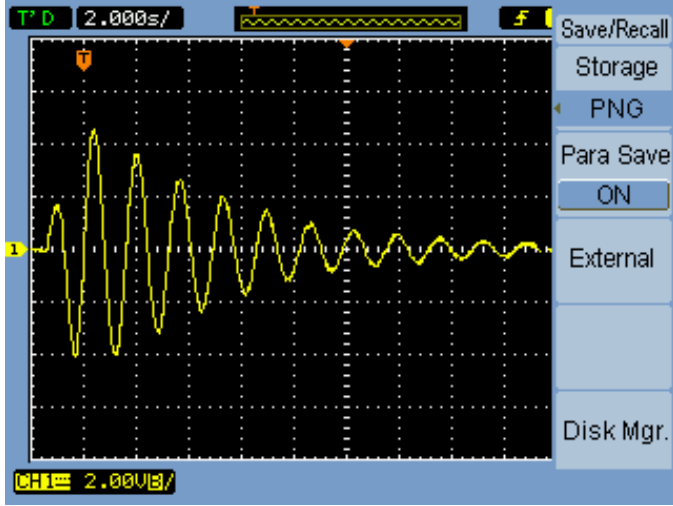


Fig. 7. Controller Response with Voltage Angle Difference input Captured on Oscilloscope

0.64Hz mode is clearly visible. Also evident from Figure 8 is the fact that the damping performance of the WAPOD changes significantly as its input is changed. Using the voltage angle difference as input provides the best performance. The performance with the simulated POD algorithm is not shown in Figure 8 for clarity, the performance of the WAPOD with the voltage angle difference input is very close to the performance of the simulated POD algorithm that uses active power as input. This performance is achieved despite the presence of a stochastic time delay and noise in the input measurements of the WAPOD. As in the case with the SVC, the theoretical results in [11] agree with the experimental results.

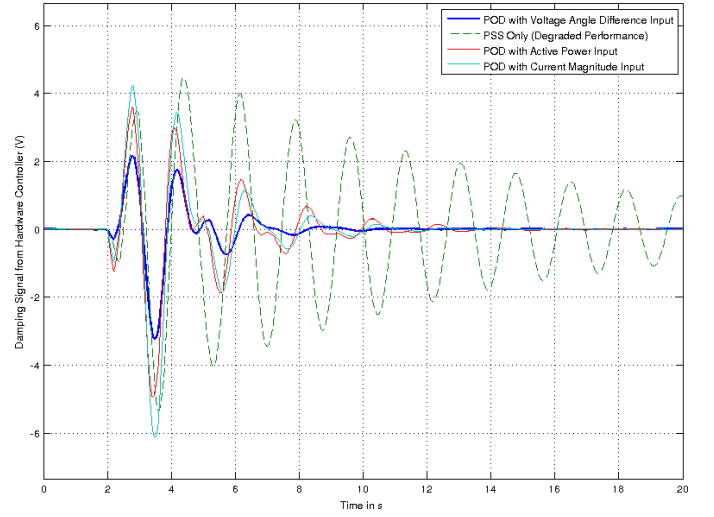


Fig. 8. Controller Response Comparison : Supplementary Generator Excitation Input

## V. ADDITIONAL INPUTS

### VI. CHALLENGES

#### A. Time Delays

The Phasor POD algorithm running in SIMULINK has close to zero time delay between network behaviour changing and the controller responding. The same algorithm, when run on the cRIO, receives data with a stochastic delay. Figure 1 illustrates the complete data path and from this, it is evident that several sources of time delay exist. Sections such as the analogue amplifiers, the FPGA execution speed (a constant  $50\mu\text{s}$ ), the real-time section of the cRIO and the PDC all represent fixed, non-zero time delays. Sections such as the D/A and A/D conversion in the real-time simulator also add a deterministic time delay. However, sections of the data path such as communication over a TCP/IP network and the PC used to extract raw measurement data from the synchrophasor stream all represent variable delays. These delays all contribute to a delayed response from the cRIO. This delay allows for a network disturbance to grow slightly before the cRIO starts responding. It also has the effect of changing the phase compensation required in the Phasor-POD algorithm. Though the delay cannot be compensated for, the phase compensation needed can be changed depending on the measured delay. Presently, the phase compensation required is determined iteratively though this can be automated using time-stamped data.

#### B. Analogue Limits and Noise

The original POD (Phasor Oscillation Damper) algorithm [1] was developed and simulated in an ideal, noise-free environment with zero delay. More importantly, no limits are imposed on the magnitude of either the controller's inputs or outputs when it is simulated. In contrast, a hardware-based implementation that uses analogue



signals is constrained by the analogue signal magnitude limits.

Consider the analogue outputs of OPAL RT's eMEGASIM simulator [7].

- **Analogue Outputs** : Number: 32 (+/-16V and +/-10mA)
- **Analogue Inputs** : Number: 128 (+/-100V and +/-10mA)

These are low level outputs and can be directly connected to the PMU inputs. However, the inputs modules of typical PMU's are rated for 0-300V and a 0-16V analogue signal will not use a significant portion of this range. Additionally, a signal of such a small magnitude will be contaminated by noise and will consequently have a poor Signal to Noise ratio. A similar argument can be made for the current outputs.

The output of the simulated POD can vary over several orders of magnitude, ranging from  $10^5$  at times of peak damping to as small as  $10^{-3}$  once the oscillation magnitude becomes small. It is difficult to accurately recreate analogue signals with such vast dynamic ranges. The voltage output module used with the cRIO here had a 24-bit resolution and was limited to 10V in magnitude. Any values generated by the POD algorithm that were greater in magnitude than 10V would cause output saturation. All these issues meant that signal magnitudes had to be amplified in certain cases to use the full measurement ranges or had to be limited in other cases, so as to capture variations without saturation.

### C. Loop Rates and FPGA Resources

The most significant challenge in the real-time implementation of the Phasor-POD algorithm was the fact that different sections of the hardware control loop run at different loop rates or step sizes. Added to this was the fact that the real-time simulator generated data every  $50\mu s$  and thus expected data from the HIL setup at the same rate while the rest of the HIL setup did not support such a high data rate. The PMU's used supported a maximum data reporting rate of 50 samples/second. Table I lists the different components of the HIL setup together with their respective loop rates.

TABLE I. COMPARISON OF LOOP RATES OF DIFFERENT COMPONENTS

Element	Loop Rate	Mode
OPAL RT Simulator	$50\mu s$	Real Time
PMU (cRIO)	20msec	Real Time
Workstation Computer	20msec	Not Real Time
POD - RT Section	20msec	Real Time
POD - FPGA	$50\mu s$	Real Time

$50\mu s$  was chosen for the FPGA loop rate in order to match the loop rate of the real-time simulator. This was to ensure that data was always available at the analogue input of the simulator and no erroneous data points were read. The  $50\mu s$  loop rate of the FPGA meant that new data was expected every  $50\mu s$ , corresponding to a 2000s/s sampling rate. The fastest execution speed of the real-time section of the cRIO was 1ms, significantly slower than the FPGA's speed. New

synchrophasor data was available from the PMU's only every 20ms. One solution to this problem was to upsample the synchrophasor data, interpolate between consecutive data points and then stream this data to the Phasor-POD algorithm on the FPGA. A FIFO<sup>5</sup> buffer would be used to buffer the data generated by the up-sampling process as it was gradually consumed by the FPGA. The major problem with this method was that the up-sampling process on the RT controller is computationally intensive and would not run at the required 20ms loop rate.

An alternative solution would be to implement a sample and hold algorithm on the FPGA. As data was extracted every 20ms, the RT controller would receive this data and send it to the FPGA. This value would then be held constant till the next data point arrives. This was implemented and found to work satisfactorily. In essence, the only difference between the Phasor-POD algorithm running the SIMULINK simulation and that on the cRIO was the data rates of their input data. The simulated POD received new data every  $50\mu s$  while the cRIO-based POD received data every 20ms.

## VII. FURTHER WORK

The WAPOD prototype as developed in this work demonstrates the possibilities of using wide area synchrophasor data for damping control. The prototype here is, however, dependent on manual input for signal selection and algorithm parameter values. These two processes can be automated by having the WAPOD itself monitor the various input signals and intelligently select the one having the highest observability of a particular mode. The algorithm parameters can also be determined adaptively on the WAPOD itself. On the same lines, this can further be extended to include selection among several measurement locations on the network. The fact that a stochastic time delay is introduced by unwrapping the synchrophasor data stream on a desktop computer can be addressed by performing this function on the WAPOD controller (here, the cRIO) itself.

## VIII. CONCLUSION

This work has demonstrated the feasibility of using wide-area power system data in the design of an oscillation damping controller. The generic nature of the developed controller was demonstrated by using an identical implementation with mere changes in parameters to suit the controlled device's input requirements and capabilities. The performance of the WAPOD can be improved by exploiting the full range of data available in a synchrophasor data stream. The flexibility of synchrophasor data was demonstrated and the wide range of inputs possible from this were also tested. The results from this work serve as a proof-of-concept to what?

## APPENDIX A

### PROOF OF THE FIRST ZONKLAR EQUATION

Appendix one text goes here.

<sup>5</sup>First In First Out

## APPENDIX B

Appendix two text goes here.

## ACKNOWLEDGMENT

The authors would like to thank...

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**Eldrich Rebello** Biography text here.