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-- Company:

-- Engineer:

-- Create Date: 00:38:27 04/01/2017

-- Design Name:

-- Module Name: fsm\_mealy\_mod - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity fsm\_mealy\_mod is

Port ( reset : in STD\_LOGIC;

clk : in STD\_LOGIC;

x : in STD\_LOGIC;

z : out STD\_LOGIC);

end fsm\_mealy\_mod;

architecture Behavioral of fsm\_mealy\_mod is

type state\_type is (S0, S1);

signal state, next\_state : state\_type;

begin

SYNC\_PROC : process (clk)

begin

if rising\_edge(clk) then

if (reset = '1') then

state <= S0;

else

state <= next\_state;

end if;

end if;

end process;

NEXT\_STATE\_DECODE : process (state, x)

begin

z <= '0';

case (state) is

when S0 =>

if (x = '1') then

z <= '1';

next\_state <= S1;

else

next\_state <= S0;

end if;

when S1 =>

if (x = '1') then

next\_state <= S0;

else

z <= '1';

next\_state <= S1;

end if;

when others =>

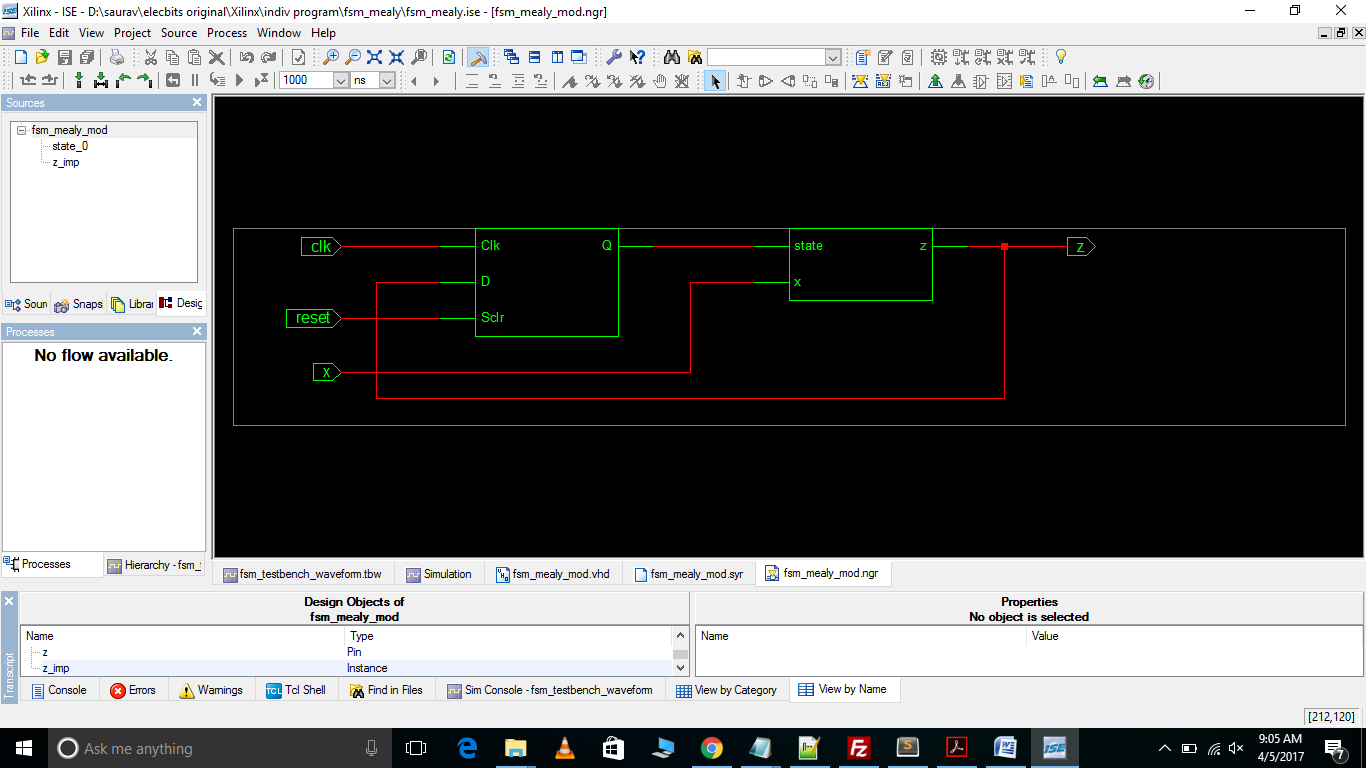
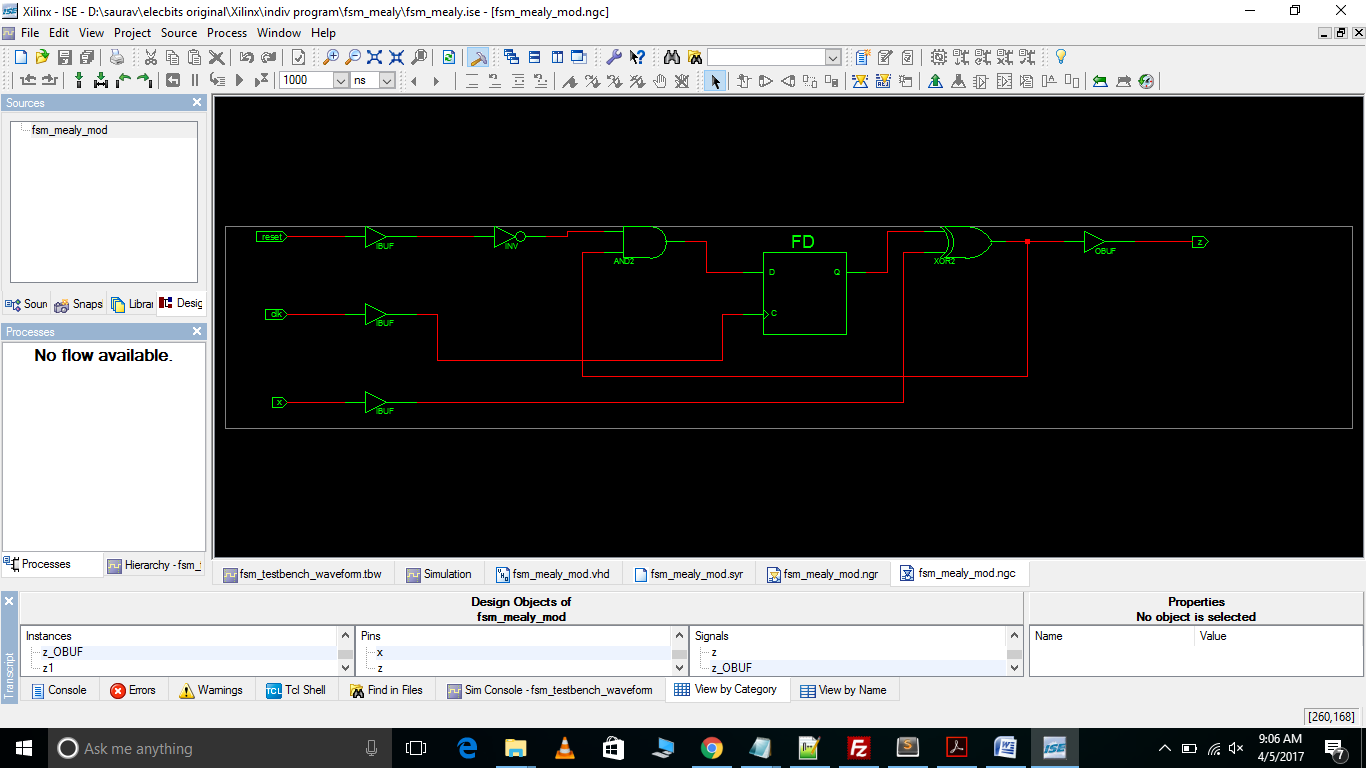
next\_state <= S0;

end case;

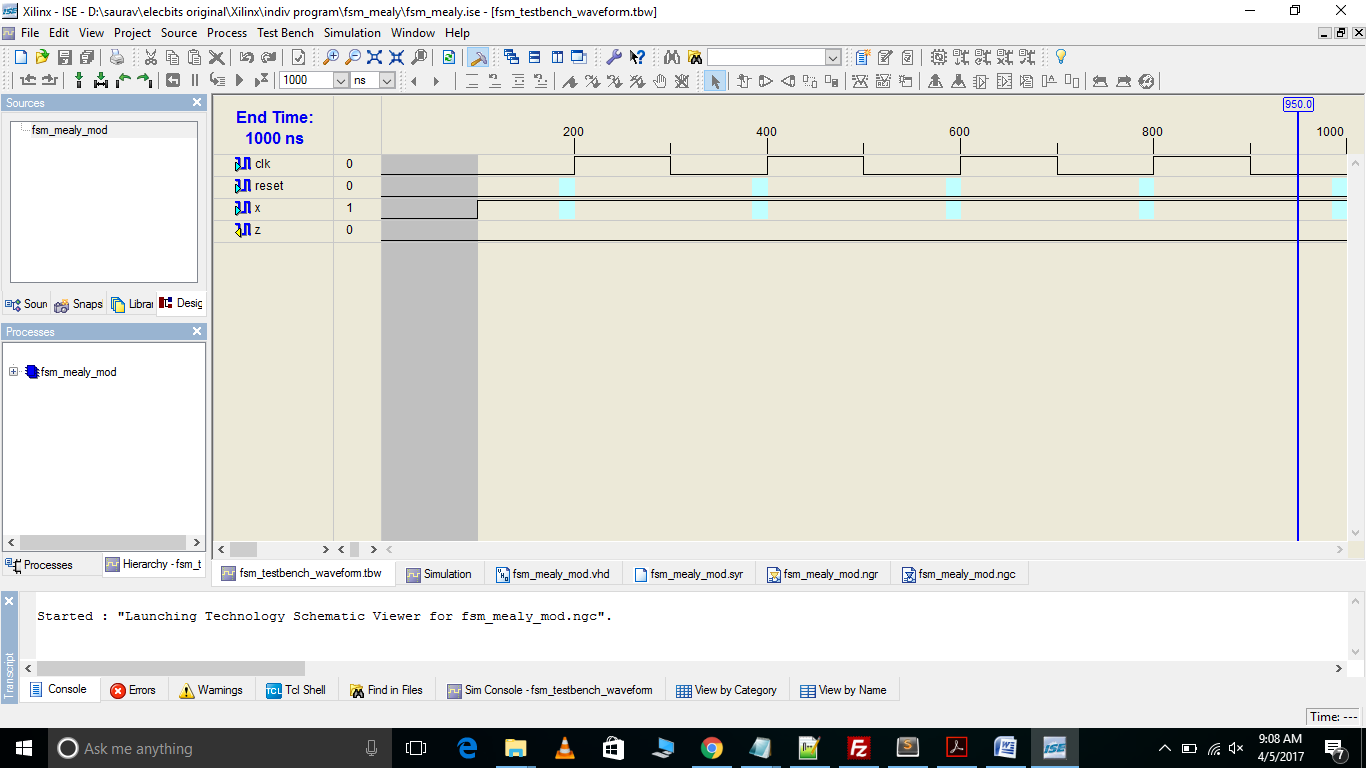
end process;

end Behavioral;

View RTL Schematic

View Technology Schematic  
  


Test Bench Waveform



Stimulation  
  
