

**COURSE DOCUMENT – A STEP GUIDE FOR DATA DOCUMENTATION**

* **TITLE OF THE PROJECT –(Max 6 words)**“Design of FSM using Xilinx”
* **CATEGORIES – (**Take reference from categories.txt**)**

**1. Software**

**2. Digital Electronics**

**3. FPGA**

**4. Programming**

* **EASY HIGHLIGHTS (Max 10)**

**1.**

**2.**

**3.**

**4.**

**5.**

**6.**

* **HARDWARE AND SOFT WARE-(Write as many as possible)**

**1. Xilinx ISE 9.2**

**2.**

* **ABSTRACT + DESCRIPTION(200-300 words)**

**Designing of State Machine using Xilinx.**

Xilinx is a technology company which is provides programmable logic devices and known for inventing FPGA. FPGA (Field Programmable Gate Array) are semiconductor device which are based on configurable logic blocks connected via various interconnects according to the required feature. Xilinx is used to for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device. Using Xilinx we can design Finite State Machine and perform various analyses. The analysis will be based on the designing of state machine using state diagram and state table.

* **ABOUT THE TECHNOLOGY WE ARE USING (100-200 words)**

State machines are nothing but a device that can be stable in more than one set of states. Its output depends on present input and present state. It can be distinguished into two groups-

Mealy and Moore Circuits-

In the theory of computation, a Mealy machine is a finite-state machine whose output values are determined both by its current state and the current inputs. This is in contrast to a Moore machine, whose output values are determined solely by its current state.

* **WORKING PRINCIPLE (100-200 words)**

In Xilinx , the analysis is done in the these following parts-  
1. Synthesis – The execution of coding logic which need to be implemented.

2. View RTL Schematic- It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

3. Test Bench – It’s used to stimulate the values depending upon the input and state provided.

* **APPLICATIONS -(Write as many as possible)**

**1.**

**2.**

* **REFRENCES -(Write as many as possible)**

**1.**

**2.**

* **BLOCK DIAGRAM**
* **PROJECT IMAGE**
* **Note :**

1. You can experiment new things on your own.

2. The word limit is just to provide a general idea of how much written part would be appropriate.

3. Block diagram: 2472 X 824 (Maintain a ratio 3:1)

4. Project Image: 400 X 300 (Maintain a ratio 4:3)