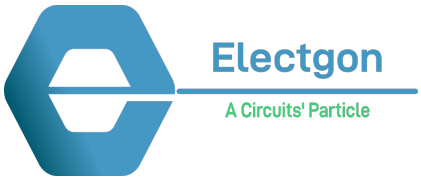


VHDL/Verilog Code Visualization

using Mentor Graphics HDL-Designer

ELECTGON
www.electgon.com
ma_ext@gmx.net

03.06.2019

Contents

Abstract

HDL Designer (aka HDS) is a Mentor Graphics tool that is used for digital design abstraction. Specifically for RTL designs. This means that it is used for viewing/building HDL files (VHDL, Verilog). It has a lot of features and options that enable digital designers to build their complex systems in an easy way. But this needs some practice first in order to get used to this tool. In this Tutorial one feature of HDS will be shown, which is visualization of design files. Other feature are interesting to know and try also but it is not covered in this tutorial.

1 Source Codes Used in This Tutorial

As a start point lets assume that we have already some design files built in VHDL. We can see then how to use HDS to visualize these files as concrete blocks.

First design file (core_logic.vhd) is doing some random logic operation as described below

```
library ieee;
use ieee.std_logic_1164.all;

entity core_logic is port(
clk, rst, core_in_1, core_in_2, core_in_3, core_in_4: in std_logic;
core_out_1: out std_logic );
end entity core_logic;

architecture rtl of core_logic is

signal int_1: std_logic;
signal int_2: std_logic;

begin
process (clk,rst)
  begin
    if (rst='1') then
    elsif (clk'event and clk='1') then
      int_1<=core_in_1 and core_in_2;
      int_2<=core_in_3 or core_in_4;
      core_out_1<=int_1 nand int_2;
    end if;

end process;
end architecture rtl;
```

Another design file (second_logic.vhd) is doing also some random function as described below

```
library ieee;
use ieee.std_logic_1164.all;

entity second_logic is port (
clk, rst, sec_in_1, sec_in_2, sec_in_3, sec_in_4: in std_logic;
sec_out_1: out std_logic );
end entity second_logic;

architecture rtl of second_logic is
signal int_1: std_logic;
signal int_2: std_logic;

begin
process (clk,rst)
  begin
    if (rst='1') then
    elsif (clk'event and clk='1') then
      int_1<=sec_in_1 xor sec_in_2;
```

```
      int_2<=sec_in_3 and sec_in_4;
      sec_out_1<=int_1 nor int_2;
    end if;

end process;
end architecture rtl;
```

At last, we have a design file (top_design.vhd) that include previous designs as described below

```
library ieee;
use ieee.std_logic_1164.all;

entity top_design is port (
clk, rst, core_in_1, core_in_2, core_in_3, core_in_4, sec_in_1, sec_in_2,
    sec_in_3, sec_in_4: in std_logic;
core_out_1, sec_out_1: out std_logic);
end entity top_design;

architecture rtl of top_design is

component core_logic port (
clk, rst, core_in_1, core_in_2, core_in_3, core_in_4: in std_logic;
core_out_1: out std_logic);
end component core_logic;

component second_logic port (
clk, rst, sec_in_1, sec_in_2, sec_in_3, sec_in_4: in std_logic;
sec_out_1: out std_logic);
end component second_logic;

begin
U0: core_logic
port map (clk, rst, core_in_1, core_in_2, core_in_3, core_in_4, core_out_1);

U1: second_logic
port map (clk, rst, sec_in_1, sec_in_2, sec_in_3, sec_in_4, sec_out_1);

end architecture rtl;
```

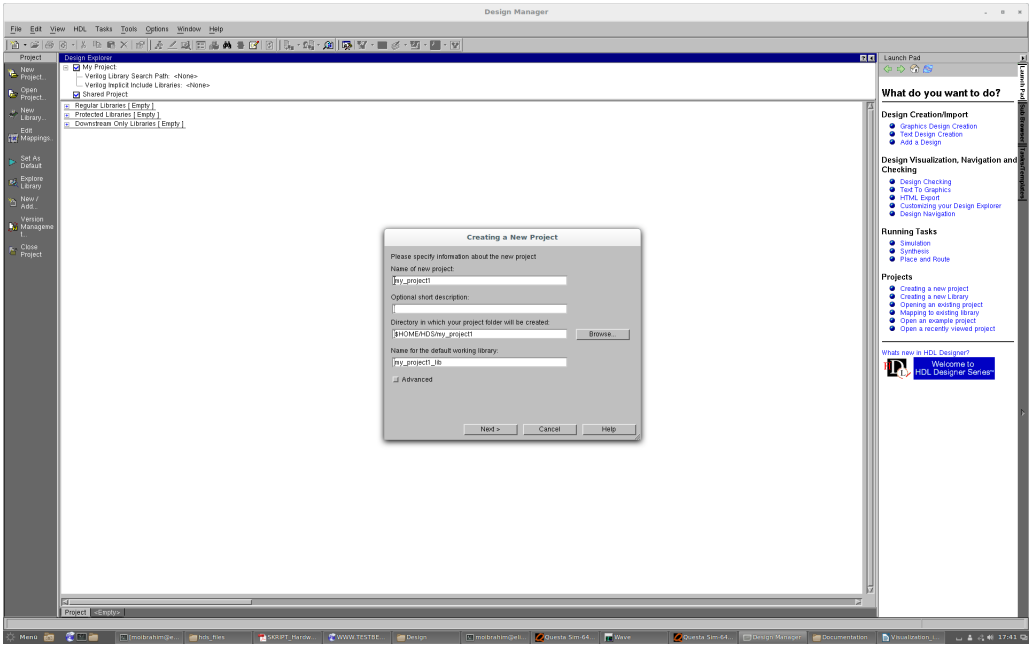
2 Visualization Steps

HDS structure is based on projects. A project contains one or more libraries. A library contains one or more components (or design units). Thus in order to view design files in HDS, we have to create a project, within this project we create a library which will include our design files.

Open HDS in your system. In windows you can open it by invoking it directly from start menu then browse to HDL designer.

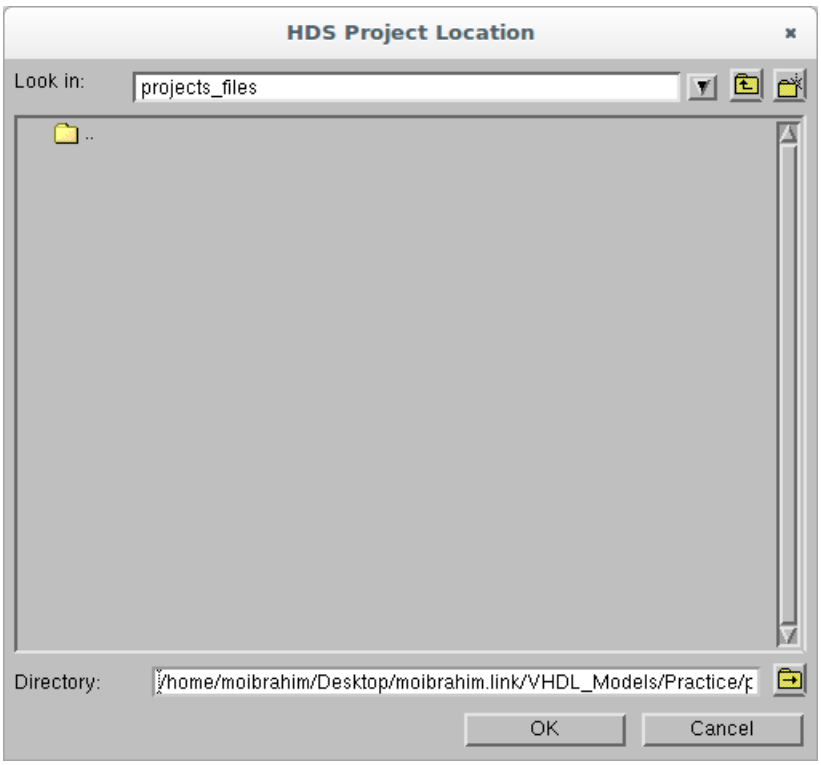
In Linux, you should know what is the environment variable defined for this tool (ask your system administrator if you didn't install it yourself). I assume for first time users, the

following wizard will start by invoking HDS. If not you can bring it by clicking on Top menu on File>>New>>Project

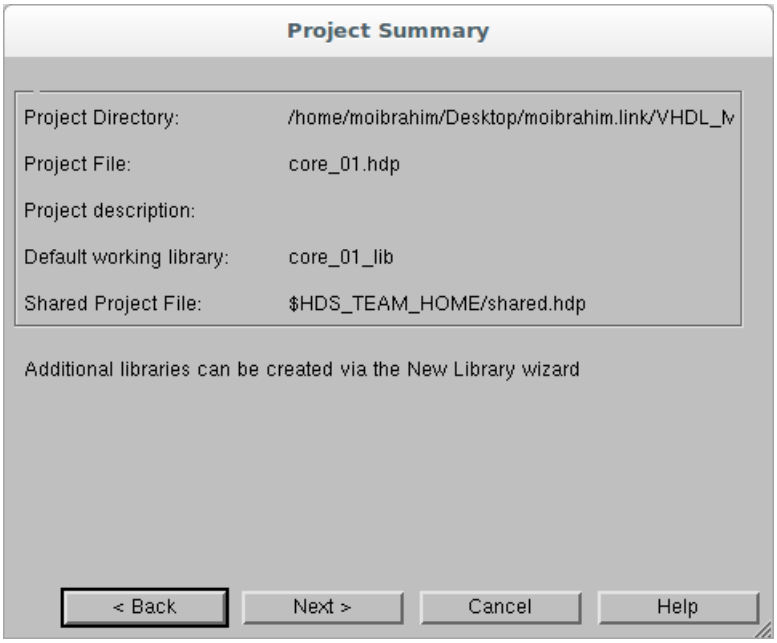


This wizard asks about new project name along with what the name of default library of this project. In This tutorial lets call first project as core_01 and use default library name as provided by HDS.

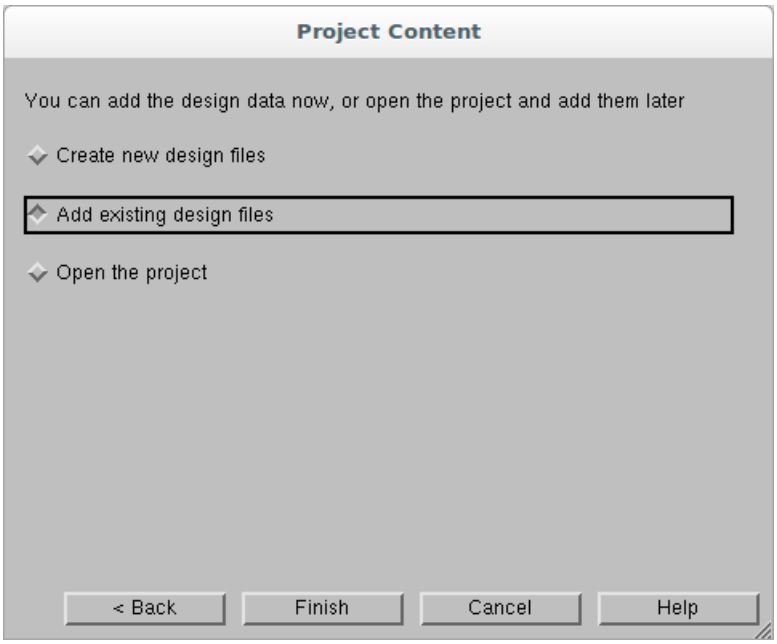
Click on Browse button to specify where would you like to save this project. Choose your preferred directory. Then click Next.



A confirmation message to assure the correct provided information for this project. Click Next.

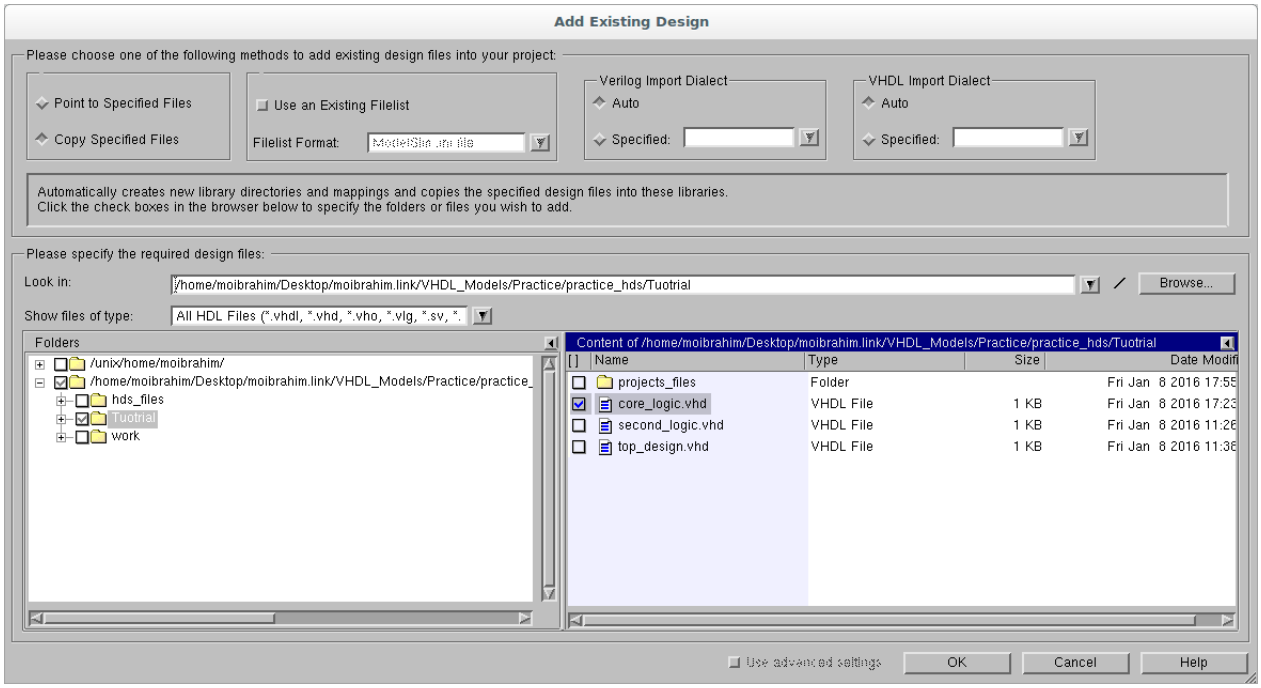


Next dialog is asking whether you need to create new design files or import existing files or just open the project. In our tutorial we have design files are ready, so we choose Add existing Design files.

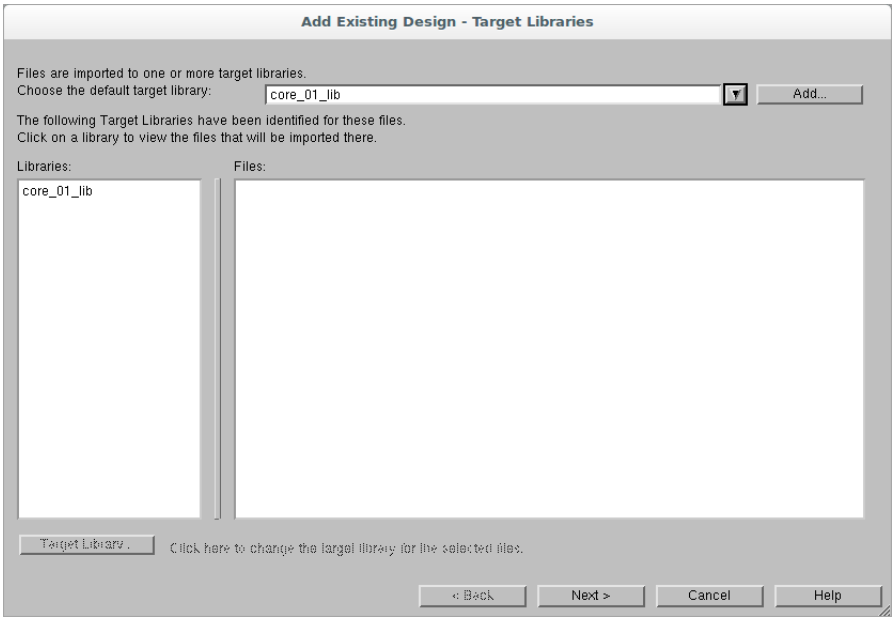


After you Click Finish. Another wizard is opening asking for design files that you wish to include in this project. Browse to the directory of these files. An important option is choose “Copy Specified Files“ in the upper left corner. This to get a copy of the original files to be included in project directory. The other option “Point to Specified Files“ will just point to the source files and this is not helpful in some cases.

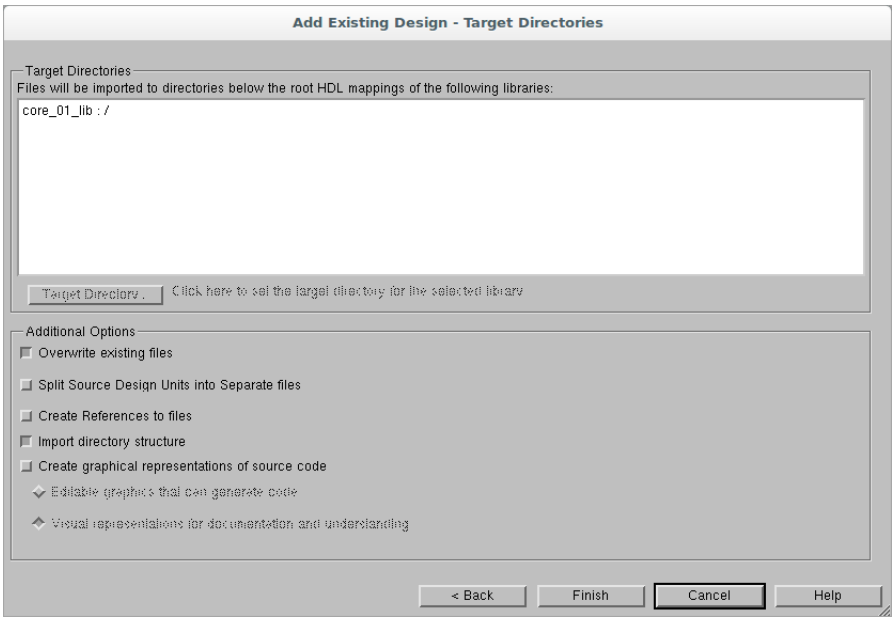
Make sure you tick on the design file that you need to include. In our tutorial here, we will add core_logic.vhd in this project.



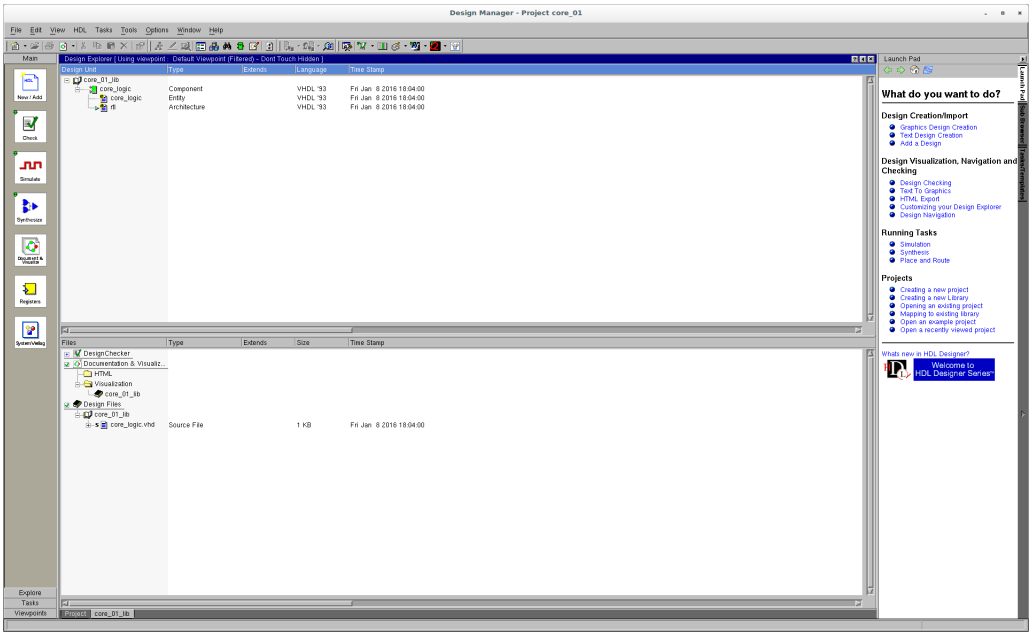
After you click OK, confirmation dialog will appear to make sure you added the right files.



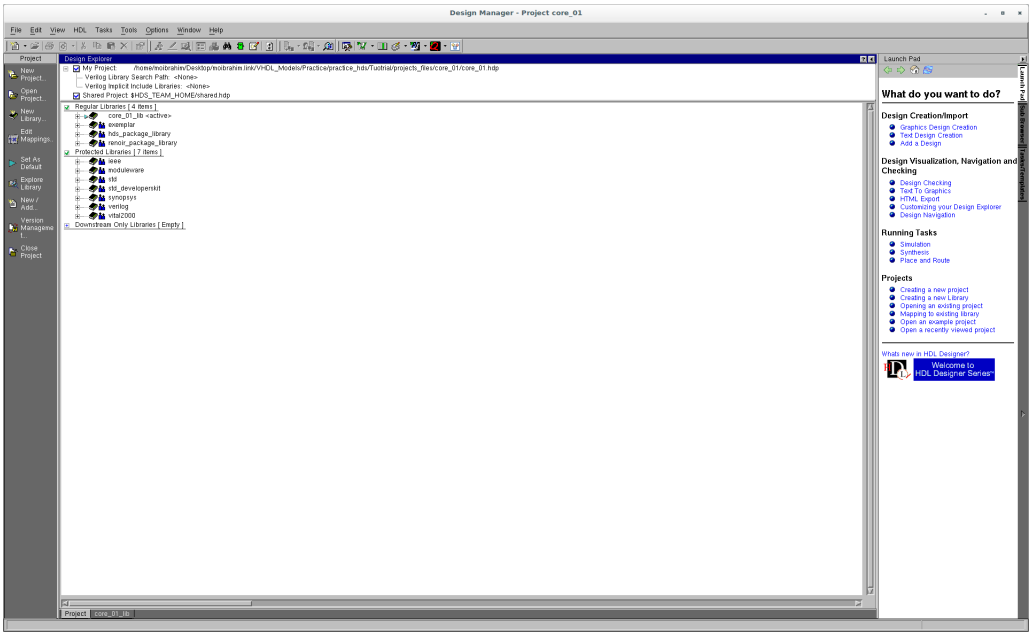
After you click Next. Additional Options are displayed. It is not important to choose any of these options now. So process further by clicking Finish.



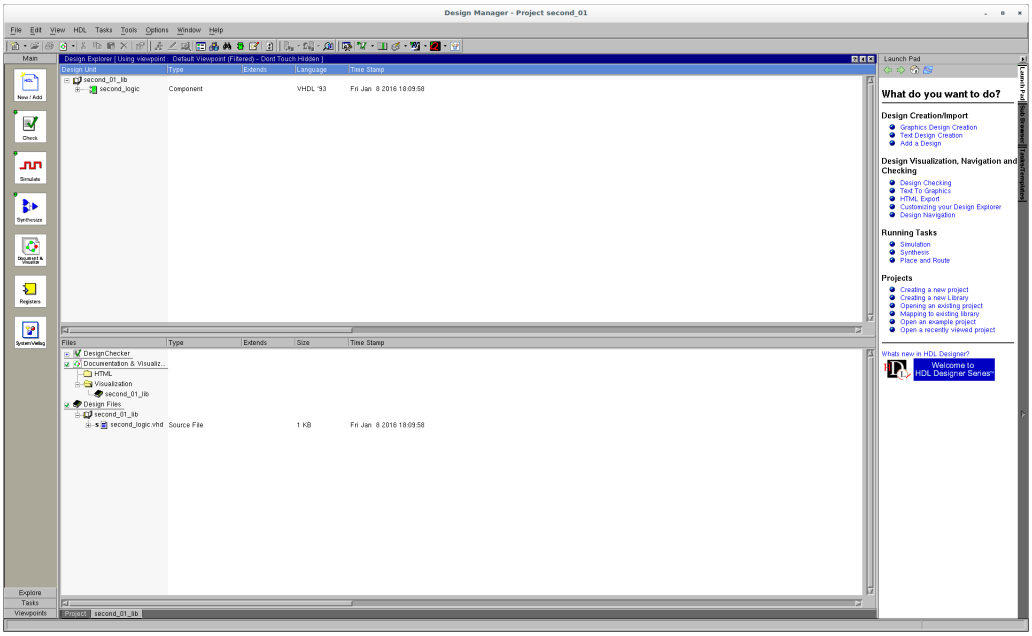
Now Project has been created. You can overlook about the opened project and which libraries it has.



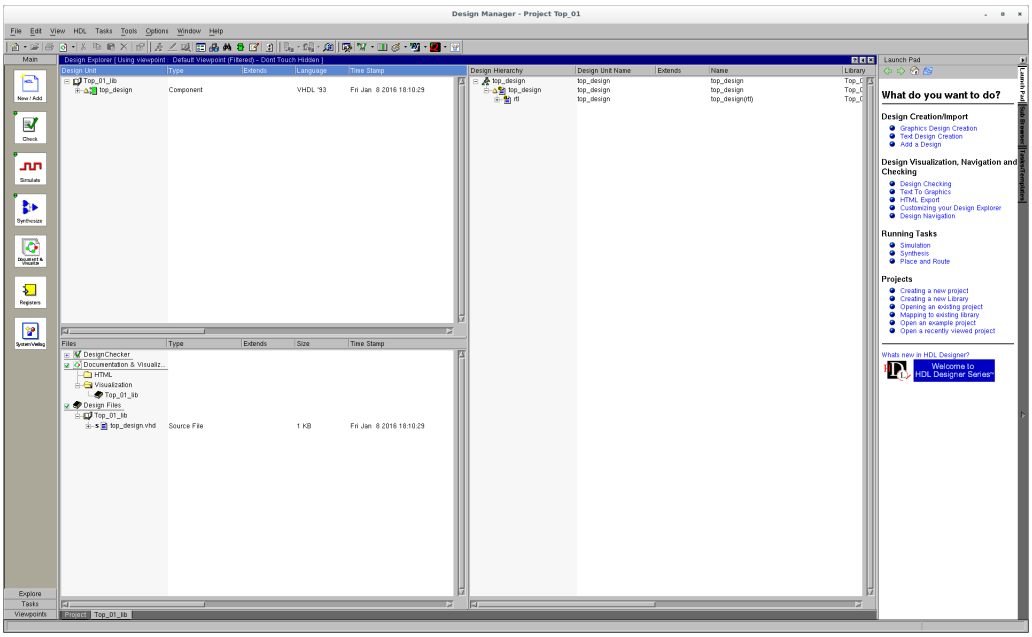
Note that at the lower bar of the opened browser, you can switch view between the library or the project.



In the same way we can create new Project for the other source file second_logic.vhd. Here I called this project second_01.

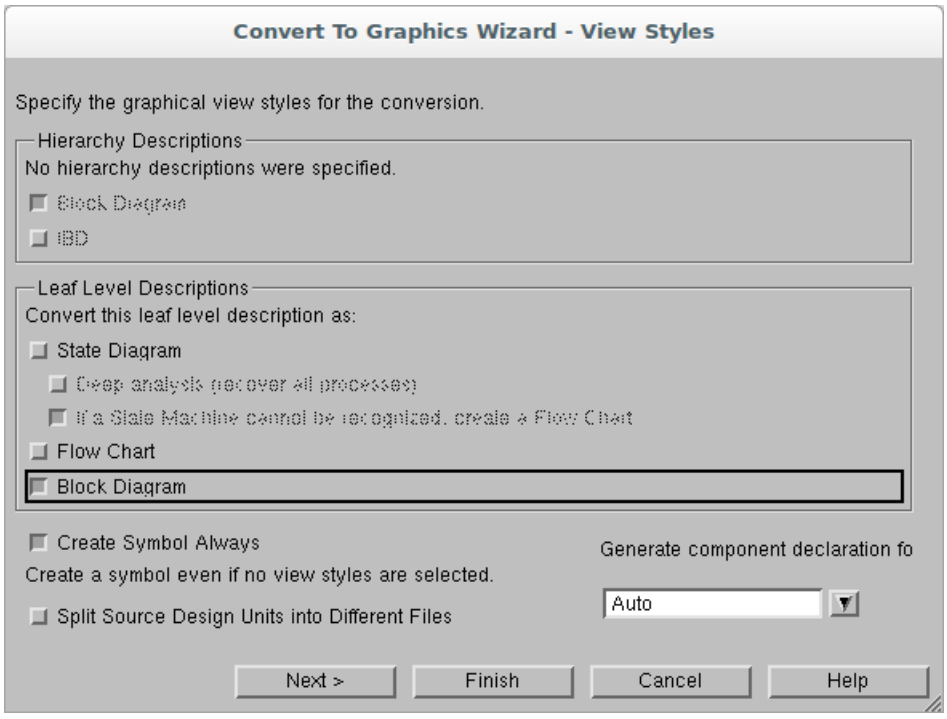


Also for the top_design. Here I called this project Top_01.

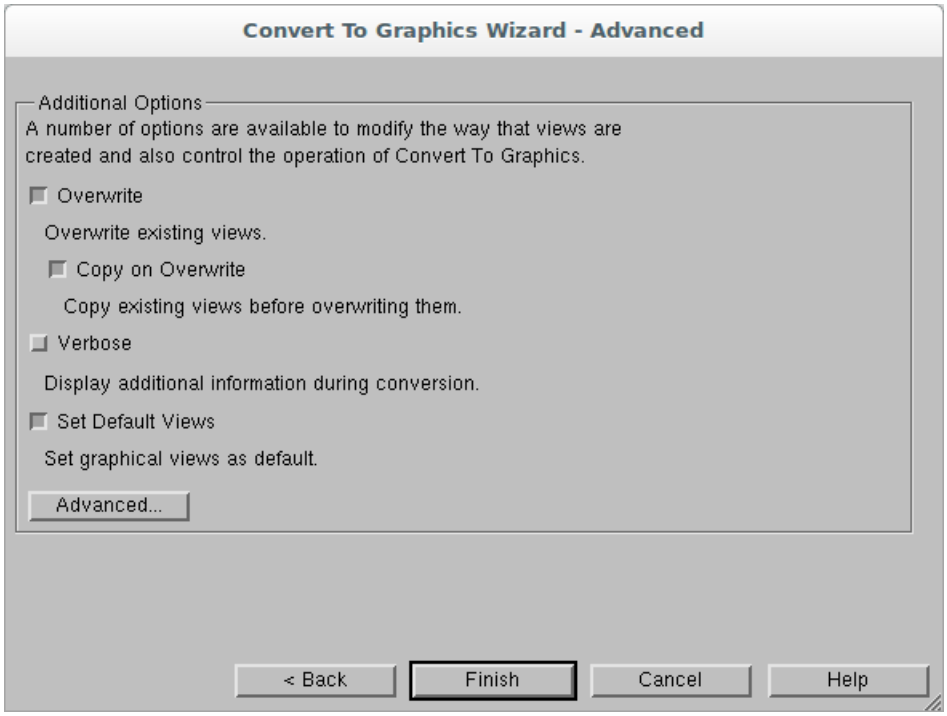


Now we want to see how to make visualization for the added designs. Open the project core_01 again.

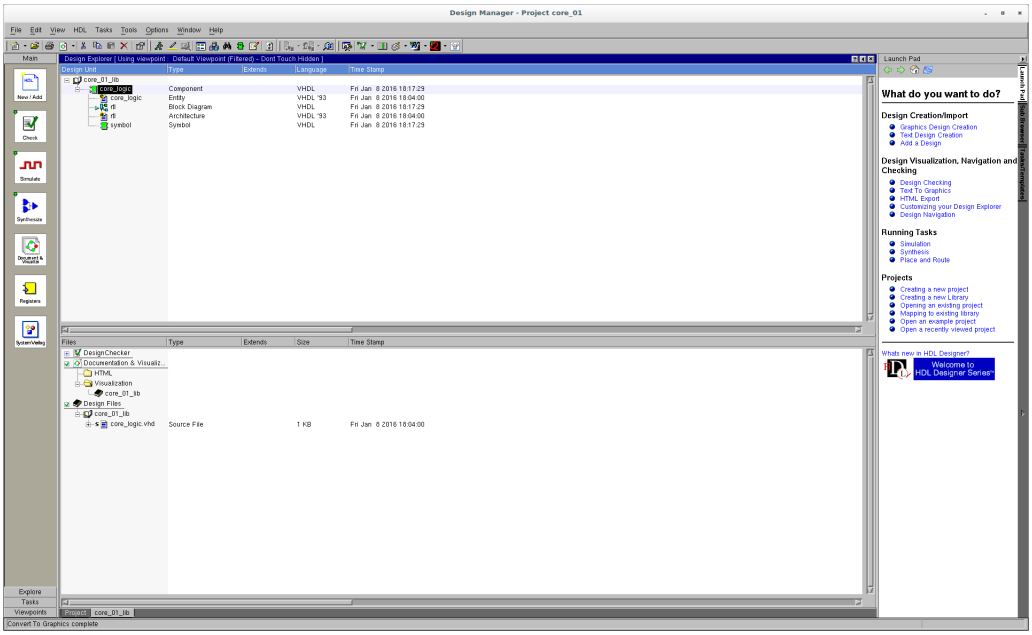
Click on the component core_logic to highlight it then from the top menu bar choose HDL>>Convert To Graphics>>Single Level.



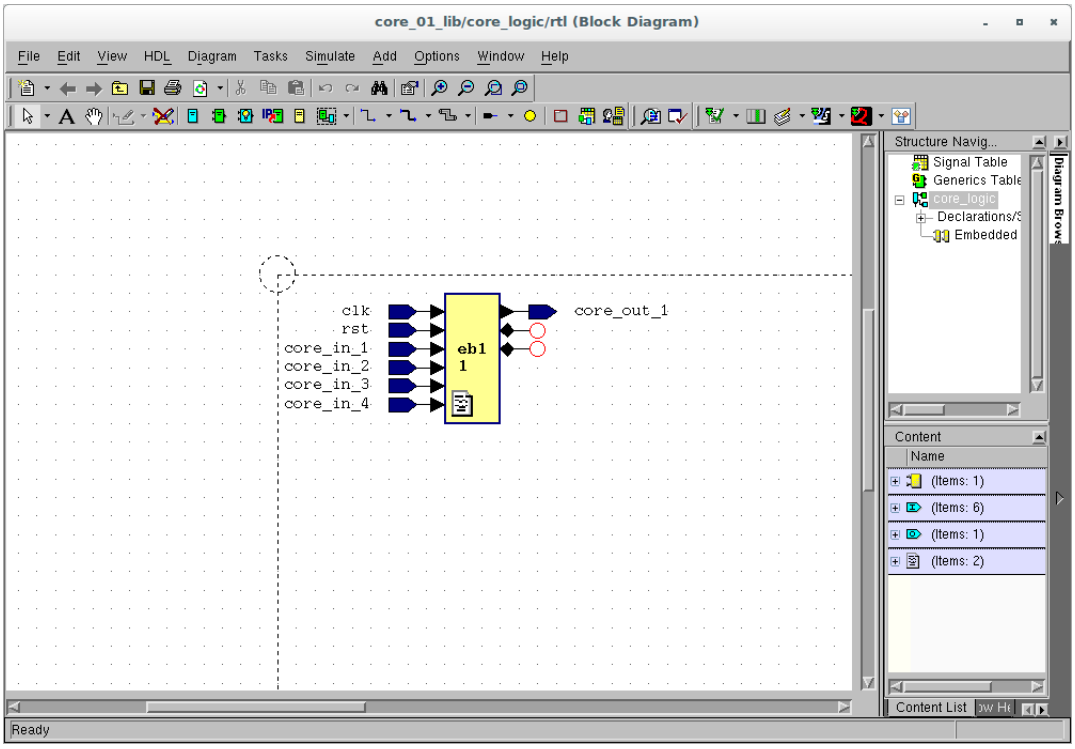
In the appeared dialog, choose to view this component as a block diagram. Click Next then choose the following options as shown in screen shot



After you click Finish, you can see now new view has been added to our component.

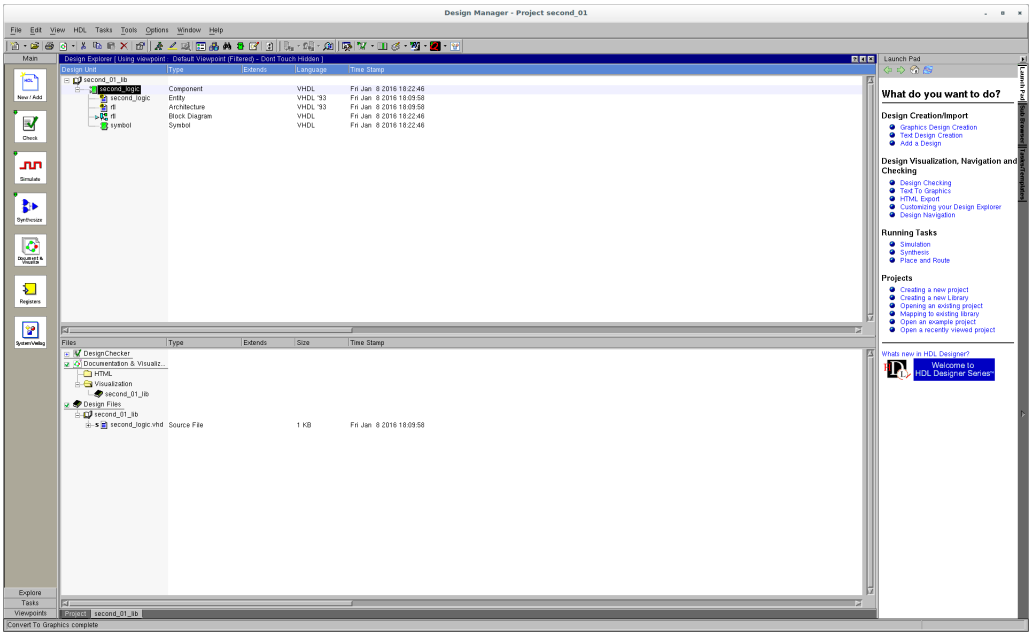


double click on this new view.

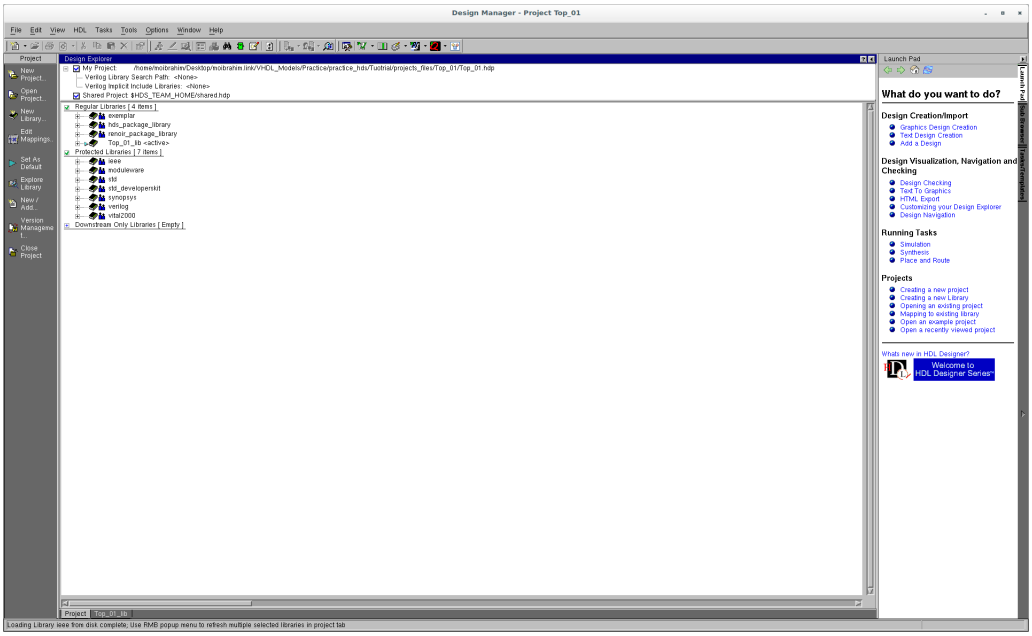


As you see it is just a trial from the HDS to represent this design in a graphical way. Since it is lowest level design and no more details included in the source file, it is just represented as single block which if you clicked on, it will open the process that describes behavior of this component.

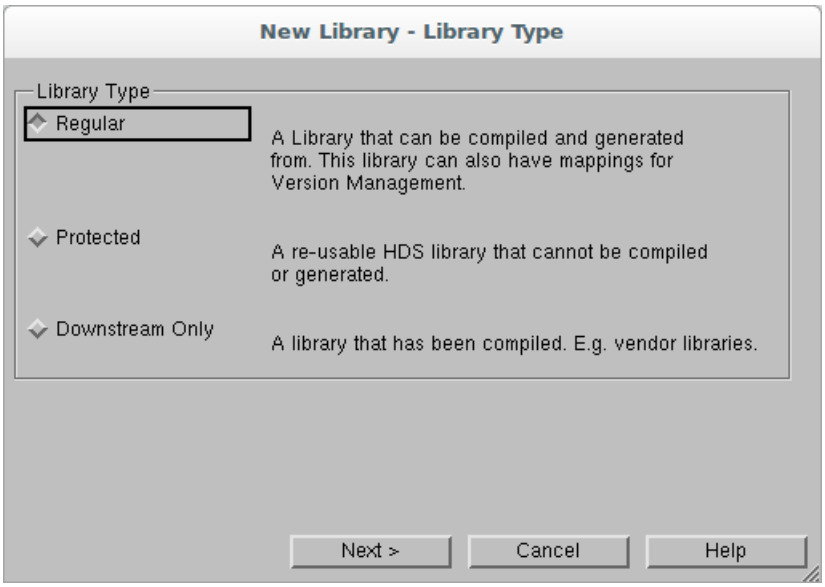
In the same way, we can visualize the other component second_logic.



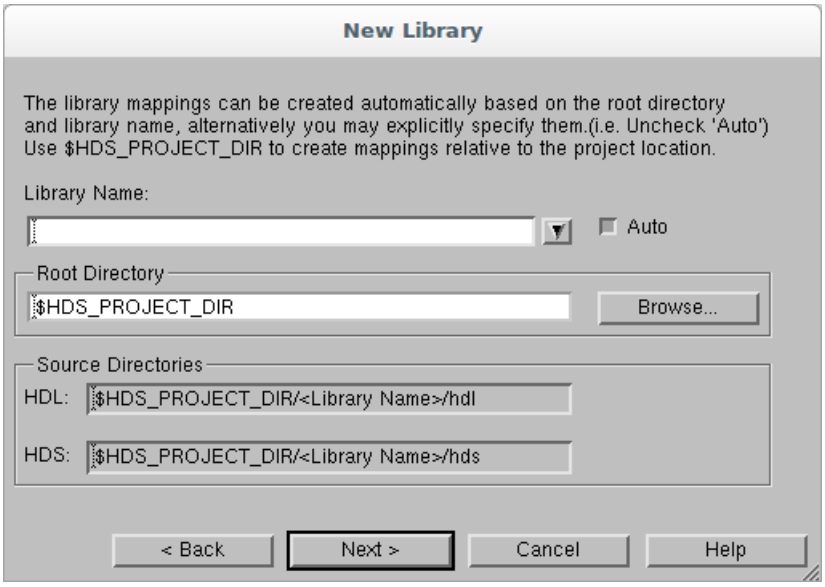
Now for the top component we can follow also same steps. However additional step is needed in order to view submodules of this design. Open project for the top_design (Top_01). Navigate to the Project pane.



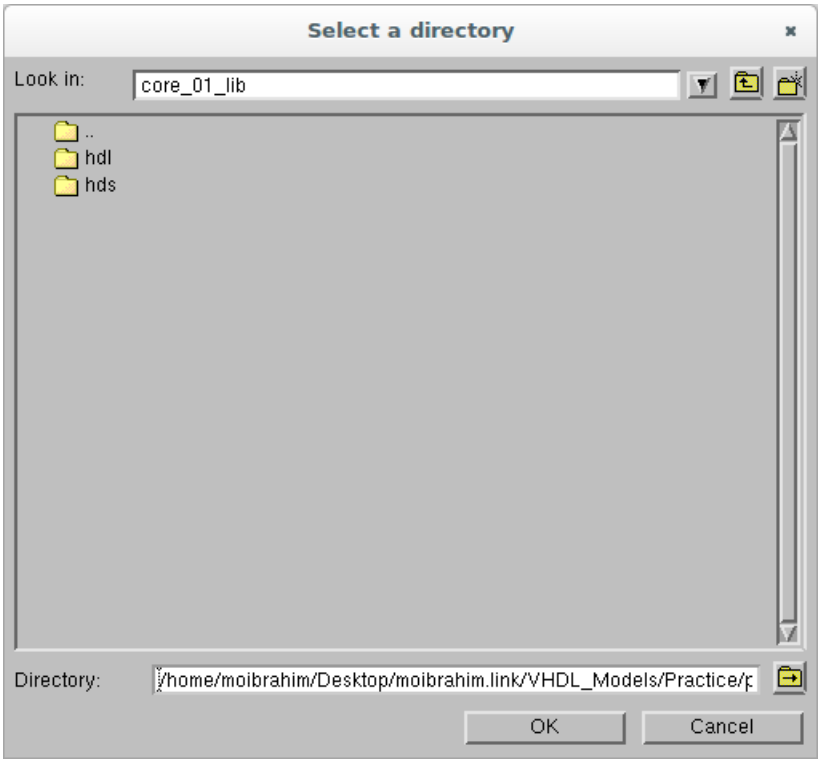
Right click on “Regular Libraries“ and choose ’New Library’. In the appeared dialog choose ’Regular’ then click Next.



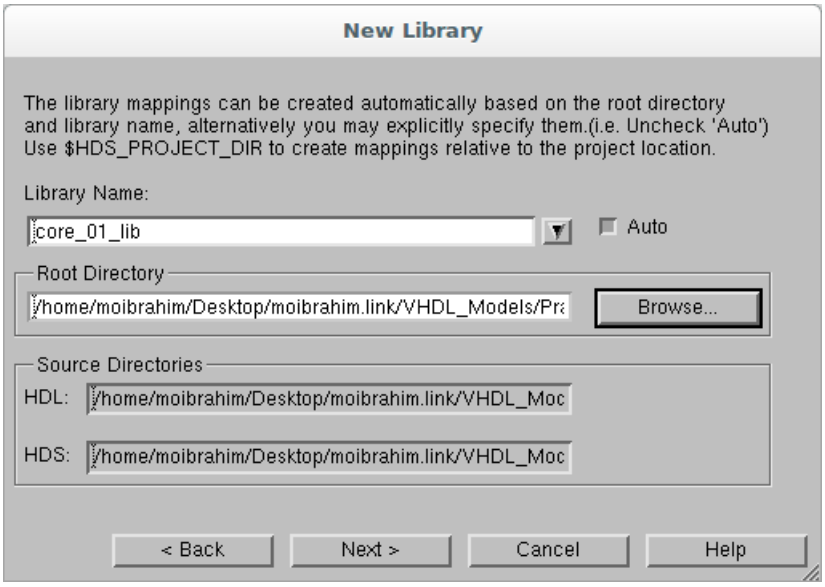
In next dialog, we need to libraries of core_01 and second_01 so that we can be able to view its components block diagram within project Top_01. So click on Browse button.



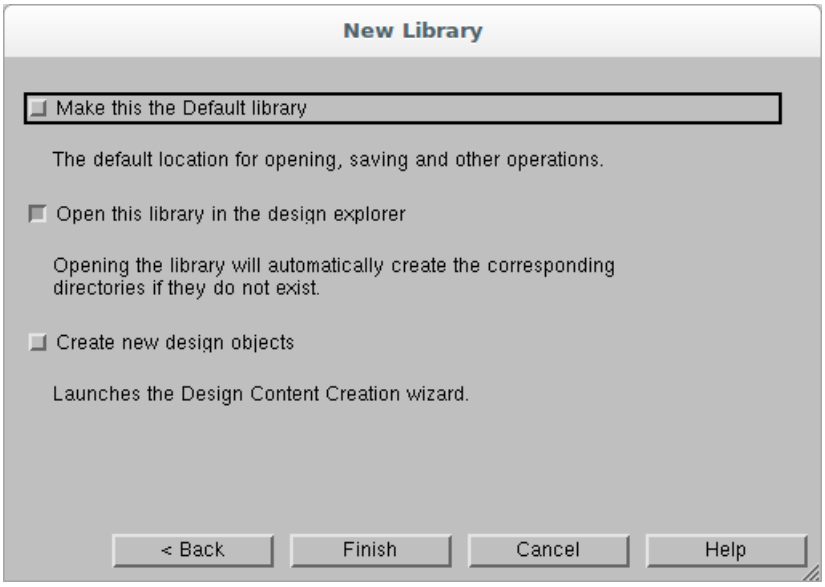
Navigate through core_01>core_01_lib then click OK



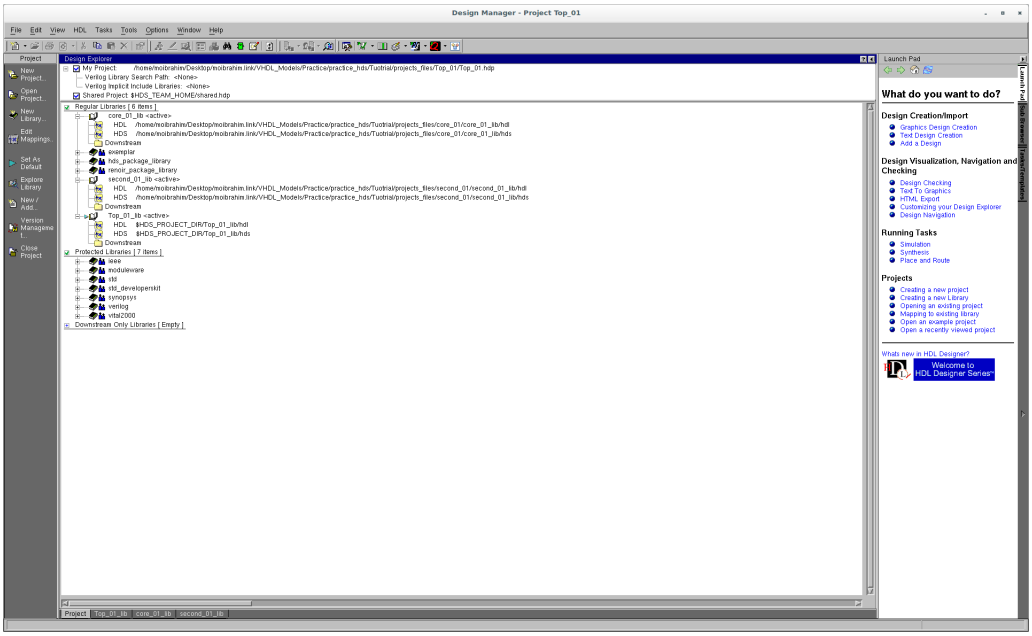
Now you can see library name of project core_01 is updated automatically in the library name field.



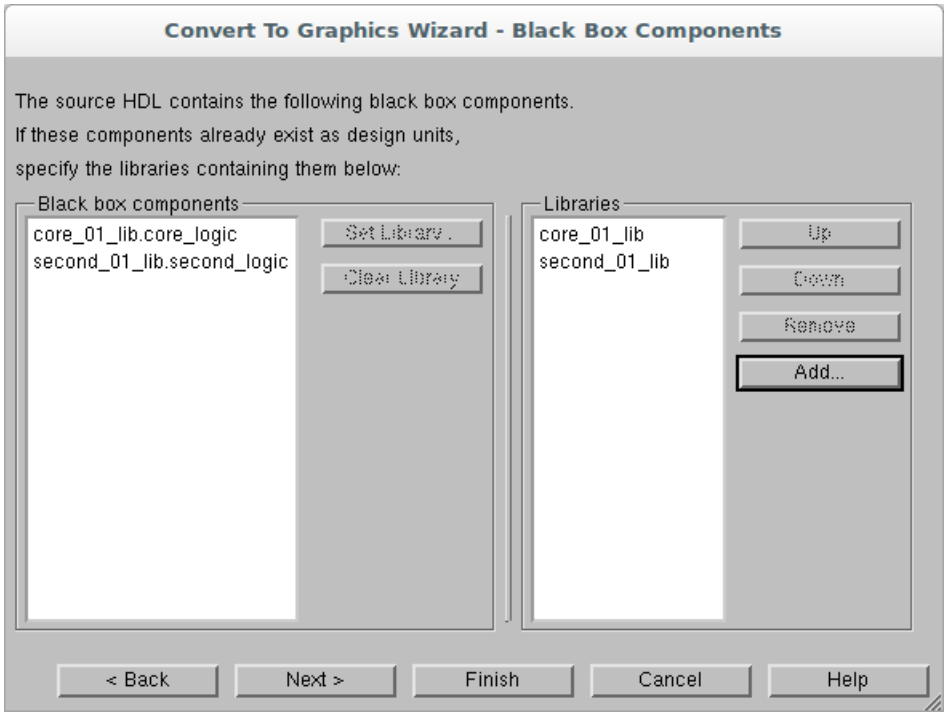
Click Next, in the appeared dialog don't choose this library as a default library. You can now click on Finish button.



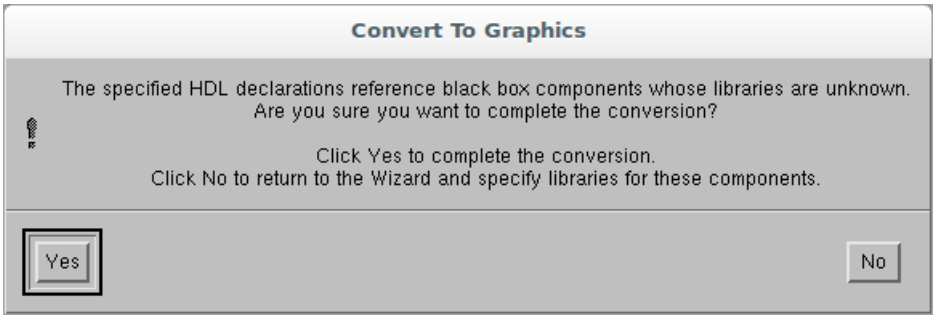
In the same way you can add the other library of second_01. You can find now that all libraries have been added.



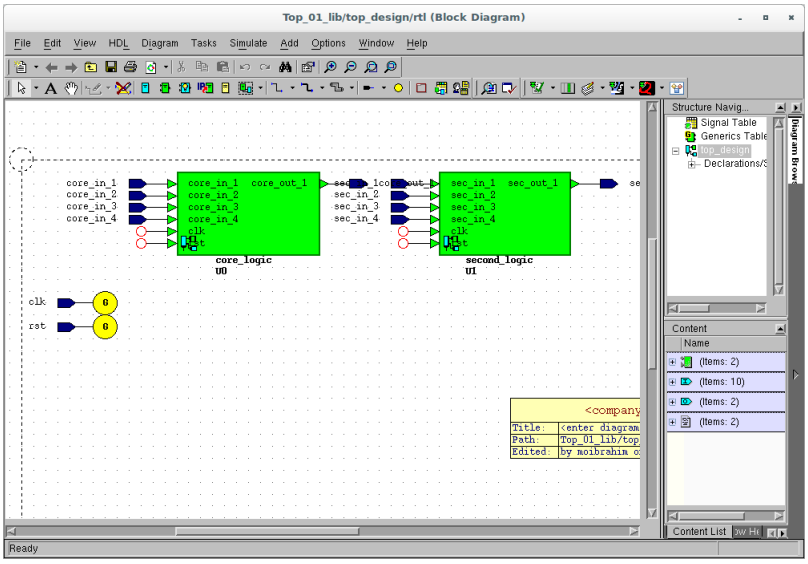
Now we can proceed in normal steps to visualize the top_design. One more dialog will appear is asking you where to find libraries of submodules. Choose as shown in the following figure.



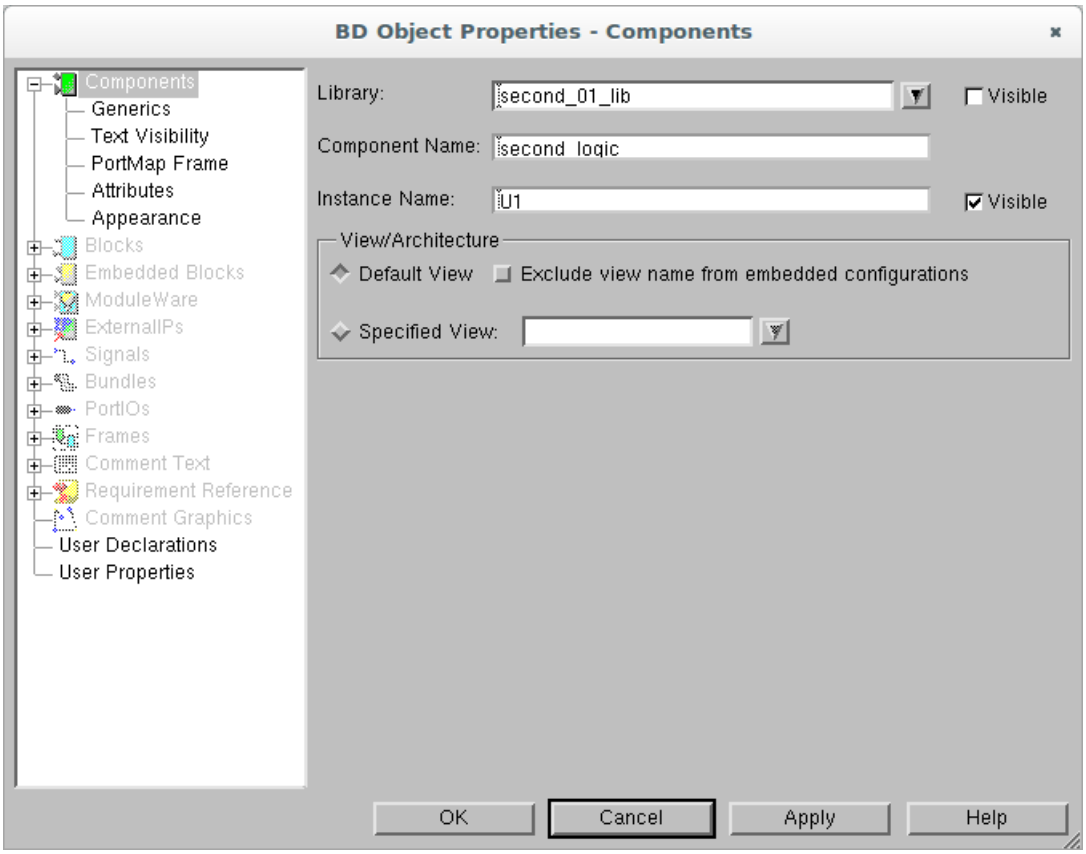
After you Click Next then Finish, a warning message says that the submodules are still not recognized and treated as black boxes. Ignore this message and click Yes.



Now you can see content of the top_design as shown below. Note now if you double click on any of the submodules, it will open graphical view also of that submodule.



Another workaround to get the submodules block diagram is to right click on the component. Then choose 'Object Properties'. The following window will appear.



You can choose then which library includes this component.