Timing of Data Transmission

There are three basic timing models used for communication between two ICs: system-synchronous, source-synchronous, and self-synchronous.

0.0.1 System-Synchronous

Transmission between the communicating ICs includes only the data as can be declared by figure 1. The two ICs are having the same clock which is provided by external oscillator. Both ICs will operate according to this clock then.

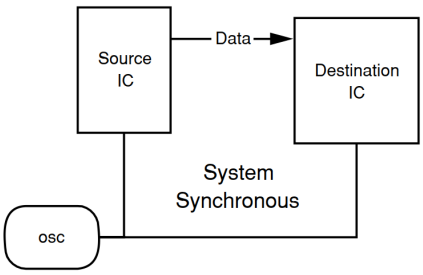

Figure 1: System Synchronous

0.0.2 Source-Synchronous

In this communication both data and used clock are transmitted from the source IC to the destination IC.

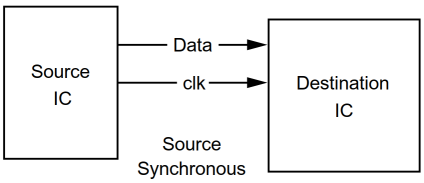

Figure 2: Source Synchronous

The output time of the forwarded clock is adjusted so that the clock transitions in the middle of the data cell. Two important points shall be taken into consideration in this communication. First, the destination IC will have different clock domains, at least one for the received clock and another for the global IC operation. Second point is timing constraints that should be precisely adopted to match the condition of having clock edges transitions in the middle of the data cell. This second point appears crucial for large parallel data transmission such as 32 bits as well as high data rate transmission.

0.0.3 Self-Synchronous

The self-synchronous model is shown in Figure 3. Here, the data stream contains both the data and the clock.

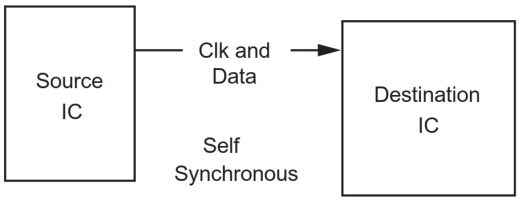

Figure 3: Self-Synchronous

The clock is recovered by means of PLL. It can detect the clock cycle according to the period of 1 bit. This can be implemented if the transmitted data is using some coding techniques such as Manchester coding. It is known also as self-clocking signal.