

## Article

# A Novel Variable-Step Algorithm for DC-Side Voltage Stability Control Strategy in UPQC to Improve Power Quality

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**Abstract:** With the development of semiconductor technology, the increasing number of power electronic converters and nonlinear loads has further exacerbated power-quality issues in the grid. To address this, this paper presents an improved DC-side voltage control strategy for UPQC, aiming to enhance power quality under complex conditions. First, an adaptive filter is integrated into the linear active disturbance rejection control (LADRC) to address control accuracy issues caused by noise and parameter variations. To solve the voltage sag problem resulting from the filter, the effects of fixed-step and various variable-step algorithms within the filter are analyzed, and the optimal control strategy is identified. Simulation results demonstrate that the proposed arctangent function-based variable step-size algorithm (VAV-LADRC) strategy effectively improves the UPQC system's performance in mitigating voltage sags, swells, and harmonics under dynamic load changes, enhancing the stability of the DC-side voltage. To further validate the generalizability of the method, a co-simulation of a photovoltaic power-generation system with the UPQC is conducted, simulating variations in solar irradiance. The results show that the proposed method maintains excellent control performance under complex conditions, providing a better practical solution for the efficient use of green energy.



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## 1. Introduction

Advances in semiconductor technology have led to an increased penetration of power electronic devices in power-distribution systems, including power electronic converters and nonlinear loads, further deteriorating the power quality in distribution networks. Nonlinear loads draw non-sinusoidal currents from the grid, which pass through the power supply system, causing non-sinusoidal voltage drops and subsequently disturbing the voltage at the load end. To tackle a range of power-quality problems, including poor power factor resulting from reactive power, voltage sags and swells, as well as voltage and current harmonics, and to enhance the overall performance of distribution networks, various custom power devices like distribution static compensators (DSTATCOM), dynamic voltage restorers (DVR), active power filters (APF), and unified power-quality conditioners (UPQC) are commonly utilized [1–3]. While DSTATCOM and APF address current-related power-quality problems, DVR compensates for voltage-related issues. However, UPQC can address both current and voltage power-quality problems simultaneously [4]. In the absence of external energy storage or energy support, compensating for voltage interruptions using UPQC becomes complex. Furthermore, numerous stringent power-quality

requirements have driven the integration of UPQC with distributed energy resources (such as photovoltaic and wind energy) to realize multifunctional systems [5,6]. Thus, to simultaneously address power-quality issues arising from both current and voltage, while also providing green energy support, UPQC remains one of the most effective solutions available.

The choice of a suitable control strategy is crucial in determining the expected performance of any power electronic system. Consequently, the performance of the UPQC system largely depends on its control strategy. In the UPQC system, maintaining a stable DC-link voltage is crucial for the proper functioning of power converters and directly impacts overall system performance and power quality. The DC-link voltage acts as a buffer between the AC and DC sides of the system, and its stability is essential for effective voltage and current regulation. Various DC-link voltage control strategies have been proposed, each with distinct advantages and limitations.

Traditional PI control methods are widely adopted for their simplicity and ease of implementation. However, their fixed-gain characteristics lead to compromised dynamic performance during sudden load changes or grid disturbances. Fuzzy logic controllers demonstrate superior adaptability to non-linear system conditions through rule-based decision-making but require significant computational resources and expert knowledge for membership function tuning. More recently, sliding mode control approaches have gained attention for their strong robustness against parameter variations, though they introduce undesirable voltage chattering that may increase switching losses. Any fluctuations or instability in the DC-link voltage can lead to poor load regulation, voltage sags, and harmonic distortion, degrading the overall system performance [7].

However, in some cases, a single control strategy is typically adopted, which may not ensure optimal steady-state and dynamic performance of the control system [8]. A data-driven control (DDC) approach focused on efficiency has been introduced to optimize the scale of the UPQC system. This approach is model-free and demonstrates notable robustness against parameter fluctuations. Nonetheless, it is relatively complex and less prevalent in engineering applications. On the other hand, artificial neural networks (ANN) have emerged as a promising tool for enhancing power quality, owing to their simplicity and the absence of intricate control frameworks or system models. However, this technique is limited by its suboptimal real-time performance and its inability to guarantee convergence [9]. Most of the current UPQC control methods require precise model parameters, involve complex controller design, and have limited disturbance rejection capabilities, making it difficult to address the intermittent and stochastic nature of distributed generation.

Linear active disturbance rejection control (LADRC) originated in 1998, proposed by Professor J.H. as active disturbance rejection control (ADRC) [10], and was later linearized by Professor Z.G. to form LADRC [11]. Subsequently, a bandwidth tuning method for LADRC was introduced [12], simplifying the parameter tuning process by consolidating it into two bandwidth parameters. ADRC views all uncertainties in a system as unknown disturbances, which are estimated through an expansion state observer (ESO). The reference input is differentiated to obtain its higher-order differential state variables, which are then subjected to nonlinear state error feedback (NLSEF) from the states observed by the ESO, ultimately converting the system into a cascaded integrator form. The key difference between LADRC and ADRC is that the ESO and state feedback in LADRC are linear, which simplifies the parameter tuning by reducing it to the adjustment of two bandwidth parameters.

Currently, LADRC is widely applied in electrical control fields, such as motor control, robotic control, aircraft control, and grid-connected inverter control [13–17]. In Ref. [18],

LADRC was applied to wind power grid-connected inverters. In Ref. [19], LADRC was used to replace traditional PI control in phase-locked loop (PLL) design, effectively suppressing system oscillations. Furthermore, Ref. [20] improved the total disturbance observation gain coefficient in traditional LADRC by incorporating a proportional-differential element in the control gain and performing loop correction. This modification reduced the amplitude reduction and phase lag of the disturbance observation, effectively minimizing the fluctuations in the inverter's DC-link voltage. In Ref. [21], LADRC was applied to microgrid inverters, where a time-frequency domain LADRC controller was designed. Compared to traditional PI dual-loop control, this approach demonstrated better disturbance rejection and dynamic performance, with no need for decoupling design and reduced dependency on model parameters.

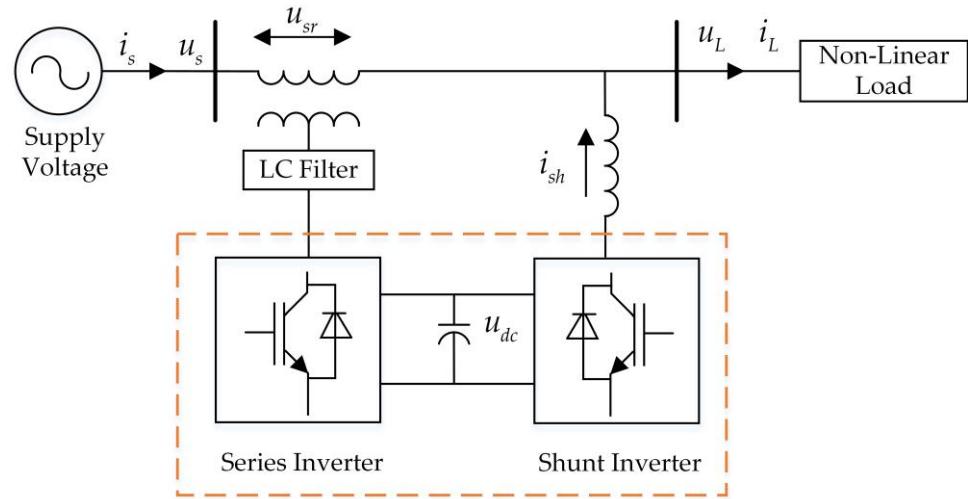
Nowadays, neural network-based soft computing techniques are widely used in the field of power quality to develop adaptive control schemes. In Ref. [22], the least mean squares (LMS) algorithm was used for adaptive estimation of the reference signal required for a switched converter, implemented through weight update equations. Ref. [23] proposed a variable-step LMS algorithm to overcome the slow convergence issues caused by fixed-step algorithms.

This paper proposes a novel control method for the DC-side voltage regulation of the UPQC system, aimed at mitigating voltage sags, swells, and harmonics in the power grid. The main contributions of this work are as follows:

1. To address the control accuracy issues caused by noise and parameter variations in traditional LADRC control methods, an adaptive filter is introduced into the LADRC, enhancing the system's robustness and control precision.
2. To resolve the voltage sag problem introduced by the adaptive filter, the effects of both fixed-step and variable-step algorithms within the adaptive filter are analyzed, and the optimal control strategy is selected to maximize the stability of the DC-side voltage.
3. To validate the generalization ability of the proposed method, a photovoltaic power-generation system is incorporated, and the dynamic variations of solar irradiance in real-world conditions are simulated. This further evaluates the method's applicability in the context of renewable energy generation, providing a more efficient implementation solution for producing green and clean energy.

## 2. The Structure of the UPQC System

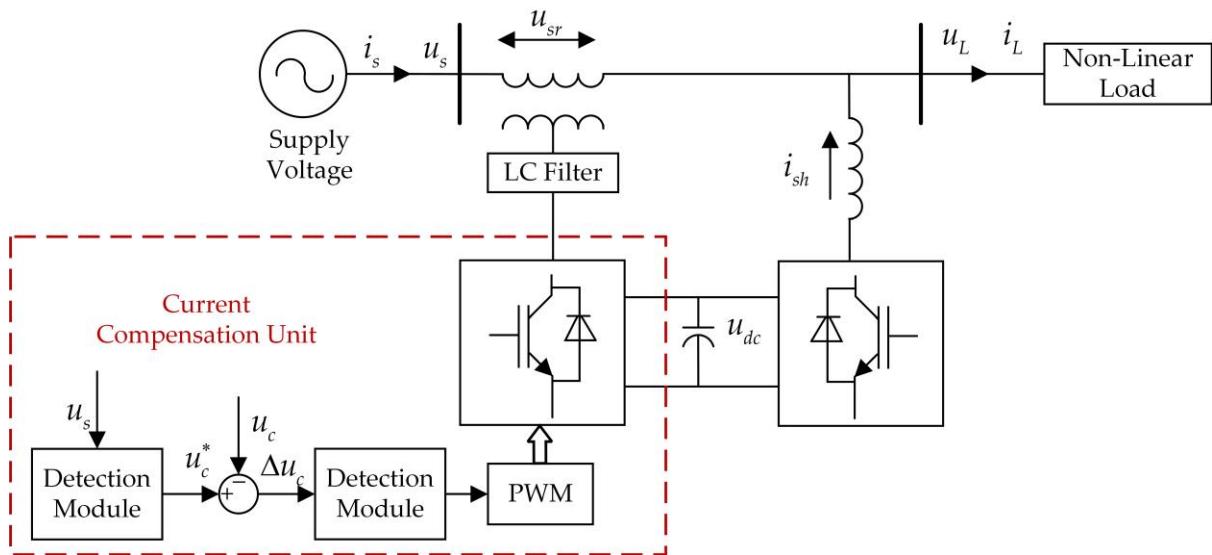
The traditional UPQC is a multifunctional power quality management device that integrates both voltage and current compensation functions [24]. The series side functions as the voltage compensation unit, primarily aimed at improving the quality of the grid voltage. The parallel side serves as the current compensation unit, with its core function being the dynamic compensation of harmonic currents introduced by nonlinear loads, thereby maintaining the sinusoidal and symmetrical nature of the grid current and improving the overall power quality. The overall structure of the UPQC is shown in Figure 1.



**Figure 1.** UPQC structure block diagram.

### 2.1. Series Inverter Control Structure

The traditional UPQC, as a multifunctional power quality management device that integrates both voltage and current compensation functions, has its voltage compensation unit primarily aimed at improving the quality of the grid voltage. This unit works by real-time detection of voltage fluctuations or distorted signals on the grid side and generates corresponding compensation signals to dynamically regulate the grid voltage, as shown in Figure 2.



**Figure 2.** UPQC series side structure block diagram.

The control of the voltage compensation unit relies first on the precise detection of the grid voltage. Real-time three-phase grid-side voltage signals  $u_s$  are obtained via voltage transformers. To achieve accurate compensation of the grid voltage, fast fourier transform (FFT) or low-pass filters are commonly used to extract the fundamental sinusoidal components  $u_{sf}$ . The detected voltage signals are then separated into harmonic components  $u_{sh}$ , fundamental components  $u_{sf}$ , and fluctuation components  $\Delta u_s$ , satisfying the following relationship:

$$u_s = u_{sf} + u_{sh} + \Delta u_s \quad (1)$$

By detecting the deviation components of the grid voltage, a reference signal can be further provided to the control unit for voltage compensation. The core of the voltage control section lies in generating a compensation signal based on the detected grid voltage deviation to correct voltage distortion. Let  $u_L$  denote the load voltage and  $u_s$  represent the real-time detected voltage. The difference between the two is the output compensation voltage  $u_c$  of the series compensation unit, as given by:

$$u_c = u_s - u_L \quad (2)$$

By applying an appropriate control method, the compensation signal is transformed into a PWM signal to control the series compensator. This enables the DVR to inject a compensation voltage into the grid that is in inverse phase with the grid voltage distortion. That is, the UPQC injects a compensation quantity  $u_c$  through the series compensation unit to counteract the voltage distortion, ultimately ensuring that the output voltage of the distribution network and the load voltage are both sinusoidal and at the fundamental frequency. The PI controller is a crucial component of the voltage compensation unit, and the output of the PI controller provides the reference value for the compensation voltage, denoted as:

$$u_c(t) = K_p \cdot e_u(t) + K_i \cdot \int e_u(t) dt \quad (3)$$

where  $K_p$  is the proportional gain and  $K_i$  is the integral gain. The PI controller adjusts the compensation voltage  $u_c(t)$  in real time, gradually reducing the grid-side voltage deviation to zero, thereby achieving voltage stability and effective harmonic compensation.

The voltage compensation unit generates control signals to drive the inverter through the PWM generator. The basic principle of PWM modulation is to compare the compensation voltage reference value  $u_c(t)$  with the carrier signal  $u_{\text{carrier}}(t)$ , thereby generating a switching signal.

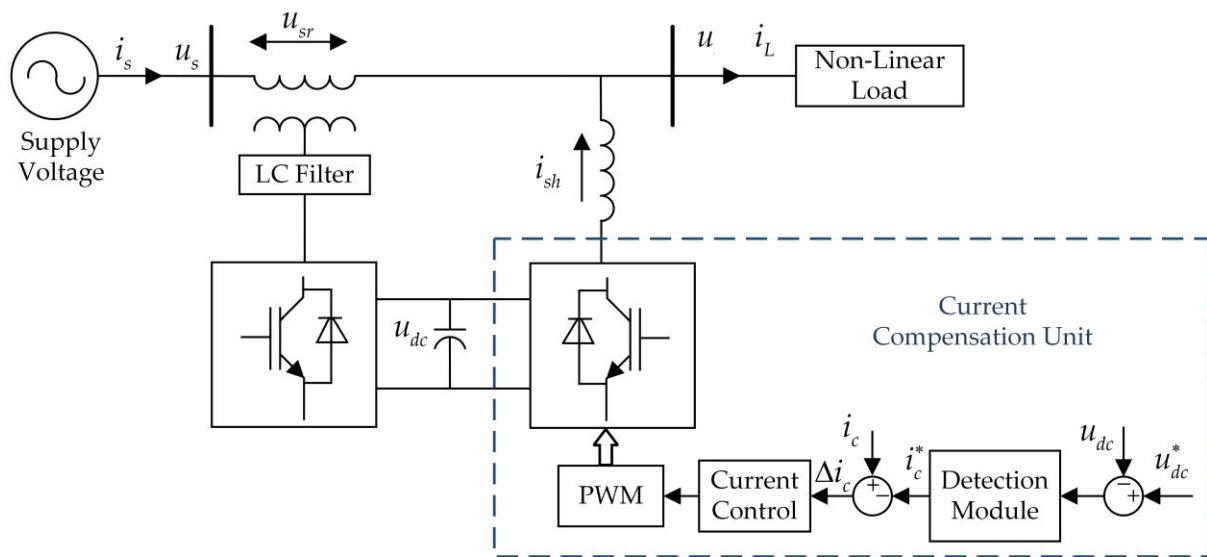
The series voltage compensation unit primarily achieves voltage compensation through an inverter installed between the load side and the grid. This inverter monitors and analyzes the grid voltage in real time, generating the corresponding compensation voltage signal to compensate for irregular waveforms such as harmonic components and instantaneous voltage sag in the grid voltage. The voltage waveform is precisely adjusted to maintain the load-side voltage in a stable and ideal state, thereby protecting sensitive loads and ensuring a high-quality supply of grid voltage.

## 2.2. Shunt Inverter Control Structure

When current disturbances occur, the series converter will be activated. Figure 2 illustrates the control structure of the series converter. The reference signal is generated in the  $dq$  reference frame. High-order harmonic components are filtered out using a low-pass filter (LPF). Finally, through the inverse park transformation, the reference signal is converted from the  $dq$  coordinate system to the  $abc$  coordinate system, as shown in Figure 3.

If the load current harmonics are used as the compensation reference, according to Kirchhoff's Current Law, the relationship between the grid source current  $i_s$ , the load current  $i_L$ , and the compensation current  $i_c$  output by the parallel compensation unit is given by:

$$i_L = i_s + i_c \quad (4)$$



**Figure 3.** UPQC shunt side structure block diagram.

The load current consists of the fundamental sine component  $i_{sf}$ , harmonic components  $i_{sh}$ , and the fluctuation component of the source current  $\Delta i_s$ :

$$i_L = i_{sf} + i_{sh} + \Delta i_s \quad (5)$$

The basic function of the parallel compensation unit is to inject a compensation current that is equal in magnitude and opposite in direction to the load harmonic current, thereby ensuring that the grid current retains only the fundamental component. The overall mathematical model of the parallel compensation unit is:

$$L \frac{di_c}{dt} + Ri_c = u - u_s \quad (6)$$

where  $L$  represents the equivalent inductance of the system;  $R$  is the equivalent resistance of the parallel compensation unit;  $u$  is the output voltage of the inverter, generated by the controller.

In addition, the parallel compensation unit not only filters the high-frequency components of the compensation current to ensure the quality of the injected current, but also dynamically responds to the fluctuations in the grid voltage. It compensates for unbalanced currents to some extent, thereby enhancing the robustness of the system.

### 3. DC Bus Voltage Control Strategy

The performance and stability of the UPQC are closely related to its internal control structure and DC voltage regulation technology. Since the inverter circuit contains numerous power semiconductor devices, which generate switching losses during operation, the DC side capacitor voltage will continuously decrease without energy replenishment, causing the UPQC to fail in its compensation tasks. On the other hand, when switching devices are turned on or off, they also interfere with the DC side voltage, leading to voltage fluctuations.

From the perspective of energy conservation in the UPQC, the energy required to maintain a constant DC side voltage is provided by the parallel converter. The parallel converter exchanges power with the AC grid by outputting active current components, thereby achieving control of the DC side voltage.

### 3.1. Active Disturbance Rejection Controller

LADRC is a linearized control method. Its core idea is to use a simple integrator chain as the standard form and then generalize the parts of the system dynamics that differ from the standard form as generalized disturbances, compensating for them. Therefore, LADRC can effectively handle all uncertainties, with advantages such as a simple topology, low-parameter tuning difficulty, and wide applicability [25–27]. The structure of the ADRC primarily consists of three parts: Linear tracking differentiator (LTD), linear extended state observer (LESO), and linear state error feedback (LSEF). For the DC voltage control of the UPQC system, it can be simplified as a first-order control. In the design of the voltage-current dual-loop control system of the inverter, the control bandwidth of the current inner loop is usually much larger than that of the voltage outer loop. When designing the controller for the voltage outer loop, the dynamic process of the current inner loop can be ignored, and the output current  $i_d$  is considered to track the given value  $i_d^*$  of the voltage control outer loop in real time. For a first-order controlled object, the following can be derived:

$$u_0 = f[\omega(t), t] + (b - b_0)i_d^* + b_0i_d^* \quad (7)$$

where  $f[\omega(t), t]$  represents the model errors, input power, and other internal and external disturbances and uncertainties;  $b$  is the unknown controller gain; and  $b_0$  is the set approximate controller gain.

Consider  $f[\omega(t), t]$  and  $(b - b_0)i_d^*$  as the total disturbances, and design a second-order LESO for state variable observation and disturbance estimation:

$$\begin{cases} e = z_1 - u_{dc} \\ \dot{z}_1 = z_2 - \beta_1 e + b_0 i_d^* \\ \dot{z}_2 = -\beta_2 e \end{cases} \quad (8)$$

$$\begin{cases} \beta_1 = 2\omega_0 \\ \beta_2 = \omega_0^2 \end{cases} \quad (9)$$

where  $e$  is the state variable observation error;  $\beta_1$  and  $\beta_2$  are the correction coefficients of the extended state observer, and  $\omega_0$  is the observation bandwidth of the observer.

In ADRC,  $z_1$ ,  $z_2$  and  $b_0$  are key control variables.  $z_1$  represents the system's total disturbance estimation, including both external disturbances and internal system dynamics.  $z_2$  is the second-order disturbance estimate obtained via the LESO, which represents the rate of change of the disturbance or its higher-order dynamic features.  $b_0$  is the control gain used to adjust the effectiveness of disturbance compensation, ensuring robust system performance. By estimating these disturbances in real time, ADRC allows for dynamic compensation of both external disturbances and internal uncertainties.

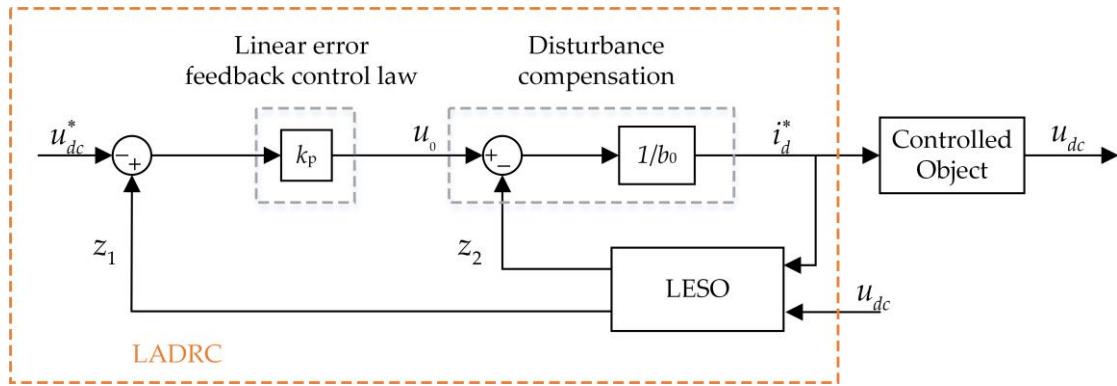
$$i_d^* = \frac{1}{b_0}[k_p(u_{dc}^* - z_1) - z_2] \quad (10)$$

where  $u_{dc}^*$  is the expected value of the DC side capacitor voltage, and  $k_p$  is the proportional gain of the controller.

By substituting Equation (10) into Equation (7), we obtain:

$$u_0 = k_p(u_{dc}^* - z_1) \quad (11)$$

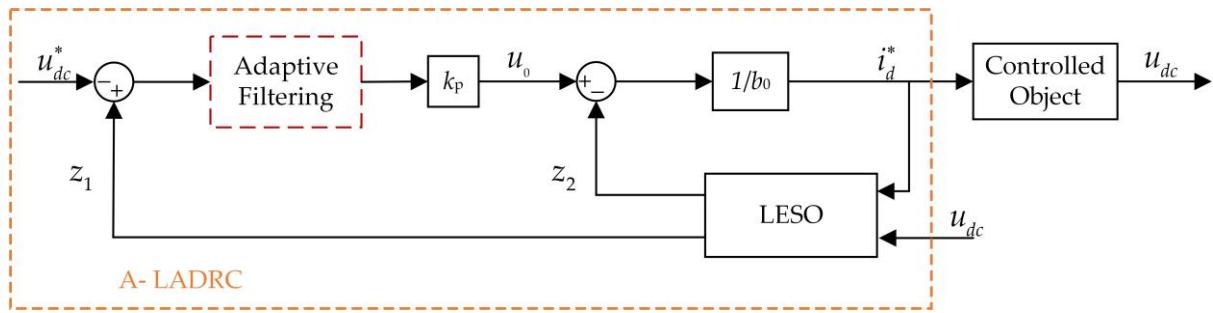
The simplified first-order LADRC control structure can be obtained, as shown in Figure 4.



**Figure 4.** LADRC control structure block diagram.

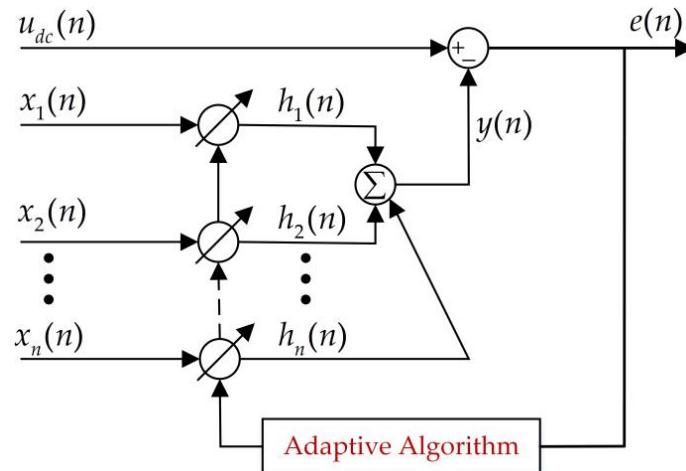
### 3.2. Active Disturbance Rejection Controller Combined with Adaptive Filter Structure

In order to achieve precise control of the DC-side voltage, it can be seen from the first-order LADRC control structure that the discrepancy among the reference and estimated variables must be addressed prior to the proportional section of the control framework. Therefore, an adaptive filter part is introduced before the proportional section to filter the deviation signal, reducing signal fluctuations during the input filtering stage, and thus minimizing the impact on DC-side voltage control [28]. Figure 5 shows the adaptive filter combined with linear active disturbance rejection control (A-LADRC).



**Figure 5.** A-LADRC structure block diagram.

The specific internal structure of the adaptive filter is shown in Figure 6.



**Figure 6.** Adaptive filter structure.

In the above model,  $x(n)$  is the input signal,  $y(n)$  is the output signal, and  $h(n)$  represents the filter weights. As shown in figure, the filter handles the input by assigning weights, with the weights in the predictor being updated iteratively through an adaptive algorithm.

The weight vector is denoted as:

$$H(n) = [h_1(n), h_2(n), \dots, h_{D-1}(n)]^T \quad (12)$$

The input vector is denoted as:

$$X(n) = [x_1(n), x_2(n), \dots, x_n(n)]^T \quad (13)$$

By setting the initial values of the weight vector  $h(n)$  and the sampling signal  $x(n)$ , the desired signal  $u_{dc}^*$  is determined, and the output  $y(n)$  is calculated as follows:

$$y(n) = \sum_{m=0}^{D-1} h(n)x(n-m+D) \quad (14)$$

We define the target output of the filter as  $d(n)$ , the difference between the target output and the predicted output is the error, as follows:

$$e(n) = u_{dc}(n) - z_1(n) \quad (15)$$

From the relationship between the output and input of the filter, it can be observed that as the error signal of the filter continuously approaches zero, the filtering effect of the deviation signal can be effectively guaranteed, minimizing influence of disturbances on the system. The weight update process of the filter is associated with the adaptive algorithm module in the model. Among these algorithms, the LMS algorithm is the most widely used due to its simple structure, strong robustness, and ease of implementation [29,30].

$$\nabla e^2(n) = -2e(n)x(n) \quad (16)$$

Using the gradient descent method, the weight vector can be updated as:

$$h(n+1) = h(n) + \mu e(n)x(n) \quad (17)$$

The control strategy for the DC side voltage using the LADRC method is as follows:

$$\begin{cases} \dot{z}_1(n) = z_2(n) - \beta_1[z_1(n) - u_{dc}(n)] + b_{u0}i_d^*(n) \\ \dot{z}_2(n) = -\beta_2[z_1(n) - u_{dc}(n)] \\ x(n) = u_{ref}(n) - z_1(n) \\ y(n) = h^T(n)X(n) \\ e(n) = [u_{ref}(n) - z_1(n)] - y(n) \\ h(n+1) = h(n) + \mu e(n)X(n) \\ u_0(n) = k_p \cdot y(n) \\ i_d^*(n) = [u_0(n) - z_2(n)]/b_0 \end{cases} \quad (18)$$

### 3.3. Improved Control Strategy Combined with the Variable Step-Size Algorithm

In the LMS algorithm, the variation of the  $\mu$  value should ensure the algorithm has excellent convergence speed and steady-state error. The traditional fixed step-size algorithm fails to simultaneously ensure a positive correlation between the fixed step-size  $\mu$  and the convergence speed requirements and steady-state error. Therefore,  $\mu$  should be designed to vary with the iteration process to balance convergence speed and steady-state error.

### 3.3.1. The Instantaneous Error-Based Variable Step-Size Algorithm

To address the constraints of the fixed-step algorithm, this paper incorporates a variable step-size algorithm based on instantaneous error into the model, leading to the combination of the instantaneous error adaptive filter and LADRC (IVA-LADRC). This adjustment replaces the fixed step-size with a variable one, facilitating more accurate control of voltage. The instantaneous error variable step-size algorithm dynamically adjusts the step-size to optimize both control accuracy and response speed. When the system error is large, the step-size is increased to accelerate the convergence rate; conversely, when the error is small, the step-size is reduced to enhance precision and avoid overshoot. The mathematical expression is as follows:

$$\mu(n) = a\mu(n - 1) + be^2(n) \quad (19)$$

The parameters  $a$  and  $b$  play complementary roles in the instantaneous error-based variable step-size algorithm:  $a$  determines the smoothness and stability of the step-size; when  $a$  is large, the step-size changes more smoothly but adapts more slowly to environmental variations. Meanwhile,  $b$  governs the sensitivity of the step-size to the error; when  $b$  is large, the step-size responds more rapidly to error changes but may lead to oscillations. In this paper,  $a = 0.7$  and  $b = 0.01$ .

### 3.3.2. The Improved Variable Step-Size Algorithm for the S-Function

In contrast to the instantaneous error, the S-function adaptive filter integrated with LADRC (SVA-LADRC) incorporates a nonlinear mapping mechanism, which dynamically transforms the error into a smooth and constrained step-size. This significantly enhances the robustness and convergence performance of the algorithm. By controlling the steepness of the S-function, the sensitivity of step-size variation can be flexibly adjusted, effectively avoiding oscillations and instability caused by noise or sharp fluctuations in error, which are typical issues in the instantaneous error algorithm. Additionally, it suppresses excessive step-size adjustment under extreme error conditions. This approach is well-suited for nonlinear, dynamic environments, or optimization scenarios with high noise levels, exhibiting stronger adaptability and stability. The mathematical expression is as follows:

$$\mu(n) = b\left(\frac{1}{1 + e^{-a|e(n)|}} - 0.5\right) \quad (20)$$

In the S-function variable step-size algorithm, the parameters  $a$  and  $b$  control the sensitivity of step-size adjustment and the central position, respectively. Parameter  $a$  determines the steepness of the S-function; the steeper the function, the more sensitive the step-size is to error changes. However, if  $a$  is too large, it may lead to oscillations, while if it is too small, the adjustment may become sluggish. Parameter  $b$  determines the horizontal shift of the S-function, affecting the threshold range for step-size adjustment. When  $b$  is large, it is suitable for scenarios with larger errors, and when  $b$  is small, it is better for precise adjustment in cases of small errors. In this paper,  $a = -0.015$  and  $b = 0.001$ .

### 3.3.3. The Variable Step-Size Algorithm Based on the Arctangent Function

Although the specific principles of variable step-size algorithms differ, they all adhere to a core adjustment strategy. Generally, a larger step-size is employed in the early stages of iteration or when the error is significant to accelerate convergence. In the steady state or when the error has been minimized, a fixed step-size factor is applied to reduce the mean square error. This paper proposes the use of the arctangent function to create a nonlinear relationship between the error and the step-size. The arctangent function adaptive filter combined with linear active disturbance rejection control (AVA-

LADRC) demonstrates better convergence, stability, and noise adaptability compared to the S-function and instantaneous error variable step-size algorithms. Due to the bounded and smooth output of the arctangent function, it provides rapid convergence when the error is large and gradually decreases the step-size as the error reduces, thereby avoiding the risk of over-adjustment. Moreover, the nonlinear characteristics of the arctangent function make the step-size adjustment more flexible, capable of adapting to different error environments and noise variations, thus improving the stability and robustness of the system. In contrast, the S-function may converge slowly under some extreme conditions, and the instantaneous error method is overly sensitive to error fluctuations, potentially leading to unstable behavior. The improved method introduces three adjustable parameters to account for different noise conditions. The modified step-size coefficient is represented as:

$$\mu(n) = b \left( \frac{3}{(1 + \exp(-a|\arctan(e(n))|))^c} - 1 \right) \quad (21)$$

The parameters  $a$ ,  $b$ , and  $c$  in the variable step-size adaptive algorithm influence different characteristics of the algorithm. Parameter  $a$  controls the algorithm's sensitivity to the error; increasing  $a$  accelerates the convergence speed but may increase the steady-state error. Parameter  $b$  affects the upper limit of the maximum step-size; increasing  $b$  can accelerate convergence, but if  $b$  is too large, it may lead to an increase in the error. Parameter  $c$  mainly adjusts the smoothness of the algorithm; increasing  $c$  enhances the convergence speed and smoothens the bottom of the response, but it also increases computational complexity. In this paper,  $a = 0.97$ ,  $b = 0.003$ , and  $c = 4$ .

The variable step-size algorithm in Equation (21) ensures fast convergence while avoiding oscillations caused by excessive step-size adjustments. Compared to the instantaneous error-based algorithm in Equation (19), the nonlinear characteristics of the arctangent function in Equation (21) accelerate convergence when the error is large and smoothly adjust the step-size when the error is small, thereby improving control accuracy. Moreover, in contrast to the S-function algorithm in Equation (20), the algorithm in Equation (21) demonstrates better stability and robustness under noisy conditions or when error fluctuations are significant. Its three adjustable parameters allow the algorithm to flexibly adapt to different operating environments and error conditions, resulting in superior control performance in various scenarios. Therefore, in this study, we consider the variable step-size algorithm in Equation (21) to be the optimal choice.

#### 4. Simulation Verification

To test the control performance of the proposed algorithm, a simulation platform was built to replicate various operational conditions in real-world scenarios. A comprehensive evaluation of the algorithm's performance in dynamic environments was conducted, focusing on its convergence speed, stability, and robustness. Table 1 below presents the system parameters used in the experimental platform.

**Table 1.** Parameters of system.

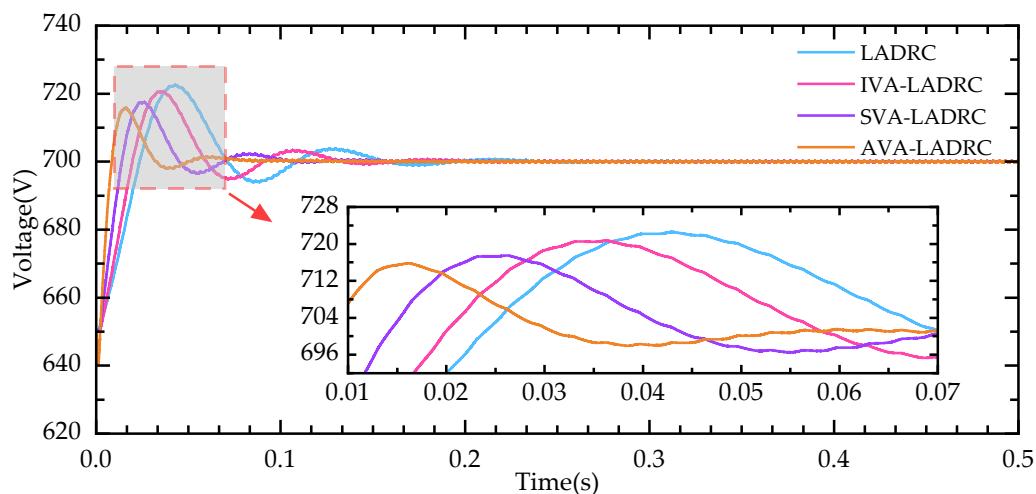
Parameters	Value
Line to Line Voltage of the Grid	380 V
Phase Voltage of the Grid	220 V
Grid Frequency	50 Hz
Forward Voltage Drop	0.8 V

**Table 1.** Cont.

Parameters	Value
Nonlinear Load	50 Ω 300 mH
Sudden Nonlinear load	50 Ω 300 mH
Voltage Sag	266 V
DC Link Voltage	700 V
DC Link Capacitance	3300 μF
Line Impedance	10 mH
Inverter Resistance	1 mΩ

#### 4.1. Normal Stable Conditions

Figure 7 illustrates the DC-side voltage waveform, showing the stability and convergence of the voltage under four different control methods: LADRC, IVA-LADRC, SVA-LADRC, and VAV-LADRC. The analysis does not take into account variations on the grid side and load side.

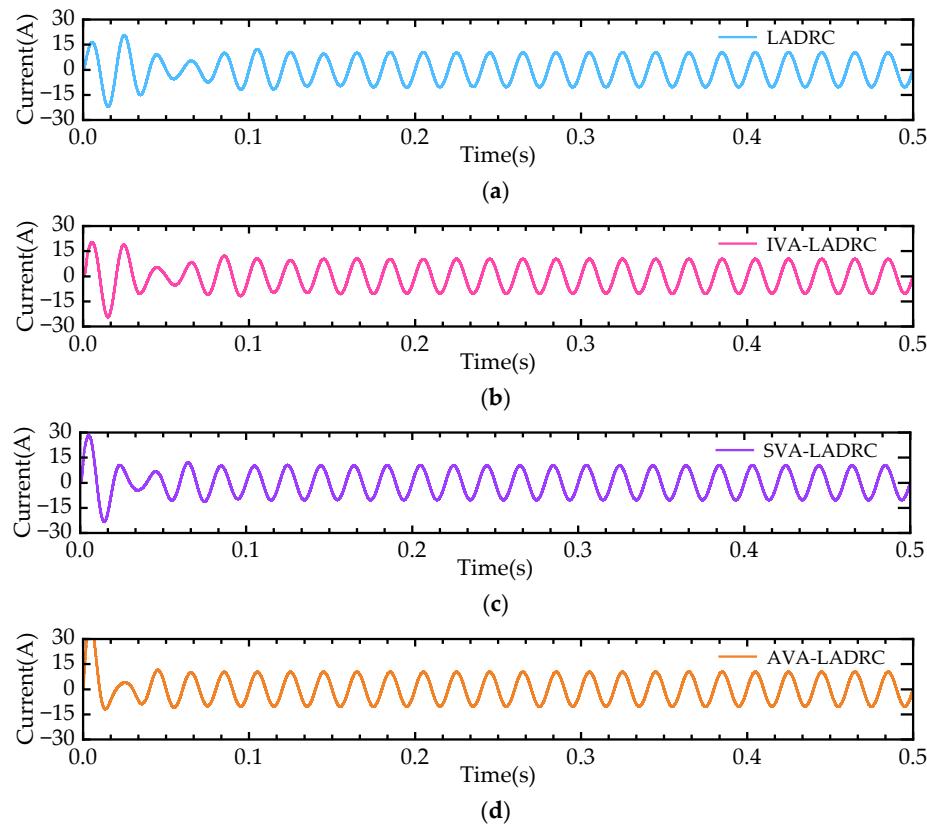


**Figure 7.** DC-side voltage waveform under normal states.

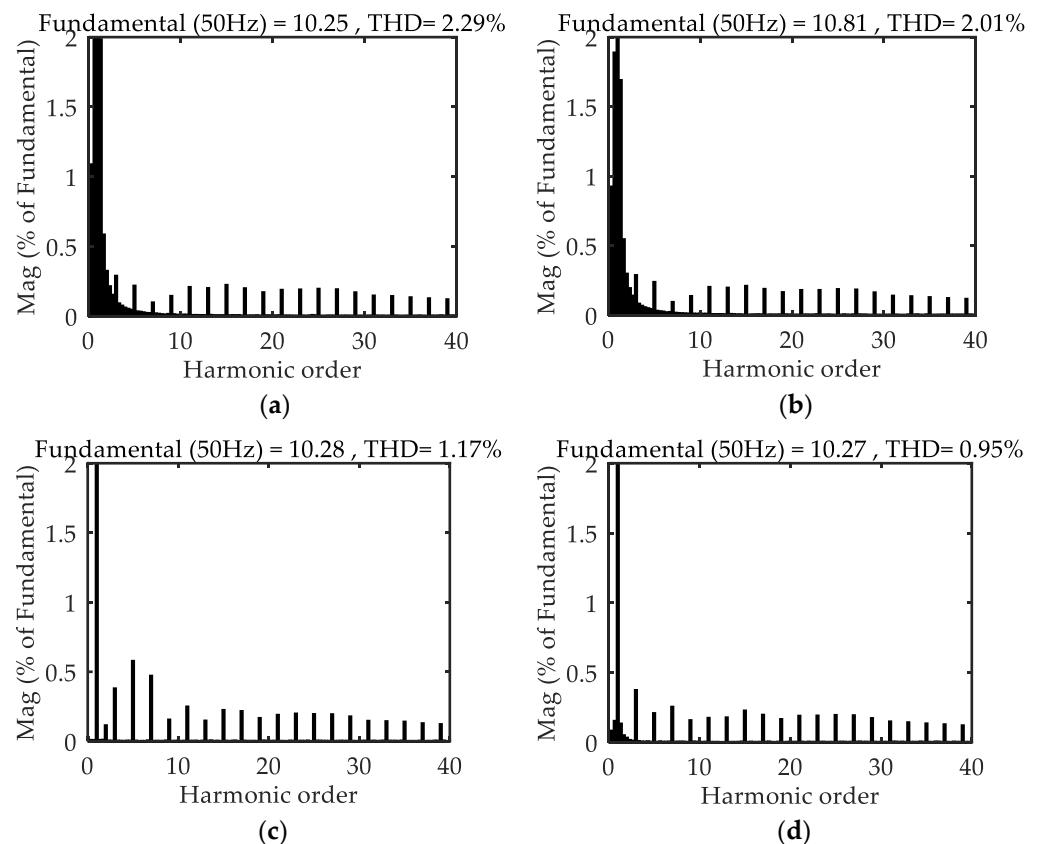
By comparing the test results shown in Figure 7, it can be observed that, under the VAV-LADRC method, the fluctuations and convergence speed of the DC-side voltage near normal conditions are significantly lower than those of the other three methods. Furthermore, the VAV-LADRC method demonstrates stronger robustness and more precise steady-state control when addressing voltage control issues, exhibiting superior control characteristics.

Considering that the load is nonlinear in practical situations, harmonic distortion will occur in the current waveform. Figure 8 shows the current waveform after harmonic compensation at 0.15 s, once the system reaches stability. The compensated current values are presented in Figure 9.

By performing a Fourier transform analysis on the steady-state period (0.15 s), it can be observed that the proposed improvement method significantly reduces the spikes in the waveform compared to traditional methods. Under the traditional LADRC method, the THD of the phase A current is 2.29%; under the IVA-LADRC control method, it is 2.01%; under the SVA-LADRC control method, it is 1.17%; and under the proposed AVA-LADRC method, the THD is reduced to 0.95%. The proposed method significantly reduces the harmonic content, particularly the higher-order harmonics, and effectively suppresses them, leading to a substantial decrease in THD.



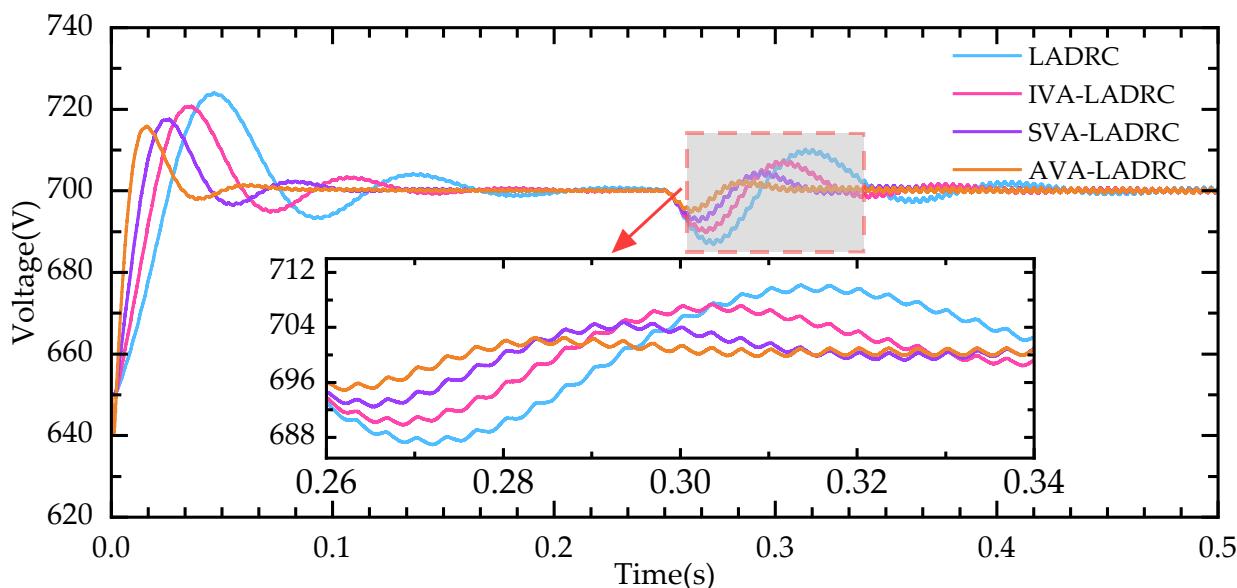
**Figure 8.** Current waveform under stable states: (a) LADRC; (b) IVA-LADRC; (c) SVA-LADRC; (d) VAV-LADRC.



**Figure 9.** THD of phase A current under stable states: (a) LADRC; (b) IVA-LADRC; (c) SVA-LADRC; (d) VAV-LADRC.

#### 4.2. Sudden Load Conditions

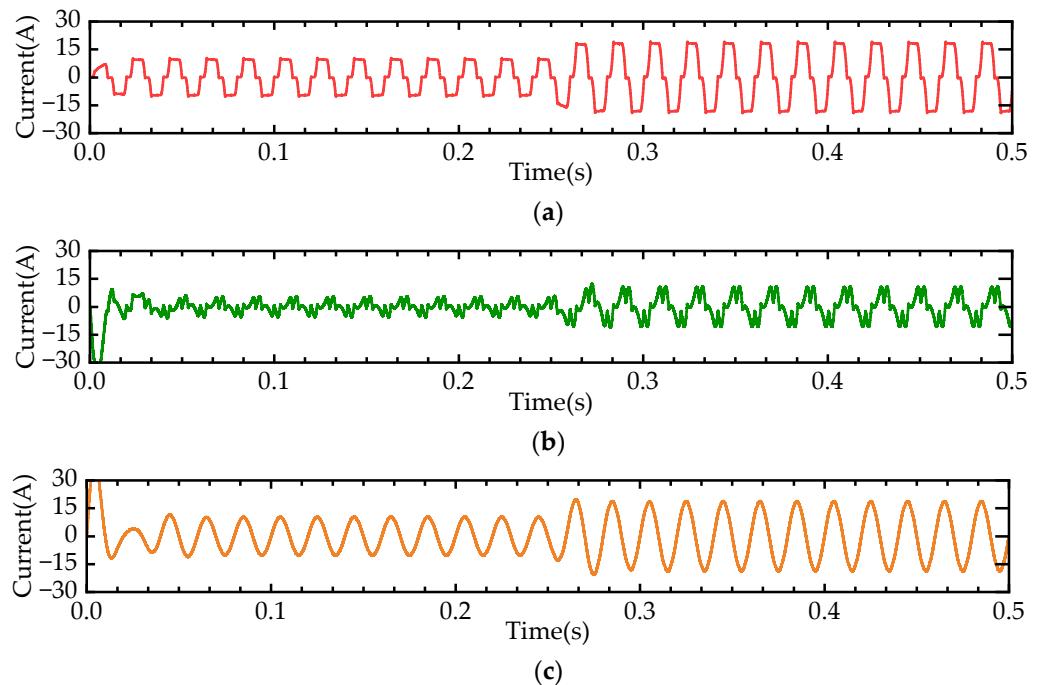
In practical applications, sudden load changes can cause voltage fluctuations, which may affect the normal operation of the system. To assess the performance of the proposed control strategy in responding to sudden load changes, we will simulate the system response under varying load conditions. By comparing the performance of different control methods after the load change, we can further validate the adaptability and effectiveness of the proposed method in real-world load-variation scenarios. Figure 10 below shows the DC-side voltage waveform when the load changes suddenly to  $50\ \Omega$  and  $300\text{ mH}$  at  $0.25\text{ s}$ .



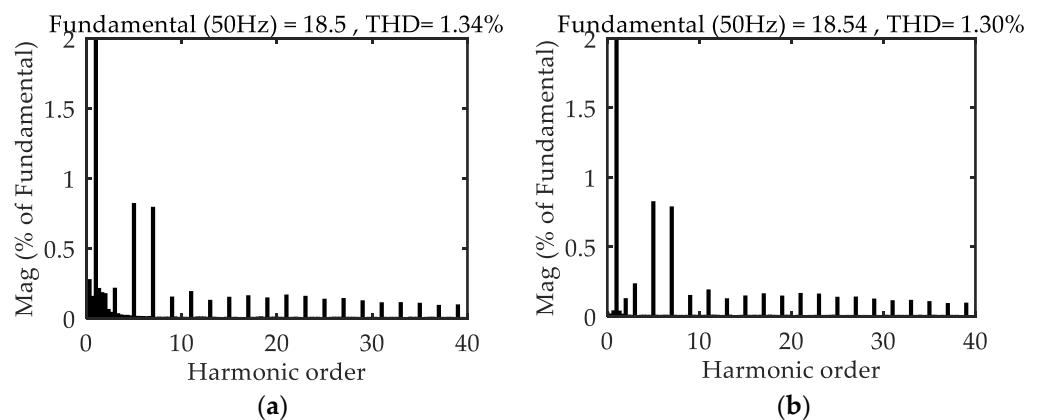
**Figure 10.** DC-side voltage waveform under sudden load conditions.

As shown in Figure 10, the improved control strategy achieves more stable control. Compared to traditional methods, this approach demonstrates superior performance in maintaining steady-state voltage and suppressing voltage fluctuations, effectively reducing voltage deviations and improving steady-state accuracy. Furthermore, the proposed method exhibits better convergence characteristics, enabling the system to stabilize more quickly in a shorter time, significantly enhancing the control response speed and precision. This ultimately improves the stability and reliability of the system under dynamic conditions.

Taking phase A as an example, as shown in Figure 11a, the waveform of the load current under a sudden change at  $0.25\text{ s}$  is displayed. Figure 11b shows the waveform of the compensating current injected by the device, while Figure 11c presents the compensated grid current waveform. Clearly, when the system encounters a sudden change in the nonlinear load, the proposed improved control method still maintains superior performance, significantly improving both the current waveform and the DC-side voltage waveform. Figure 12 show the THD of phase A current at different times after the load change.



**Figure 11.** Current waveform under sudden load conditions using the AVA-LADRC method: (a) Load current; (b) Inject current; (c) Grid current.

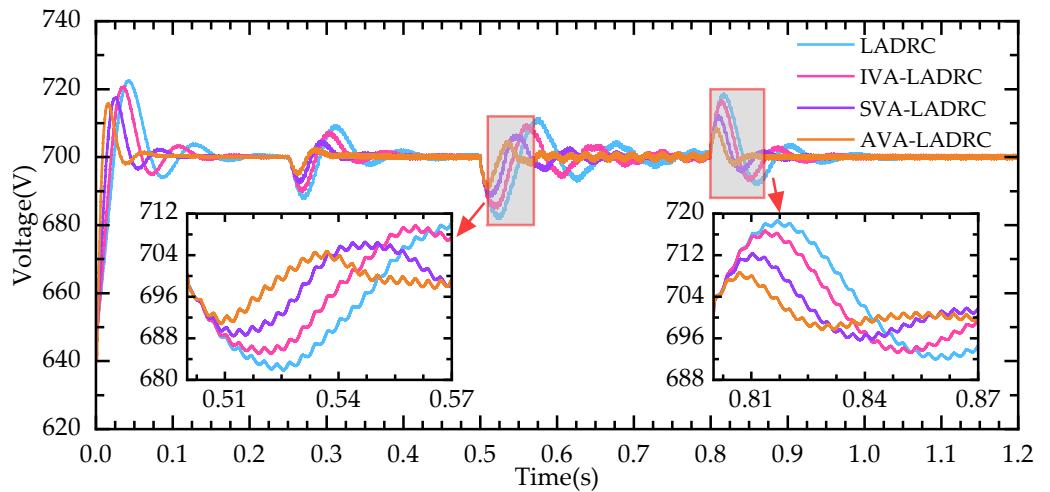


**Figure 12.** THD of phase A current at different times under sudden load conditions: (a) 0.3 s; (b) 0.4 s.

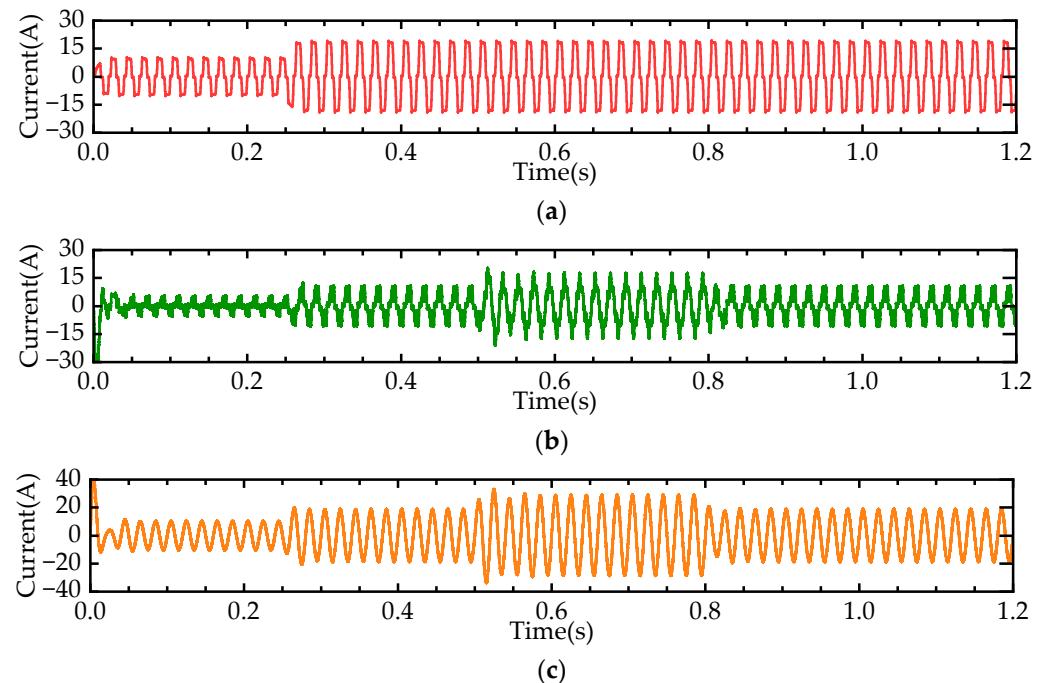
#### 4.3. Voltage Sag Conditions

A sudden voltage drop on the supply side is a common power-quality issue in electrical systems, typically caused by factors such as short-circuit faults, large power equipment startups, system overloads, line switching or tripping, and natural disasters. This issue significantly impacts the system's operational stability and the reliability of load equipment. To investigate the effects of sudden voltage drops on system performance, this chapter presents a simulation study, modeling a scenario where the supply-side voltage drops from 380 V to 266 V at 0.5 s and recovers to the rated value at 0.8 s. As shown in Figure 13:

Under the condition of a sudden voltage drop on the supply side, the proposed control strategy significantly improves the stability of the DC-side voltage. Compared to traditional methods, this approach can suppress voltage fluctuations more quickly after the voltage drop, avoiding the larger fluctuations and recovery delays that may occur with traditional methods, while maintaining higher steady-state accuracy. Under this condition, the system's load current, compensation current, and grid current are shown in Figure 14:



**Figure 13.** DC-side voltage waveform under voltage sag states.

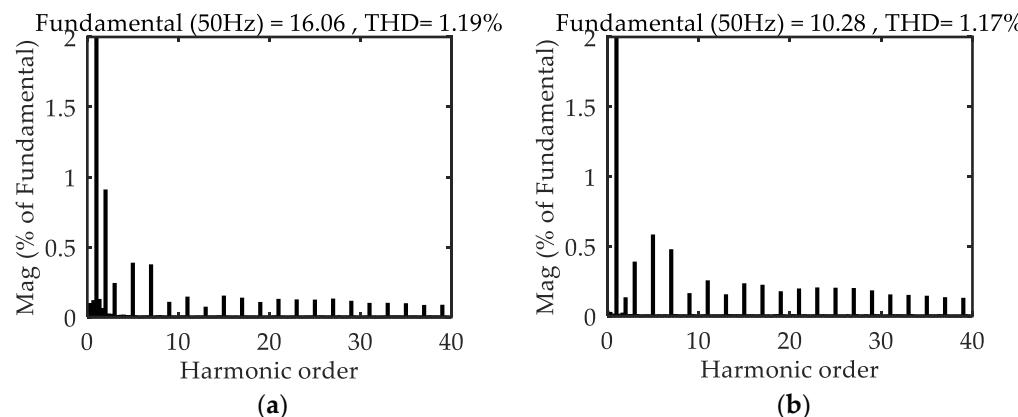


**Figure 14.** Current waveform under voltage sag conditions using the AVA-LADRC method: (a) Load current; (b) Inject current; (c) Grid current.

By analyzing the data in Figure 14, it is evident that under the condition of a sudden voltage drop on the supply side, the proposed improved control method still effectively maintains the system's stable operation. It prevents the adverse effects of severe voltage fluctuations on system performance, while effectively suppressing high-frequency noise and harmonics in the current waveform. This results in a significant reduction in the THD of the current. This optimization ensures a smoother recovery process after the voltage drop, enhancing the overall dynamic response and power quality. The THD of the phase A current at 0.6 s and 0.9 s is shown in Figure 15.

The improved control method can significantly reduce the harmonic distortion rate, greatly improving the system's power quality and enhancing the operational efficiency and stability of the equipment. The reduction in harmonics minimizes energy losses, equipment overheating, and the risk of failures caused by excessive harmonics, thereby extending the lifespan of the system and equipment. Furthermore, the optimized control method enhances the smoothness of the current and voltage waveforms, reduces the system's

pollution to the grid, and complies with power quality standards, thereby strengthening the system's reliability.



**Figure 15.** THD of phase A current at different times under voltage sag conditions: (a) 0.6 s; (b) 0.9 s.

## 5. Grid-Connected Photovoltaic Power Generation System

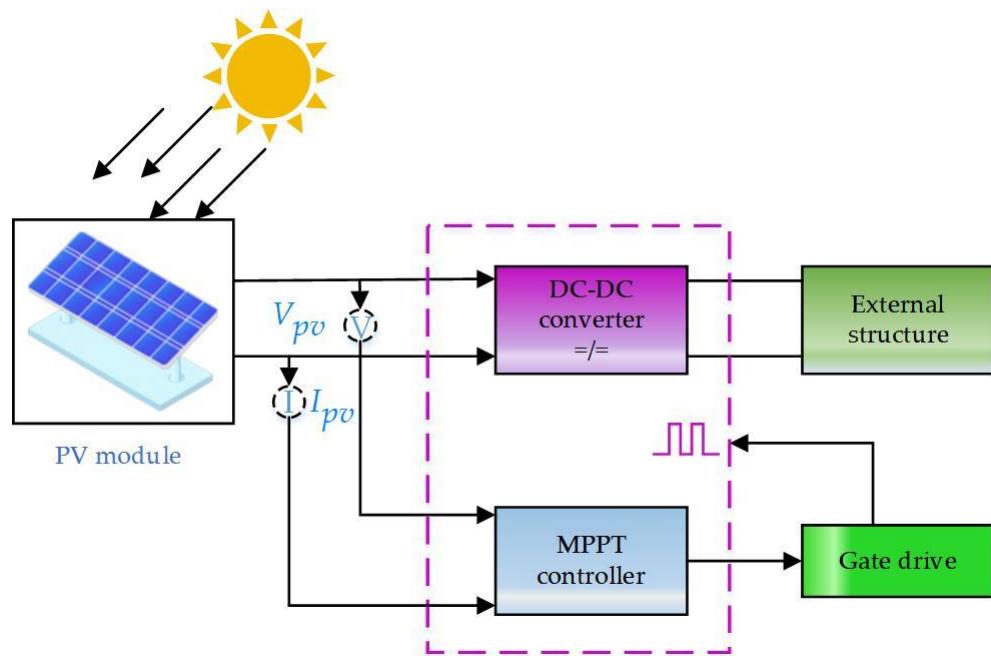
To test the applicability of the proposed control strategy in the current renewable energy-generation environment, this paper integrates the renewable energy-generation system into the grid for evaluation. As a typical renewable energy application, the photovoltaic (PV) grid-connected system has strong dynamic characteristics and a complex operating environment, thus requiring advanced control strategies. By incorporating the proposed improved control method into the PV grid-connected system, we can evaluate its stability and response speed under different operating conditions, providing a theoretical foundation for optimizing control strategies in future energy systems.

### 5.1. Principle of Photovoltaic Systems

PV power generation is a renewable energy technology that converts solar radiation into electricity through photovoltaic modules [31–33]. When sunlight hits the semiconductor materials in the PV panels, the photovoltaic effect releases electrons, generating electrical current. The electricity produced is clean, renewable, and low-maintenance. With technological advancements, costs have decreased, making PV an integral part of sustainable energy.

Maximum Power Point Tracking (MPPT) is a key technology in PV systems. It dynamically adjusts voltage or current to ensure the system operates at its maximum power point, optimizing panel output and enhancing overall efficiency [34,35]. In environments with fluctuating sunlight, MPPT algorithms continuously track the optimal operating point, ensuring maximum power generation under varying weather conditions. The structure of the PV grid-connected system is shown in Figure 16.

In this study, the current of the typical harmonics is primarily analyzed on the output current of the photovoltaic system, which is the current fed into the grid through the inverter. This point is where changes in solar radiation directly affect the harmonic content and distortion characteristics of the current. In Figure 16, the structure of the photovoltaic system is shown, and the harmonic analysis is based on the output current at the inverter output terminal. Additionally, the proposed AVA-LADRC is applied to the photovoltaic system to address disturbances caused by variations in solar radiation and optimize system performance. AVA-LADRC dynamically adjusts the control step size and real-time system parameters to ensure MPPT and minimize power loss. The algorithm works in coordination with the inverter control system in the photovoltaic system, effectively responding to environmental changes.



**Figure 16.** Photovoltaic system working principle block diagram.

ANN methods have significant advantages in MPPT due to their strong non-linear modeling capabilities and high precision in power tracking. The conventional inputs for an ANN-based MPPT system are typically solar irradiance, temperature, photovoltaic voltage ( $V_{PV}$ ), and photovoltaic current ( $I_{PV}$ ). In this section, alternative inputs based on the importance of the power-voltage relationship slope are proposed. These inputs include the error signal ( $dP/dV$ ) and the second input, which is the rate of change of the error signal ( $\Delta E$ ). At the maximum power point, the error signal is zero ( $dP/dV = 0$ ). When the photovoltaic voltage deviates slightly from this point, a response is required to address this deviation. The second input ( $\Delta E$ ) represents the trend of the error change, indicating whether the error is increasing or decreasing. Figure 17 illustrates the ANN architecture used for MPPT,

$$E(n) = \frac{\Delta P}{\Delta V} = \frac{V_{PV}(n)I_{PV}(n) - V_{PV}(n-1)I_{PV}(n-1)}{V_{PV}(n) - V_{PV}(n-1)} \quad (22)$$

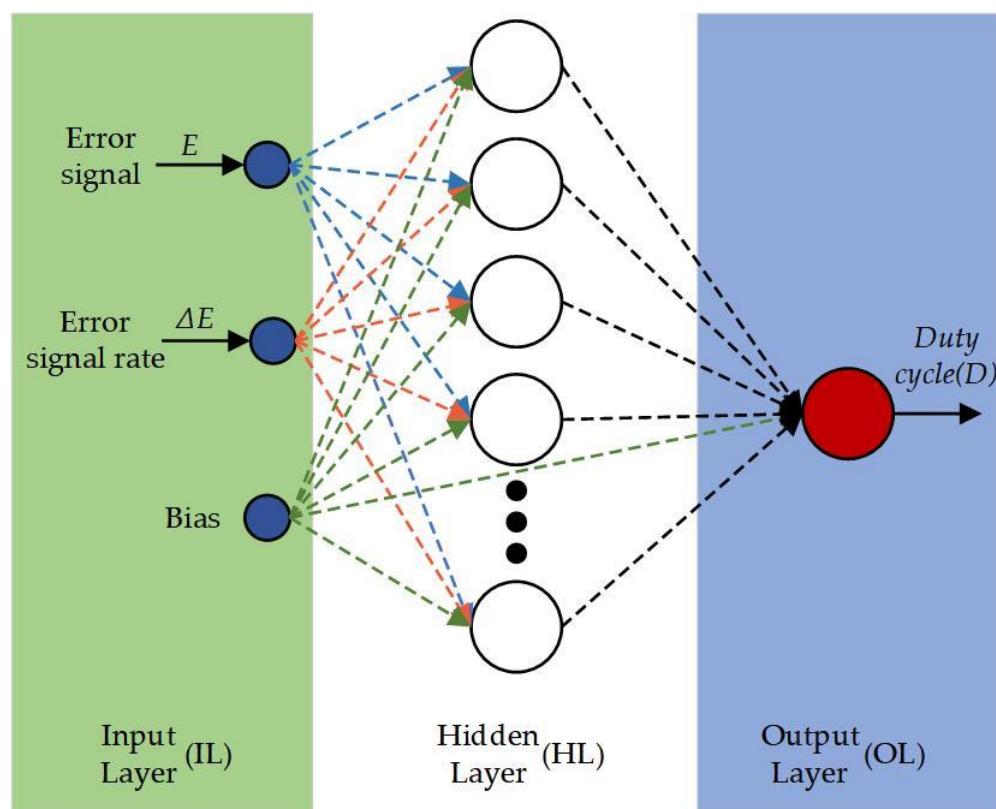
$$\Delta E(n) = E(n) - E(n-1) \quad (23)$$

where  $E$  represents the error signal and  $\Delta E$  represents the rate of change of the error signal.

In the UPQC system presented in this paper, the PV power-generation system is integrated on the load side, operating in parallel with the load, and together with the UPQC, they collaboratively optimize power quality. The parameters of the photovoltaic power-generation system are shown in Table 2.

**Table 2.** Parameters of photovoltaic power-generation system.

Parameters	Value
Temperature	25 °C
Maximum Power Point Output Voltage	250 V
Maximum Power Point Output Current	40 A
Open-circuit Voltage	330 V
Short-circuit Current	48 A



**Figure 17.** ANN control structure diagram.

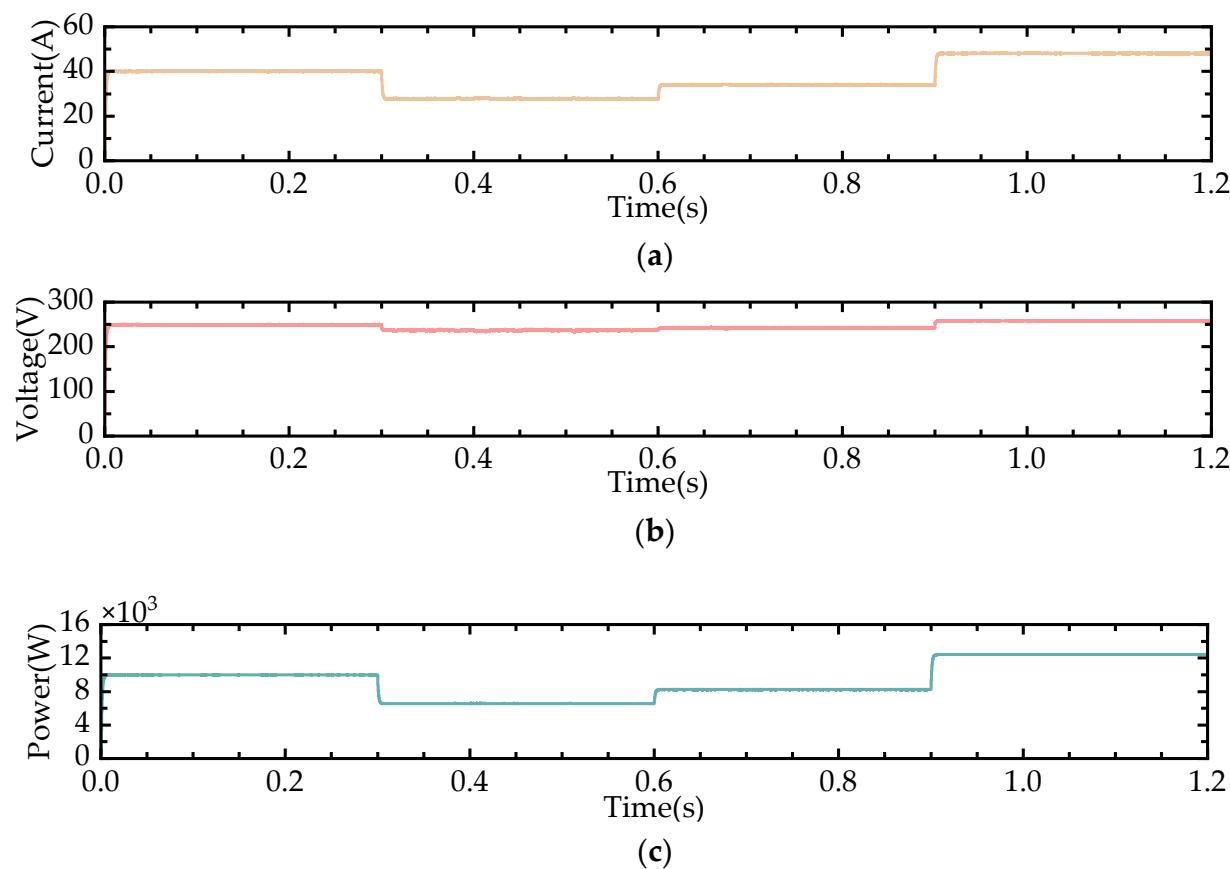
### 5.2. System Simulation Verification Under Dynamic Solar Irradiance

In order to comprehensively validate the superiority of the photovoltaic grid-connected system in practical applications, this study simulates varying solar irradiance conditions and explores the impact of solar irradiance variations on system performance. Solar irradiance is one of the key factors affecting photovoltaic power generation efficiency. By conducting experiments under different irradiance conditions, the stability, response speed, and energy output capability of the photovoltaic grid-connected system under varying weather, time periods, and seasonal changes can be more accurately reflected. The variation of solar irradiance is shown in Table 3, and Figure 18 illustrates the current, voltage, and power output of the photovoltaic module under varying irradiance conditions.

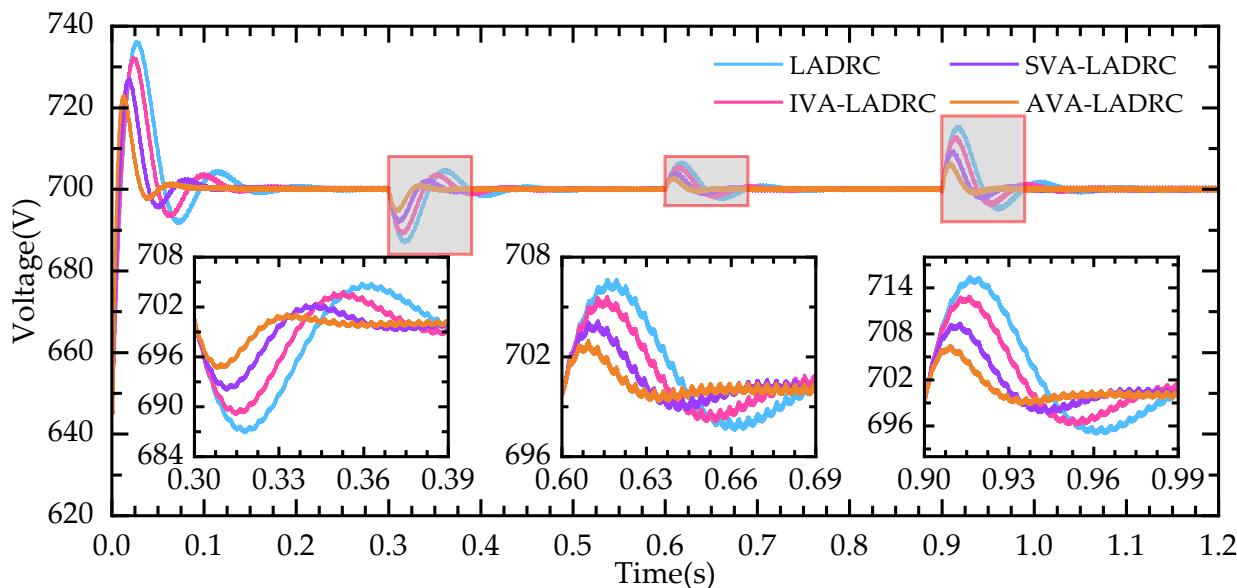
**Table 3.** Dynamic variation of solar irradiance.

Time	Irradiance
0–0.3 s	1000 W/m <sup>2</sup>
0.3–0.6 s	700 W/m <sup>2</sup>
0.6–0.9 s	800 W/m <sup>2</sup>
0.9–1.2 s	1200 W/m <sup>2</sup>

Figure 19 demonstrates that, as the solar irradiance changes, the AVA-LADRC control method continues to effectively stabilize the DC-side voltage. Compared to the other three control methods, this approach exhibits superior performance under dynamic irradiance conditions, ensuring the stability of the voltage waveform and control accuracy. After grid connection, the load current, compensation current, and phase A grid current waveforms of the system are shown in Figure 20.

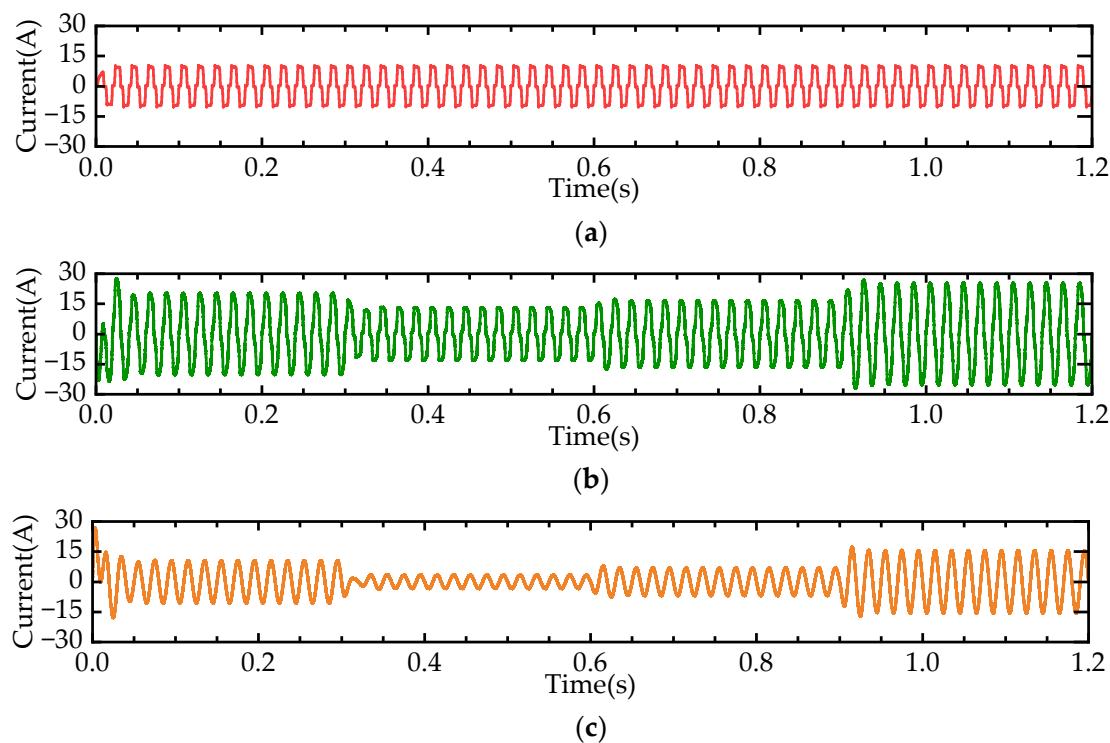


**Figure 18.** Photovoltaic module output: (a) Current; (b) Voltage; (c) Power.

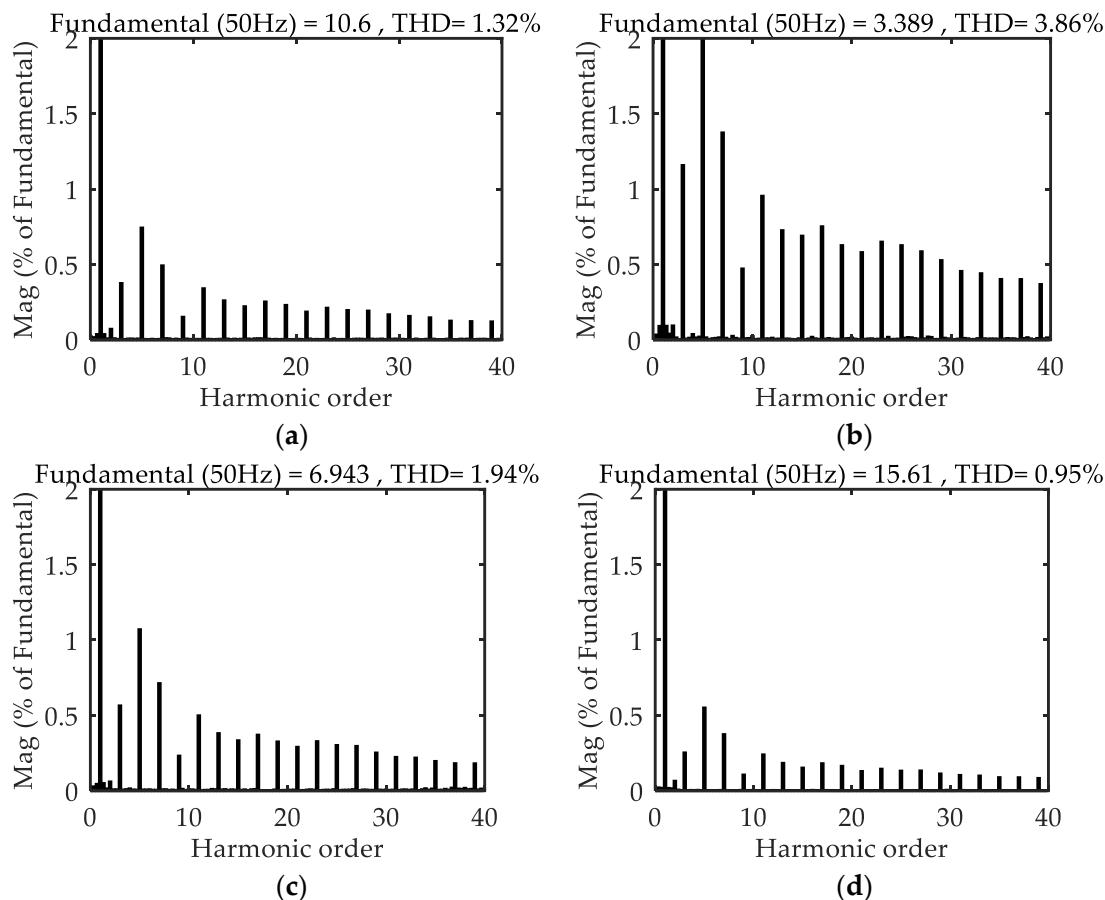


**Figure 19.** DC-side voltage waveform under dynamic solar irradiance.

It can be observed that the control strategy proposed in this study still maintains good control performance in the photovoltaic grid-connected system, with stable output current waveforms. The THD of the phase A current at different time points under varying irradiance conditions are shown in Figure 21.



**Figure 20.** Current waveform under dynamic solar irradiance using the AVA-LADRC method:  
(a) Load current; (b) Inject current; (c) Grid current.



**Figure 21.** THD of phase A current at different times under dynamic solar irradiance using the AVA-LADRC method: (a) 0.1 s; (b) 0.4 s; (c) 0.7 s; (d) 1 s.

As shown in Figure 21, the proposed VAV-LADRC control method not only effectively reduces the impact of harmonics but also maintains excellent current quality despite fluctuations in the photovoltaic output power. The harmonic distortion rate remains at a consistently low level and meets the grid-connected system control requirement of 5%. This further validates the strong adaptability and stability of the method.

## 6. Conclusions

This paper proposes an improved control method aimed at enhancing the performance of the UPQC DC-side voltage control and verifies its application in a renewable energy grid-connected system. Through comparative experiments with LADRC, IVA-LADRC, SVA-LADRC, and VAV-LADRC methods, the superiority of the proposed approach in voltage stability and harmonic suppression is validated, with notable advantages in dynamic response and control accuracy. To further evaluate the performance of the VAV-LADRC control method, the photovoltaic power-generation system was integrated into the system, and the stability of the system was simulated under dynamic light intensity variations. Experimental results show that the proposed control strategy can effectively maintain the stability of the DC-side voltage in a dynamically changing light environment, significantly reducing voltage fluctuations, and performing well in harmonic suppression, with all indicators meeting the system's technical requirements. This further validates the stability and robustness of the method in complex grid-connected environments.

In conclusion, the proposed improved control method not only achieves excellent control performance in UPQC DC-side voltage regulation but also demonstrates strong adaptability and stability in photovoltaic grid-connected systems, showing promising prospects for engineering applications. As the proportion of renewable energy integrated into the grid continues to increase, distributed energy systems and power electronics technologies will play a more significant role in improving power quality. The application of the proposed control strategy in UPQC systems provides valuable insights for future power-quality management in smart grids and microgrids. Future research can further optimize the method to address more complex grid environments and explore its integration and application in large-scale photovoltaic, wind energy, and other renewable energy grid-connected systems.

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## Abbreviations

The following abbreviations are used in this manuscript:

DSTATCOM	Distribution static compensator
DVR	Dynamic voltage restorer
APF	Active power filter
UPQC	Unified power quality conditioner
DDC	Data-driven control
ANN	Artificial neural network
LADRC	Linear active disturbance rejection control
ADRC	Active disturbance rejection control
ESO	Extended state observer
NLSEF	Nonlinear state error feedback
PLL	Phase-locked loop
LMS	Least mean squares
FFT	Fast fourier transform
LPF	Low-pass filter
DC	Direct current
AC	Alternating current
LTD	Linear tracking differentiator
LESO	Linear extended state observer
LSEF	Linear state error feedback
A-LADRC	Adaptive filter combined with linear active disturbance rejection control
IVA-LADRC	Instantaneous error adaptive filter combined with linear active disturbance rejection control
SVA-LADRC	S-function adaptive filter combined with linear active disturbance rejection control
AVA-LADRC	Arctangent function adaptive filter combined with linear active disturbance rejection control
THD	Total harmonic distortion
PV	Photovoltaic
MPPT	Maximum power point tracking
P&O	Perturb and observe
Inc-Cond	Incremental conductance

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