adder Project Status (05/20/2022 - 16:52:00)			
Project File:	adder_vhdl.xise	**Parser Errors:**	No Errors
Module Name:	adder	**Implementation State:**	Programming File Generated
Target Device:	xc3s200-4vq100	• **Errors:**	No Errors
Product Version:	ISE 13.4	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	2	3,840	1%	
Number of occupied Slices	1	1,920	1%	
Number of Slices containing only related logic	1	1	100%	
Number of Slices containing unrelated logic	0	1	0%	
Total Number of 4 input LUTs	2	3,840	1%	
Number of bonded IOBs	5	63	7%	
Average Fanout of Non-Clock Nets	1.60			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:				

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Pt 20. maj 16:49:53 2022	0	0	0

Translation Report	Current	Pt 20. maj 16:51:36 2022	0	0	0
Map Report	Current	Pt 20. maj 16:51:39 2022	0	0	2 Infos (2 new)
Place and Route Report	Current	Pt 20. maj 16:51:43 2022	0	0	1 Info (1 new)
Power Report					
Post-PAR Static Timing Report	Current	Pt 20. maj 16:51:45 2022	0	0	6 Infos (6 new)
Bitgen Report	Current	Pt 20. maj 16:51:58 2022	0	0	1 Info (1 new)

Secondary Reports		**[-]**
Report Name	**Status**	**Generated**
WebTalk Report	Current	Pt 20. maj 16:51:59 2022
WebTalk Log File	Current	Pt 20. maj 16:52:00 2022

Date Generated: 05/20/2022 - 16:52:00