three_state_line_buffer Project Status (05/20/2022 - 17:18:01)			
Project File:	line_buffer.xise	**Parser Errors:**	No Errors
Module Name:	three_state_line_buffer	**Implementation State:**	Programming File Generated
Target Device:	xc3s200-4vq100	• **Errors:**	No Errors
Product Version:	ISE 13.4	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	
Number of bonded IOBs	4	63	6%	
Average Fanout of Non-Clock Nets	2.00			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Pt 20. maj 17:15:56 2022	0	0	0
Translation Report	Current	Pt 20. maj 17:17:28 2022	0	0	0
Map Report	Current	Pt 20. maj 17:17:31 2022	0	0	2 Infos (0 new)

Place and Route Report	Current	Pt 20. maj 17:17:34 2022	0	0	1 Info (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Pt 20. maj 17:17:36 2022	0	0	6 Infos (0 new)
Bitgen Report	Current	Pt 20. maj 17:17:59 2022	0	0	1 Info (0 new)

Secondary Reports		**[-]**
Report Name	**Status**	**Generated**
WebTalk Report	Current	Pt 20. maj 17:17:59 2022
WebTalk Log File	Current	Pt 20. maj 17:18:01 2022

Date Generated: 05/20/2022 - 17:18:01