mux_withselect Project Status (05/27/2022 - 16:28:18)					
Project File:	mux_withselect.xise	Parser Errors:	No Errors		
Module Name:	mux_withselect	Implementation State:	Programming File Generated		
Target Device:	xc3s200-4vq100	• Errors:	No Errors		
Product Version:	ISE 13.4	• Warnings:	No Warnings		
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed		
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:			
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)		

Device Utilization Summary					
Logic Utilization		Available	Utilization	No	te(s)
Number of 4 input LUTs	1	3,840	1%		
Number of occupied Slices	1	1,920	1%		
Number of Slices containing only related logic	1	1	100%		
Number of Slices containing unrelated logic	0	1	0%		
Total Number of 4 input LUTs	1	3,840	1%		
Number of bonded IOBs	4	63	6%		
Average Fanout of Non-Clock Nets	1.00				

Performance Summary					[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Re	port	
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Rep	ort	
Timing Constraints:					

Detailed Reports				[-]		
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Pt 27. maj 16:25:52 2022	0	0	0	

Translation Report	Current	Pt 27. maj 16:27:16 2022	0	0	0
Map Report	Current	Pt 27. maj 16:27:20 2022	0	0	2 Infos (2 new)
Place and Route Report	Current	Pt 27. maj 16:27:24 2022	0	0	1 Info (1 new)
Power Report					
Post-PAR Static Timing Report	Current	Pt 27. maj 16:27:26 2022	0	0	6 Infos (6 new)
Bitgen Report	Current	Pt 27. maj 16:28:16 2022	0	0	1 Info (1 new)

Secondary Reports				
Report Name	Status	Generated		
WebTalk Report	Current	Pt 27. maj 16:28:16 2022		
WebTalk Log File	Current	Pt 27. maj 16:28:18 2022		

Date Generated: 05/27/2022 - 16:28:18