bin_to_sevenSegment Project Status (05/27/2022 - 16:52:57)			
Project File:	bin_to_sevenSeg.xise	**Parser Errors:**	No Errors
Module Name:	bin_to_sevenSegment	**Implementation State:**	Programming File Generated
Target Device:	xc3s200-4vq100	• **Errors:**	No Errors
Product Version:	ISE 13.4	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	7	3,840	1%	
Number of occupied Slices	4	1,920	1%	
Number of Slices containing only related logic	4	4	100%	
Number of Slices containing unrelated logic	0	4	0%	
Total Number of 4 input LUTs	7	3,840	1%	
Number of bonded IOBs	12	63	19%	
Average Fanout of Non-Clock Nets	3.18			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:				

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Pt 27. maj 16:50:09 2022	0	0	0

Translation Report	Current	Pt 27. maj 16:52:27 2022	0	0	0
Map Report	Current	Pt 27. maj 16:52:30 2022	0	0	2 Infos (2 new)
Place and Route Report	Current	Pt 27. maj 16:52:34 2022	0	0	1 Info (1 new)
Power Report					
Post-PAR Static Timing Report	Current	Pt 27. maj 16:52:36 2022	0	0	6 Infos (6 new)
Bitgen Report	Current	Pt 27. maj 16:52:55 2022	0	0	1 Info (1 new)

Secondary Reports		**[-]**
Report Name	**Status**	**Generated**
WebTalk Report	Current	Pt 27. maj 16:52:55 2022
WebTalk Log File	Current	Pt 27. maj 16:52:57 2022

Date Generated: 05/27/2022 - 16:52:57