Project Proposal – Integrated Circuit DC-DC Converter

WPI ECE524 Spring Semester 25

Joshua Andrade and Daniel Raymond

May 7, 2025

# Design Concept

## Project Outline

DC-DC converters are a necessary part of analog, digital, and mixed signal circuits. The ripple voltage introduced by switch-mode converters is problematic for sensitive circuits, however the efficiency compared to linear converters is important for low-power-system-on-chip applications. This project will explore the design of a switch-mode DC-DC converter and its effects on mixed-signal circuits.

## Specifications

A Buck Converter topology will provide the correct ranges of output voltages for modern CMOS process nodes, while enabling a battery or USB power source. A good example of such a design comes from the Raspberry Pi RP2350 [1] that implements a combined switch-mode and linear voltage regulator. Our voltage regulator will inherit these parameters as a target to meet. The remaining design limitations are assigned from the course.

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Min. | Nom. | Max. |
| Vin (v) | 2.7 |  | 5.5 |
| Vout (v) | 0.55 | 1.1 | 3.3 |
| Iout,linear (mA) |  |  | 1 |
| Iout,buck (mA) |  |  | 200 |
| Cout (uF) |  |  | 30 |
| L (uH) |  |  | 10 |
| MOSFET width (um) | 0.18 |  |  |

# Project Scope

The design for this project included a transistor-level schematic and simulation for the core systems of the regulator, including the buck power stage and feedback amplifier. The non-critical elements, such as the voltage reference and PWM generator were designed with Spice/Verilog-A descriptive models. Effects on other circuits was simulated by characterizing the output waveform of the regulator in the time and frequency domain.

# Implementation

## Regulator Core

The regulator core consisted of a high-current push-pull pair of MOSFETs, with a PMOS ‘pass’ transistor and a NMOS 'freewheeling' transistor. Together, this pair controlled the current through the external inductor in continuous conduction buck switching. [2]

## Voltage Reference

The voltage reference requires no output current, but must provide the target voltage for the output regulation. The reference was implemented as a DC voltage source, but could be derived from a BGR.

## Difference Amplifier

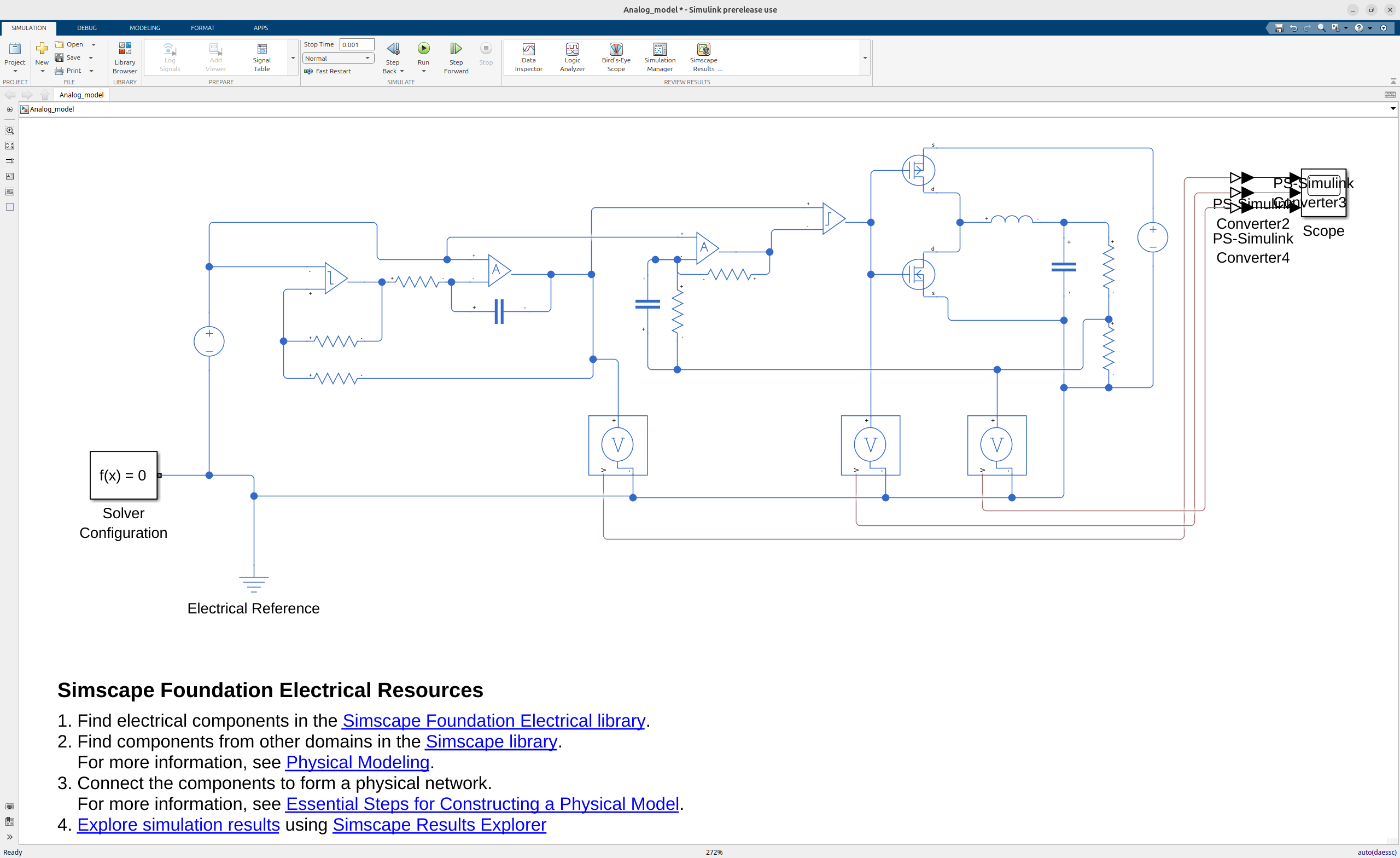
The difference amplifier provided the closed-loop feedback and compensation needed for stable operation . The input took the difference between the output voltage and reference voltage and generated an error to adjust the duty cycle of the buck converter. Bandwidth and the compensation needed for stability were important design considerations.

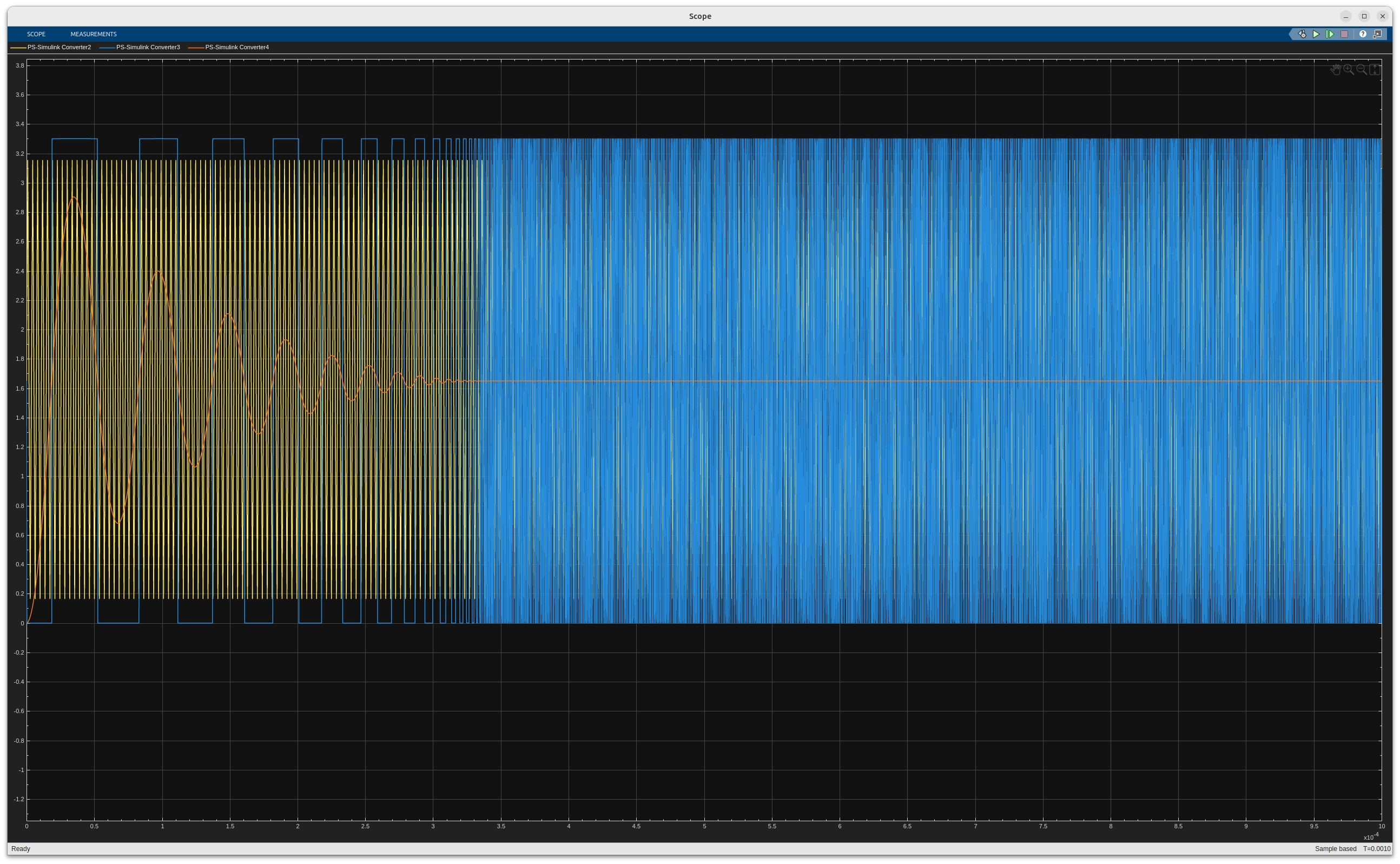
## PWM Generator

The PWM signals could be generated from a triangle waveform compared with an analog error value from the difference amplifier. However, for the speed of simulation, an equivalent Verilog-A model was used to map in input voltage to a PWM duty percentage.

## High-level Diagram

A Simulink model was used to demonstrate the theory of operation before implementation in analog models.

Figure 1: Simulink Model of buck converter

Figure 2: Simulation of demonstrating preliminary functionality

# Methodology

Most of the work for this project was completed through MATLAB and Cadence Virtuoso. Matlab Simulink was used to model the circuit as a whole and find the necessary specifications for the sub-circuit components. The analog/mixed-signal circuits of the DC-DC converter were tested with the use Verilog-A models along with the simulation of TSMC 180nm process, both in Cadence Virtuoso.

# Implementation

## Error Amplifier

The error amplifier was the block that compares the output of the buck converter to a reference voltage, so that the reference voltage was the desired output voltage. The error voltage was fed into the PWM generator to modulate duty cycle of the switching, that way the feedback loop was closed and the output voltage was maintained close to the desired output voltage.

An important design requirement of the error amplifier was a high bandwidth, to ensure that it could regulate under fast load transients. Even though output swing and open loop gain were not critical design parameters for the error amplifier, they were still considered when designing the error amplifier.

Below is a schematic of the final error amplifier design including an ideal bias circuit and necessary test sources.

A computer screen shot of a computer scheme

AI-generated content may be incorrect.

Figure 3: Error amplifier schematic

It was a rather simple design, with an NMOS differential pair and an active current mirror load. The output of the differential stage was connected to a common-drain stage for buffering. The transistors on the bottom serve as a current source for the stage, and the bias voltage for those current sources were provided by the drain of a diode-connected NMOS with a 50uA current going through it.

The simple design resulted in fewer components, thus it allowed for a higher bandwidth. It also provided sufficient gain and output swing to drive the PWM.generator. Figures 4 and 5 showcase these specifications which are recorded in Table 1, notably it’s gain-bandwidth product of 36.65GHz. The output swing was nearly rail to rail, however the input should be maintained above 0.7 V to prevent the differential input pair from entering cut-off.

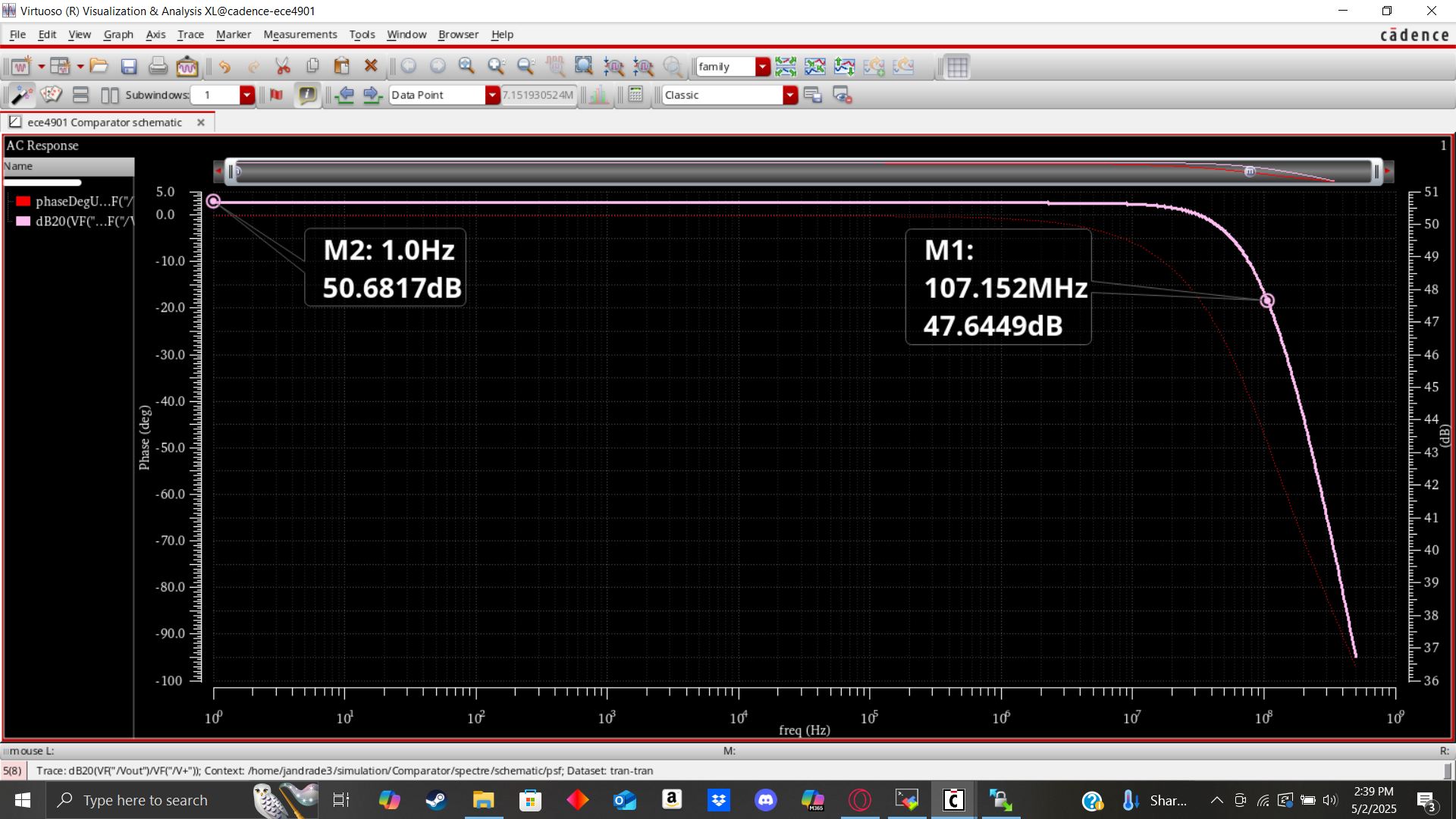


Figure 4: AC analysis performed showcasing open loop gain, and -3dB frequency



Figure 5: DC analysis performed mapping output swing to input voltage

|  |  |
| --- | --- |
| Specification | Value |
| Open Loop Gain | 50.68dB |
| Bandwidth | 107MHz |
| Output Swing | 425nV -> 3.26 V |
| GBP | 36.65GHz |

Table 1: Feedback amplifier specifications

## Buck Converter

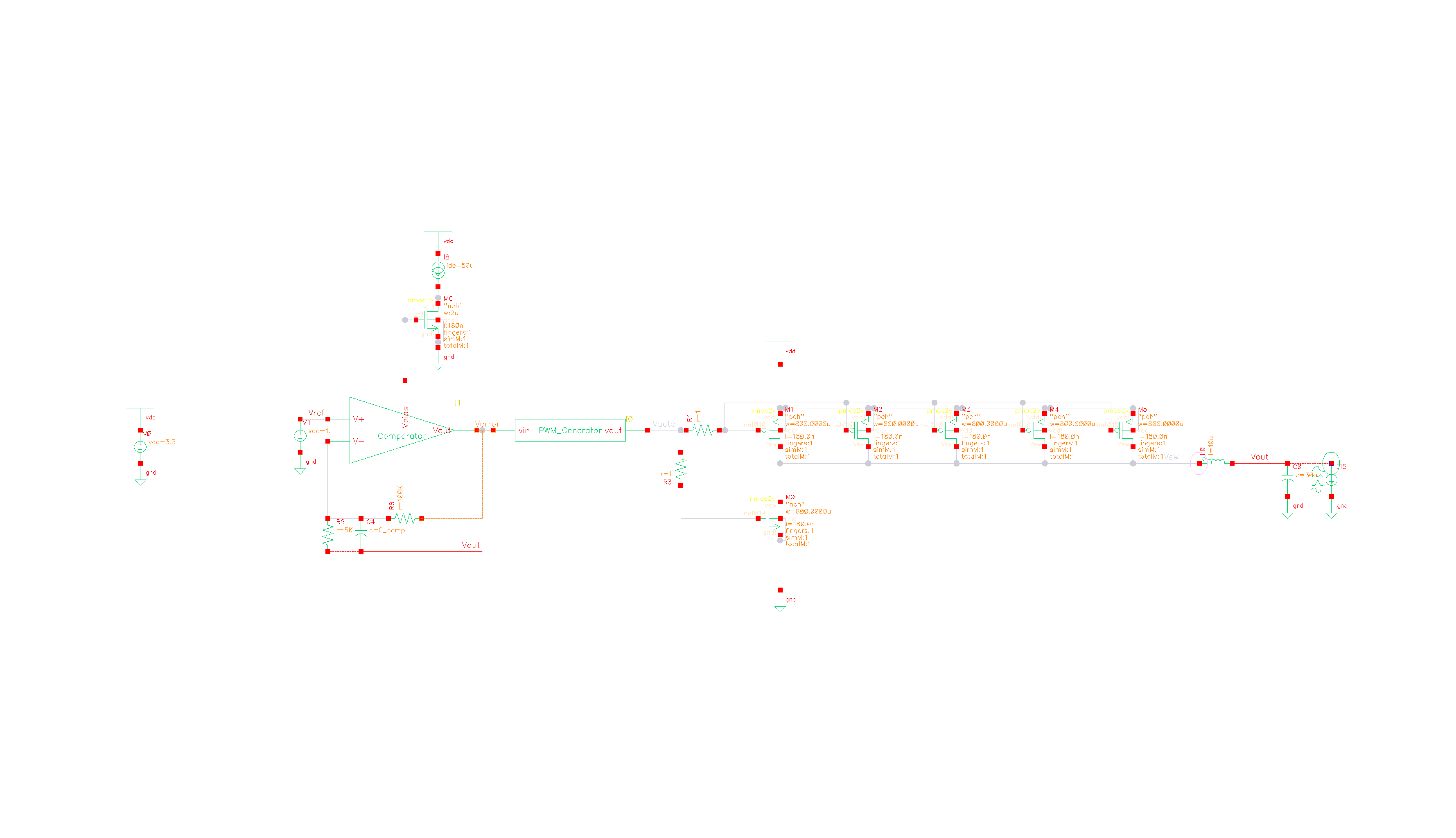


Figure 6: Buck converter schematic

The power stage of the buck converter was designed using the TSMC18 standard and the specifications set out initially. A switching frequency of 2MHz was decided on to balance small output ripple with switching losses and parasitics. The maximum filter component sizing was preferred for this switching frequency to keep current ripple at 18.5% and voltage ripple at just 76uV. The peak conducted current through either FET was 218.5mA when the output power was 220mW. With the goal of high efficiency in mind, conductive losses of less than 5% were decided on, necessitating a FET triode channel resistance of 0.23 Ohms. With a minimum length of 180nm, the width for the NMOS was 800um and the width for the PMOS was 4000um, necessitating the use of 5 parallel 800um PMOS FETs.

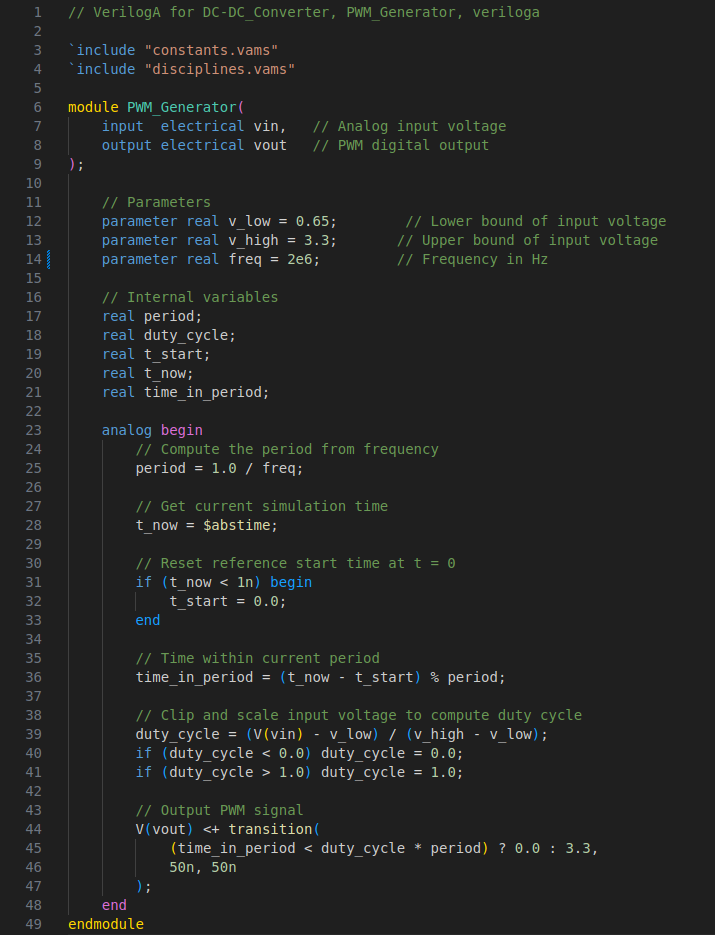
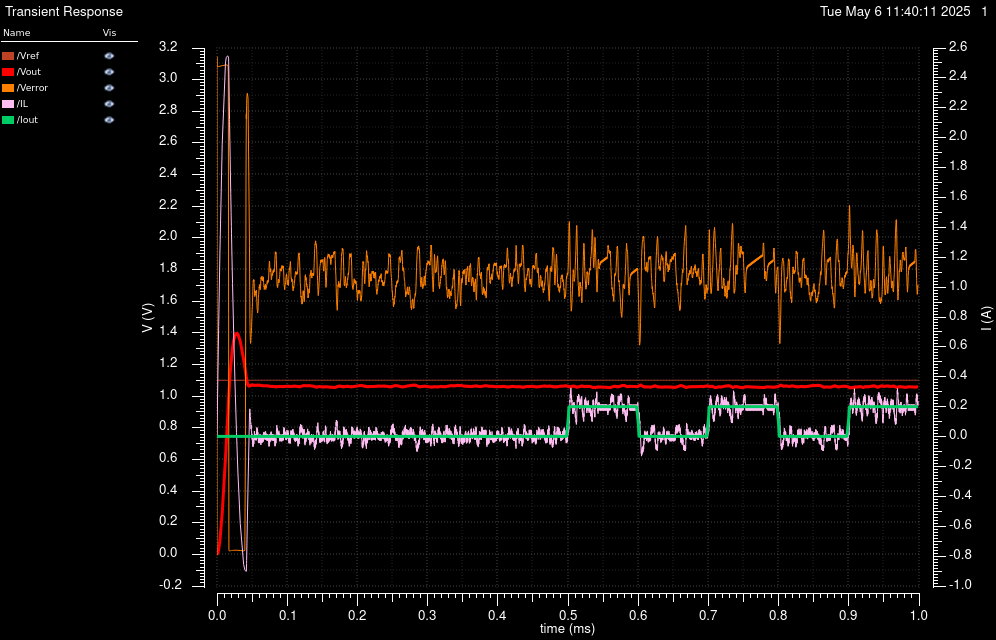


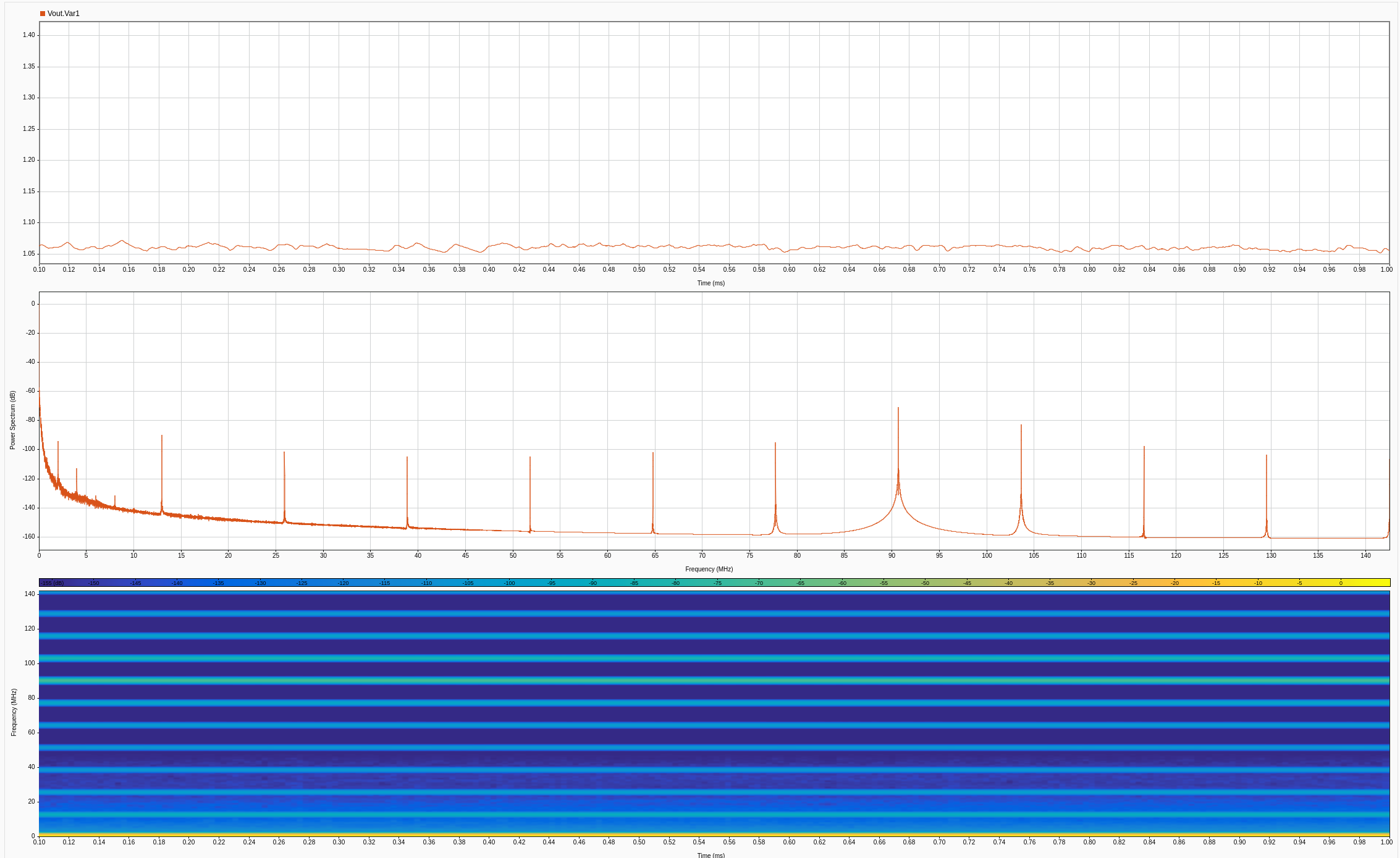
Figure 7: PWM generator Verilog-A implementation

The PWM generator modeled in Simulink was too complex to simulate in combination with the buck converter core, so a simpler implementation used Verilog-A. This descriptive model similarly mapped an input voltage taken from the feedback amplifier and converted it into a PWM signal with known frequency and variable duty cycle. The duty cycle mapped linearly with the input voltage to act transparently in the feedback loop.

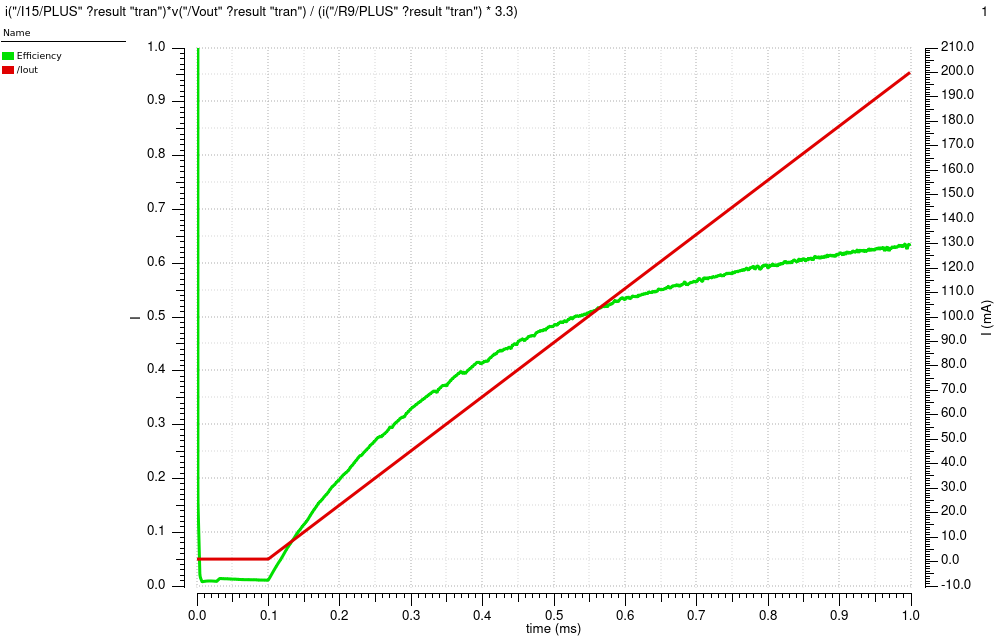
# Results

Figure 8: Buck converter startup and load step operation

The output regulation of the buck converter suffered slight overshoot on startup, but maintained very stable operation. The output voltage overshot the target voltage on startup but this could easily be a resolved with a soft start circuit that ramped up the target voltage. When regulating around the target voltage, the error amplifier output remained between the bounds of it's output swing and the PWM generator was able to modulate the inductor current on a cycle-by-cycle basis. This response allowed for the output voltage to stay very stable, even during load steps from 1 mA to 200 mA.

Figure 9: Output voltage frequency spectrum

The output noise of the buck converter was low, as shown in figure 9 while sweeping the output current from 0-200 mA. The switching circuit experiences ringing at harmonics of the 2 MHz PWM frequency, with the highest amplitude around 90 MHz. The noise was low in amplitude with a peak of -60dB, and a low total harmonic energy.

Figure 10: Output current and regulator efficiency

The benefit to the buck converter was it’s efficiency of over 60%. This value was much greater than the theoretical limit for a linear supply of just 33%, which demonstrated that the regulator was working as intended. At low output currents, the efficiency dropped because of the bias losses in the feedback amplifier and switching losses that remained constant. This efficiency curve showed that it would be more efficient than a linear regulator for output currents greater than 50 mA.

# Conclusion

The design for an integrated circuit DC-DC converter was a complex project that incorporated multiple discrete sub-circuits and descriptive models. These functional blocks were designed and evaluated separately to ensure proper functionality before integration in the final schematic. The simple theory of operation of mapping feedback error transparently through a buck converter resulted in stable voltage regulation that tolerated output current transients. This regulator exceeded the efficiency of a linear regulator for output currents greater than 50 mA, and provided a low-noise output with less than -60 dB of frequency content.

## Improvements

Further improvements that add complexity might include a more robust gate drive circuit that would eliminate cross-conduction through the FET switches, a variable switching frequency to prevent high noise in narrow frequency windows, and a feedback amplifier that allows for individual tuning of the different types of compensation (such as a PID controller). These features would have slowed down the design process, but could increase the efficiency and decrease the noise.

# References

1. [RP2350 Datasheet: A microcontroller by Raspberry Pi. Section 6.3](https://datasheets.raspberrypi.com/rp2350/rp2350-datasheet.pdf" \l "%5B%7B%22num%22%3A449%2C%22gen%22%3A0%7D%2C%7B%22name%22%3A%22XYZ%22%7D%2C115%2C676.832%2Cnull%5D)
2. Chen, K.-H. (2016). *Power management techniques for Integrated Circuit Design*. Wiley.
3. Razavi, B. (2017). *Design of Analog CMOS Integrated Circuits.* McGraw Hill Education.