VIN   VCC   VS   VD   VBUS

```
 2                                                                                              TP17
───○         Input Protection         DC-DC            Output Switch                           ○  TestPoint
 1                                                                                          2
───○                                                                                      ──  Conn_01x02
XT60_M           VIN  VOUT_NO_LIMIT       VIN    VOUT       VIN    VOUT                     1   J2
J3                    VSMOND─ IS_MON                                                           ──
                 VCC  PGOODD─ VS_GOOD                   VDMON─ VD_MON   OUTPUT_DIS─LOAD_DISCHRG    TP18
GND                   ENABLE─ INPUT_EN                  VSMON─ VS_MON   OUTPUT_EN ─LOAD_TG      ○  TestPoint
                      FAULTD─ IS_GOOD                   IL_MON─ IL_MON                      GND
```

File: input.kicad_sch

```
                      PHASE_2_P─ P2_H
                      PHASE_2_N─ P2_L                   VDMON─ VD_MON
                      PHASE_1_P─ P1_H                   VSMON─ VS_MON
                      PHASE_1_N─ P1_L                   IL_MON─ IL_MON
                                                        ID_MON─ ID_MON
```

File: dc-dc.kicad_sch

         VCC   +5V   +5V   +3V3

```
  5v Regulator                 3v3 Regulator
      VIN  VOUTD                   VIN  VOUTD
           PGOODD─ 5V_GOOD              PGOODD─ 3V3_GOOD
```

File: 5V_regulator.kicad_sch   File: 3v3_regulator.kicad_sch

```
                                              +5V       1
                                              +3V3      2
                                              GND       3
                                              PHASE_1_P 4
                                              PHASE_1_N 5
                                              GND       6
                                              PHASE_2_P 7
                                              PHASE_2_N 8
                                              GND       9
                                              VS_MON    10    J1
                                              VD_MON    11    Conn_01x22
                                              IS_MON    12
                                              GND       13
                                              IL_MON    14
                                              ID_MON    15
                                              VS_GOOD   16
                                              IS_GOOD   17
                                              5V_GOOD   18
                                              3V3_GOOD  19
                                              INPUT_EN  20
                                              OUTPUT_EN 21
                                              OUTPUT_DIS 22
```

VIN

R14
100k

VSMON

D2
3.425

R16
5820

GND

VIND

TP1
TestPoint

C1
10u

C2
10u

C12
10u

C13
10u

C14
82u

SW1

Q1
EPC2302
100V 101A 1.9mE

G1

TP3
TestPoint

L1
4.7u

R5
5m

SW2

Q2
EPC2302
100V 101A 1.9mE

G2

GND

TP2
TestPoint

VOUTa

G3

Q3
EPC2302
100V 101A 1.9mE

TP4
TestPoint

SW2

G4

Q4
EPC2302
100V 101A 1.9mE

GND

C15
82u

C16
10u

C17
10u

C18
10u

C19
10u

C49
10u

IDP

IDN

R6
12m

VOUT

VOUT

R17
100k

VDMON

D3
3.425

R18
5820

GND

TP5
TestPoint

C4
100n

R1
0

U1

BOOT

HI

LI

VCC

NC

GND

UGH

UGL

PHASE

LGL

LGH

D3

B4

A4

A3

C4

A2

D2

D1

D4

A1

B1

R2
2.2

R3
1

R4
2.2

R7
1

TP7
TestPoint

G1

SW1

TP9
TestPoint

G2

+5V

C3
1u

GND

TP6
TestPoint

C6
100n

R8
0

U3

BOOT

HI

LI

VCC

NC

GND

UGH

UGL

PHASE

LGL

LGH

D3

B4

A4

A3

C4

A2

D2

D1

D4

A1

B1

R9
2.2

R10
1

R11
2.2

R12
1

TP8
TestPoint

G3

SW2

TP10
TestPoint

G4

+5V

C5
1u

GND

P1_HD

P1_LD

P2_HD

P2_LD

LSP

LSN

Vin+

Vin−

U7
INA281A2

+3V3

V+

GND

OUT

IL_MON

C20
1uF

GND

GND

IDP

IDN

Vin+

Vin−

U8
INA281A2

+3V3

V+

GND

OUT

ID_MON

C21
1uF

GND

GND

$$\max(I) = (V\_ISET / 40) / R25$$
$$25 = (2 / 40) / 0.002$$

NT5
NetTie_2

VOUT_NO_LIM

Q7
SiR5607DP

R25
2m

Q8
SiR5607DP

VIN

VOUT

TP15
TestPoint

TP16
TestPoint

VCAP

VIN

TP11
TestPoint

R33
68k

TP12
TestPoint

R34
68k

TP13
TestPoint

R28
100k

UV

OV

R35
1.2k

TP14
TestPoint

R29
4.3k

$$V\_OV = (R34 + R35) / R35 * 0.99$$
$$57 = (68k + 1.2k) / (1.2k) * 0.99$$

VCC   SENSE+   SENSE−   G_BP   GATE

15 SENSE+   14 SENSE−   13 G_BP

UV   OV   RPFG   VCAP   ENABLE   ISET

UV 3
OV 4
G_RP 16
VCAP 1
ENABLED 5
ISET 2

FLB
FB_PG
TIMER
TIMER_OFF
PWRGD
FAULT

11 FLB
10 FB_PG
8 TIMER
9 TIMER_OFF
12 PGOOD
6 FAULT

R32
29k

GND

R24
0

C44
1uF

GND   GND

C46
50nF

C45
20nF

GND

ENABLE

U5
ADM1270ACPZ

GND   EP

7   17

GND

R38
100k

GND

+3V3

R30
100k

R31
100k
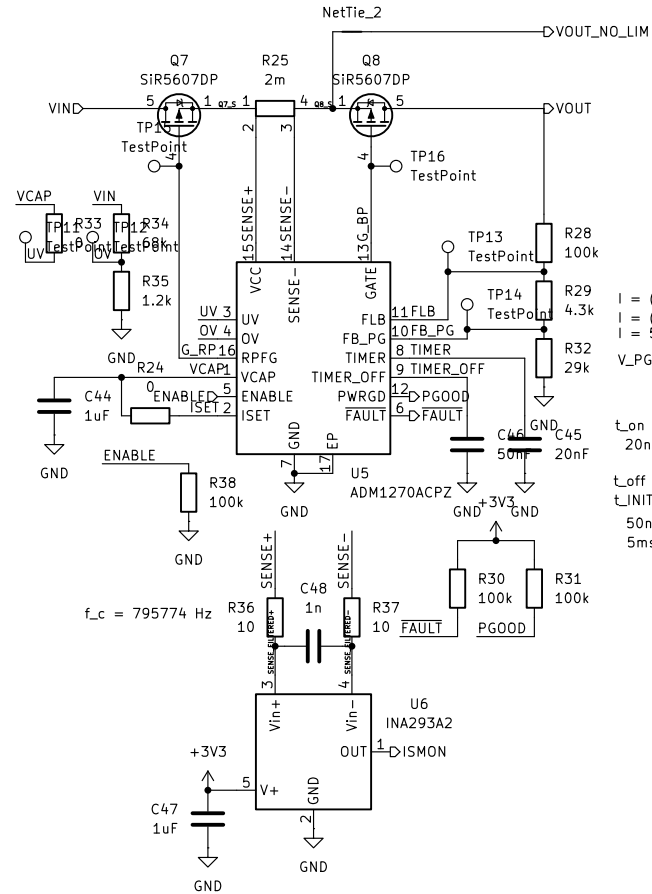
$$I = (VOUT * (R29 + R32) / (R28 + R29 + R32)) / 40 / R25 \ \{I < \max(I)\}$$
$$I = (VOUT * 3.102) \ \{VOUT < 8.06\}$$
$$I = 5 \ \{VOUT < 0.806\}$$

$$V\_PG = (R28 + R29 + R32) / R32$$
$$4.60 = 133.3/29$$

$$t\_on = 2V * (C\_TIMER / 20uA)$$
$$20nF = (2ms * 20uA) / 2V$$

$$t\_off = 2 * (C\_TIMER\_OFF / 1uA)$$
$$t\_INITIAL = 2V * (C\_TIMER\_OFF / 20uA)$$
$$50nF = (100ms * 1uA) / 2V$$
$$5ms = 2V * (50nF / 20uA)$$

FAULT   PGOOD

$$f\_c = 795774 \ Hz$$

R36
10

C48
1n

R37
10

SENSE+   SENSE−

Vin+   Vin−

U6
INA293A2

+3V3

OUT
ISMON

V+

C47
1uF

GND

GND

GND

Q5
SiR5607DP

Q6
SiR5607DP

VIND 5 1 COM_S1 5 VOUT

R1
51k

LOAD_TGD

+3V3

R23
100k

LOAD_DISCHRGD 2 6 Q9A

1

GND