PRELIMINARY

MOSTEK®

16,384 x 1-BIT DYNAMIC RAM

MK4516(N/E)-10/12/15

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Active power 150mW maximum
  Standby power 17mW maximum
- 100ns access time, 220ns cycle time (MK4516-10)
  120ns access time, 250ns cycle time (MK4516-12)
  150ns access time, 310ns cycle time (MK4516-15)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and are protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MK4164 (64K RAM)
- 128 refresh cycles (2msec)
- Offers two variations of hidden refresh
- Indefinite D_{OUT} hold using $\overline{CAS}$ control

DYNAMIC RAMS

DESCRIPTION

The MK4516 is a single +5V power supply version of the industry standard MK4116, 16,384 x 1 bit dynamic RAM.

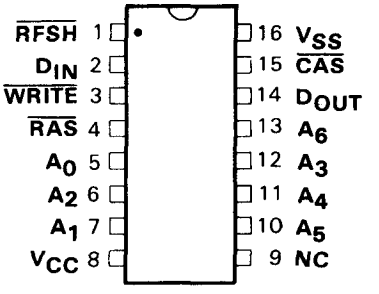
The high performance features of the MK4516 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatability, and +5V only operation.

The MK4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH. The output of the MK4516 can be held valid indefinitely by holding $\overline{CAS}$ active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previous cycle.

The MK4516 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM. The MK4516 is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance. The compatability with the MK4164 will also permit a common board design to service both the MK4516 and MK4164 (64K RAM) designs. The MK4516 will therefore permit a smoother transition to the 64K RAM as the industry standard MK4027 did for the MK4116.

The user, requiring only a small memory size, need no longer pay the three power supply penalty for achieving the economics of using dynamic RAM over static RAM when using this new generation device.

PIN OUT



PIN FUNCTIONS

A_0-A_6	Address Inputs	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Col. Address Strobe	$\overline{WRITE}$	Read/Write Input
D_{IN}	Data In	$\overline{RFSH}$	Refresh
D_{OUT}	Data Out	V_{CC}	Power (+5V)
		V_{SS}	GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	$V_{CC}+1$	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) $V_{CC} = 5.0V \pm 10\%$

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT t_{RC} = 220ns t_{RC} = 250ns t_{RC} = 310ns		 27 25 23	 mA mA	 2 2 2
I_{CC2}	STANDBY CURRENT Power supply standby current (RAS = V_{IH}, D_{OUT} = High Impedance)		3	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0V \leq V_{IN} \leq +5.5V$, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)	-10	10	μA	
 V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2mA	 2.4	 0.4	 V V	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RFSH}$ cycles before proper device operation is achieved. If refresh counter is to be effective a minimum of 64 active $\overline{RFSH}$ initialization cycles is required. The internal refresh counter must be activated a minimum of 128 times every 2ms if the $\overline{RFSH}$ refresh function is used.
4. AC characteristics assume t_T = 5ns
5. V_{IH} min. and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Load = 2TTL loads and 50pF.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. $\overline{RFSH} = V_{IH}$. $\overline{CAS} = V_{IH}$ or V_{IL}, but is allowed to make an active to inactive transition during the $\overline{RAS}$ active time of $\overline{RAS}$-only refresh cycle. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS} = V_{IH}$, data output is high impedance. If $\overline{CAS} = V_{IL}$, the data output will contain data from the last valid read cycle.
11. $\overline{RAS} = V_{IH}$. $\overline{CAS} = V_{IH}$ or V_{IL}, but is allowed to make an active to inactive transition during the Pin 1 refresh cycle. ADDRESSES and $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS} = V_{IH}$, data output is high impedance. If $\overline{CAS} = V_{IL}$, the data output will contain data from the last valid read cycle.

NOTES (Continued)

12. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write.
16. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. If the $\overline{RFSH}$ function is not used, pin 1 may be left open (no connect).
18. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
19. If t_{CRP} is not satisfied then the following types of cycles will occur. a) A hidden REFRESH cycle can take place with the data valid from last read cycle as long as $\overline{CAS}$ does not make an active to inactive transition. b) A $\overline{RAS}$ only cycle can also occur if $\overline{CAS}$ makes an active to inactive transition beyond t_{CRP} min. The data out buffer will go to a high impedance mode after CAS makes an inactive transition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [3,4,5,10,11,17,18]

($0°C \leq T_A \leq 70°C$), $V_{CC} = 5.0V \pm 10\%$

		MK4516-10		MK4516-12		MK4516-15			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	220		250		310		ns	6,7
t_{RMW}	Read modify write cycle time	260		295		365		ns	6,7
t_{PC}	Page mode cycle time	120		140		165		ns	6,7
t_{RAC}	Access time from $\overline{RAS}$		100		120		150	ns	7,8
t_{CAC}	Access time from $\overline{CAS}$		50		60		75	ns	7,9, 10,11
t_{OFF}	Output buffer turn-off delay	0	35	0	40		40	ns	12
t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5
t_{RP}	$\overline{RAS}$ precharge time	110		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ hold time	50		60		75		ns	
t_{CSH}	$\overline{CAS}$ hold time	100		120		150		ns	
t_{CAS}	$\overline{CAS}$ pulse width	50	∞	60	∞	75	∞	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	50	20	60	20	75	ns	13
t_{RRH}	Read command hold time referenced to $\overline{RAS}$	20		25		35		ns	14
t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RAH}	Row Address hold time	15		15		20		ns	
t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CAH}	Column Address hold time	15		20		25		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	65		80		100		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	14
t_{WCH}	Write command hold time	35		40		50		ns	

SYM	PARAMETER	MK4516-10		MK4516-12		MK4516-15		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	85		100		125		ns	
t_{WP}	Write command pulse width	30		35		45		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	35		40		50		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	35		40		50		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	15
t_{DH}	Data-in hold time	35		40		45		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	85		100		120		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		70		80		ns	
t_{REF}	Refresh period		2		2		2	ms	
t_{WCS}	WRITE command set-up time	0		0		0		ns	16
t_{CWD}	$\overline{CAS}$ to WRITE delay	50		60		75		ns	16
t_{RWD}	$\overline{RAS}$ to WRITE delay	100		120		150		ns	16
t_{FSR}	$\overline{RFSH}$ set-up time referenced to RAS	110		120		150		ns	
t_{RFD}	$\overline{RAS}$ to $\overline{RFSH}$ delay	110		120		150		ns	
t_{FC}	$\overline{RFSH}$ cycle time	220		250		310		ns	
t_{FP}	$\overline{RFSH}$ active time	100		120		150		ns	
t_{FHR}	$\overline{RFSH}$ hold time referenced to RAS	0		0		0		ns	
t_{FI}	$\overline{RFSH}$ inactive time	110		120		150		ns	
t_{FRD}	$\overline{RFSH}$ to $\overline{RAS}$ delay (Test mode write only)	50		50		50		ns	
t_{CPN}	$\overline{CAS}$ precharge time	25		30		40		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	-20		-20		-20		ns	19

OPERATION

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK4516 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the 7 row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the

worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4516 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state. Note that $\overline{CAS}$ can be left active (low) indefinitely. This permits either $\overline{RAS}$-only or $\overline{RFSH}$ refresh cycles to occur without invalidating D_{OUT}.

PAGE MODE OPERATION

The Page Mode feature of the MK4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4516, this results in as much as a 50% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4516 is limited to the 128 column locations determined by all combinations of the 7 column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycle are permitted within the page mode operation.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing, this function is easily accomplished by using either $\overline{RAS}$-only or $\overline{RFSH}$ type refreshing.

$\overline{RAS}$-ONLY REFRESH

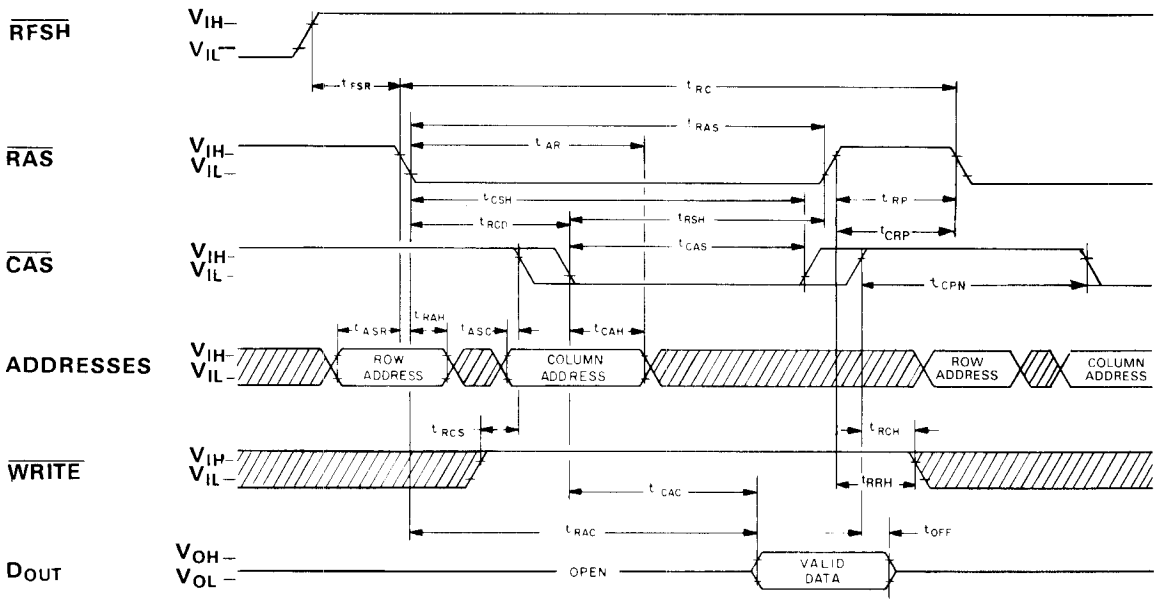
The $\overline{RAS}$-only refresh cycle supported by the MK4516 requires that a 7 bit refresh address be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time that $\overline{RAS}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{RAS}$ signal. This is useful for single step operation. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state.

PIN 1 REFRESH

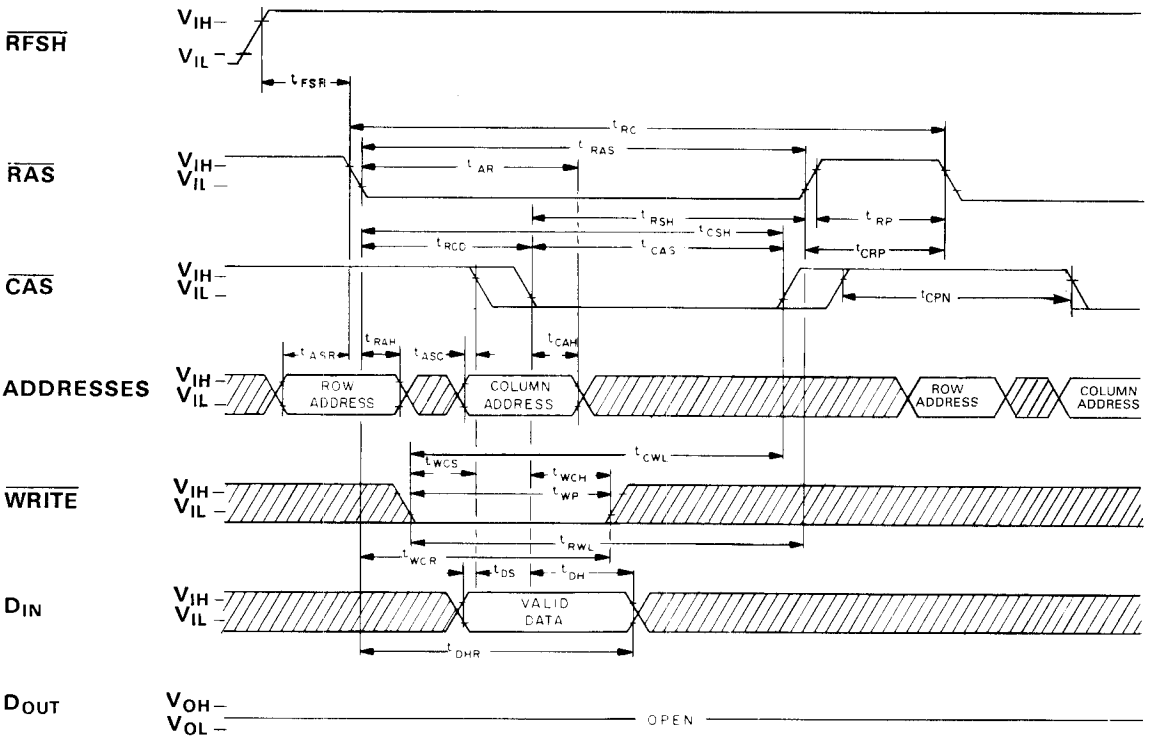
$\overline{RFSH}$ type refreshing available on the MK4516 offers an attractive alternate refresh method. When the signal on pin 1, $\overline{RFSH}$, is brought low during $\overline{RAS}$ inactive time ($\overline{RAS}$ high), an on-chip refresh counter is enabled and an internal refresh operation takes place. When $\overline{RFSH}$ is brought high (inactive) the internal refresh address counter is automatically incremented in preparation for the next refresh cycle. Data can be held valid from a previous cycle using $\overline{CAS}$ control during a $\overline{RFSH}$ type refresh cycle.

The internal refresh counter is a dynamic counter and requires refreshing. The 128 $\overline{RFSH}$ cycles every 2 milliseconds required to refresh the memory cells is adequate for this purpose. Only $\overline{RFSH}$ activated cycles affect the internal counter.

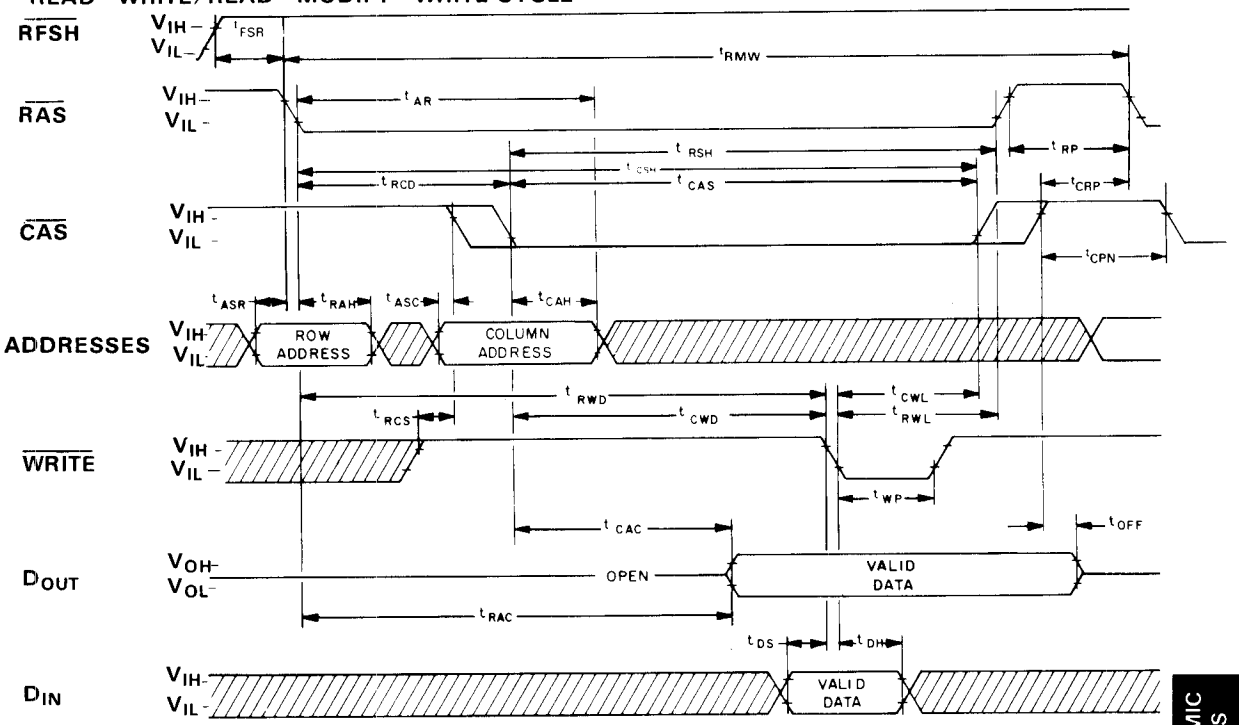
READ CYCLE



WRITE CYCLE (EARLY WRITE)



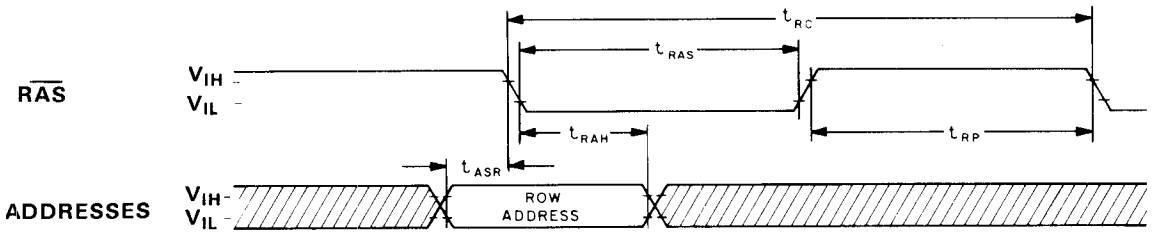
READ—WRITE/READ—MODIFY—WRITE CYCLE



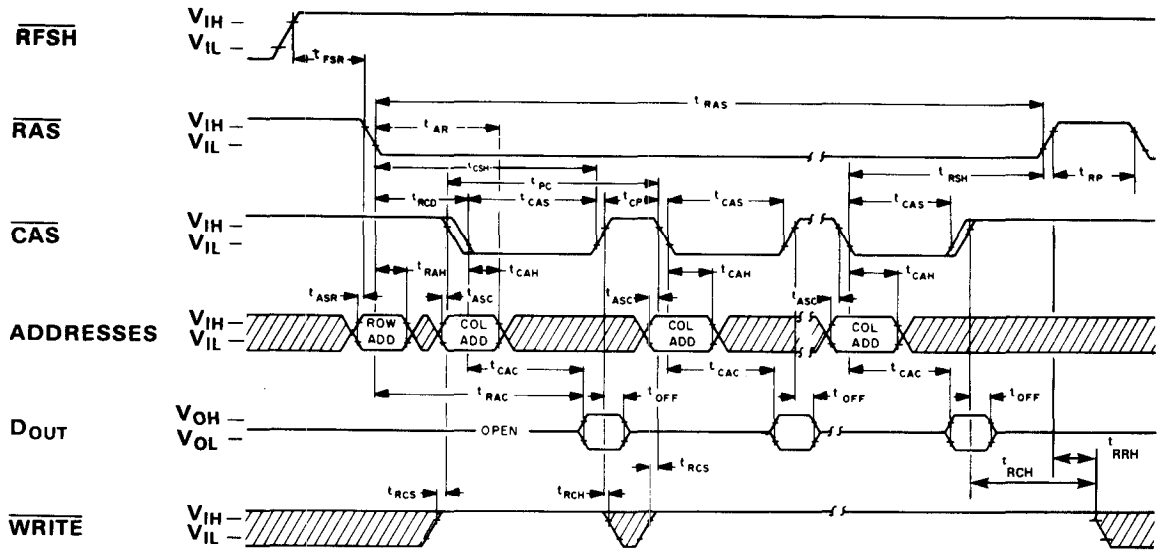
"RAS—ONLY" REFRESH CYCLE (SEE NOTE 10)

DYNAMIC RAMS

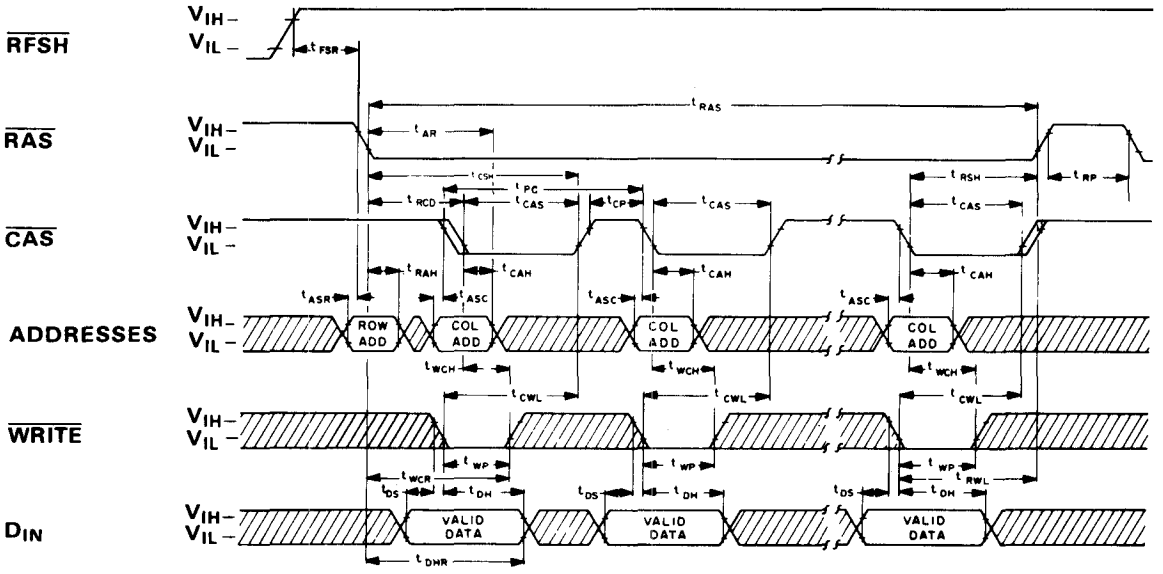
"$\overline{RAS}$—ONLY" REFRESH CYCLE



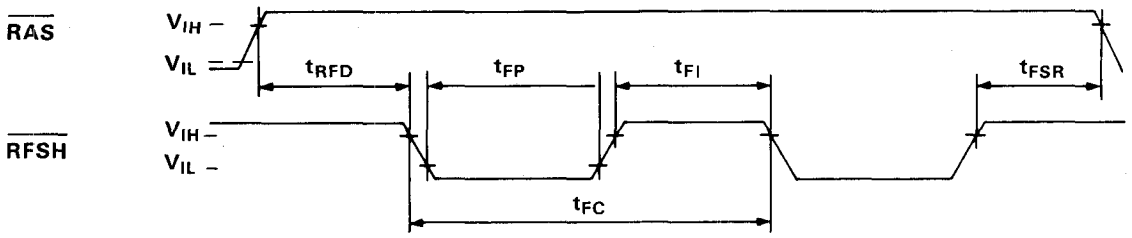
PAGE MODE READ CYCLE



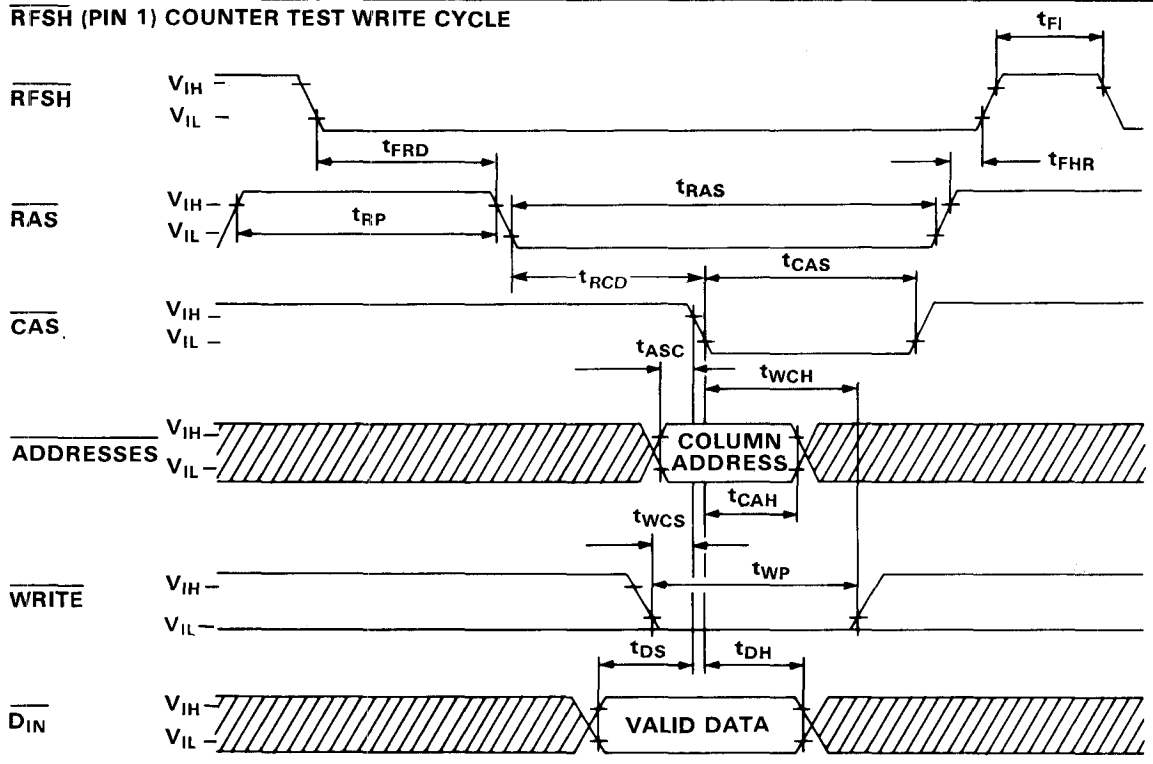
PAGE MODE WRITE CYCLE



$\overline{RFSH}$ (PIN 1) REFRESH CYCLE (SEE NOTE 11)



$\overline{RFSH}$ (PIN 1) COUNTER TEST WRITE CYCLE



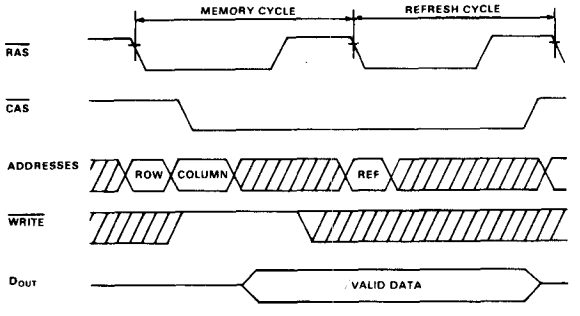
The use of $\overline{RFSH}$ mode for refreshing eliminates the need to generate refresh addresses externally.

Furthermore, when using $\overline{RFSH}$ refreshing, the address drivers, the $\overline{CAS}$ drivers, and $\overline{WRITE}$ drivers can be powered down during battery backup standby operation.

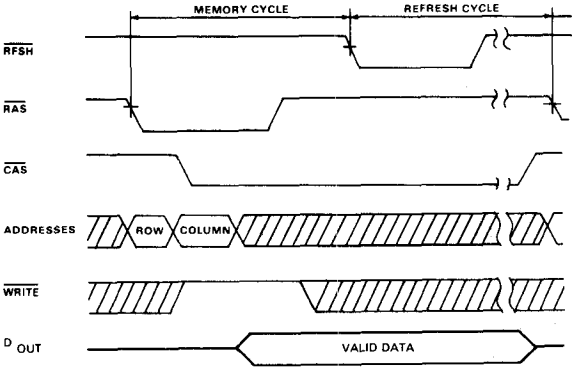
HIDDEN REFRESH

Either a $\overline{RAS}$-only or $\overline{RFSH}$ type refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figures below.)

HIDDEN $\overline{RAS}$—ONLY REFRESH CYCLE (SEE NOTE 10)



HIDDEN $\overline{RFSH}$ REFRESH CYCLE (SEE NOTE 11)



$\overline{RFSH}$ (PIN 1) TEST CYCLE

A special timing sequence using the Pin 1 counter test cycle provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

When $\overline{RFSH}$ is activated prior to and remains valid through a normal write cycle, the D_{IN} is written into the memory location defined by the current contents of the on-chip refresh counter and the column address present at the external address pins during the high-to-low transition of $\overline{CAS}$. (See Pin 1 counter test write timing diagram.)

The following test procedure may be used to verify the functionality of the internal refresh counter. There are a multitude of patterns and sequences which may also be used to verify the $\overline{RFSH}$ feature. This test should be performed after it has been confirmed that the device can uniquely address all 16,384 storage locations.

SUGGESTED $\overline{RFSH}$ COUNTER TEST PROCEDURE

1. Initialize the on-chip refresh counter. 64 cycles are adequate for this purpose.
2. Write a test pattern of zeroes into the memory at a single column address and all row addresses by using 128 $\overline{RFSH}$ (pin 1) refresh counter test write cycles.
3. Verify the data written into the RAM by using the column address used in step 2 and sequence through all row address combinations by using conventional read cycles.
4. Compliment the test pattern and repeat steps 2 and 3.