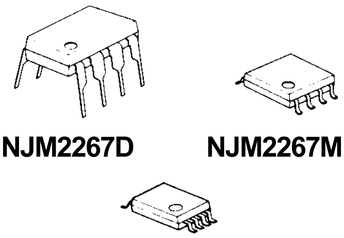
DUAL VIDEO 6dB AMPLIFIER WITH 75Ω DRIVER

■ GENERAL DESCRIPTION

NJM2267 is a dual video 6dB amplifier with 75Ω drivers for S-VHS VCRs, HI-BAND VCRs, etc..Each channel has clamp function that fixes DC level of video signal and 75Ω drivers to be connected to TV monitors directly. Further more it has sag corrective circuits that prevent the generation of sag with smaller capacitance than ever.

Its operating supply voltage is 4.85 to 9V and bandwidth is 7MHz.

■ PACKAGE OUTLINE



NJM2267D **NJM2267M**

NJM2267V

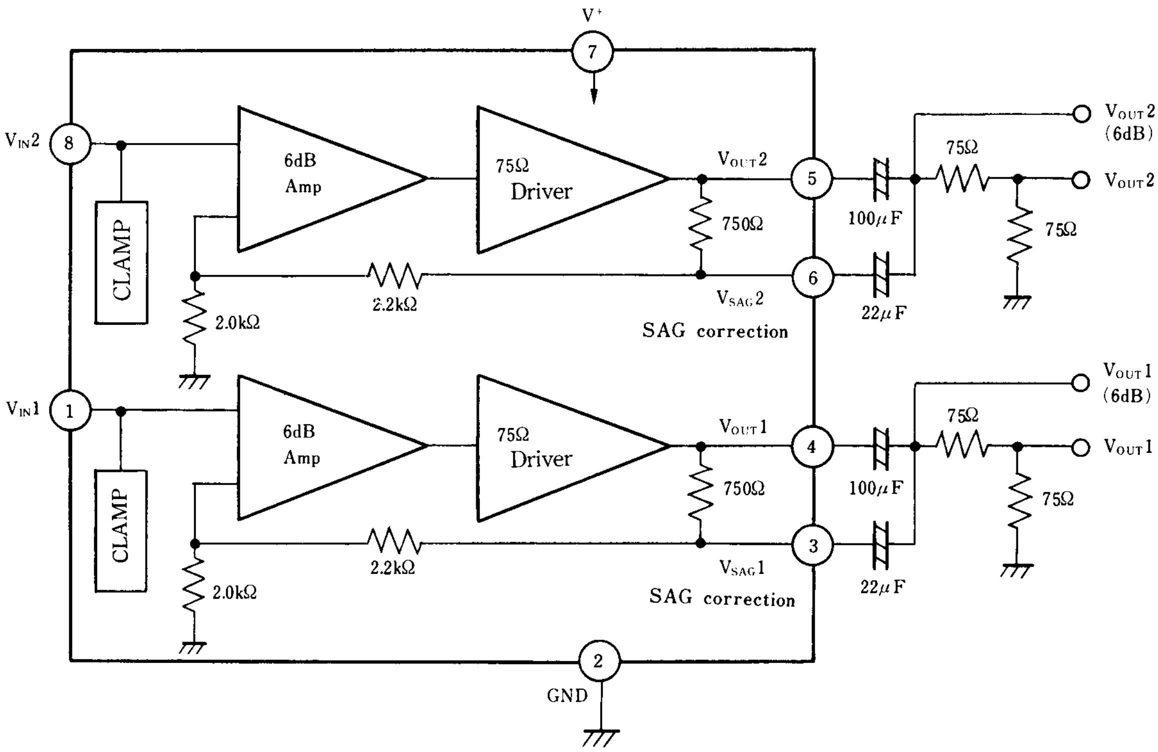
■ FEATURES

- Wide Operating Voltage (4.85V to 9.0V)
- Dual Channel
- Internal Clamp Function
- Internal Driver Circuit For 75Ω Load
- SAG Corrective Function
- Wide Frequency Range (7MHz)
- Low Operating Current 14.0mA (Dual)
- Package Outline DIP8, DMP8, SSOP8
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, TV, Video Disc Player.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SSOP8) 250	mW mW mW
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C

■ ELECTRICAL CHARACTERISTICS

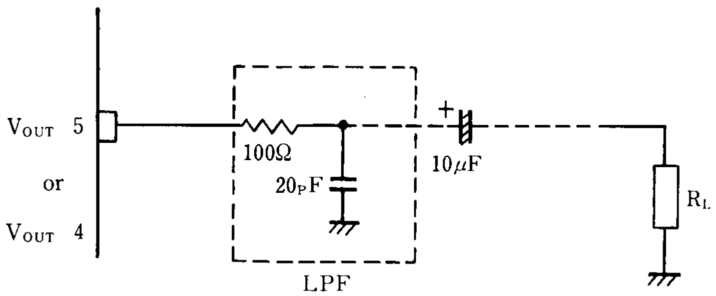
(V^+=5V, Ta=25±2°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No Signal	-	14.0	18.2	mA
Voltage Gain	G_V	V_{IN}=1MHz, $1V_{P-P}$Sinewave	5.7	6.2	6.7	dB
Frequency Characteristics	G_f	V_{IN}=$1V_{P-P}$, Sinewave, 7MHz / 1MHz	-	-	±1.0	dB
Differential Gain	DG	V_{IN}=$1V_{P-P}$, Staircase	-	1.0	3.0	%
Differential Phase	DP	V_{IN}=$1V_{P-P}$, Staircase	-	1.0	3.0	deg
Crosstalk	CT	V_{IN}=4.43MHz, $1V_{P-P}$, Sinewave	-	-70	-	dB
Gain Offset	G_{CH}	V_{IN}=1MHz, $1V_{P-P}$, G_{CH}=V_{OUT1}-V_{OUT2}	-	-	±0.5	dB
Input Clamp Voltage	V_{CL}		1.79	1.91	2.03	V
SAG Terminal Gain	G_{SAG}		35	45	-	dB

■ APPLICATION

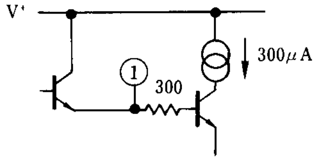
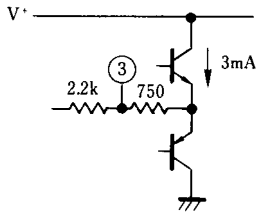
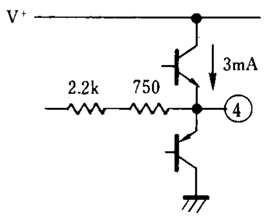
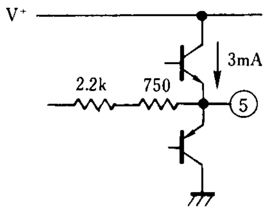
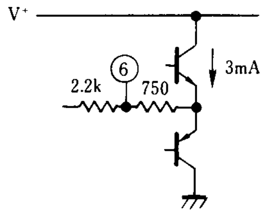
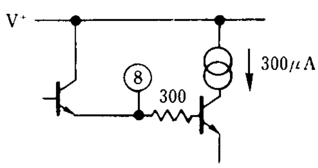
Oscillation Prevention

It is much effective to insert LPF (Cutoff Frequency 70MHz) under light loading conditions (RL » 1kΩ)

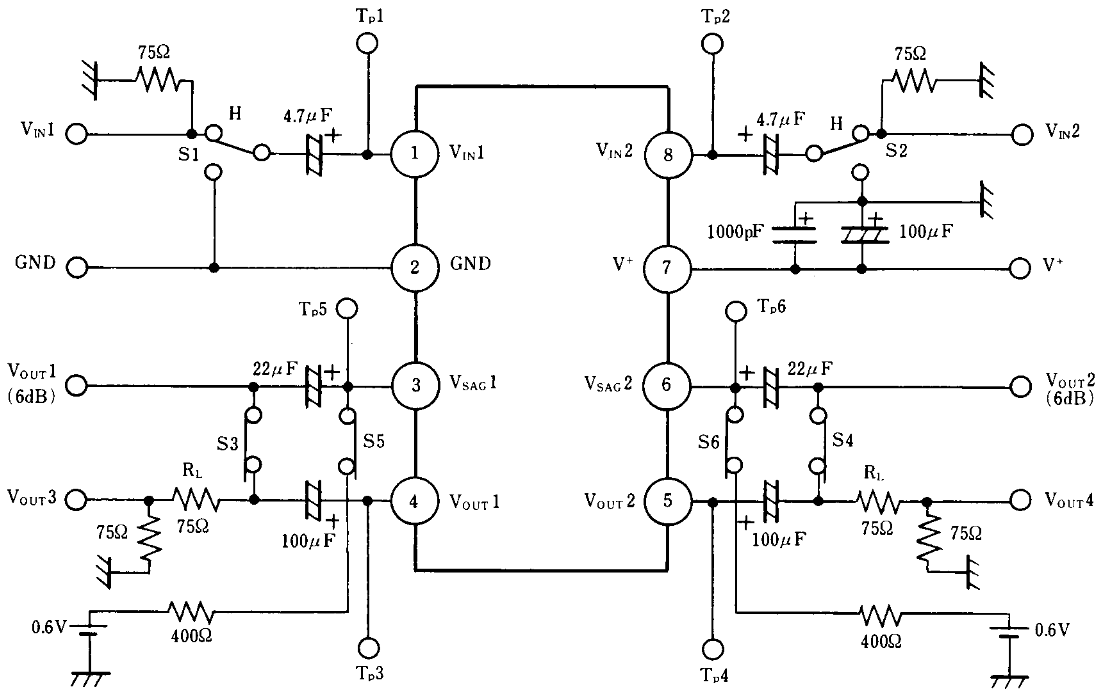


■ TERMINAL FUNCTION

(V^{+}=5.0V, Ta=25°C)

PIN No.	PIN NAME	SYMBOL	EQUIVALENT CIRCUIT	FUNCTIONS
1	Input Clamp Terminal	V_{IN1}		Input terminal of 1V_{P-P} composite signal or Y signal. Clamp level is 1.9V
2	GND	GND		Ground
3	SAG correction	V_{SAG1}		SAG caused by a coupling capacitor of the output can be prevented by connecting this terminal with the output terminal through an external capacitor.(see block diagram) When SAG correcting function is not necessary, this terminal must be connected with pin “4” directly.
4	Video Output1	V_{OUT1}		Output terminal that can drive 75Ω line.
5	Video Output2	V_{OUT2}		Output terminal that can drive 75Ω line.
6	SAG correction	V_{SAG2}		SAG caused by a coupling capacitor of the output can be prevented by connecting this terminal with the output terminal through an external capacitor.(see block diagram) When SAG correcting function is not necessary, this terminal must be connected with pin “5” directly.
7	V^{+}	V^{+}		Supply Voltage
8	Input Clamp Terminal	V_{IN2}		Input terminal of 1V_{P-P} composite signal or Y signal. Clamp level is 1.9V

■ TEST CIRCUIT



■ TEST METHODES

PARAMETER	SYMBOL	SWITCH CONDITIONS						CONDITIONS
		S1	S2	S3	S4	S5	S6	
Supply Current	I_{CC}	H	H					7PIN Sink Current
Voltage Gain	G_V	H	H	ON	ON			V_{OUT1} / V_{IN}, V_{OUT2} / V_{IN2} at V_{IN1}(V_{IN2})=1MHz, $1V_{P-P}$, Sinewave
Frequency Characteristic	G_f	H	H	ON	ON			G_{V1M}; Voltage Gain at V_{IN1} (V_{IN2})=1MHz, $1V_{P-P}$ G_{V10M}; Voltage Gain at V_{IN1} (V_{IN2})=7MHz, $1V_{P-P}$ G_f=G_{V10M}-G_{V1M}
Differential Gain	DG	H	H	ON	ON			Measuring V_{OUT3} at V_{IN1}=Staircase Signal
Differential Phase	DP	H	H	ON	ON			Measuring V_{OUT3} at V_{IN1}=Staircase Signal
Crosstalk	CT	H	L	ON	ON			V_{OUT2} / V_{OUT1} at V_{IN1}=4.43MHz, $1V_{P-P}$, Sinewave V_{OUT1} / VIN2 at V_{IN12}=4.43MHz, $1V_{P-P}$, Sinewave
Gain Offset	G_{CH}	H	H	ON	ON			G_{V1}=V_{OUT1} / V_{IN1}, G_{V2}=V_{OUT2} / V_{IN2} G_{CH}=G_{V1}-G_{V2}
Input Clamp Voltage	V_{CL}	H	H					Measuring at TP1 (TP2)
SAG Terminal Gain	G_{SAG}	H H	H H			 ON	 ON	TP3 (TP4) Voltage; Vo1A (Vo2A), TP5 (TP6) voltage; Vso1A (Vso2A) TP3 (TP4) Voltage; Vo1B(Vo2B), TP5 (TP6) voltage; Vso1B (Vso2B) G_{SAG}=20log{ (Vo1B-Vo1A) / (Vso1A-Vso1B) } G_{SAG}=20log{ (Vo2B-Vo2A) / (Vso2A-Vso2B) }

♦Clamp circuit

1. Operation of Sync-tip-clamp

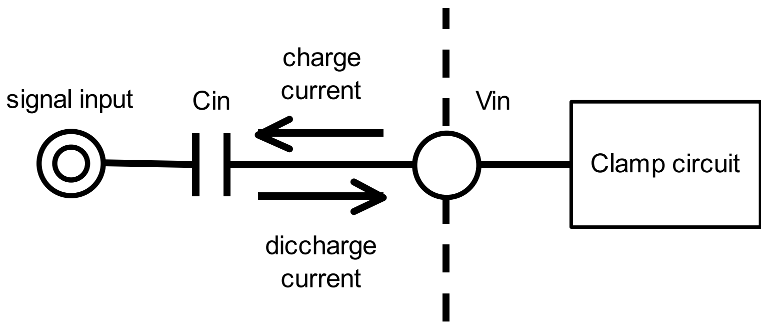
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input Cin. It is charged to the capacitor to the external input Cin at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor Cin at period other than the video signal sync tip. This is due to a small discharge current to the IC.

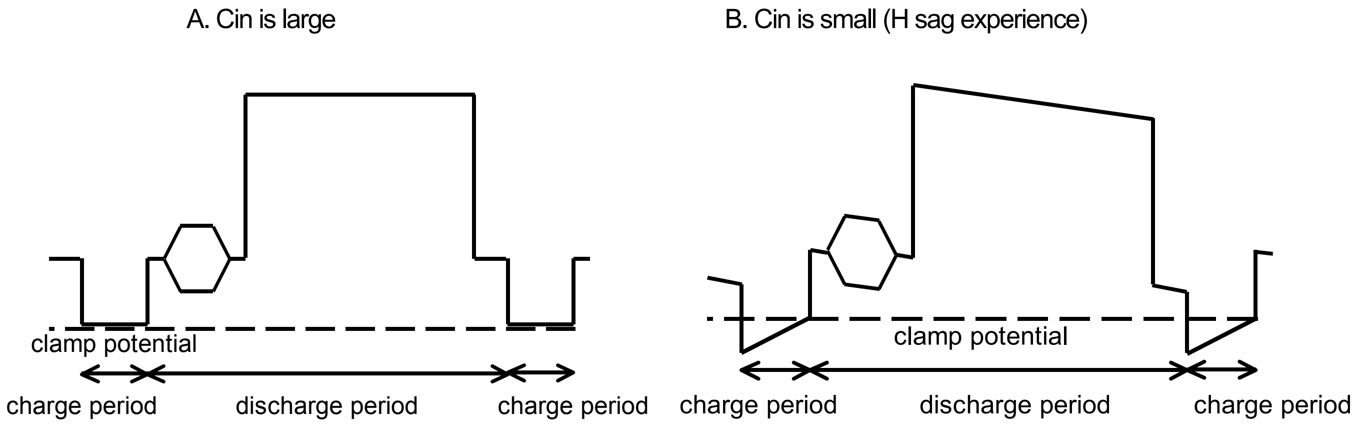
In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of Cin and discharging of Cin at every one horizontal period of the video signal.

The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor Cin.

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1uF.



< Clamp circuit >



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few kΩ. On the other hand, the input impedance of the discharge period is several MΩ. Because is a small discharge-current through to the IC.

Thus the input impedance will vary depending on the operating state of the clamp circuit.

3. Impedance of signal source

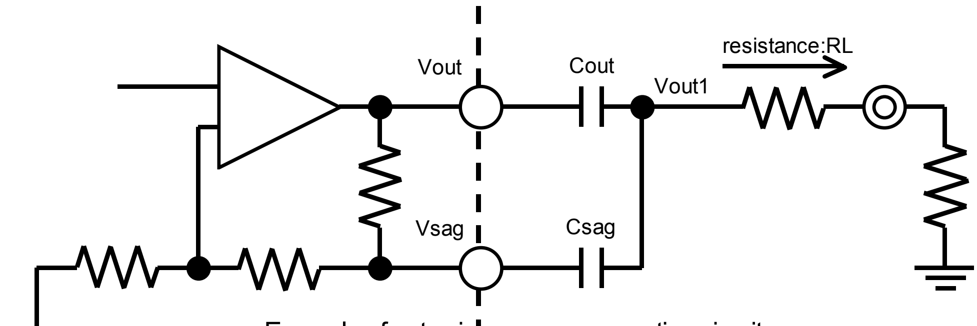
Source impedance to the input terminal, please lower than 200Ω. A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

♦ **SAG correction circuit**

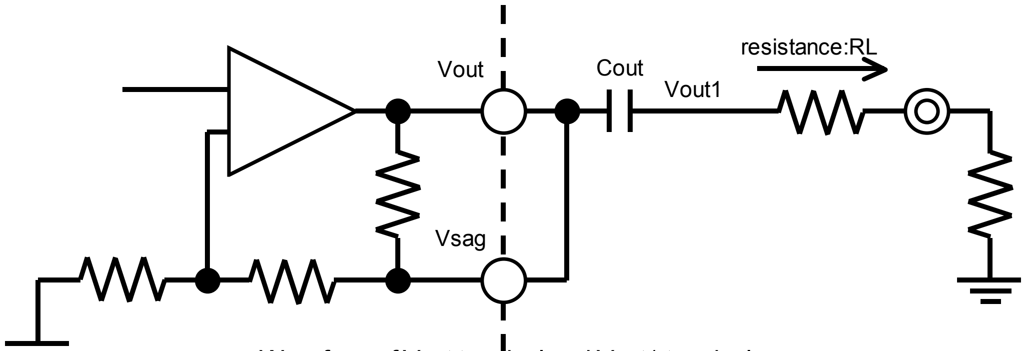
SAG correction circuit is a circuit to correct for low-frequency attenuation by high-pass filter consisting of the output coupling capacitance and load resistance. Low-frequency attenuation raises the sag in the vertical period of the video signal.

Capacitor for Vsag (Csag) is connected to the negative feedback of the amplifier. This Csag increase the low frequency gain to correct for the attenuation of low frequency gain.

Example SAG collection circuit



Example of not using sag compensation circuit



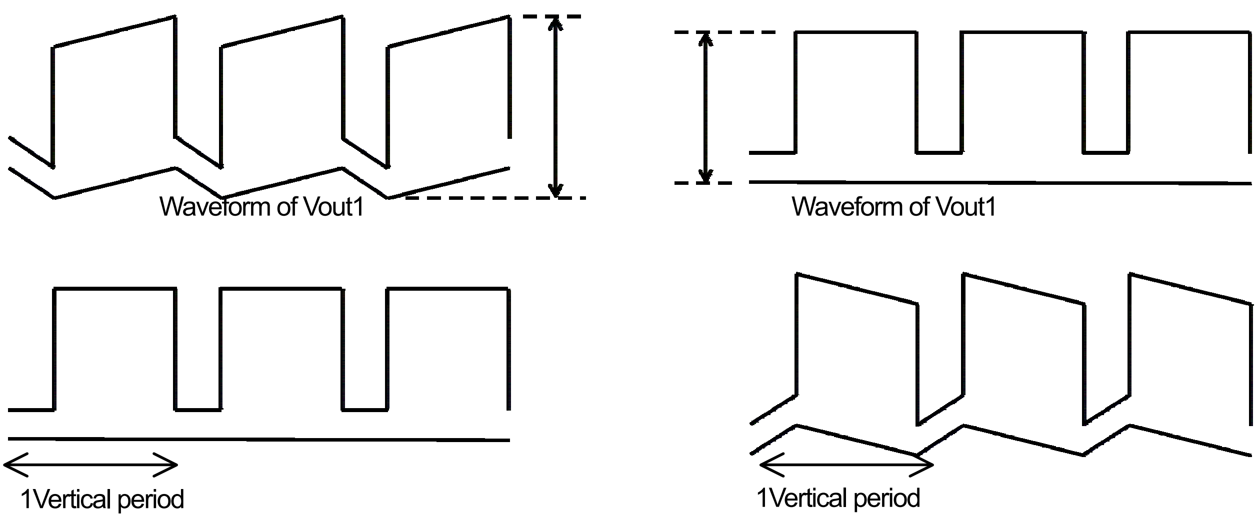
Waveform of Vout terminal and Vout1 terminal

using SAG correction circuit

Waveform of Vout

not using SAG correction circuit

Waveform of Vout



SAG correction circuit generates a low frequency component signal amplified to Vout terminal.
Changes of the luminance signal will be low-frequency components, if you want to output a large signal luminance changes. Therefore, generate correction signal of change of a luminance signal to Vout pin.
At this time, signal is over the dynamic range of Vout pin. This may cause a lack of sync signal, and waveform distortion.

Please see diagram below (green waveform), if you want to output large changes of a signal luminance, such as 100% white video signal and black signal. Thus, output signal exceed dynamic range of Vout pin and may be the signal lack.

< Countermeasure for waveform distortion >

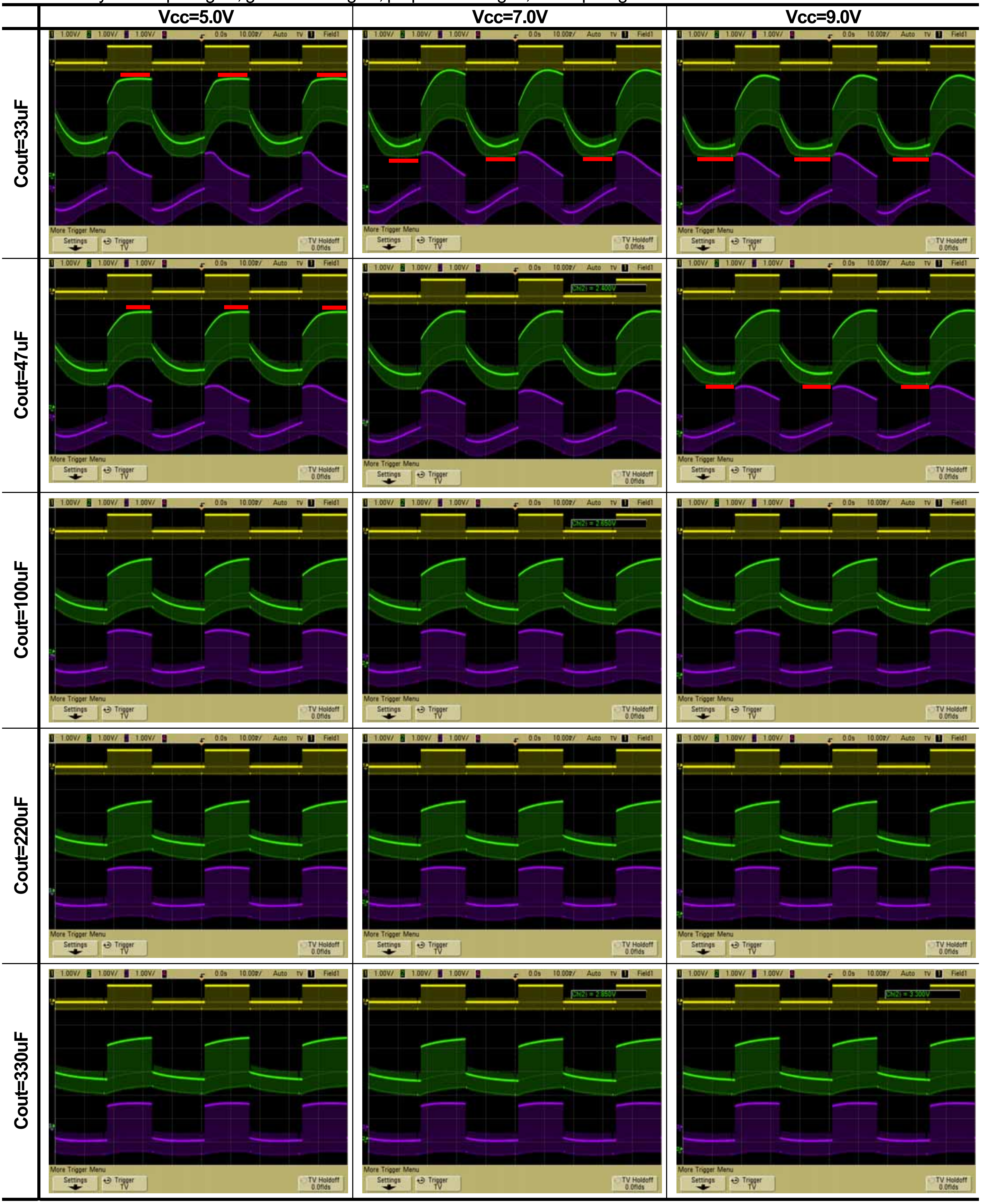
1. Please using small value the Sag compensation capacitor (VSAG).
   It can ensure the dynamic range by using small value the capacitor (VSAG). It because of low-frequency variation of Vout pin is smaller. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

2. Please do not use the sag correction circuit.
   Signal can output within dynamic range for reason it does not change the DC level of the output terminal.
   However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

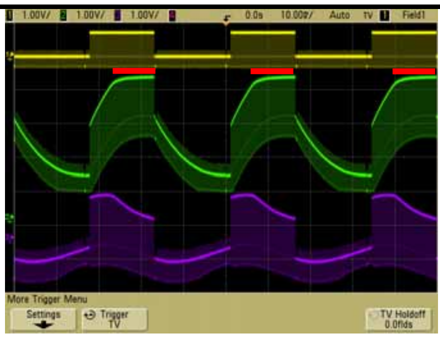
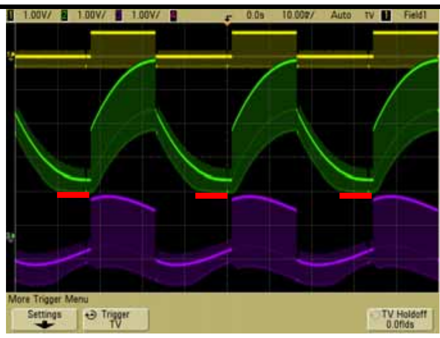
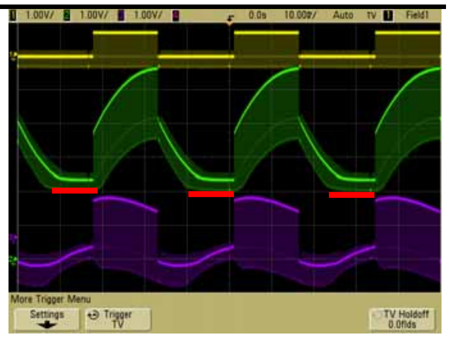
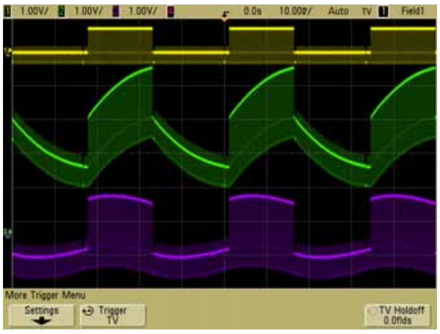
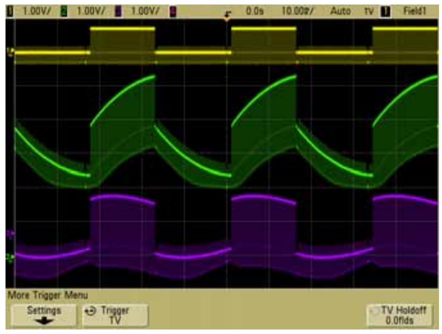
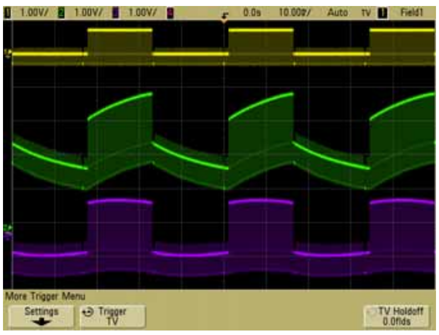
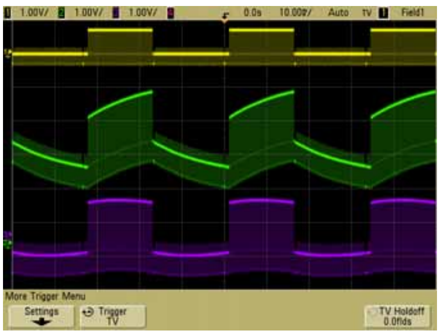
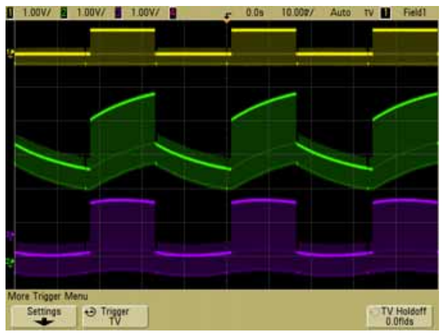
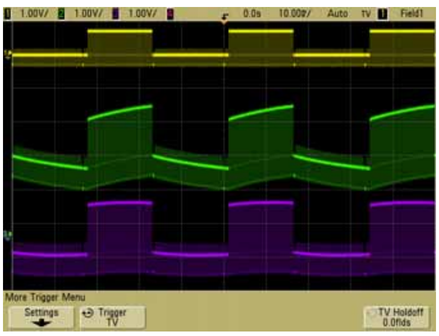
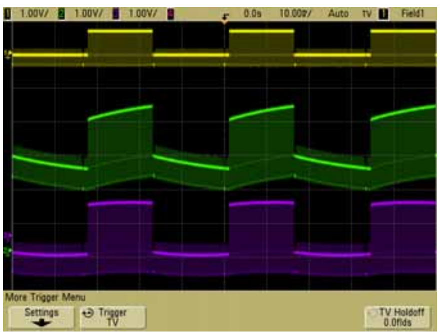
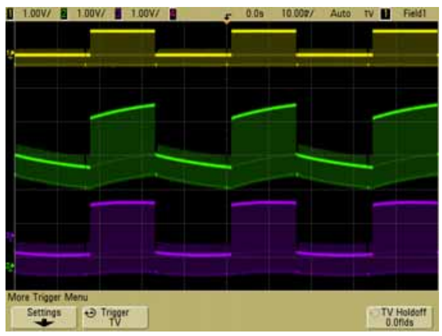
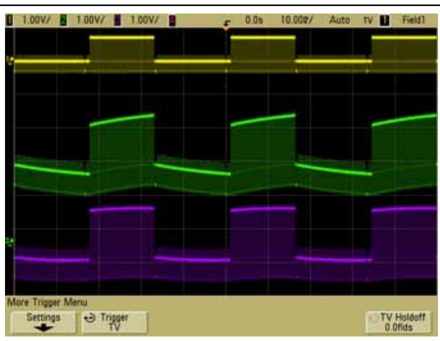
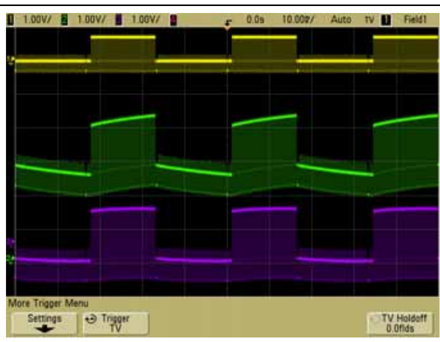
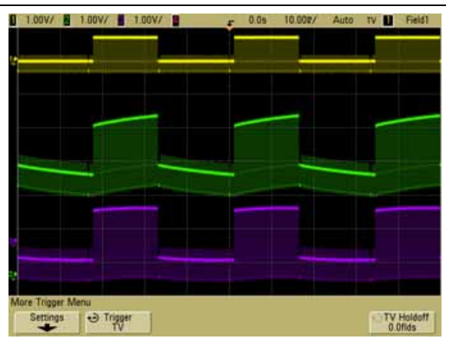
< Using SAG correction circuit >

Csag=10uF, Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω

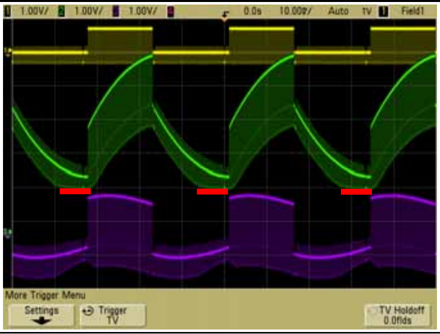
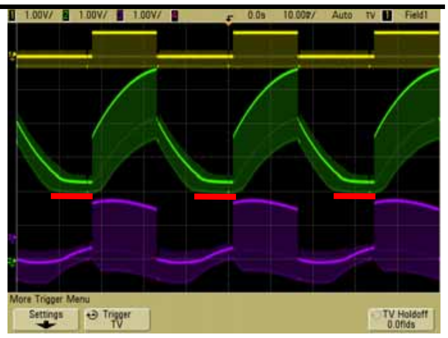
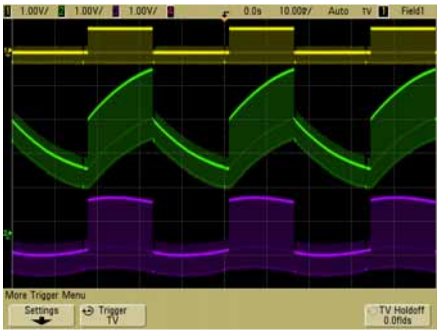
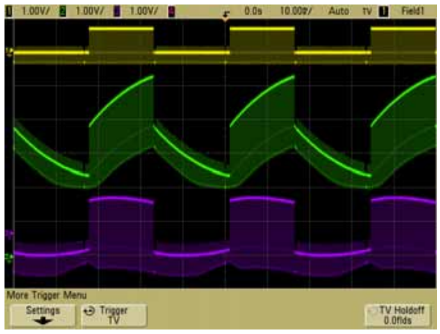
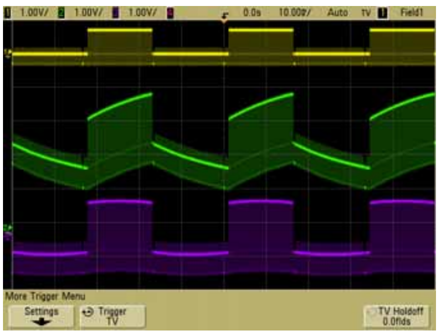
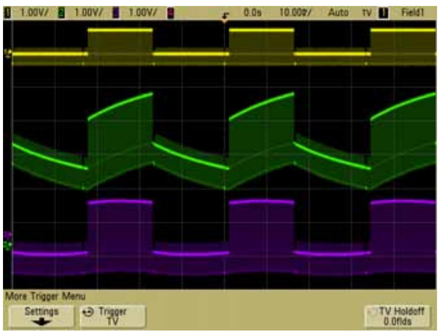
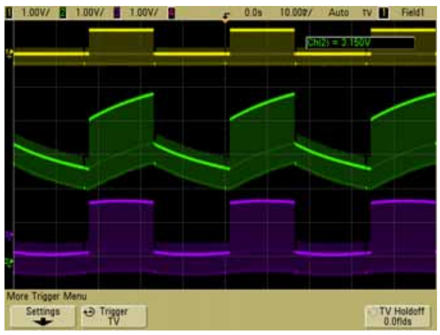
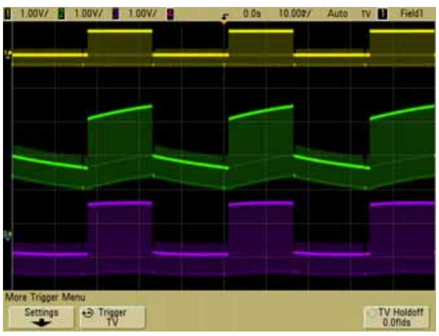
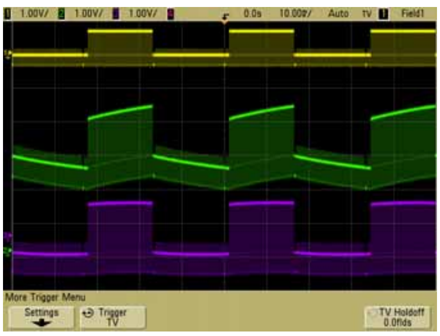
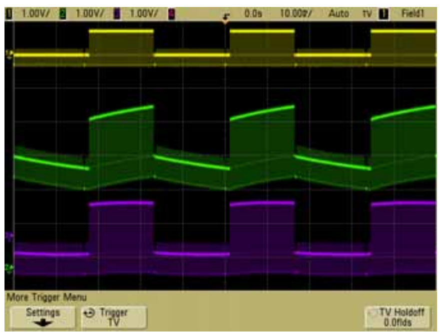
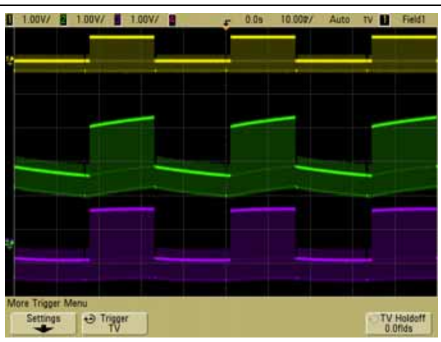
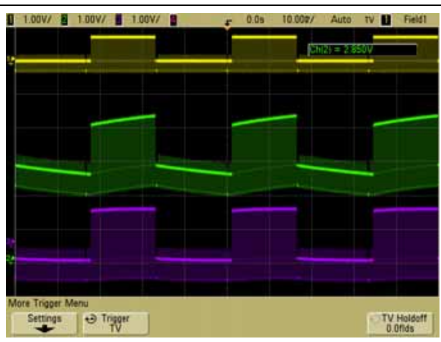
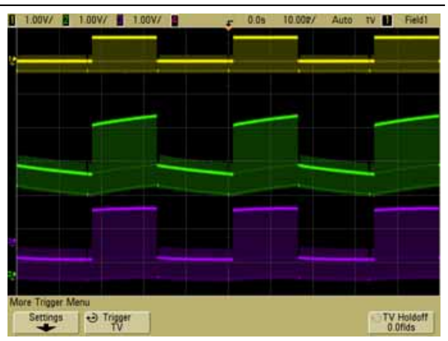
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signa, red: clip length of waveform



< Using SAG correction circuit >
Csag=22uF, Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signa, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

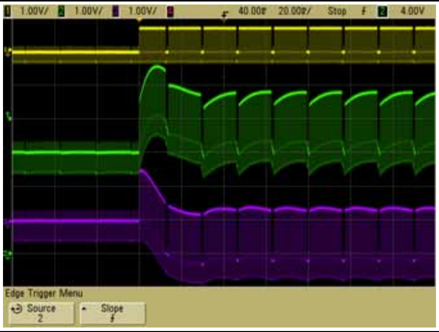
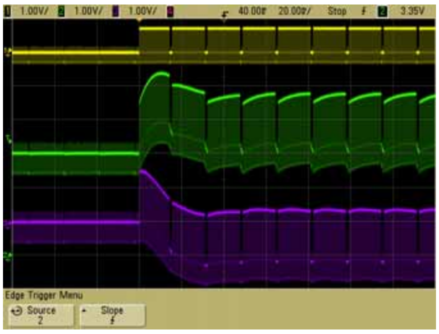
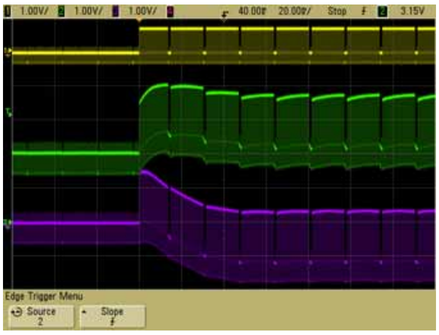
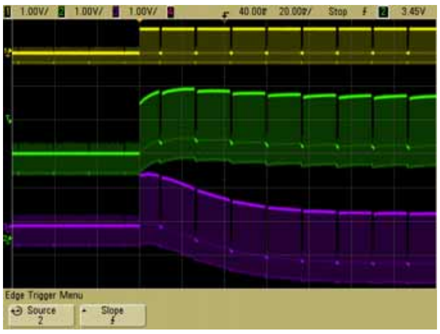
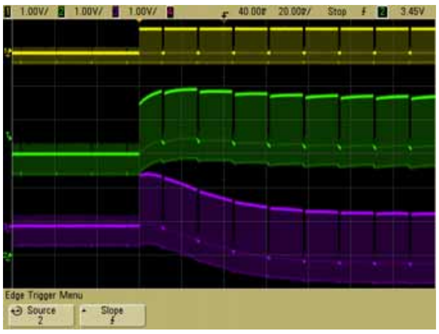
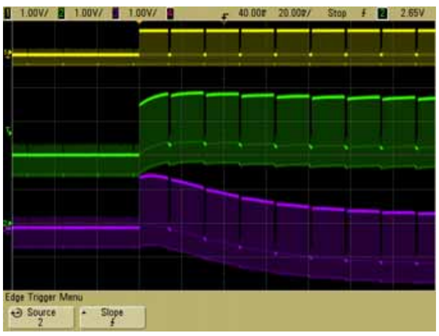
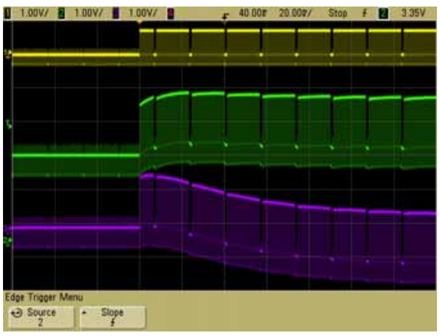
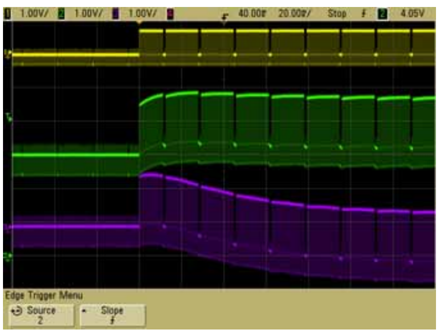
< Using SAG correction circuit >
Csag=33uF, Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signa, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

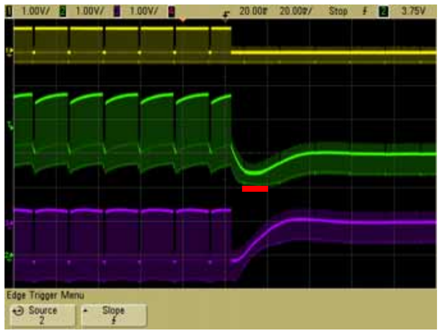
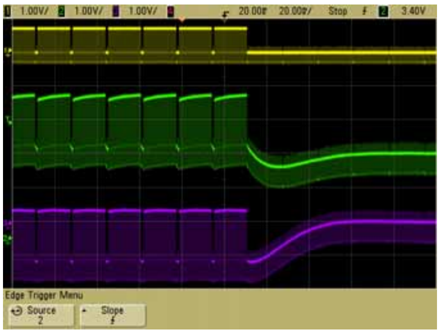
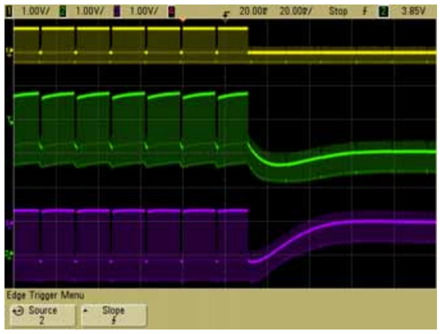
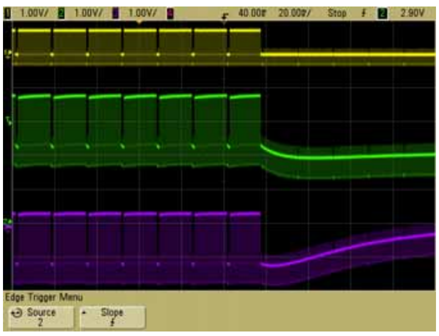
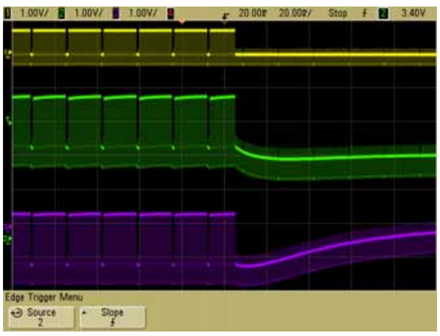
< Using SAG correction circuit >

Csag=10uF, Input signal: Black to White100%, resistance150Ω

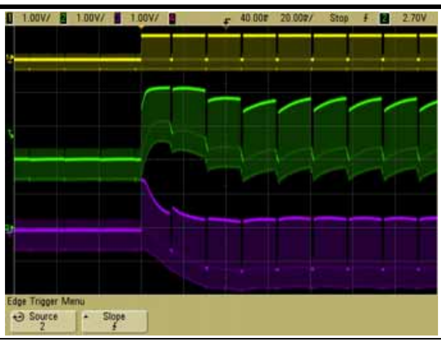
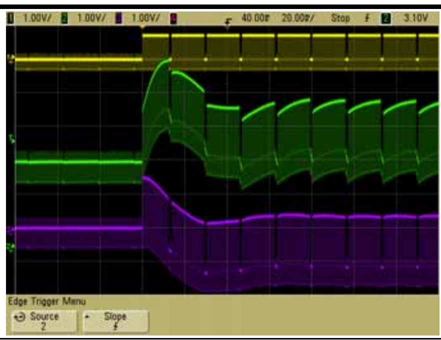
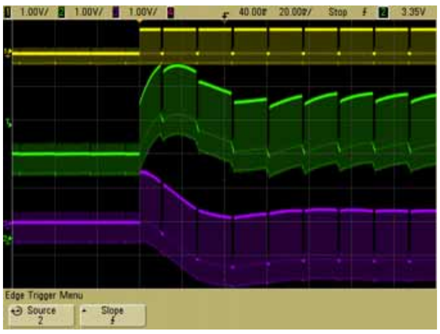
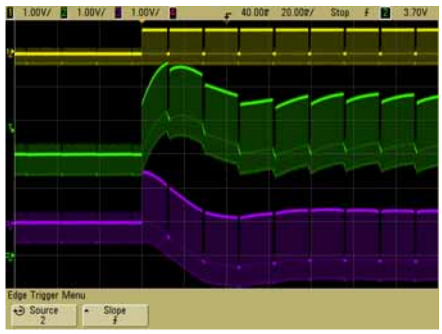
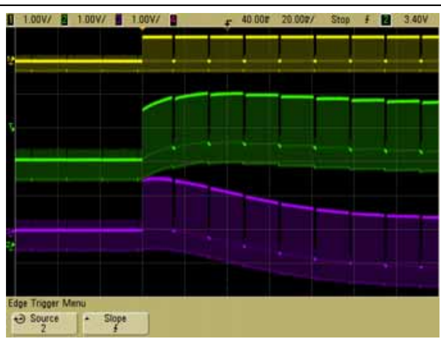
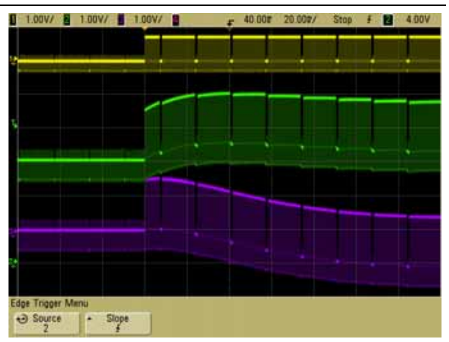
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

< Using SAG correction circuit >
Csag=10uF, Input signal: White100% to Black, resistance150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

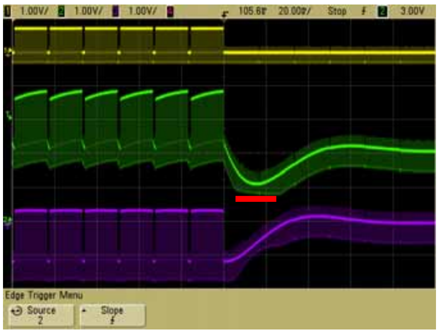
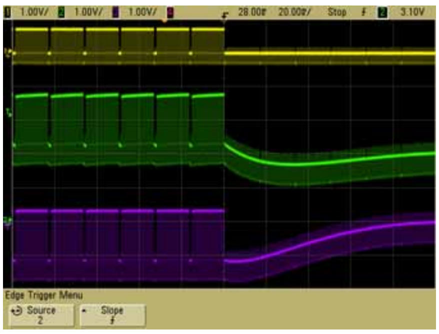
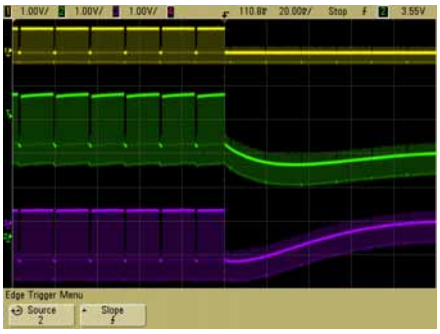
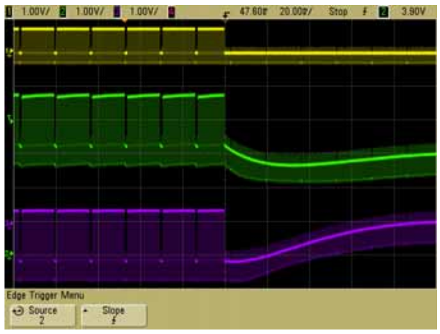
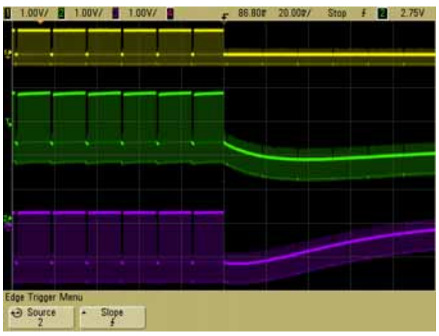
< Using SAG correction circuit >
Csag=22uF, Input signal: Black to White100%, resistance150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

< Using SAG correction circuit >

Csag=22uF, Input signal: White100% to Black, resistance150Ω

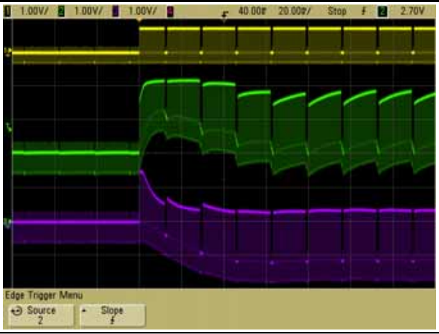
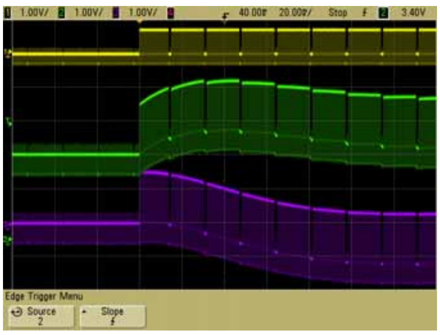
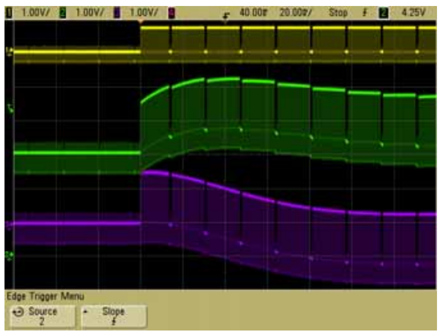
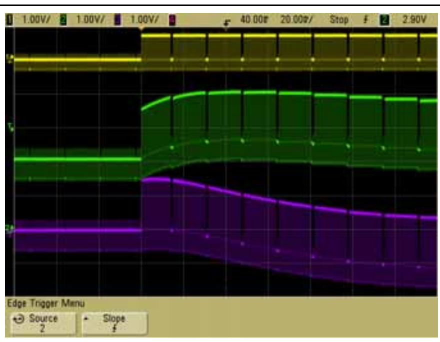
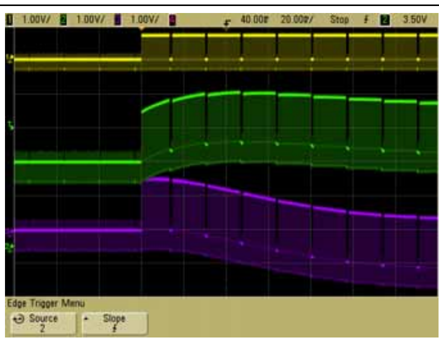
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

< Using SAG correction circuit >

Csag=33uF, Input signal: Black to White100%, resistance150Ω

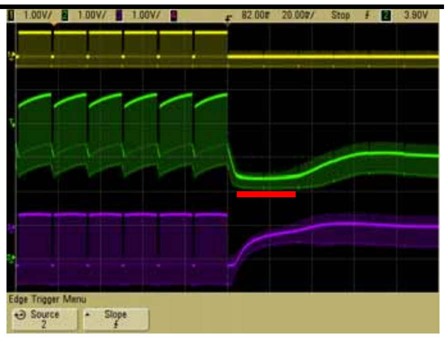
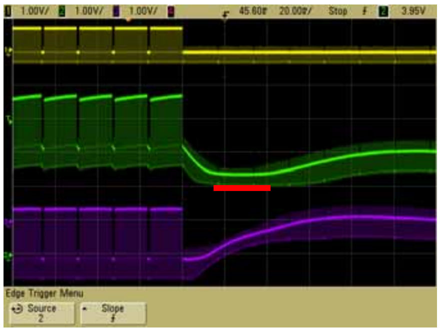
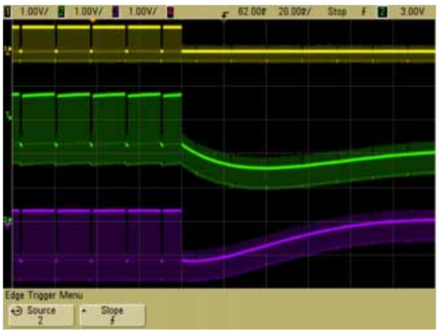
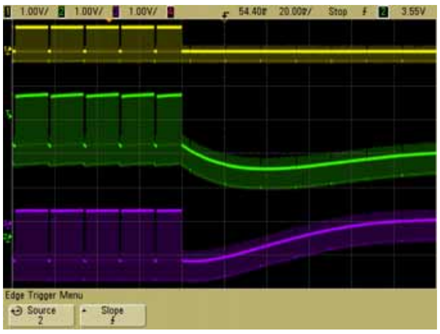
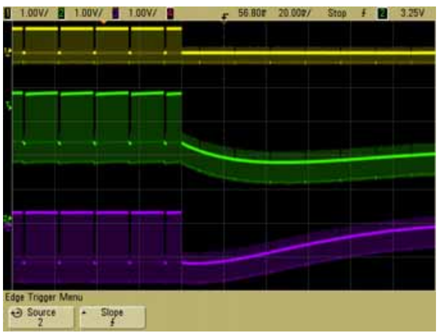
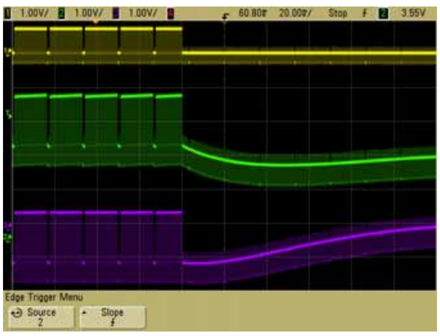
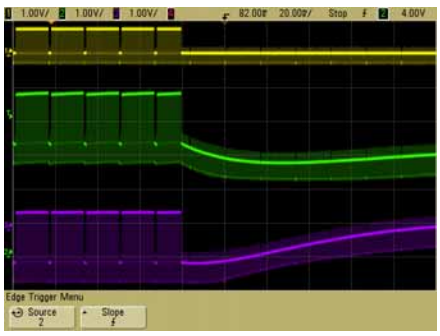
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

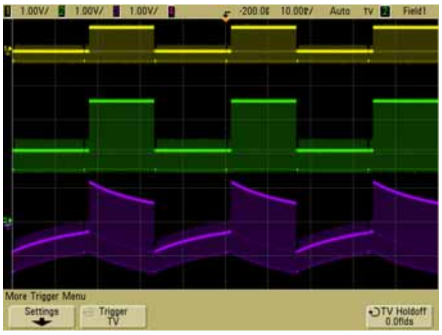
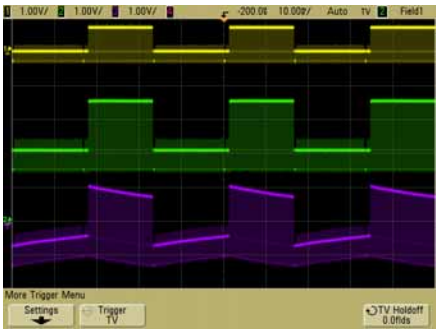
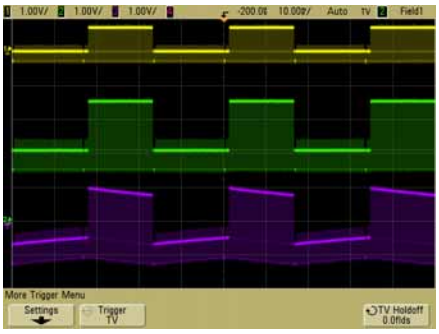
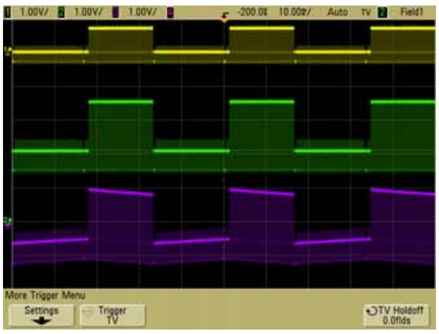
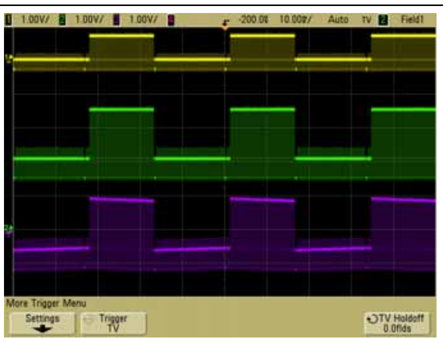
< Using SAG correction circuit >

Csag=33uF, Input signal: White100% to Black, resistance150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal, red: clip length of waveform

	Vcc=5.0V	Vcc=7.0V	Vcc=9.0V
Cout=33uF			
Cout=47uF			
Cout=100uF			
Cout=220uF			
Cout=330uF			

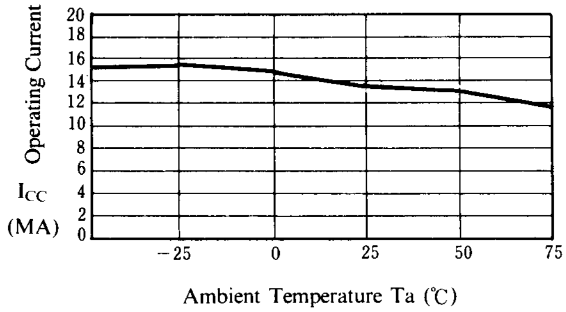
< Not using SAG correction circuit >
Vcc=5V, Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

	RL=150Ω
Cout=100uF	
Cout=220uF	
Cout=330uF	
Cout=470uF	
Cout=1000uF	

■ TYPICAL CHARACTERISTICS

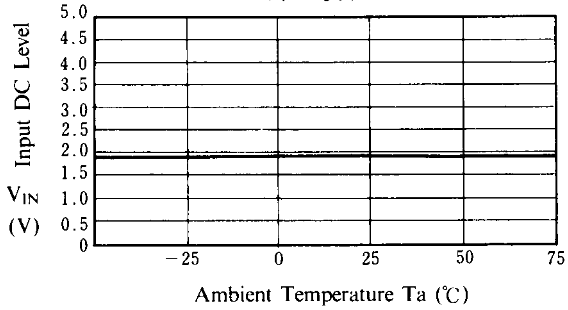
Operating Current vs. Ta

($V^+ = 5V$)



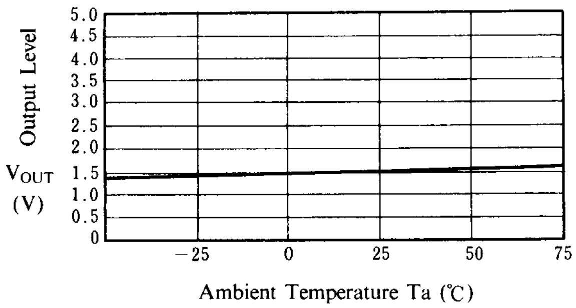
Input DC Level vs. Ta

($V^+ = 5V$)



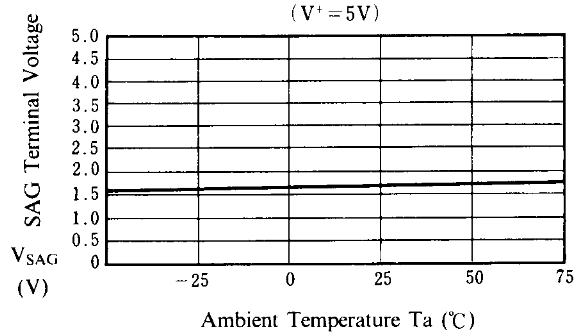
Output DC Level vs. Ta

($V^+ = 5V$)



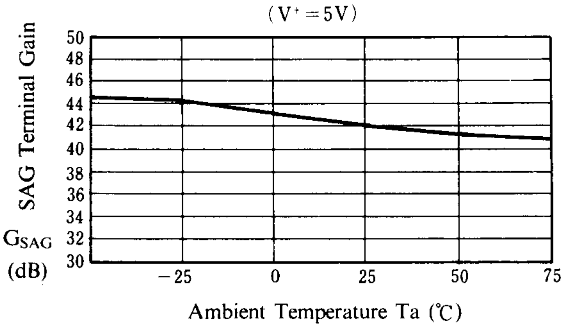
SAG Terminal Voltage vs. Ta

($V^+ = 5V$)



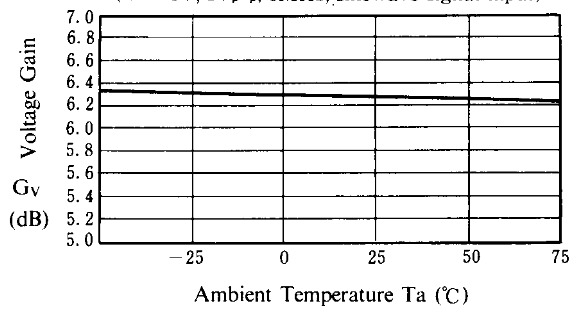
SAG Terminal Gain vs. Ta

($V^+ = 5V$)



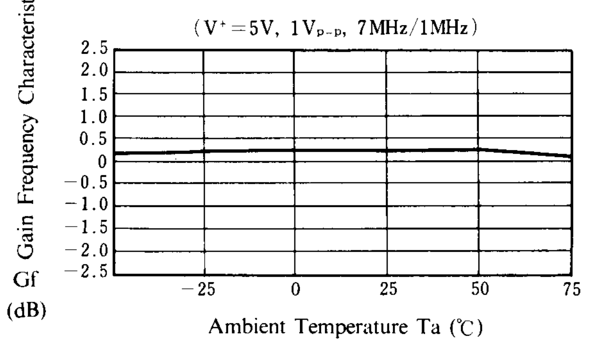
Voltage Gain vs. Ta (Clamp Type INput)

($V^+ = 5V$, $1V_{P-P}$, 1MHz, sinewave signal input)

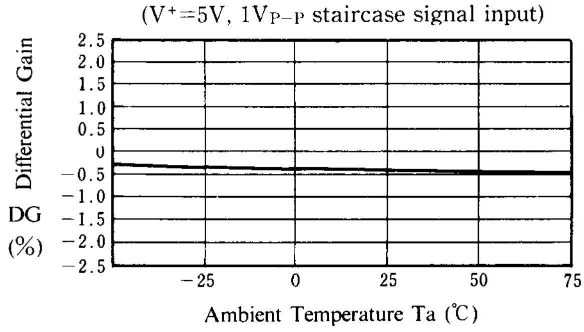


■ TYPICAL CHARACTERISTICS

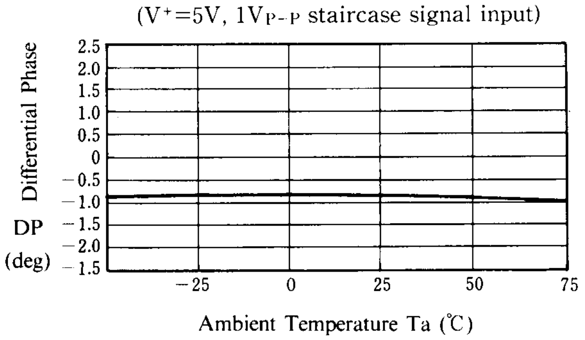
Gain Frequency Characteristics vs Ta (Clamp Type Input)



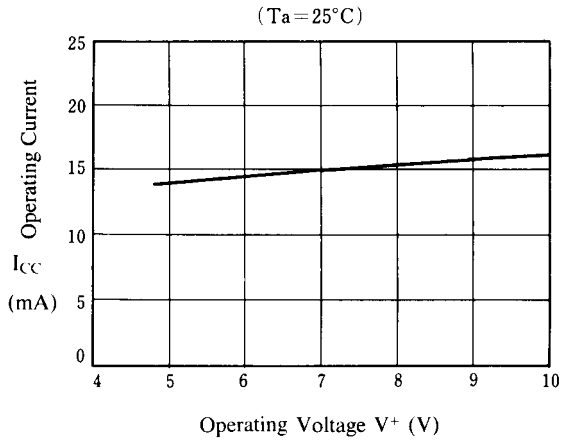
Differential Gain vs. Ta



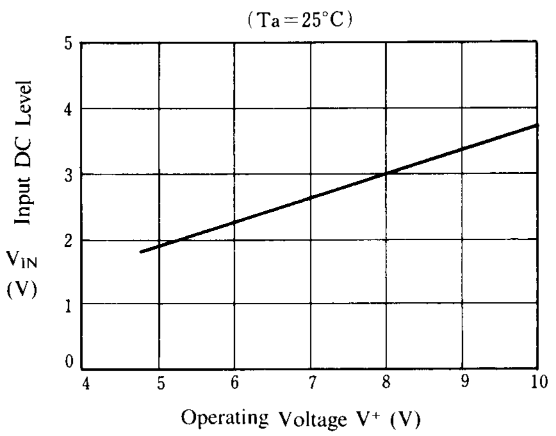
Differential Phase vs. Ta



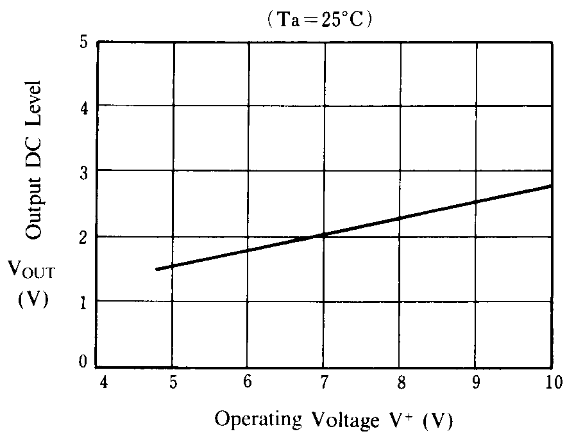
Operating Current vs. Operating Voltage



Input DC Level vs. Operating Voltage

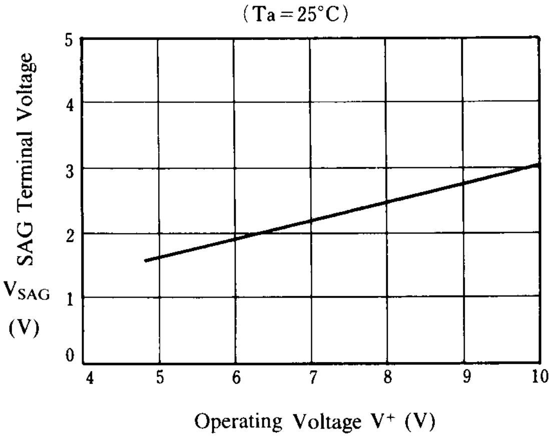


Output DC Level Vs. Operating Voltage

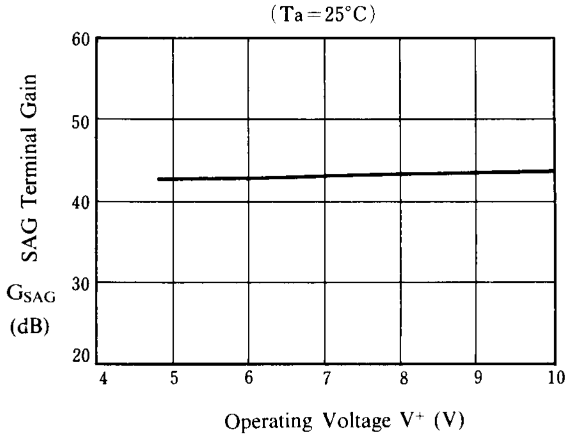


■ TYPICAL CHARACTERISTICS

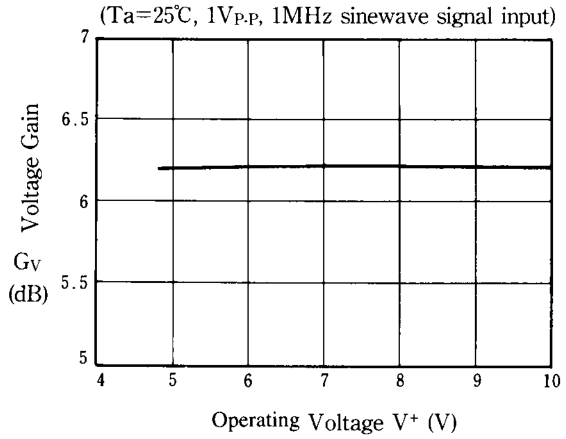
SAG Terminal Voltage vs. Operating Voltage



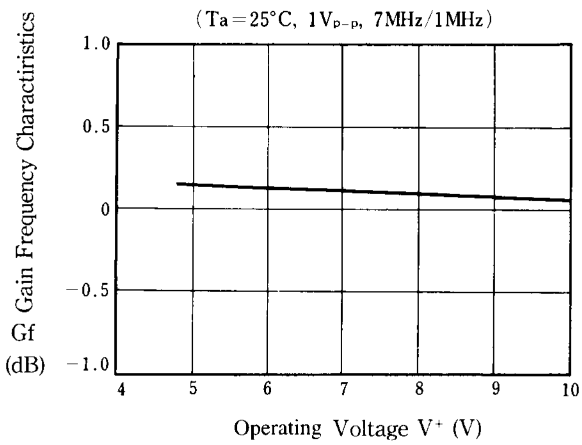
SAG Terminal Gain vs. Operating Voltage



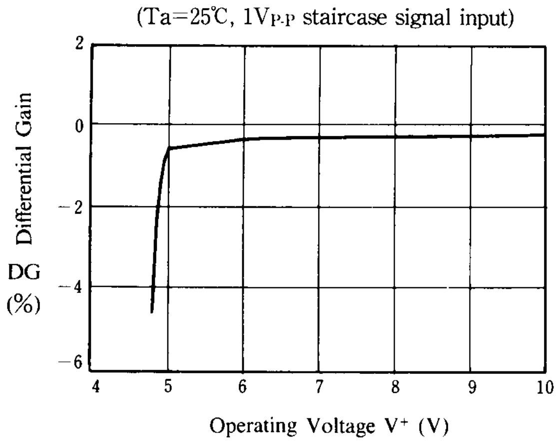
Voltage Gain vs. Operating Voltage



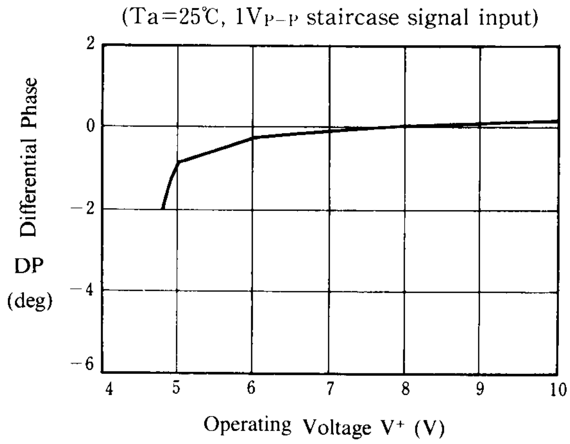
Gain Frequency Characteristics vs. Operating Voltage



Differential Gain vs. Operating Voltage



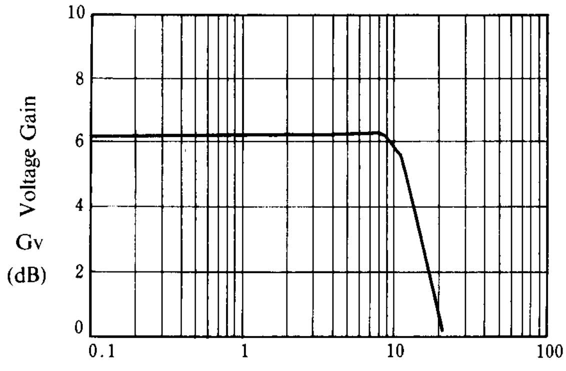
Differential Phase vs. Operating Voltage



■ TYPICAL CHARACTERISTICS

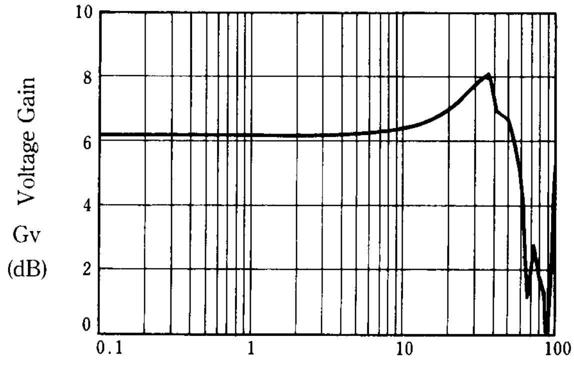
Voltage Gain vs. Frequency

(Ta=25℃, V+=5V, V1Vp-p sinewave signal input)



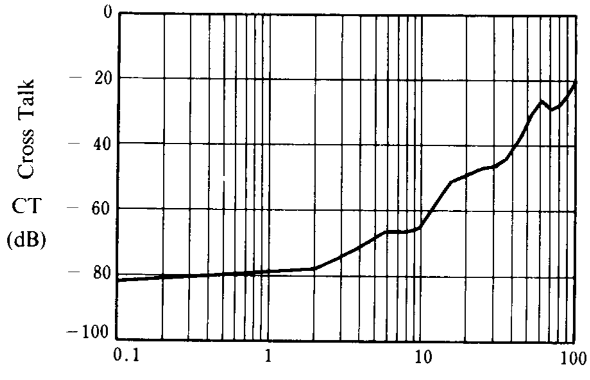
Small Signal Voltage Gain vs. Frequency

(Ta=25℃, V+=5Vp-p, 25Vp-p sinewave signal input)



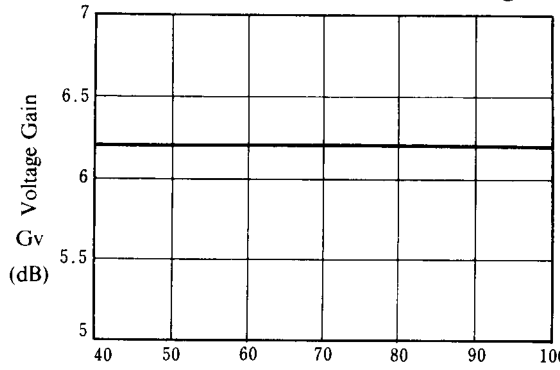
Cross Talk vs. Frequency

(Ta=25℃, V+=5V, 1Vp-p sinewave signal input)



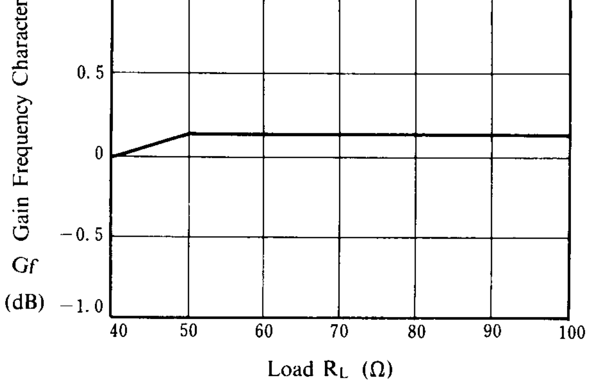
Voltage Gain vs. R_L

(Ta=25℃, V+=5V, 1Vp-p 1MHz sinewave signal input)



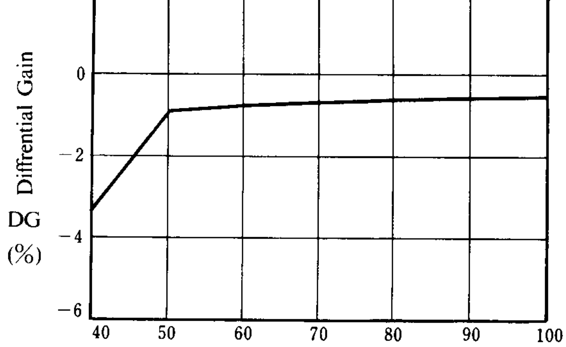
Gain Frequency Characteristics vs. R_L

(Ta=25℃, V+=5V, 1Vp-p, 7MHz/1MHz)



Differential Gain vs. R_L

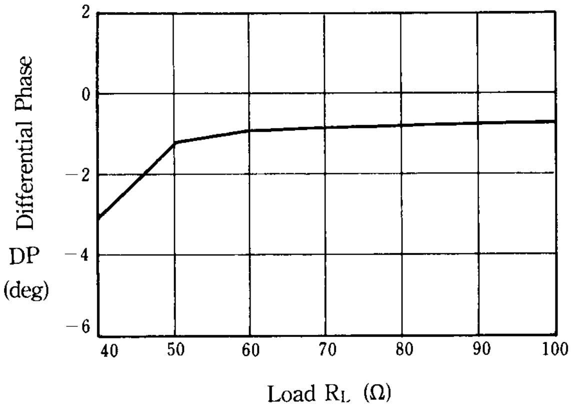
(Ta=25℃, V+=5V, 1Vp-p staircase signal input)



■ TYPICAL CHARACTERISTICS

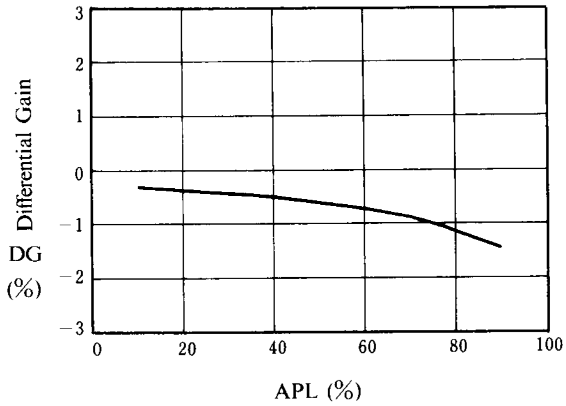
Differential Phase vs. R_L

(Ta=25℃, V+=5V, 1Vp-p sinewave signal input)



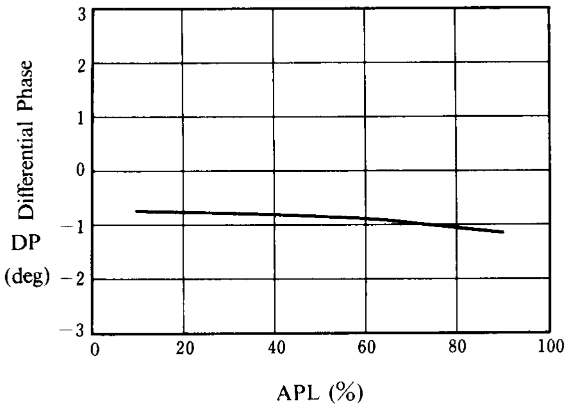
Differential Gain vs. APL

(Ta=25℃, V+=5V, 1Vp-p staircase signal input)



Differential Phase vs. APL

(Ta=25℃, V+=5V, 1Vp-p, staircase signal input)



■ APPLICATION

This IC requires 1MΩ resistance between INPUT and GND pin for clamp type input since the minute current causes an unstable pin voltage.