MC74HC373A

Octal 3-State Non-Inverting Transparent Latch

High–Performance Silicon–Gate CMOS

The MC74HC373A is identical in pinout to the LS373. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high–impedance state. Thus, data may be latched even when the outputs are not enabled.

The HC373A is identical in function to the HC573A which has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

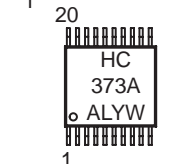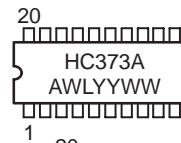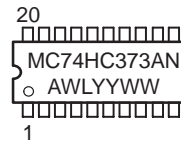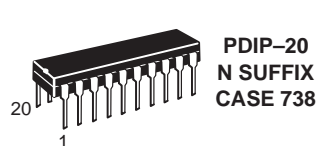The HC373A is the non–inverting version of the HC533A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates

ON Semiconductor

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MARKING DIAGRAMS

| PDIP–20 N SUFFIX CASE 738 |
| SOIC WIDE–20 DW SUFFIX CASE 751D |
| TSSOP–20 DT SUFFIX CASE 948G |

MC74HC373AN
AWLYYWW

HC373A
AWLYYWW

HC
373A
ALYW

A   = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC373AN	PDIP–20	1440 / Box
MC74HC373ADW	SOIC–WIDE	38 / Rail
MC74HC373ADWR2	SOIC–WIDE	1000 / Reel
MC74HC373ADT	TSSOP–20	75 / Rail
MC74HC373ADTR2	TSSOP–20	2500 / Reel

MC74HC373A
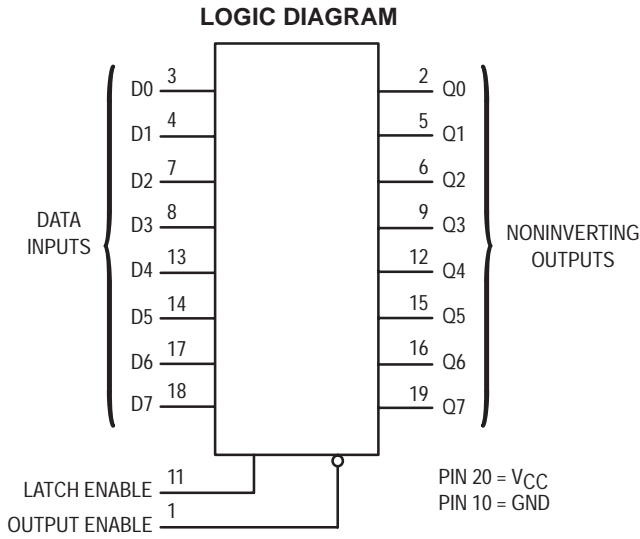
PIN ASSIGNMENT

OUTPUT ENABLE	1●	20	V_{CC}
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	LATCH ENABLE

LOGIC DIAGRAM

DATA INPUTS

D0	3
D1	4
D2	7
D3	8
D4	13
D5	14
D6	17
D7	18

NONINVERTING OUTPUTS

2	Q0
5	Q1
6	Q2
9	Q3
12	Q4
15	Q5
16	Q6
19	Q7

LATCH ENABLE 11
OUTPUT ENABLE 1

PIN 20 = V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Design Criteria	Value	Units
Internal Gate Count*	46.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	0.0075	pJ

*Equivalent to a two–input NAND gate.

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MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		-0.5 to $+7.0$	V
V_{in}	DC Input Voltage (Referenced to GND)		-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)		-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin		± 20	mA
I_{out}	DC Output Current, per Pin		± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air,	Plastic DIP†	750	mW
		SOIC Package†	500	
		TSSOP Package†	450	
T_{stg}	Storage Temperature		-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package)		260	°C

> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq V_{CC}$.
> Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
  Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
               SOIC Package: -7 mW/°C from 65° to 125°C
               TSSOP Package: -6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6.0$ V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions		V_{CC} V	Guaranteed Limit			Unit
					-55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	$V_{out} = V_{CC} - 0.1$ V	$|I_{out}| \leq 20$ µA	2.0	1.5	1.5	1.5	V
				3.0	2.1	2.1	2.1	
				4.5	3.15	3.15	3.15	
				6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low–Level Input Voltage	$V_{out} = 0.1$ V	$|I_{out}| \leq 20$ µA	2.0	0.5	0.5	0.5	V
				3.0	0.9	0.9	0.9	
				4.5	1.35	1.35	1.35	
				6.0	1.8	1.8	1.8	
V_{OH}	Minimum High–Level Output Voltage	$V_{in} = V_{IH}$	$|I_{out}| \leq 20$ µA	2.0	1.9	1.9	1.9	V
				4.5	4.4	4.4	4.4	
				6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$	$|I_{out}| \leq 2.4$ mA	3.0	2.48	2.34	2.2	
			$|I_{out}| \leq 6.0$ mA	4.5	3.98	3.84	3.7	
			$|I_{out}| \leq 7.8$ mA	6.0	5.48	5.34	5.2	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IL}$	$|I_{out}| \leq 20$ µA	2.0	0.1	0.1	0.1	V
				4.5	0.1	0.1	0.1	
				6.0	0.1	0.1	0.1	
		$V_{in} = V_{IL}$	$|I_{out}| \leq 2.4$ mA	3.0	0.26	0.33	0.4	
			$|I_{out}| \leq 6.0$ mA	4.5	0.26	0.33	0.4	
			$|I_{out}| \leq 7.8$ mA	6.0	0.26	0.33	0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				− 55 to 25°C	≤ 85°C	≤ 125°C	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 3.0 4.5 6.0	125 80 25 21	155 110 31 26	190 130 38 32	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5)	2.0 3.0 4.5 6.0	140 90 28 24	175 120 35 30	210 140 42 36	ns
t_{PLZ} t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL} t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)		15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	36	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

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Symbol	Parameter	Fig.	V_{CC} Volts	Guaranteed Limit						Unit
				− 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	4	2.0	25		30		40		ns
			3.0	20		25		30		
			4.5	5.0		6.0		8.0		
			6.0	5.0		6.0		7.0		
t_h	Minimum Hold Time, Latch Enable to Input D	4	2.0	5.0		5.0		5.0		ns
			3.0	5.0		5.0		5.0		
			4.5	5.0		5 0		5.0		
			6.0	5.0		5.0		5.0		
t_w	Minimum Pulse Width, Latch Enable	2	2.0	60		75		90		ns
			3.0	23		27		32		
			4.5	12		15		18		
			6.0	10		13		15		
t_r, t_f	Maximum Input Rise and Fall Times	1	2.0		1000		1000		1000	ns
			3.0		800		800		800	
			4.5		500		500		500	
			6.0		400		400		400	

SWITCHING WAVEFORMS
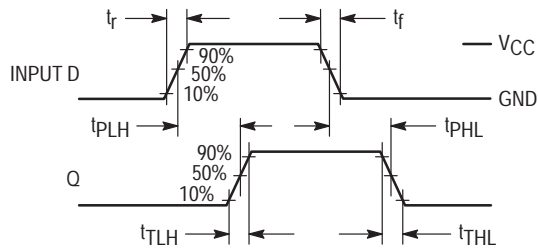
Figure 1.
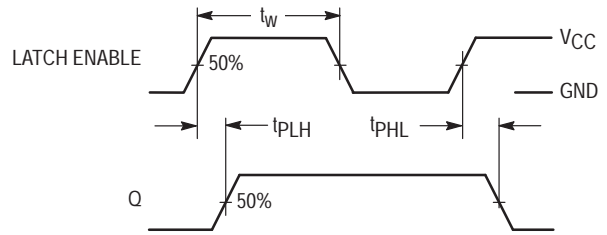
Figure 2.
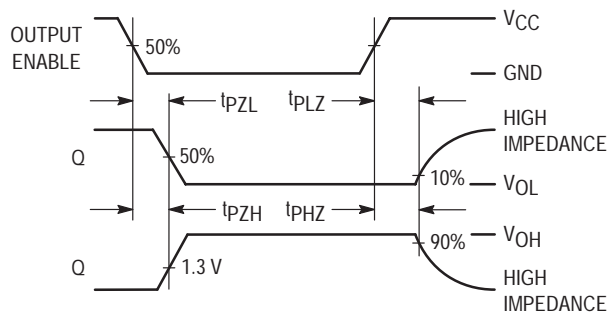
Figure 3.
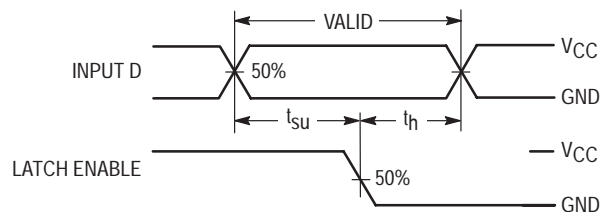
Figure 4.

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TEST CIRCUITS
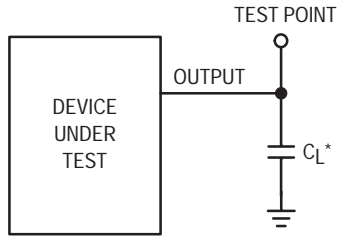
*Includes all probe and jig capacitance

Figure 5.

CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}. CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.
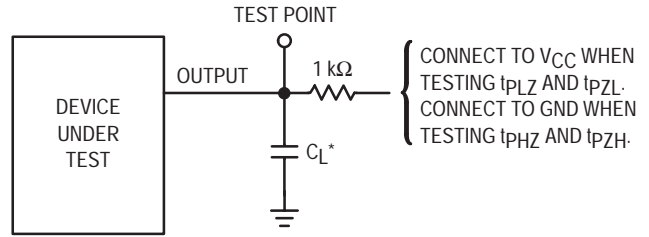
*Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM

PACKAGE DIMENSIONS

PDIP–20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E
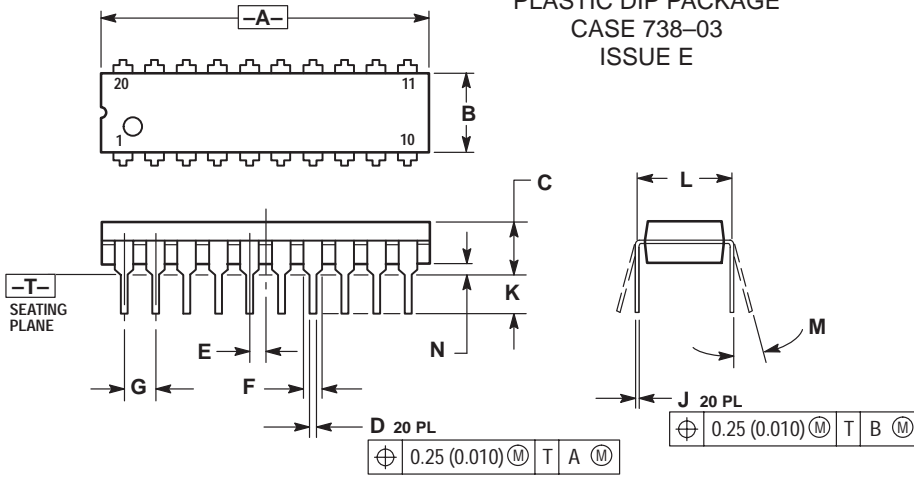
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0 °	15°	0 °	15°
N	0.020	0.040	0.51	1.01

SO–20
DW SUFFIX
CASE 751D–05
ISSUE F
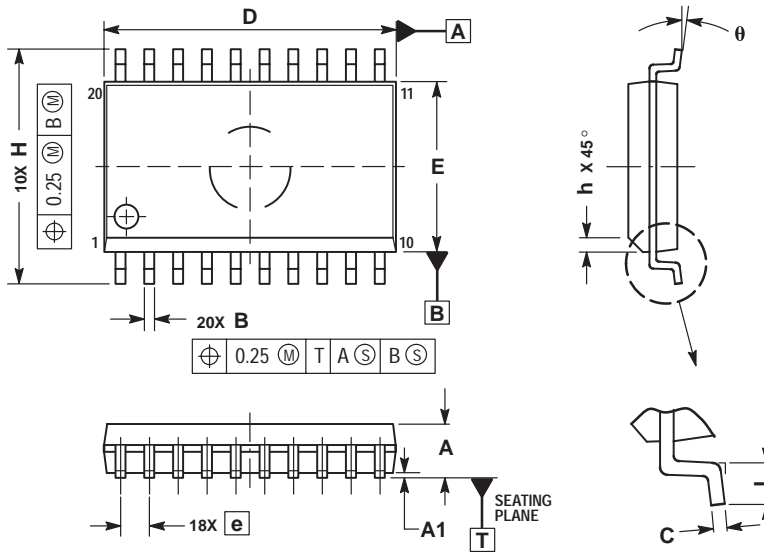
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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PACKAGE DIMENSIONS

TSSOP–20
DT SUFFIX
CASE 948E–02
ISSUE A

SECTION N–N

DETAIL E

DETAIL E

SEATING PLANE
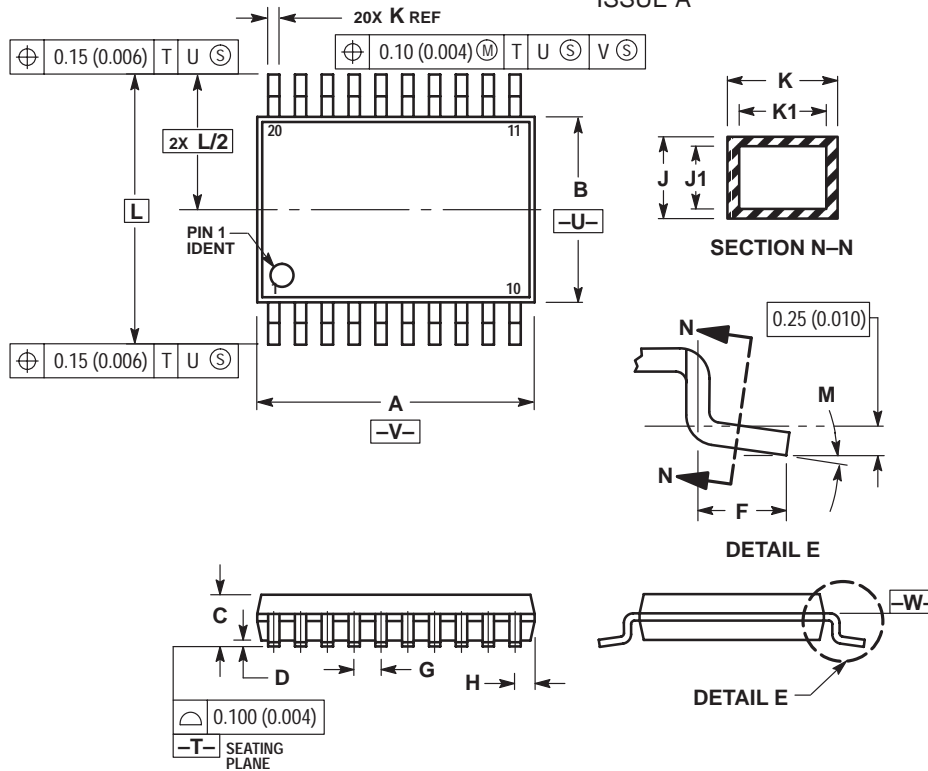
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74HC373A/D