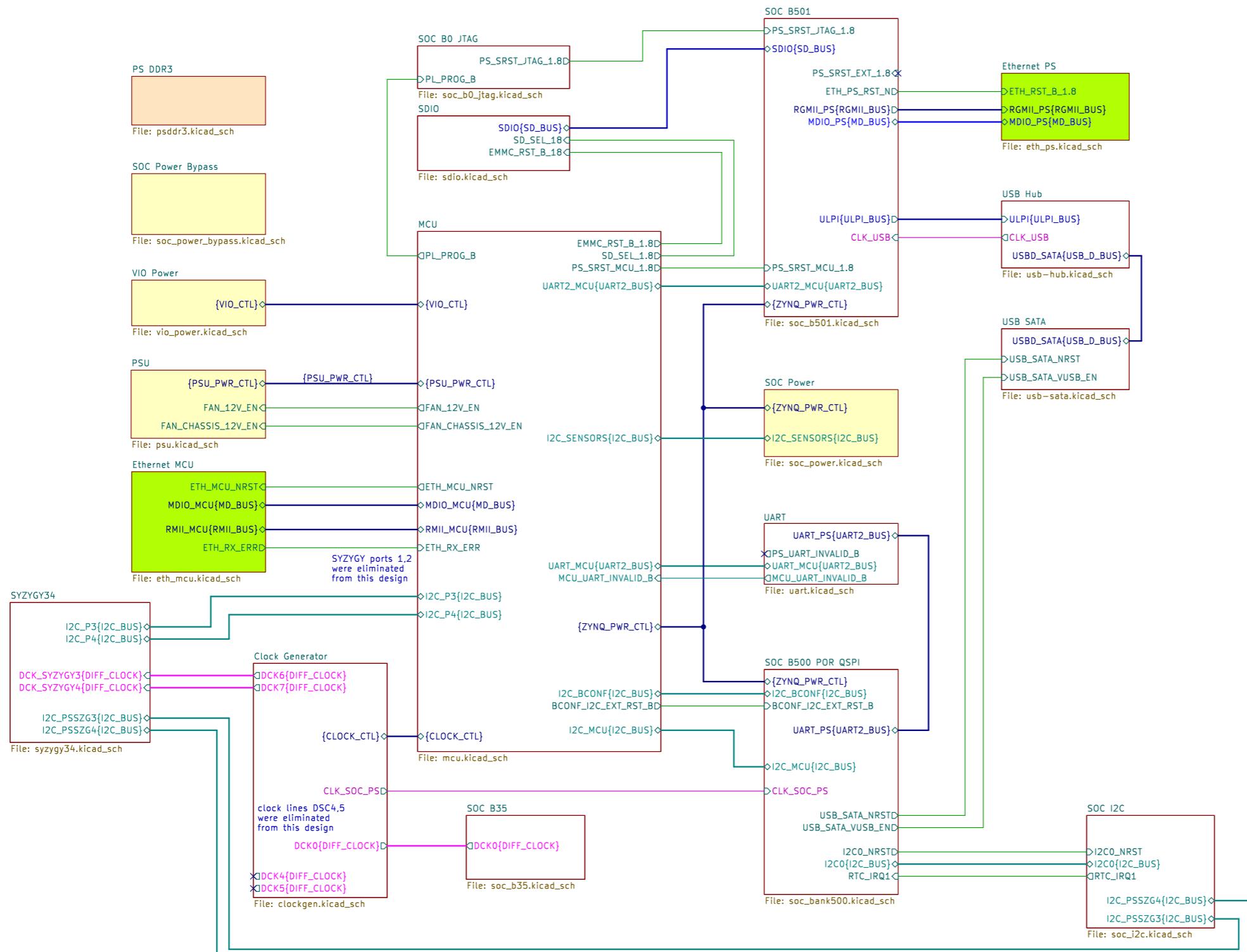


PAGE	DESCRIPTION
1 ROOT PAGE	Block Diagram of the project
2 PSU	ATX PSU connector and filters
3 SOC Power	A secondary power supply for SOC
4 MCU	MCU
5 Clock Generator	Clocks for SOC and SYZYGY, external master sync
6 UART	UART peripherals
7 SOC_B0_JTAG	SOC JTAG
8 SOC Power Bypass	SOC bypass capacitors
9 SOC_B500 POR QSPI	Power on reset, QSPI, SOC boot config
10 SOC_B501	Peripheral resets, ULPi and RGMII buses
11 PS DDR3	DDR3 RAM for SOC PS subsystem
12 SDIO	SDIO and EMMC shared bus
13 SOC_B35	A redundant clock for SOC PS
14 Ethernet PS	RGMII Ethernet peripheral
15 USB Hub	USB, ULPi transceiver and hub
16 USB SATA	USB SATA converter and SATA SSD socket
17 VIO Power	Variable IO power for SYZYGY slots
18 SYZYGY34	SYZYGY slots
19 SOC_I2C	SOC I2C
20 Ethernet MCU	10/100 RMII Ethernet for MCU

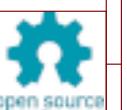


NOTE:
SYZYGY ports 1,2
were eliminated
from this design



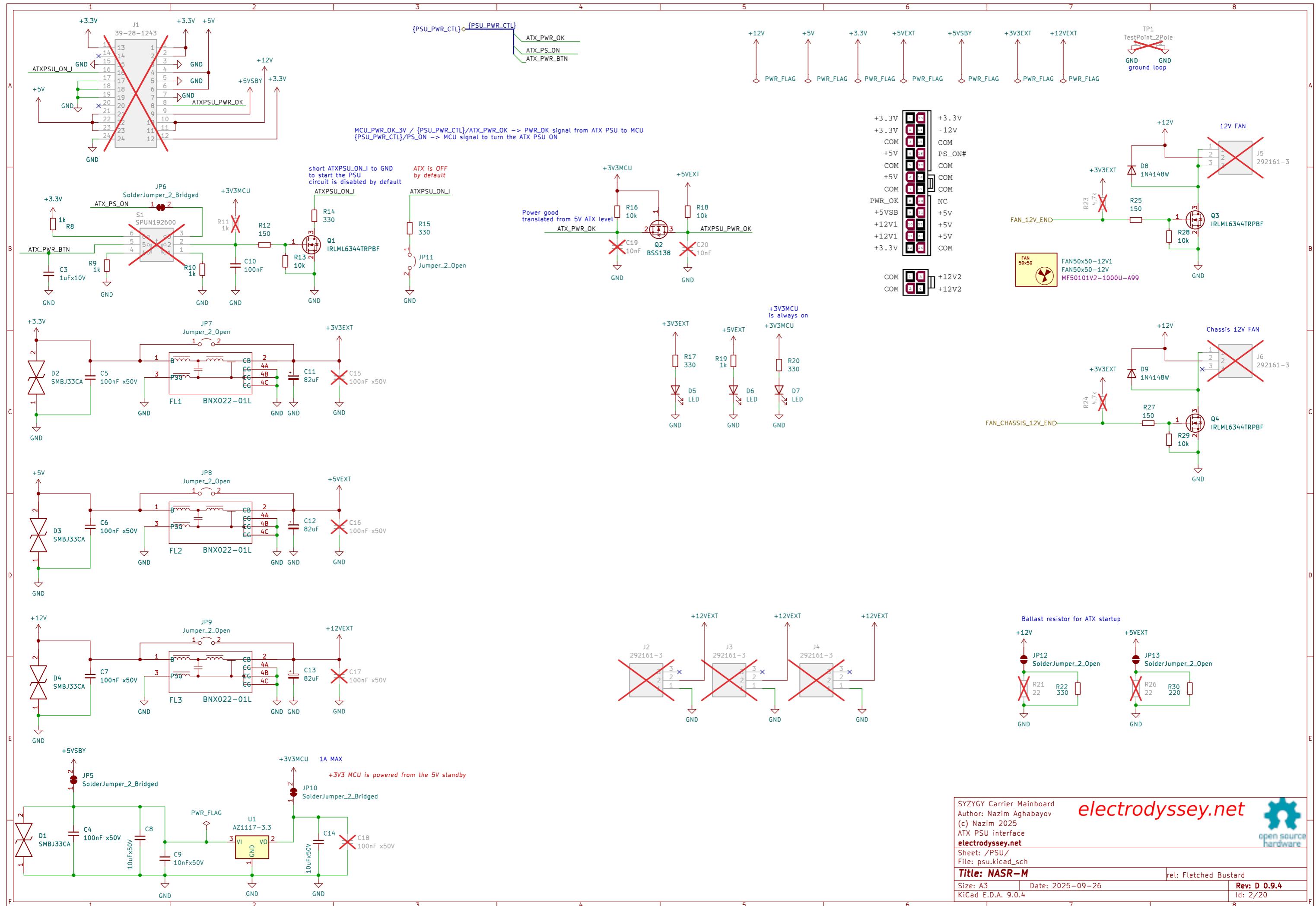
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Top Level Schema
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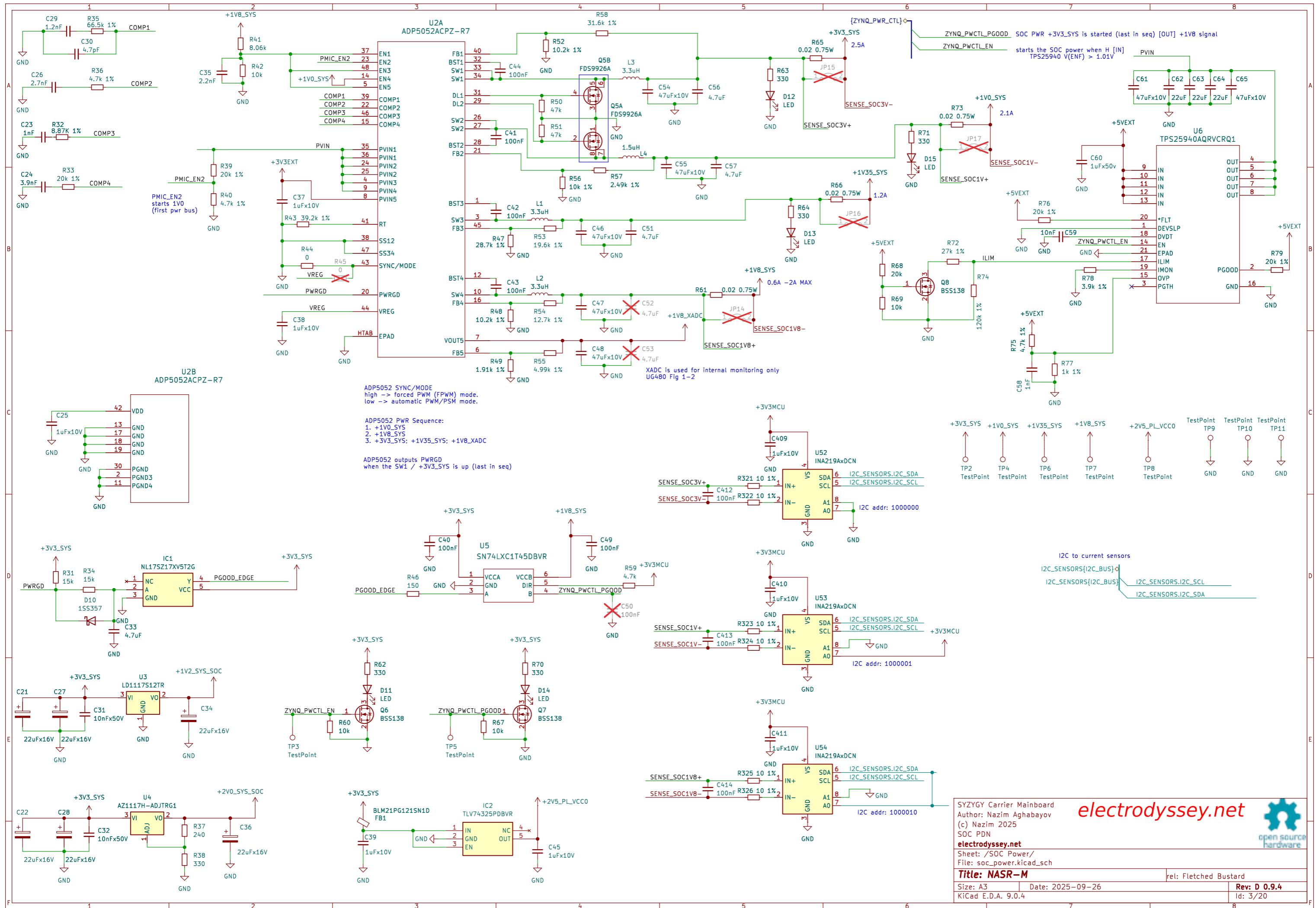
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Size: A3	Date: 2025-09-26
KiCad E.D.A. 9.0.4	Rev: D 0.9.4

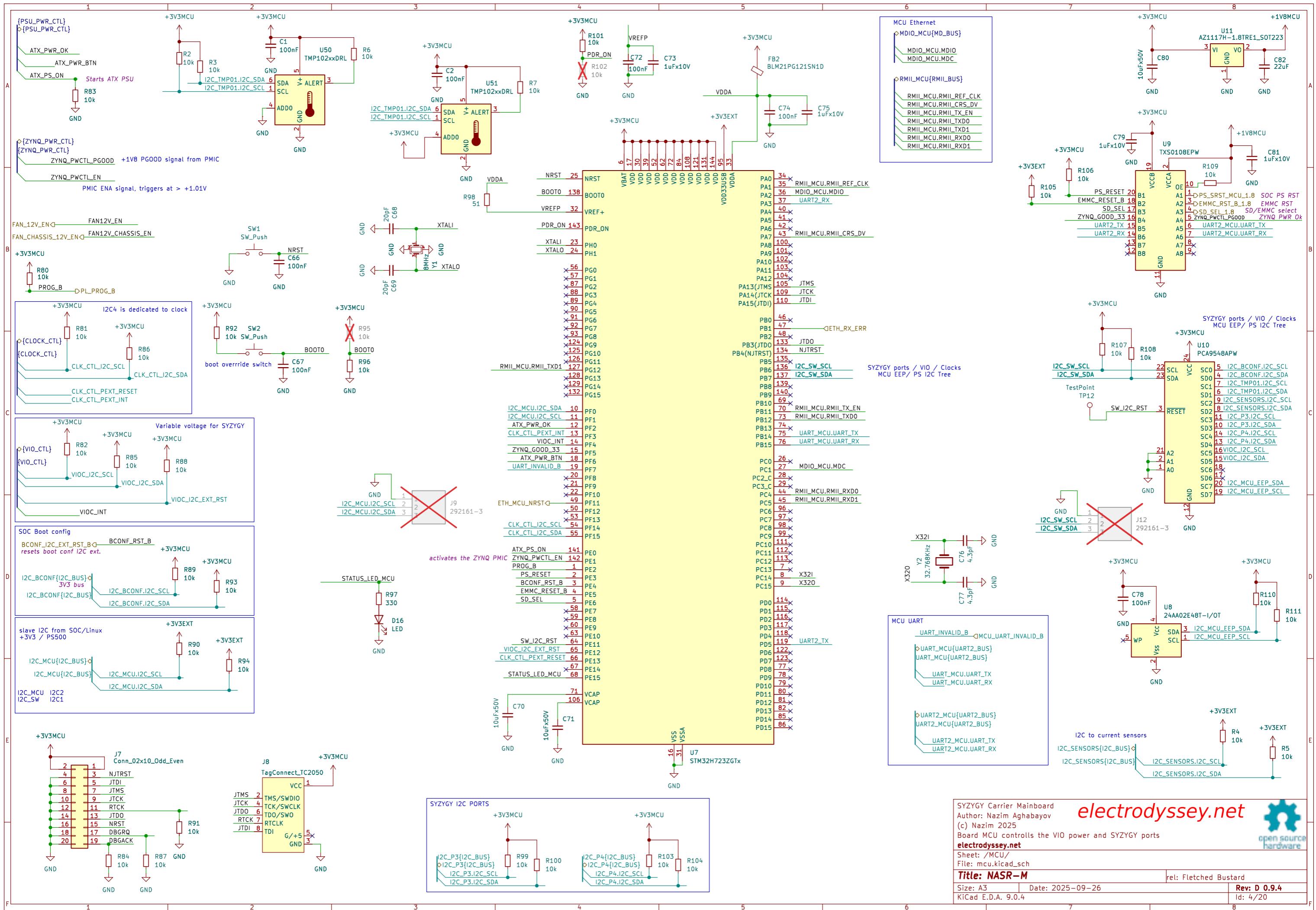
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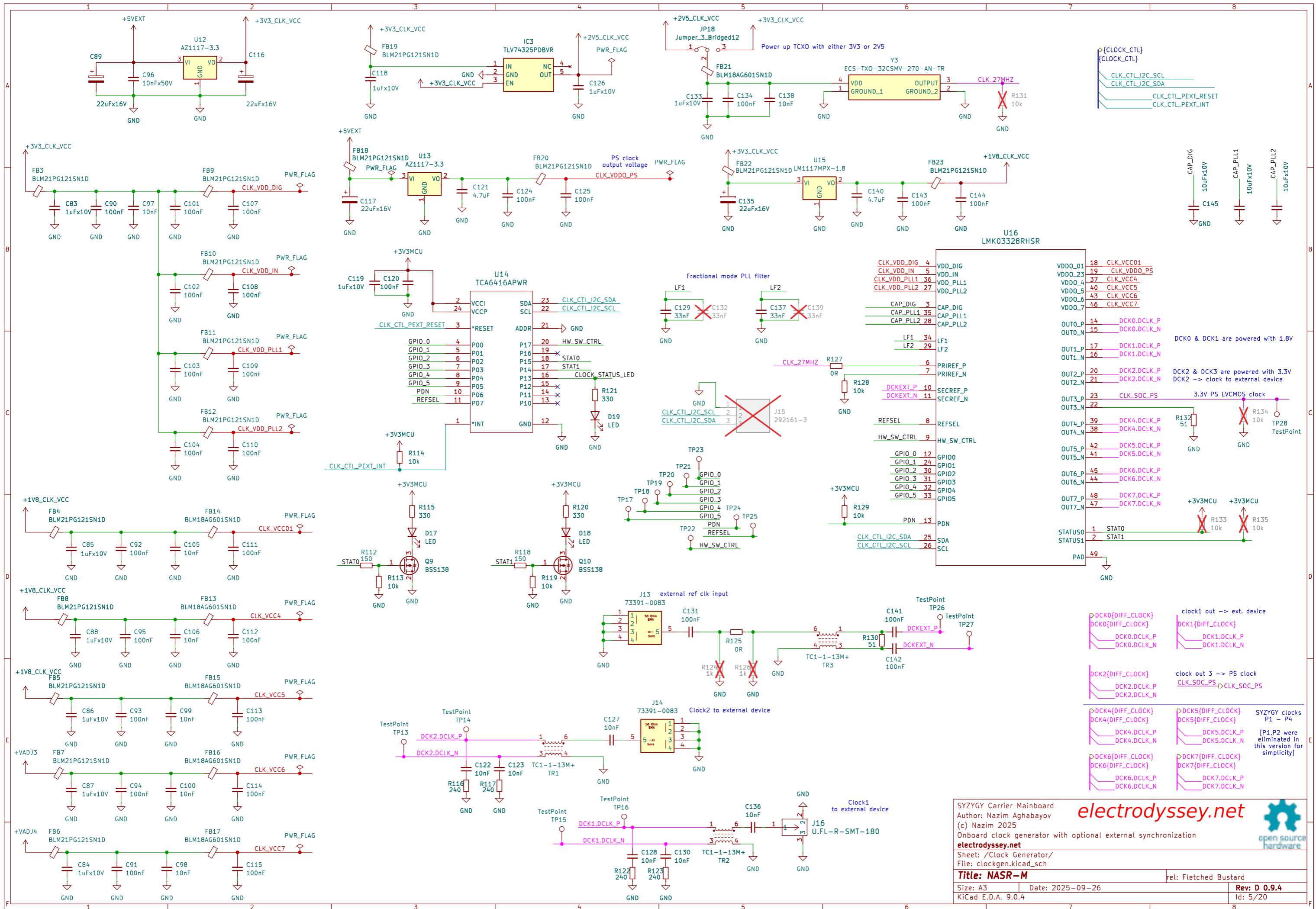




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SYZYGY Carrier Mainboard
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Board MCU controls the VIO power and SYZYGY ports
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Sheet: /MCU/
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Title: NASR-M
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SYZYGY Carrier Mainboard
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Onboard clock generator with optional external synchronization

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File: clockgen.kicad_sch

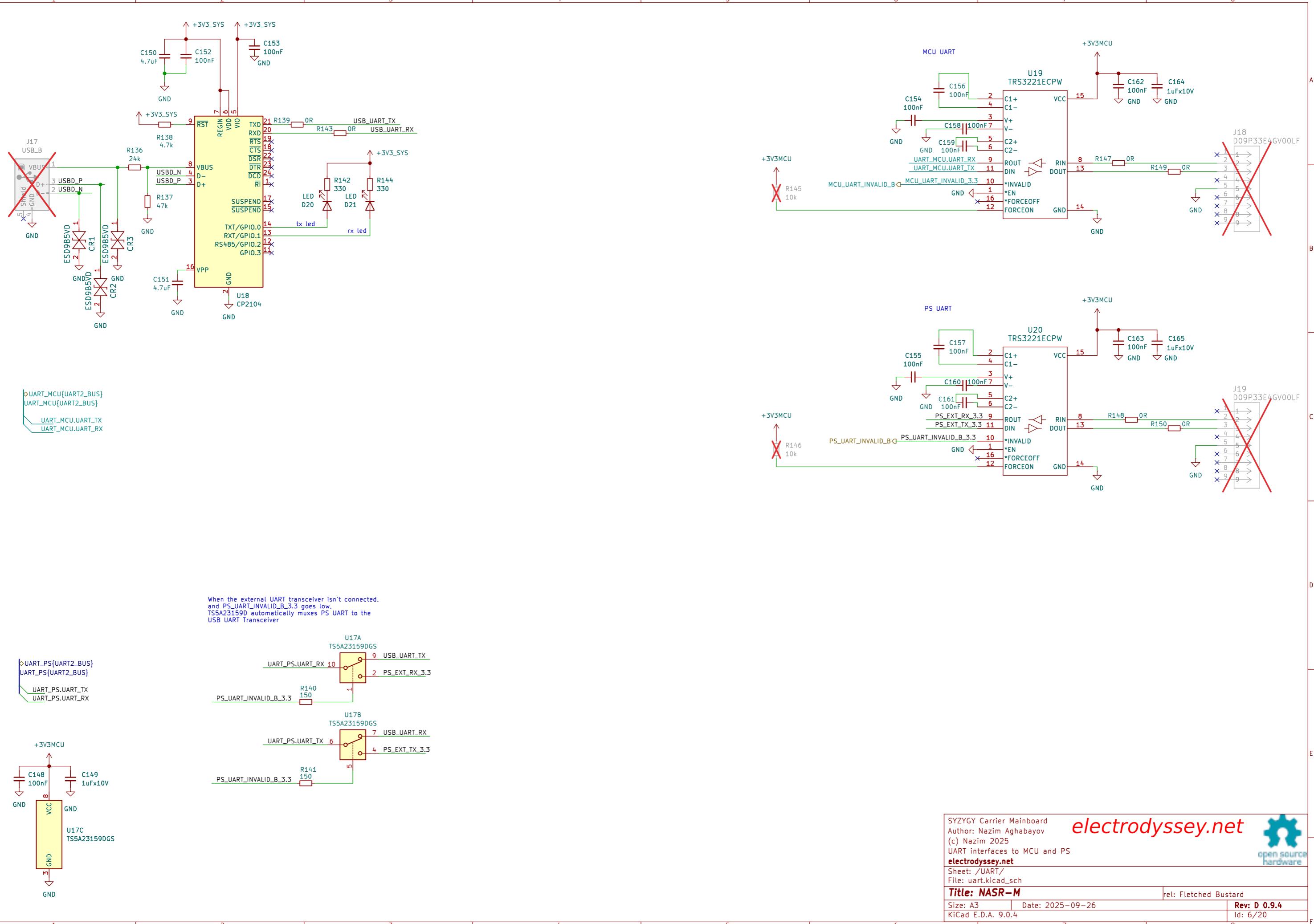
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Size: A3 Date: 2025-09-26

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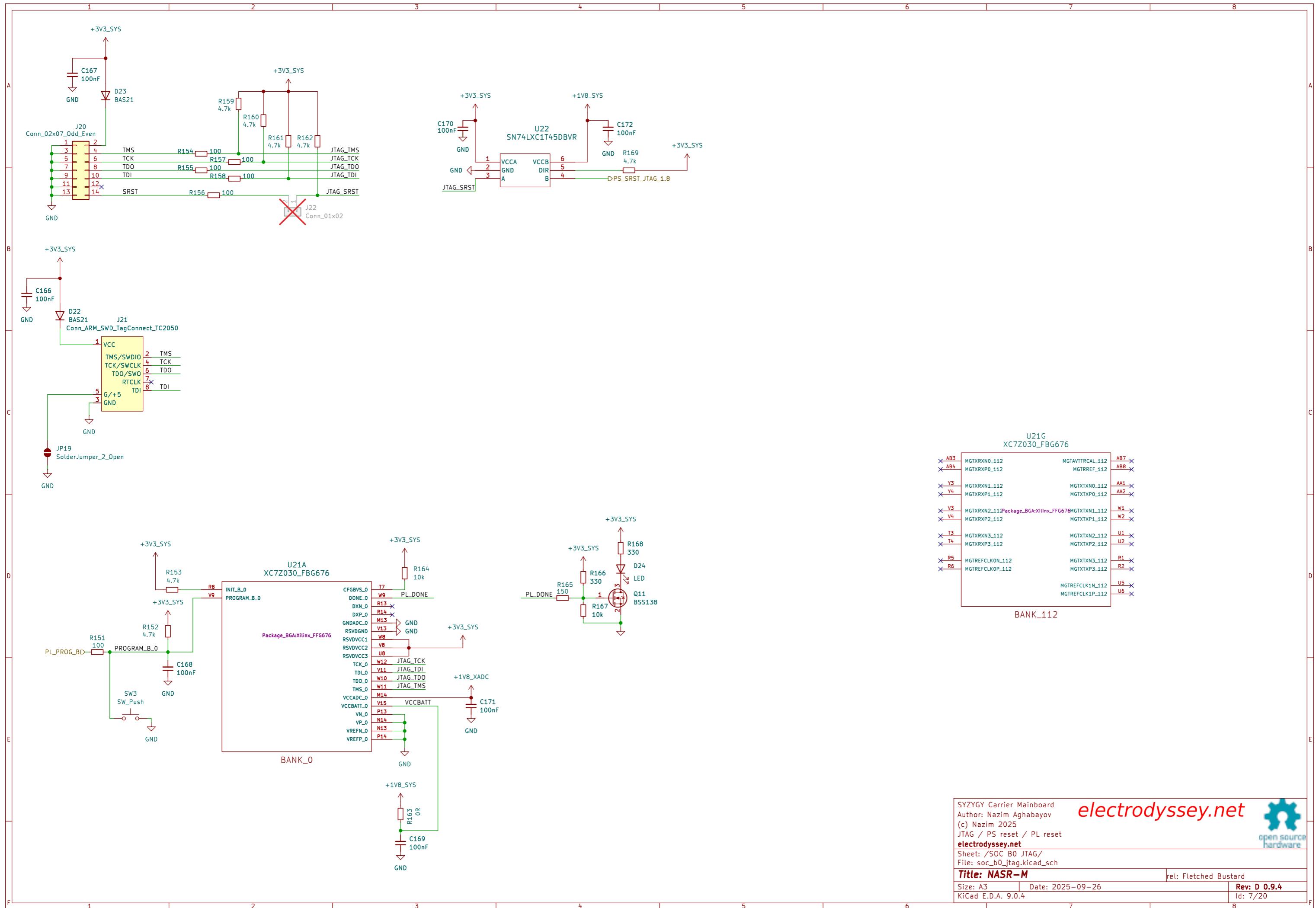
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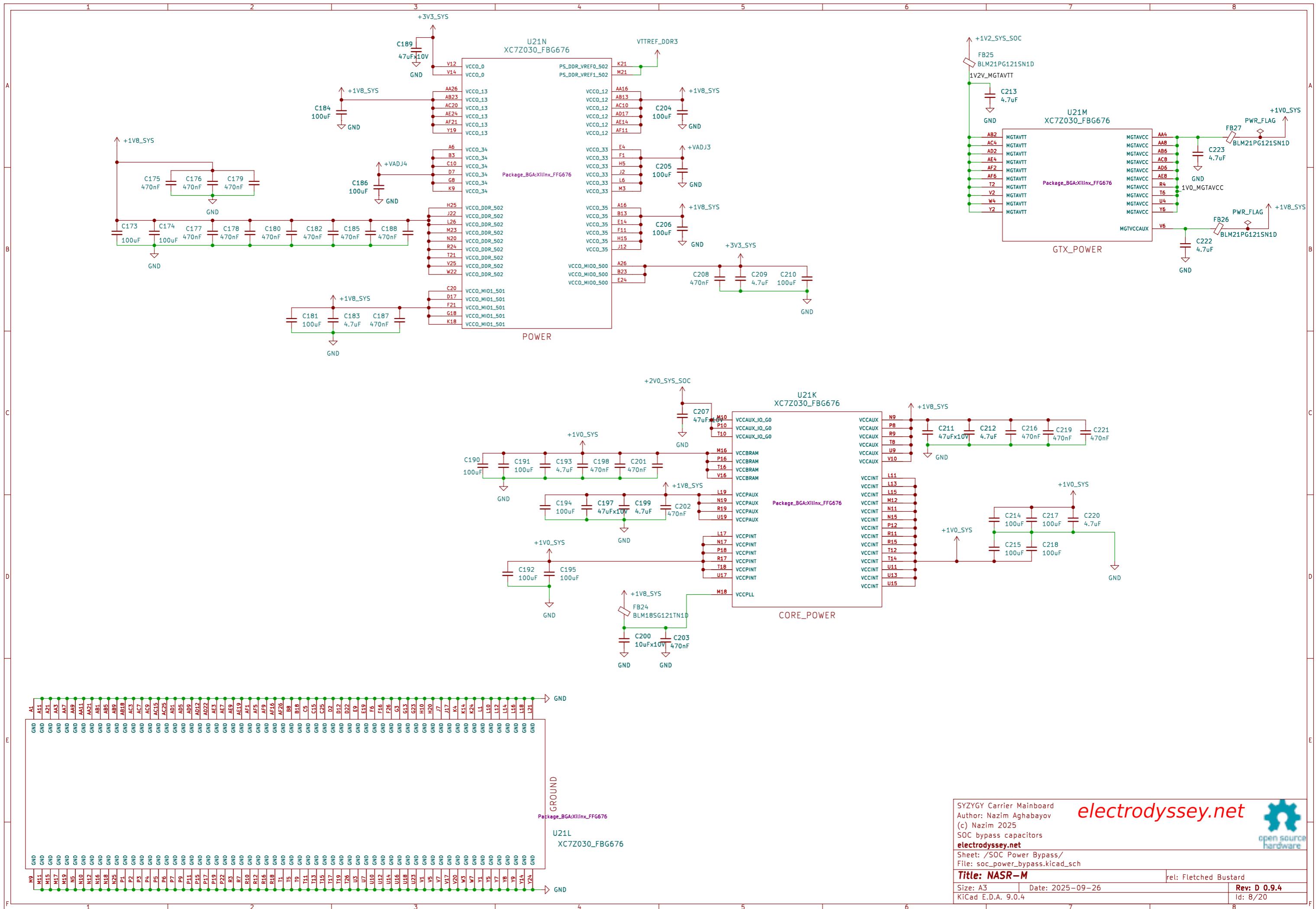
Id: 5/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
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UART interfaces to MCU and PS
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Title: NASR-M
Size: A3 Date: 2025-09-26 Rev: D 0.9.4
KiCad E.D.A. 9.0.4 Id: 6/20







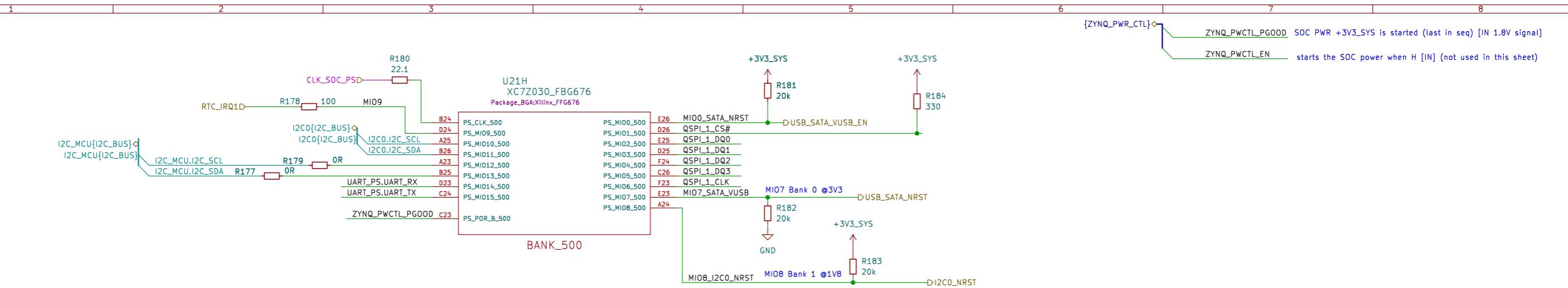
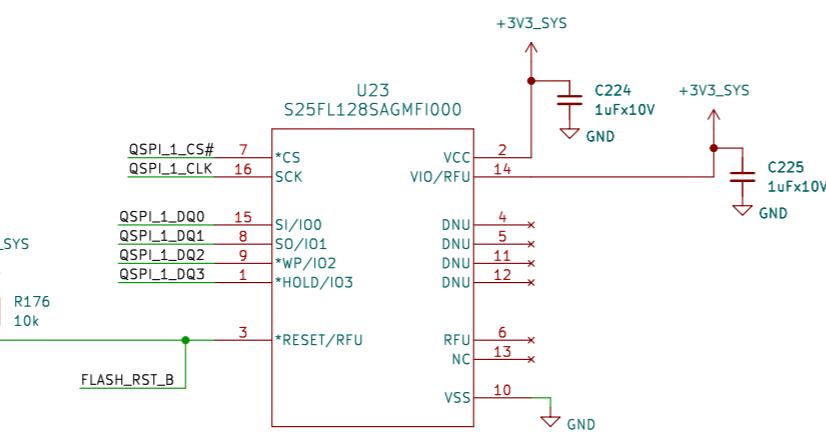


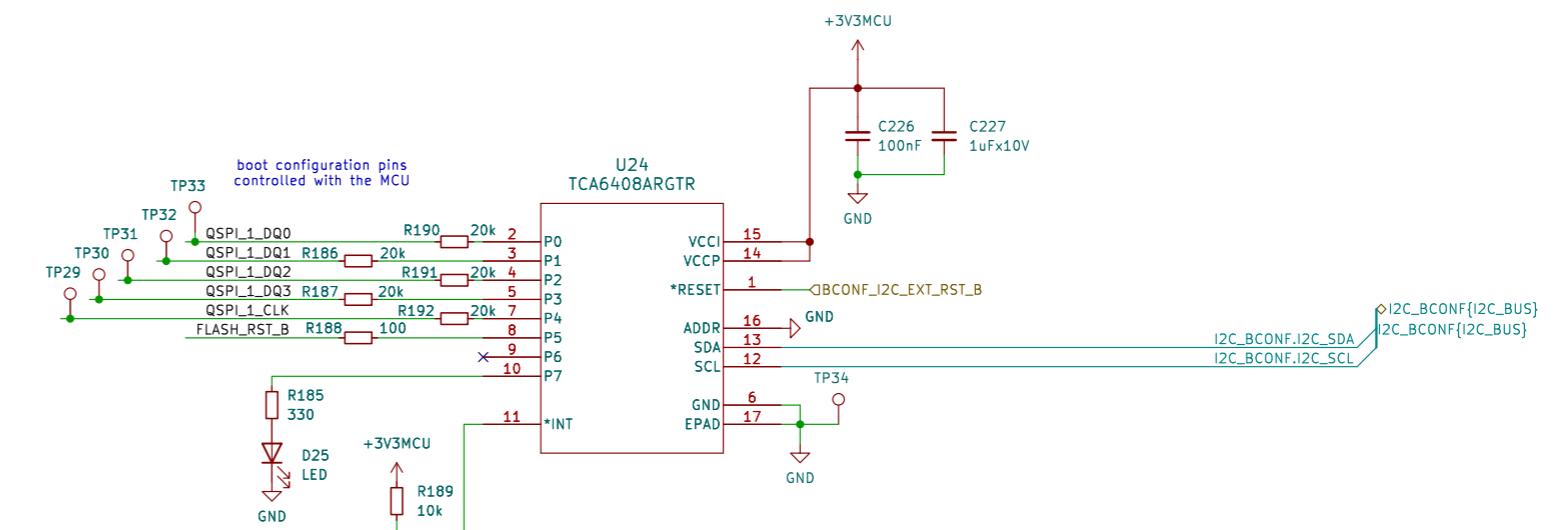
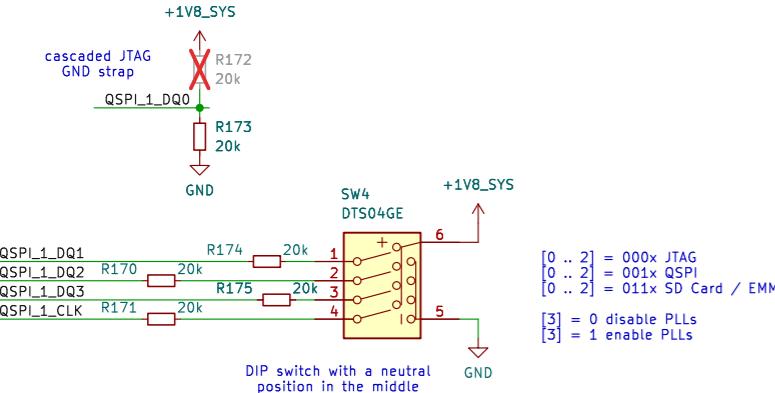
Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]	
	MODE[1]	VNMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]	
Boot Devices								
JTAG Boot Mode; cascaded is most common ^[1]	0	0	0				JTAG Chain Routing ^[2]	
NOR Boot ^[3]	0	0	1				0: Cascade mode 1: Independent mode	
NAND	0	1	0					
Quad-SPI ^[3]	1	0	0					
SD Card	1	1	0					
Mode for all 3 PLLs								
PLL Enabled		0	Hardware waits for PLL to lock, then executes BootROM.					
PLL Bypassed		1	Allows for a wide PS_CLK frequency range.					
MIO Bank Voltage^[4]								
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. 2.5 V, 3.3 V 0 0 1.8 V 1 1					
			Voltage Bank 1 includes MIO pins 16 thru 53.					

Notes:
1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure).
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

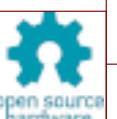


UART_PS(UART2_BUS)
UART_PS(UART2_BUS)
UART_PS.UART_RX
UART_PS.UART_TX

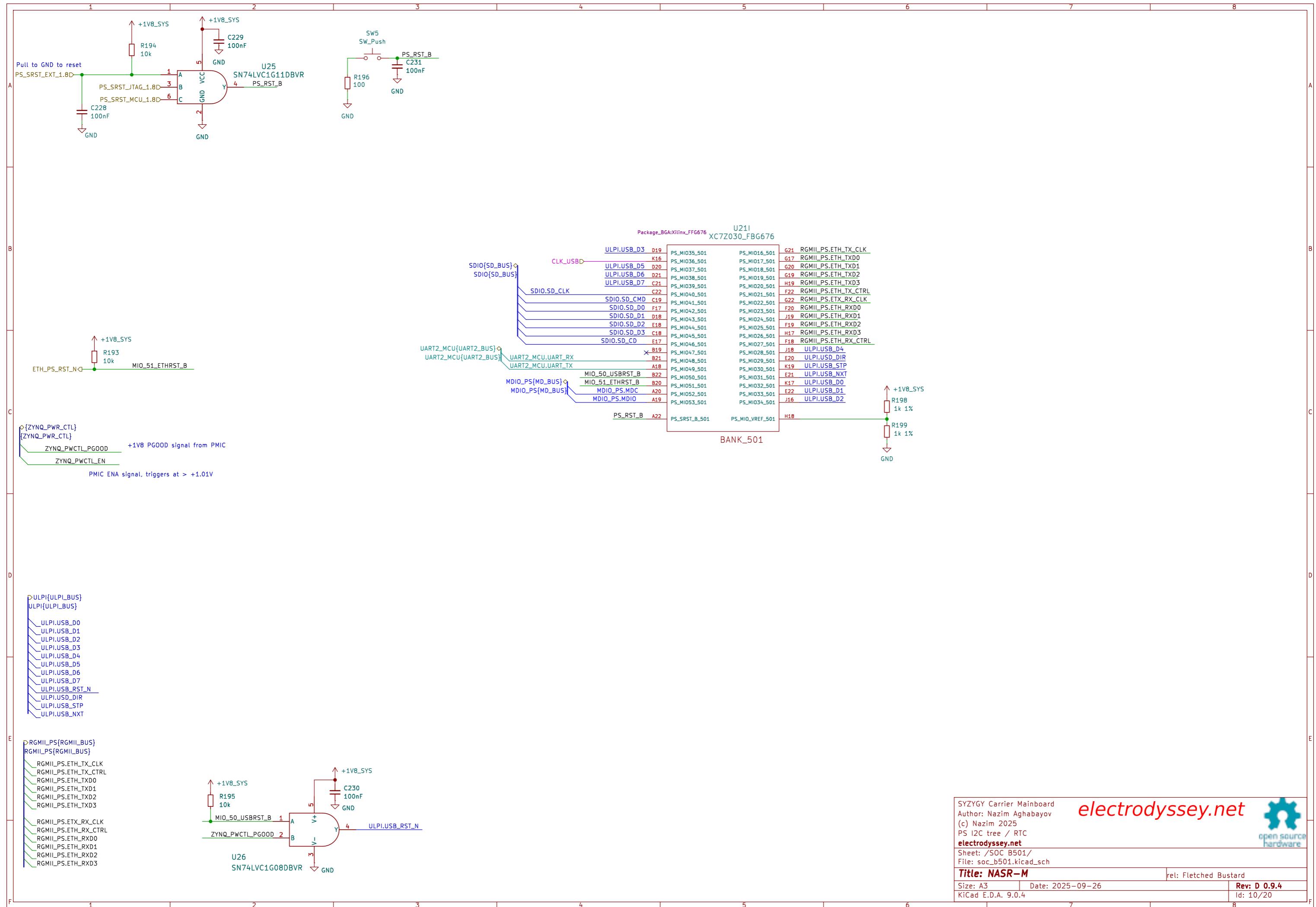


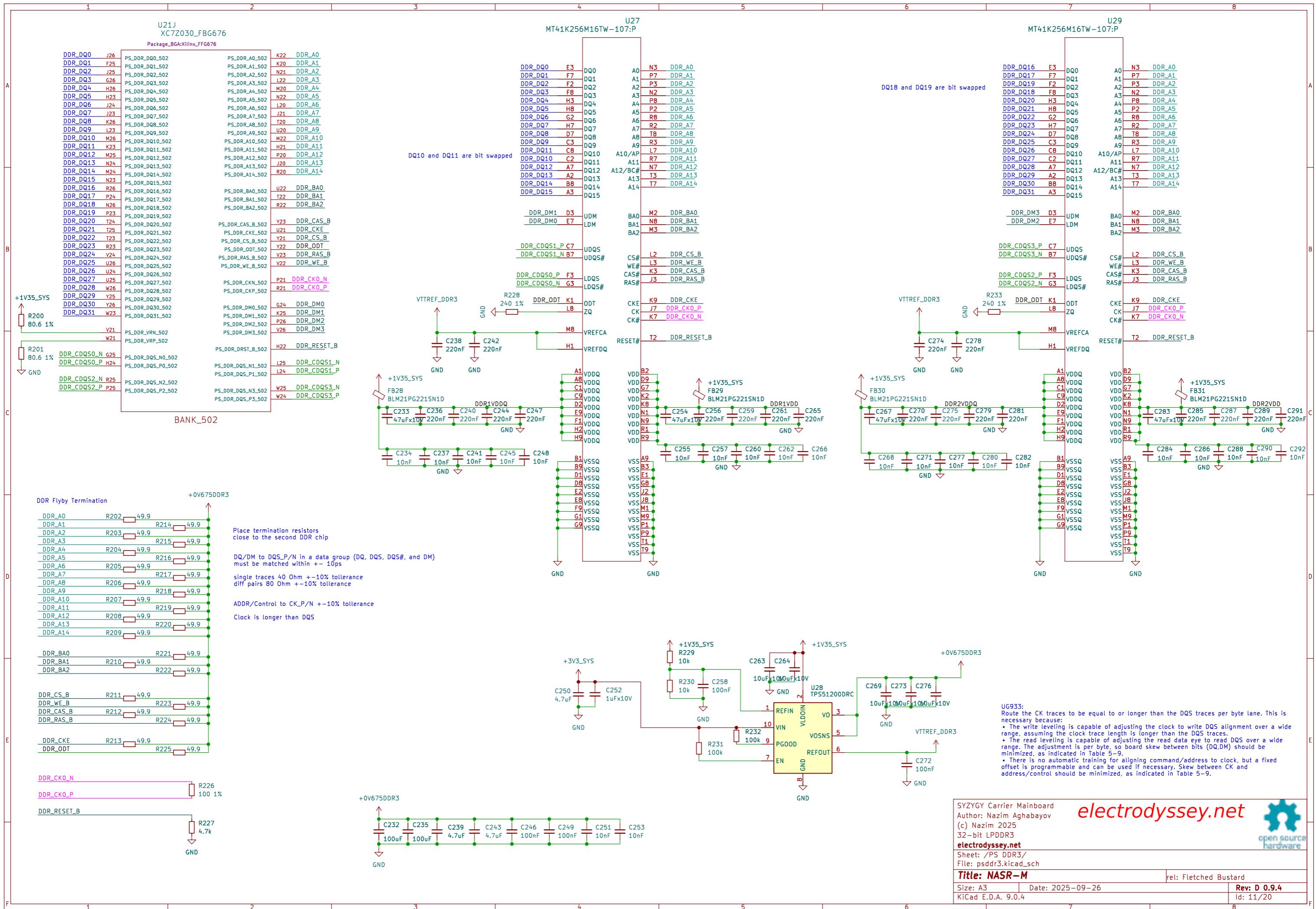
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Author: Nazim Aghabayov
(c) Nazim 2025
Bank 500; QSPI / Boot mode switches / POR
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File: soc_bank500.kicad_sch

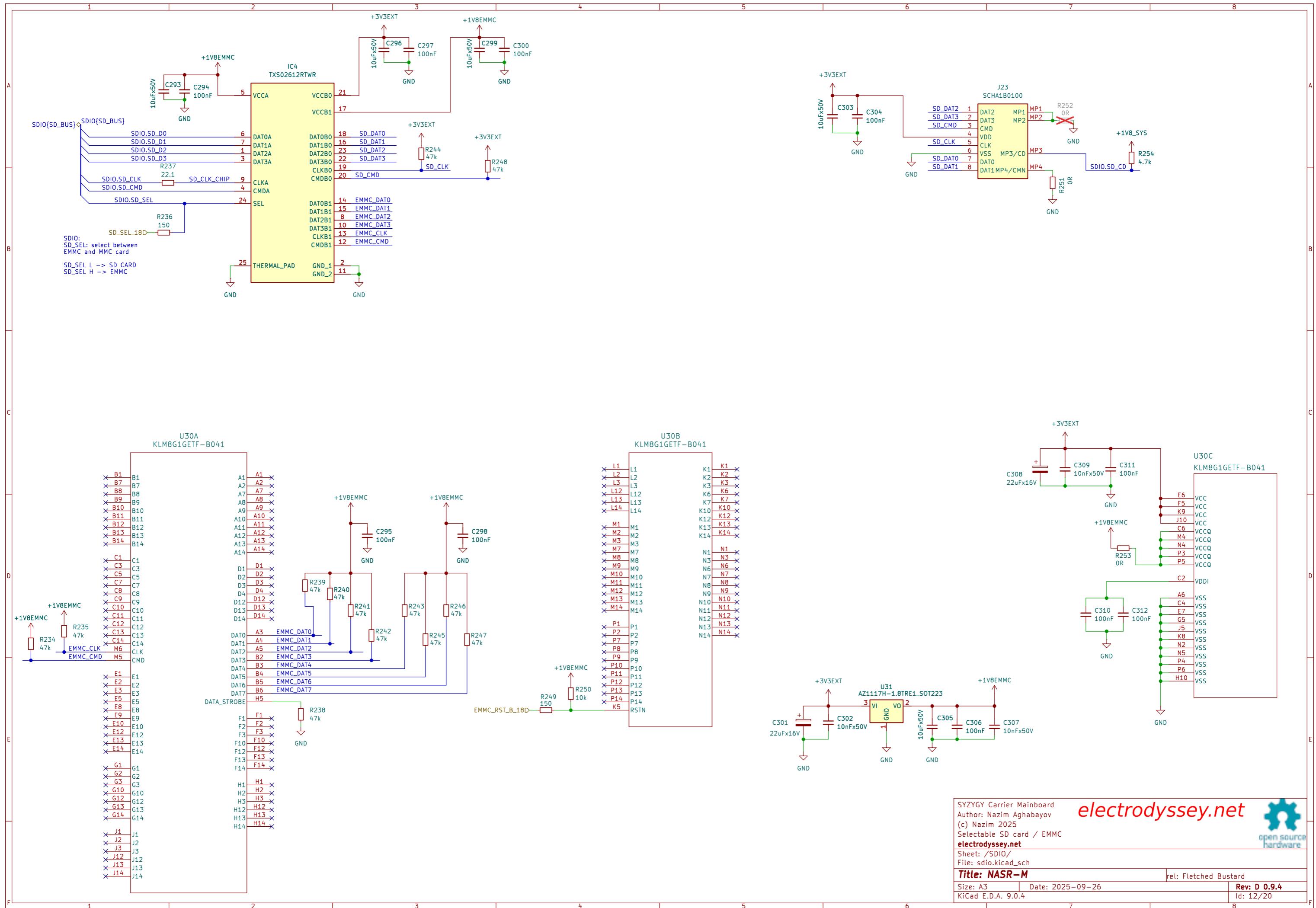
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KiCad E.D.A. 9.0.4	Rev: D 0.9.4

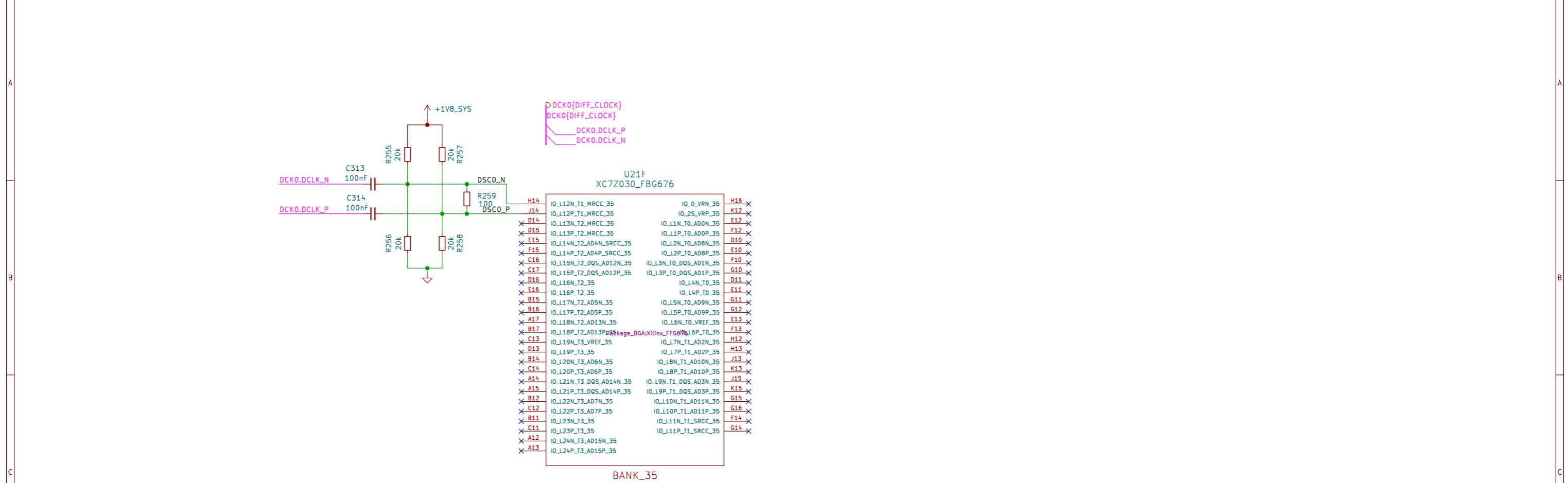


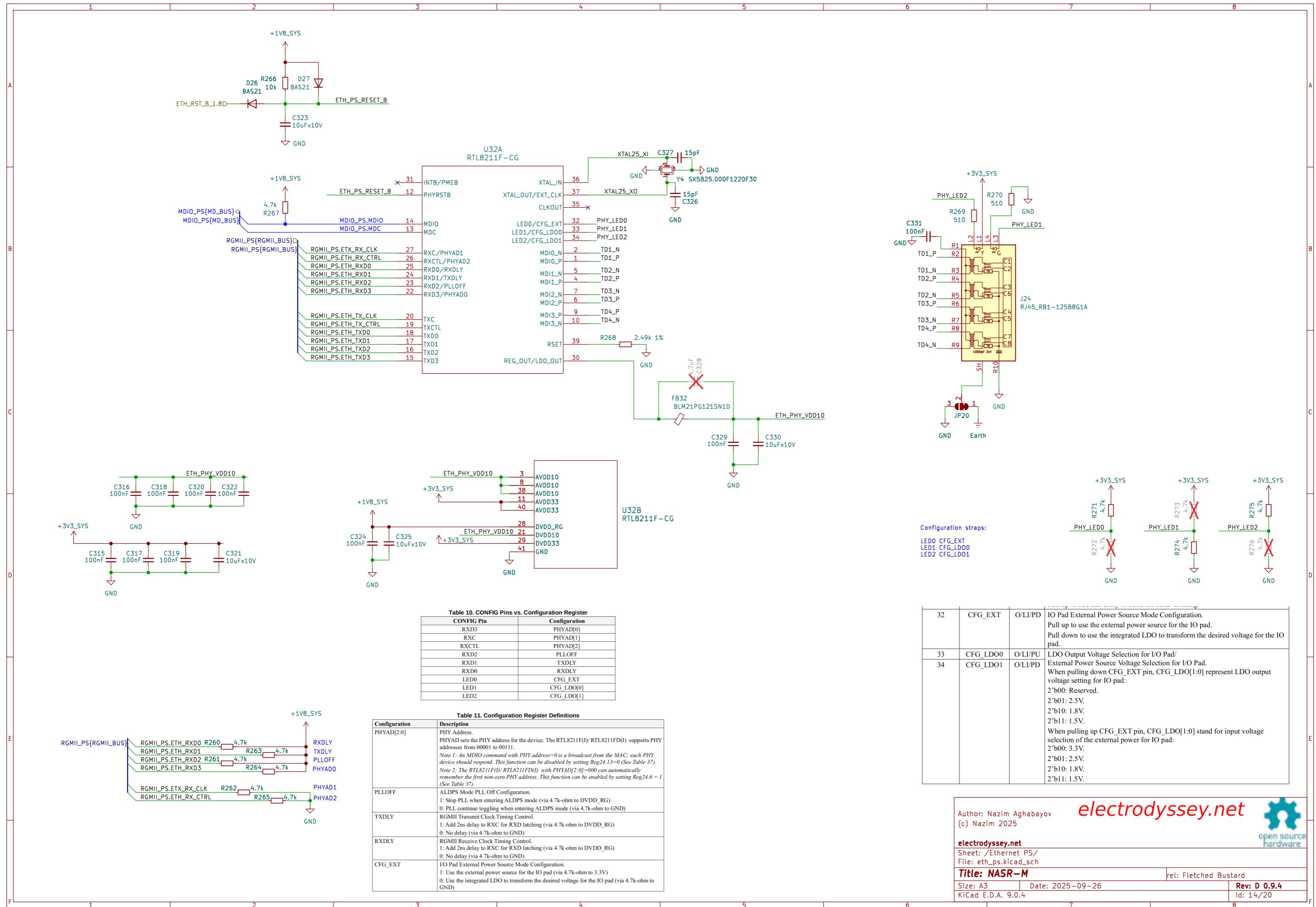
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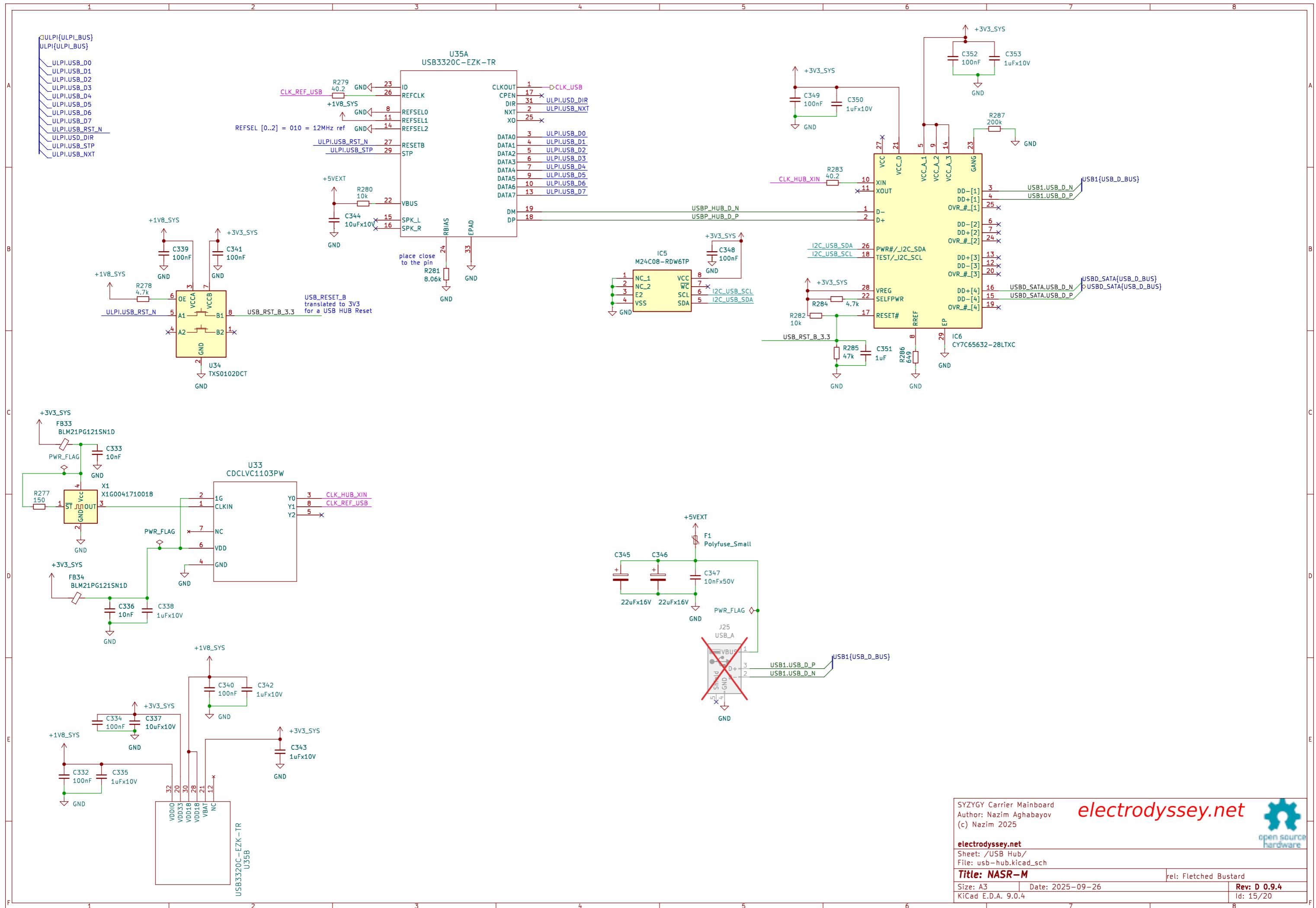
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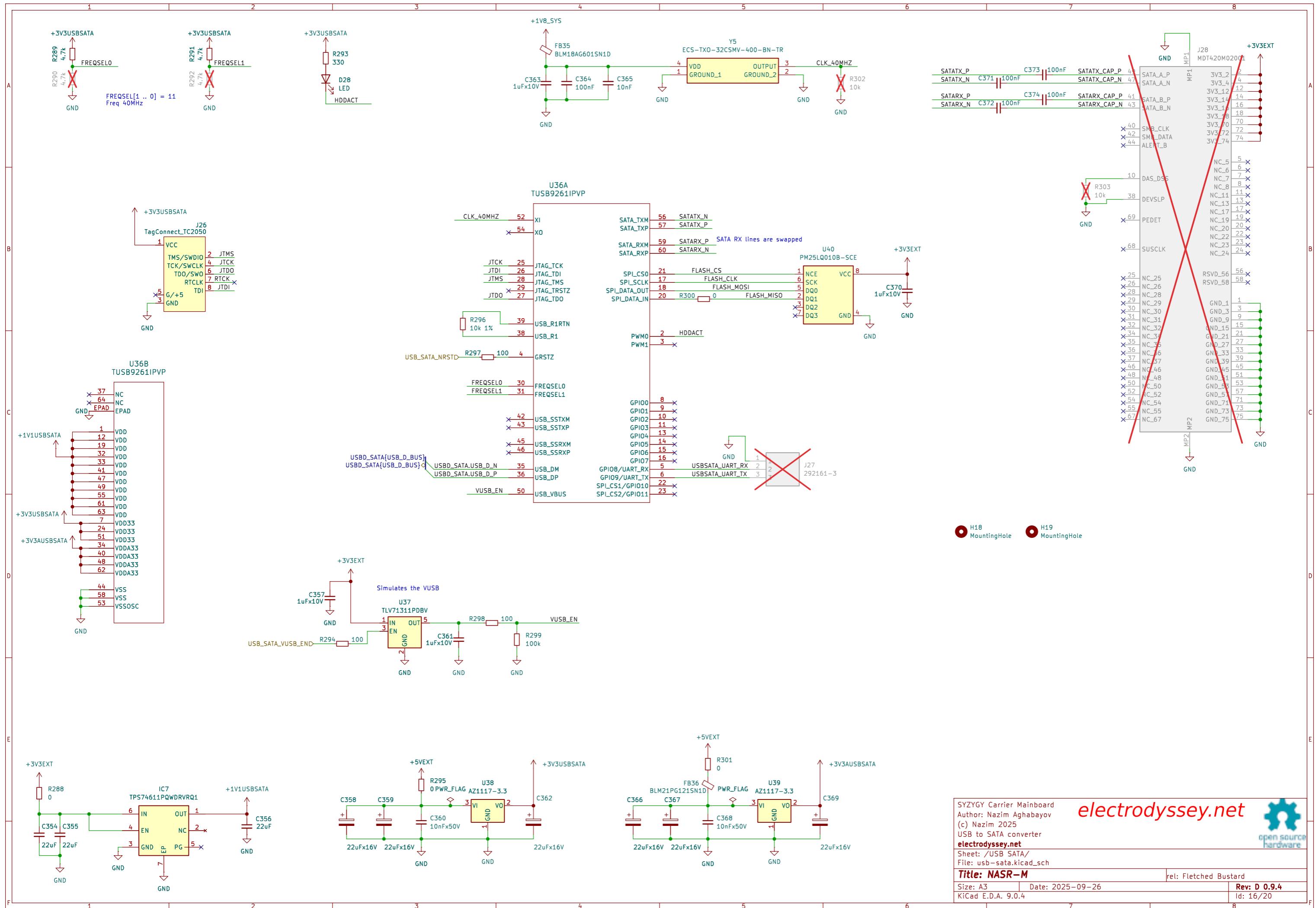
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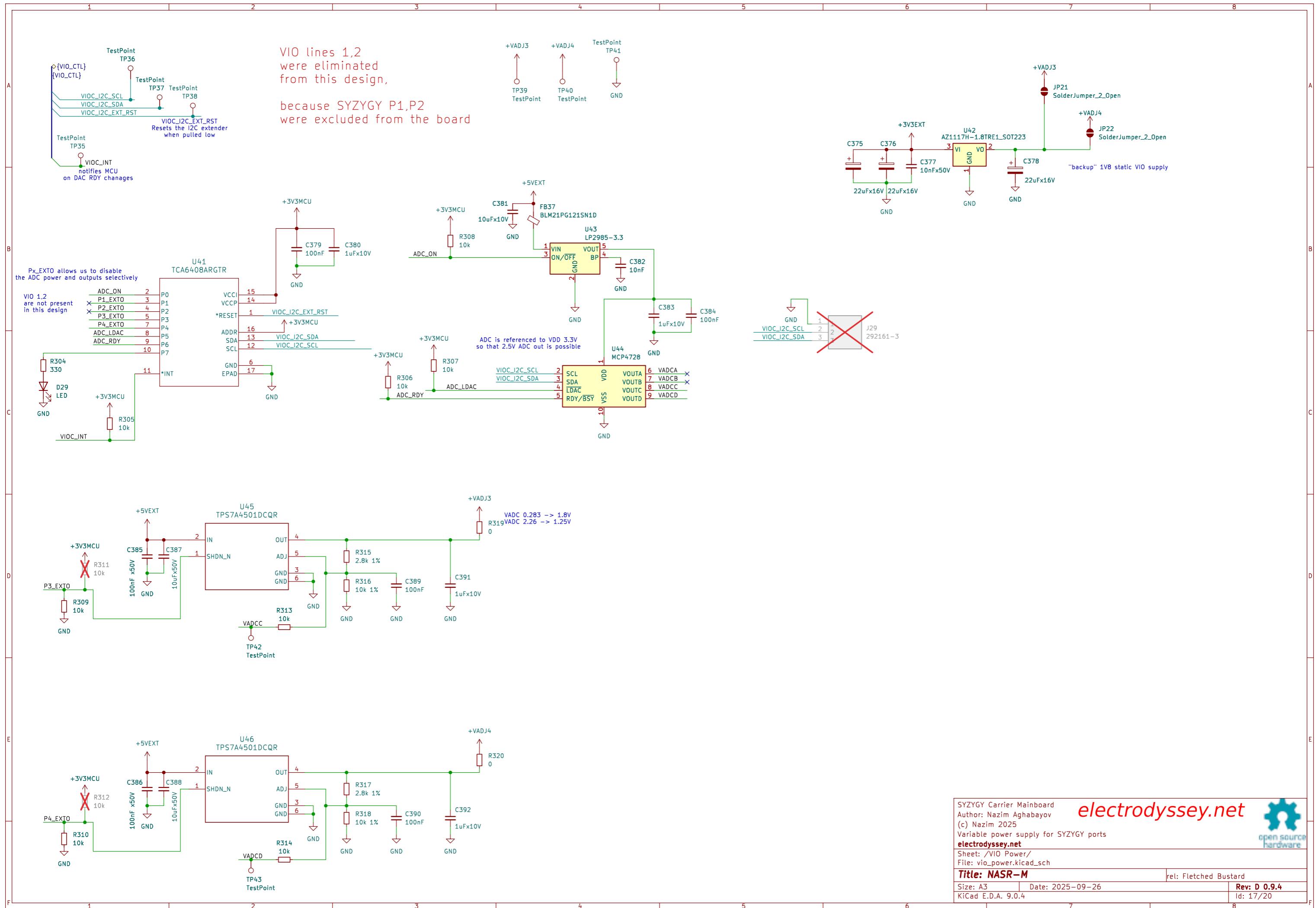


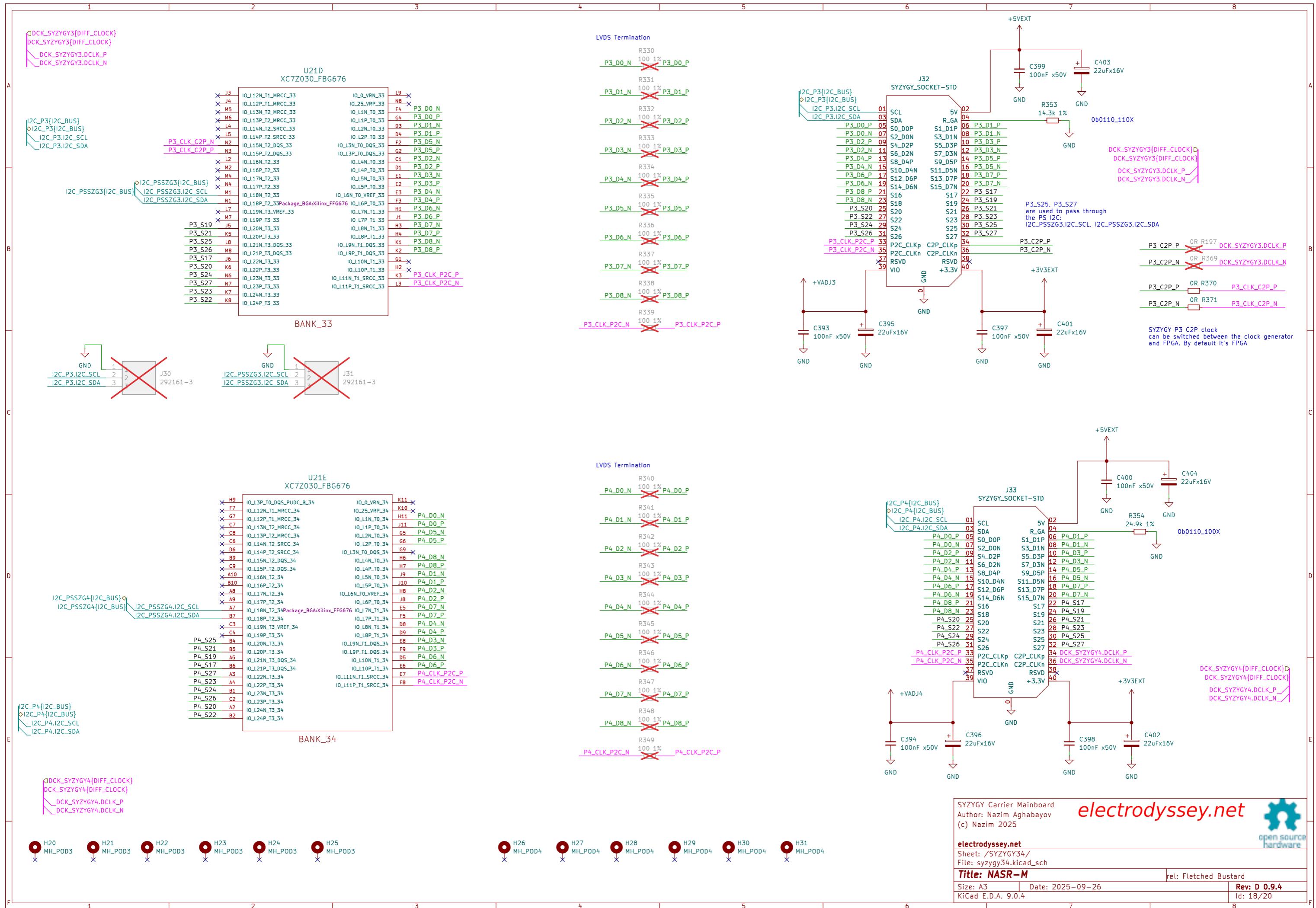
SYZYGY Carrier Mainboard
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USB to SATA converter
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Title: NASR-M		rel: Fletched Bustard
Size: A3	Date: 2025-09-26	Rev: D 0.9.4
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Sheet: /SYZYGY3/

File: syzygy3.kicad_sch

Title: NASR-M

rel: Fletchered Bustard

Size: A3 Date: 2025-09-26

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Rev: D 0.9.4

Id: 18/20

