

USB332x Family Silicon Errata and Data Sheet Clarification

This document describes known anomalies for all functional revisions of the USB332x device.

TABLE 1: SILICON ISSUE SUMMARY

Hardware Functional Rev A	Hardware Functional Rev B	Hardware Functional Rev C	Description
X	X		Module 1 : “VDD1.8 Current in Suspend Mode”
X	X		Module 2 : “ULPI Clock In Mode”
X	X	X	Module 3 : “RID Converter Cannot Detect 440K Resistor”
X	X	X	Module 4 : “Intermittent Loss of USB Link in OMAP4 Host Applications”

Legend: X = Applicable to the Functional Rev.

Silicon Errata Issue

Module 1: VDD1.8 Current in Suspend Mode

Description

The VBAT (VDD3.3) pin may draw up to 1.3mA of current from the VBAT source when all of the following conditions apply:

1. The VDD1.8 supply is removed.
2. The VBAT supply is ON.

In this mode the VBAT (VDD3.3) pin should draw $\leq 25 \mu\text{A}$.

Table 2 details which USB332x power combination modes are affected by this anomaly:

TABLE 2: THREE RAIL POWER COMBINATIONS

Power Combo	VBUS	VBAT/ VDD3.3	VDD1.8	Note	Affected by Anomaly
1	OFF	OFF	OFF	PHY is off	NO
2	ON	OFF	OFF	PHY is off, USB cable connected. VBUS current will be approximately $1 \mu\text{A}$.	NO
3	OFF	OFF	ON	ULPI registers can be read and maintain their contents as long as the RESETB pin is held high. The PHY can be placed in low power mode via the ULPI interface.	NO
4	ON	OFF	ON	Same as line 3 above, but the USB cable connection has been made. VBUS current will be approximately $1 \mu\text{A}$.	NO
5	OFF	ON	ON	Normal operating mode of the PHY when a USB cable connection is not made.	NO
6	ON	ON	ON	Normal operating mode of the PHY.	NO
7	OFF	ON	OFF	ULPI interface not functional.	YES
8	ON	ON	OFF	ULPI interface not functional.	YES

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For power combinations where VBUS, VBAT, and VDD3.3 turn on together, [Table 3](#) details the modes affected by this anomaly:

TABLE 3: TWO RAIL POWER COMBINATIONS

Power Combo	VBUS, VBAT, VDD3.3	VDD1.8	Note	Affected by Anomaly
1	OFF	OFF	PHY is off.	NO
2	OFF	ON	ULPI registers can be read and maintain their contents as long as the RESETB pin is held high. The PHY can be placed in low power mode via the ULPI interface.	NO
3	ON	ON	Normal operating mode of the PHY.	NO
4	ON	OFF	ULPI interface not functional.	YES

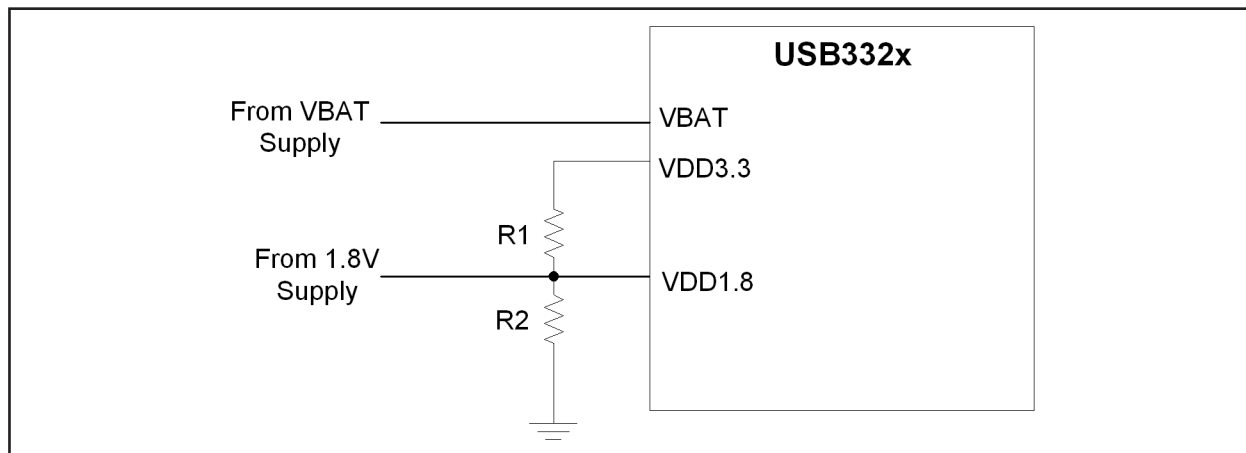
End User Implications

Removing supply voltage from both VBAT and VDD1.8 produces a leakage current of 0 μ A. If the customer elects to leave VBAT on while VDD1.8V is off, the USB332x may exhibit increased current draw (>25 μ A) from the VBAT (VDD3.3) supply when in Suspend Mode. USB functionality is not affected

Solution

- Leave the VDD1.8 supply ON whenever voltage is applied to VBAT. Standby current will be $\leq 25 \mu$ A.
- Supply voltage on VBAT from a PMIC and switch it off whenever VDD1.8 is switched off. Standby current will be 0 μ A.
- Add a LDO regulator with enable between VBAT and the battery which can be switched off whenever VDD1.8 is switched off. Standby current will be 0 μ A.
- Add a resistor divider between VDD3.3 and VDD1.8 supplies, as shown in [Figure 1](#):

FIGURE 1: RESISTOR DIVIDER CIRCUIT



Where:

R1 = 210 k Ω 1%

R2 = 309 k Ω 1%

Note: If there are other devices attached to the 1.8V on the customer platform, those device impedances need to be taken into account.

Standby current will be $\leq 30 \mu$ A.

Plan

This anomaly has been fixed in functional revision C devices and newer devices.

Module 2: ULPI Clock In Mode

Description

When using the USB332x with a 60 MHz input clock, the ULPI interface timing does not meet the ULPI specification. This only affects ULPI Clock In Mode. ULPI Clock Out Mode is not affected.

Table 4 details the various ULPI Clock In Mode timing parameters.

TABLE 4: ULPI CLOCK IN MODE TIMING

Parameter	Symbol	Condition	Min	Max	Units
Setup Time (STP, data in)	TSC, TSD	60 MHz REFCLK	-0.5		ns
Hold Time (STP data in)	THC, THD	60 MHz REFCLK	-2.5		ns
Output Delay (control out, 8-bit data out)	TDC, TDD	60 MHz REFCLK	3.0	8.0	ns

End User Implications

Click In Mode applications must be checked to ensure that the link supports this timing.

Solution

The link may be able to adjust the phase of the 60 MHz ULPI clock to optimize the timing between the link and the transceiver.

Plan

This anomaly has been fixed in functional revision C devices and newer devices.

Module 3: RID Converter Cannot Detect 440K Resistor

Description

The RID Converter does not reliably detect a 440K resistor. An "ID Floating" condition may be reported to the Vendor RID Conversion register and the Carkit Interrupt Status register.

End User Implications

The USB332x will not reliably discern the difference between a 440K ohm resistor on the ID pin and a floating ID pin. Other RID converter conversion values are still functional and their operation is not affected.

Solution

None.

Plan

This will not be addressed in a future revision of the device.

Module 4: Intermittent Loss of USB Link in OMAP4 Host Applications

Description

This anomaly may apply to any host USB link when ALL of the following conditions apply:

1. The USB332x is connected to a USB Host (EHCI or OTG controller) via ULPI and operates as a USB Host Transceiver.
2. The USB332x is moved from High Speed configuration to Full Speed by removing the HS terminations and the SuspendM == 1.

In some applications where the Texas Instruments OMAP4 is the USB Host and connects to the USB332x via ULPI, the OMAP4 can periodically lose the connection with the downstream device when attempting to suspend the USB connection. The root cause of this is that the OMAP EHCI controller can lock up when entering USB Suspend, even if the OMAP properly puts the USB332x into Low Power Mode. In the ULPI suspend signaling definition in the ULPI specification and in the majority of SoC's, the command to suspend the USB Transceiver and the command to change to the USB Transceiver's Full Speed receivers arrives in a single register command. The OMAP4 places a delay (3ms) between these commands because the OMAP4 is waiting for the downstream USB device to assert its 1.5K pull-up on DP (indicating that the downstream device is in USB suspend). During this 3ms delay, noise on the DP and DM USB signals can cause a significant number of RX CMDs and Receive data packets to be transmitted by the USB332x. As a result, the OMAP EHCI controller may miss the status update required to initiate the command to put the PHY into low power mode and place the OMAP4 EHCI controller into the USB Suspend state.

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In the OMAP EHCI controller, the Suspend bit becomes '0' by writing to the Resume bit, waiting for >20ms, and then clearing the Resume bit to stop Resume signaling on bus. If the bus has resumed into HS-IDLE mode, then the Suspend bit will be automatically cleared. Under the conditions of this anomaly, the Resume Bit does not clear at all - it remains stuck at value '1'. This behavior is the signature of this anomaly.

End User Implications

The customer's application will not be able to recover from USB Suspend and will lose communication with the downstream USB device.

Solution

1. The host SoC should command the USB332x to enable Full Speed Transceivers and enter Low Power Mode with a single command (TX CMD = 0x05h). Do not split these two steps into separate TX CMDs. The downstream USB device will always enter USB suspend when this work around is used.
2. If port resume bit on the EHCI port is not cleared in the OMAP upon attempted entry to USB suspend, then the OMAP EHCI controller failed to enter suspend. If the USB331x was suspended successfully (clearing the SuspendM bit in the Function Control Register), then the OMAP must assert either:
 - STP to bring the USB332x out of Low Power Mode or:
 - Toggle RESETB on the USB332x to restart the USB332x
3. To reduce USB noise during the undefined state prior to entering Low Power Mode, assert the ChargerPullupEnableDP or ChargerPullupEnableDM bits. Only assert one of these two bits. In applications with very low noise on USB signals DP and DM, this can provide a robust workaround to this anomaly:
 - **ChargerPullupEnDP/DM (Bits 4 and 5 of register 39h)** - These bits connect a 125k pull up resistor to the 3.3V supply of the PHY, or inject ~20uA of current onto the desired pin.

Plan

This will not be addressed in a future revision of the device.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
Rev A (April 2015)		Initial release

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