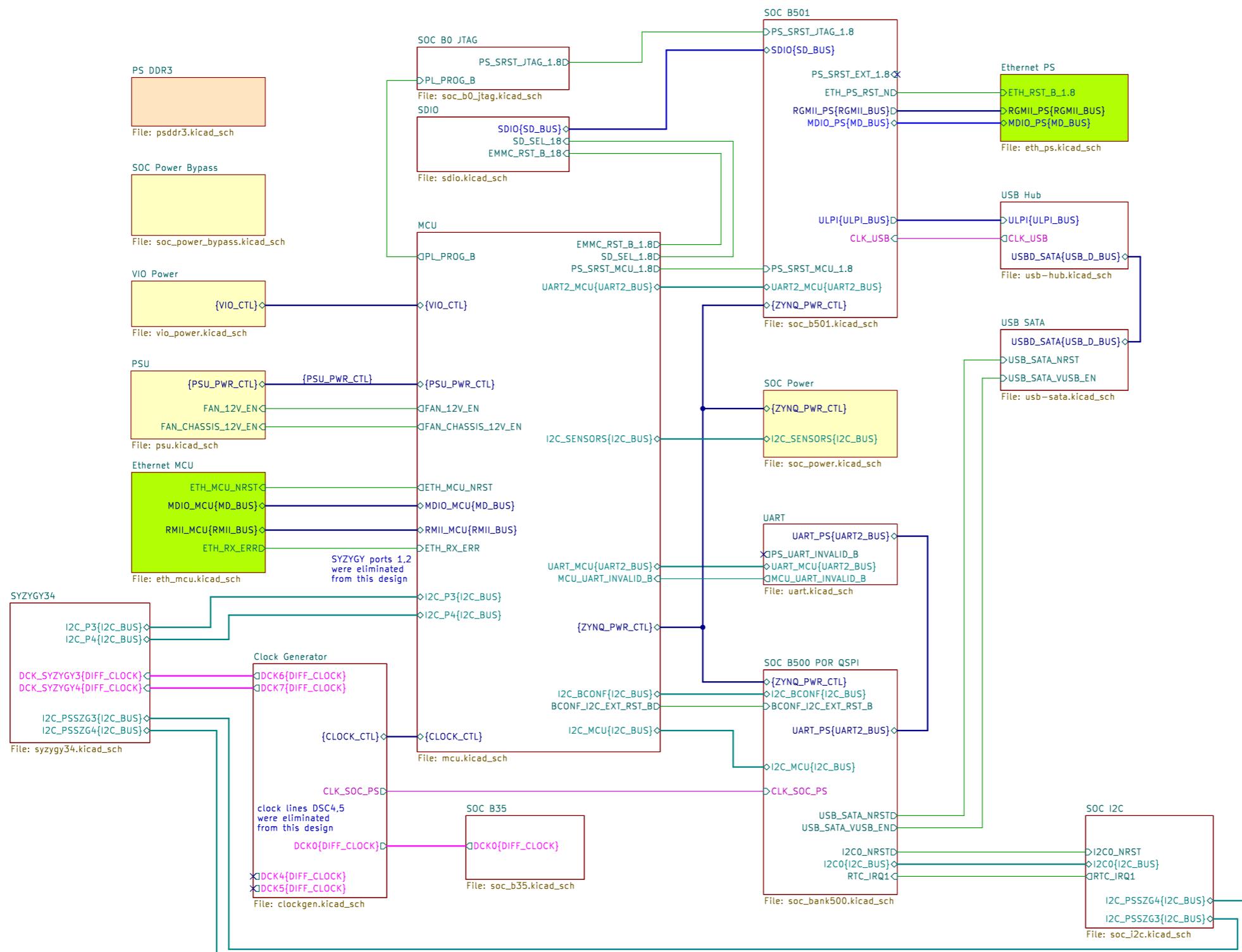


PAGE	DESCRIPTION
1 ROOT PAGE	Block Diagram of the project
2 PSU	ATX PSU connector and filters
3 SOC Power	A secondary power supply for SOC
4 MCU	MCU
5 Clock Generator	Clocks for SOC and SYZYGY, external master sync
6 UART	UART peripherals
7 SOC_B0_JTAG	SOC JTAG
8 SOC Power Bypass	SOC bypass capacitors
9 SOC_B500 POR QSPI	Power on reset, QSPI, SOC boot config
10 SOC_B501	Peripheral resets, ULPi and RGMII buses
11 PS DDR3	DDR3 RAM for SOC PS subsystem
12 SDIO	SDIO and EMMC shared bus
13 SOC_B35	A redundant clock for SOC PS
14 Ethernet PS	RGMII Ethernet peripheral
15 USB Hub	USB, ULPi transceiver and hub
16 USB SATA	USB SATA converter and SATA SSD socket
17 VIO Power	Variable IO power for SYZYGY slots
18 SYZYGY34	SYZYGY slots
19 SOC_I2C	SOC I2C
20 Ethernet MCU	10/100 RMII Ethernet for MCU



NOTE:  
SYZYGY ports 1,2  
were eliminated  
from this design

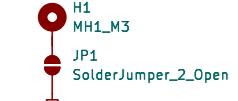
Stackup JLC10161H-2116(1.57mm±10%)  
F\_Cu, B\_Cu:  
diff 800hm track / spacing: 8.28/6 mil; 0.2103/0.1524 mm  
single 400hm: 11.23 mil; 0.2852 mm  
diff 1000hm track / spacing: 5.58/8 mil; 0.1417/0.2032 mm  
single 500hm: 7.36mil; 0.1869 mm  
-----  
In3, In5, In7 internal layers:  
diff 800hm: 6.44/8 mil; 0.1636/0.2032 mm  
single 400hm: 7.03mil; 0.1786 mm  
diff 1000hm: 4.29/11 mil; 0.1090/0.2794 mm  
single 500hm: 4.54mil; 0.1153 mm

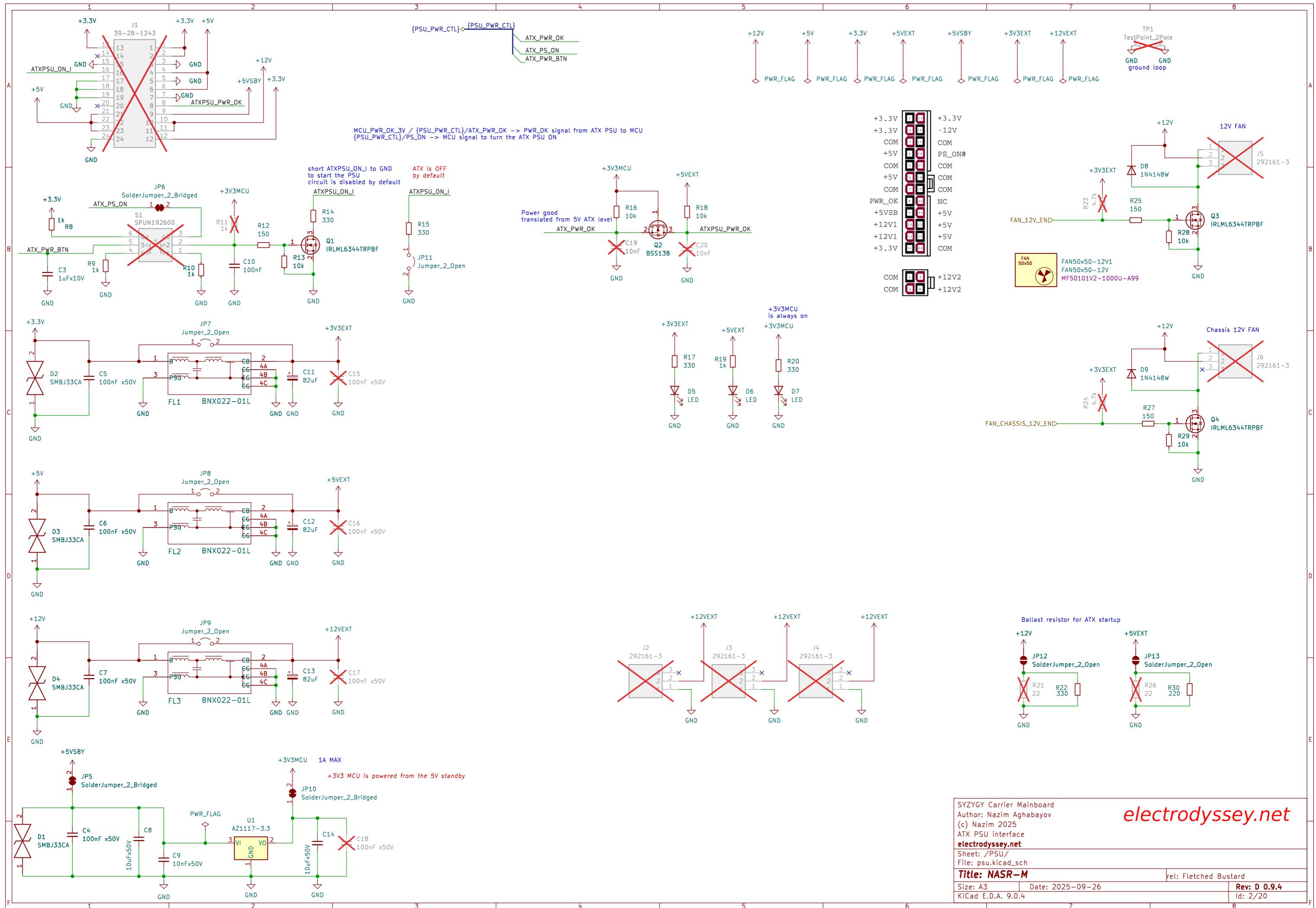


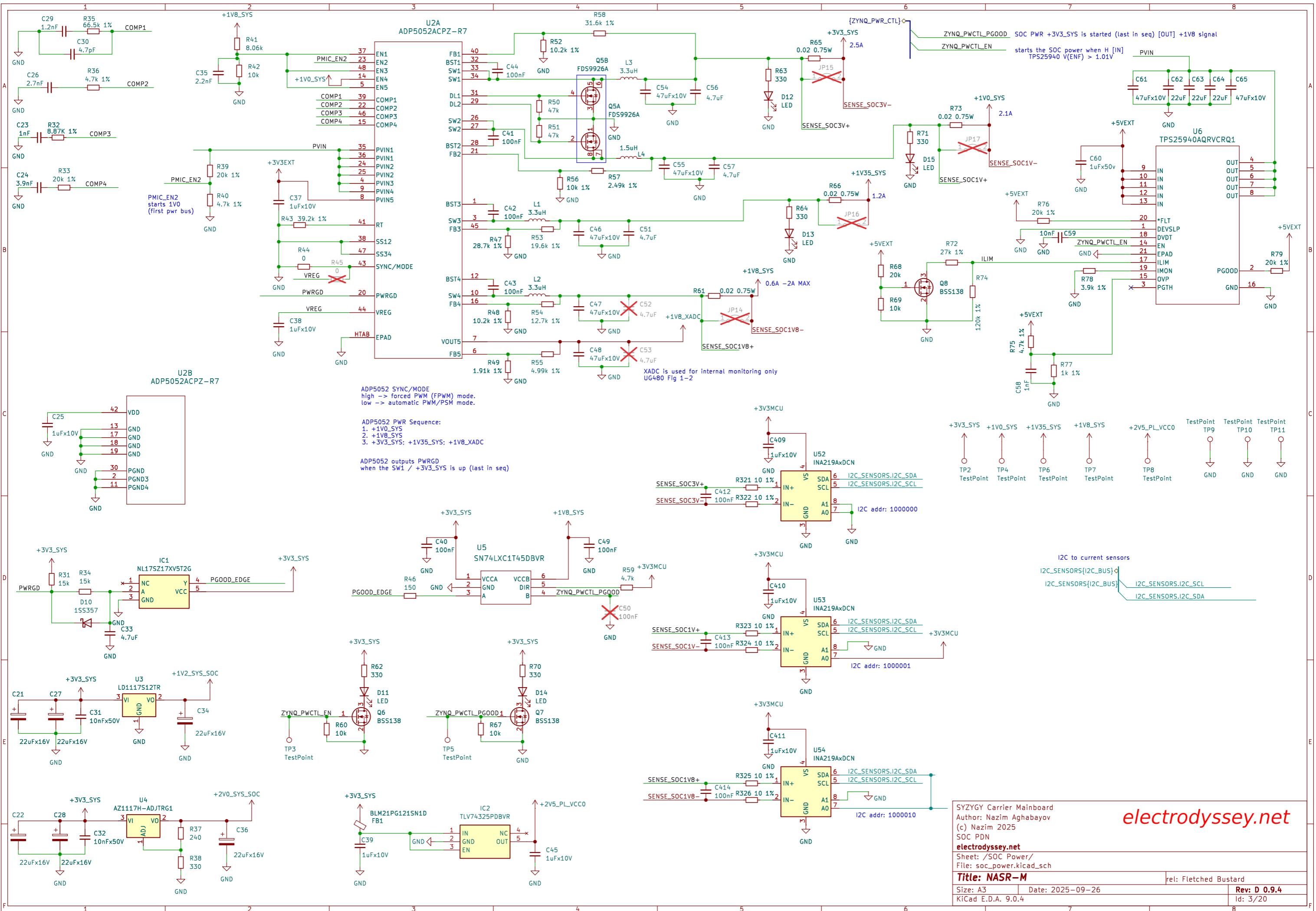
SYZYGY Carrier Mainboard  
Author: Nazim Aghabayov  
(c) Nazim 2025  
Top Level Schema  
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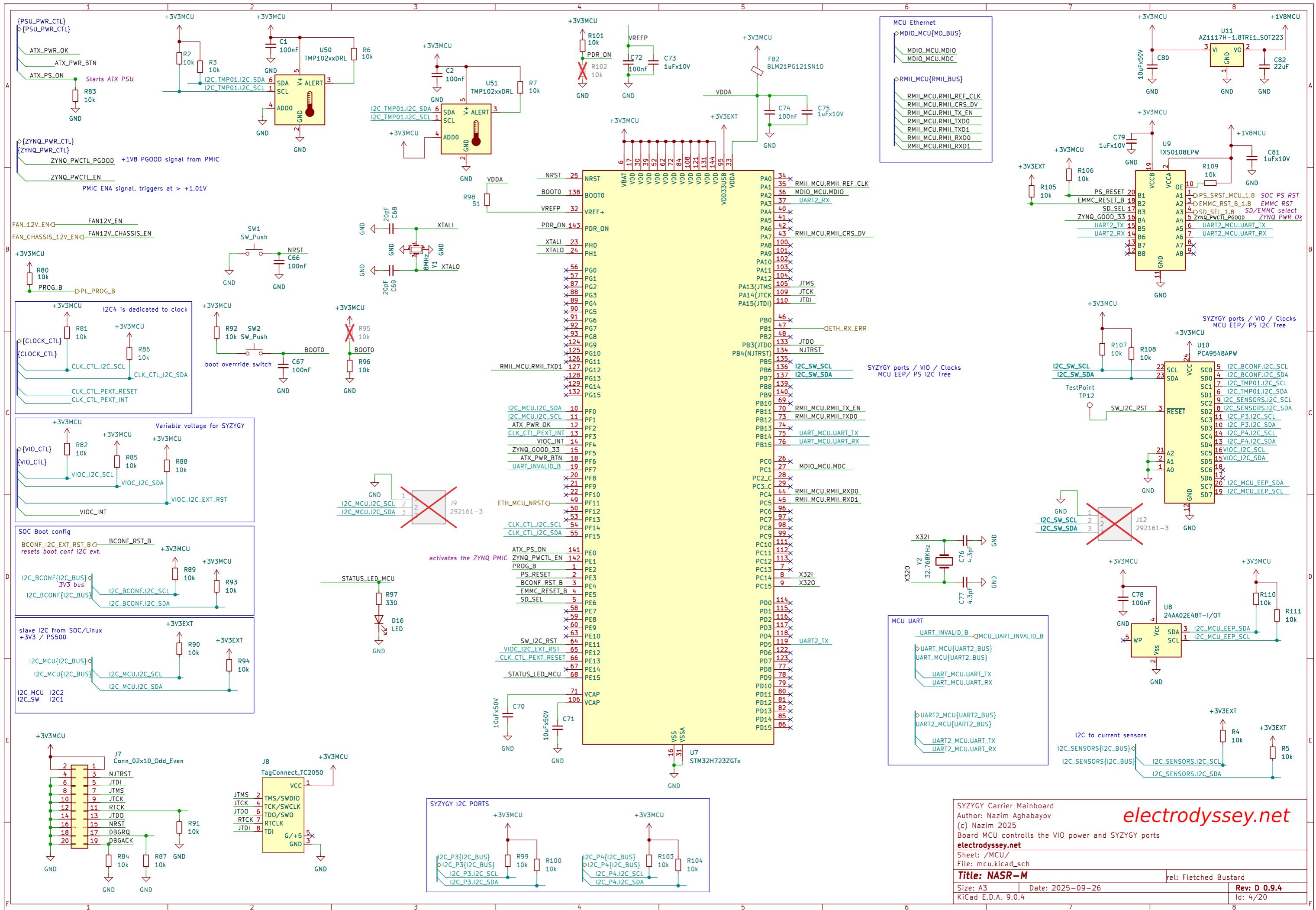
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Size: A3	Date: 2025-09-26
KiCad E.D.A. 9.0.4	Rev: D 0.9.4



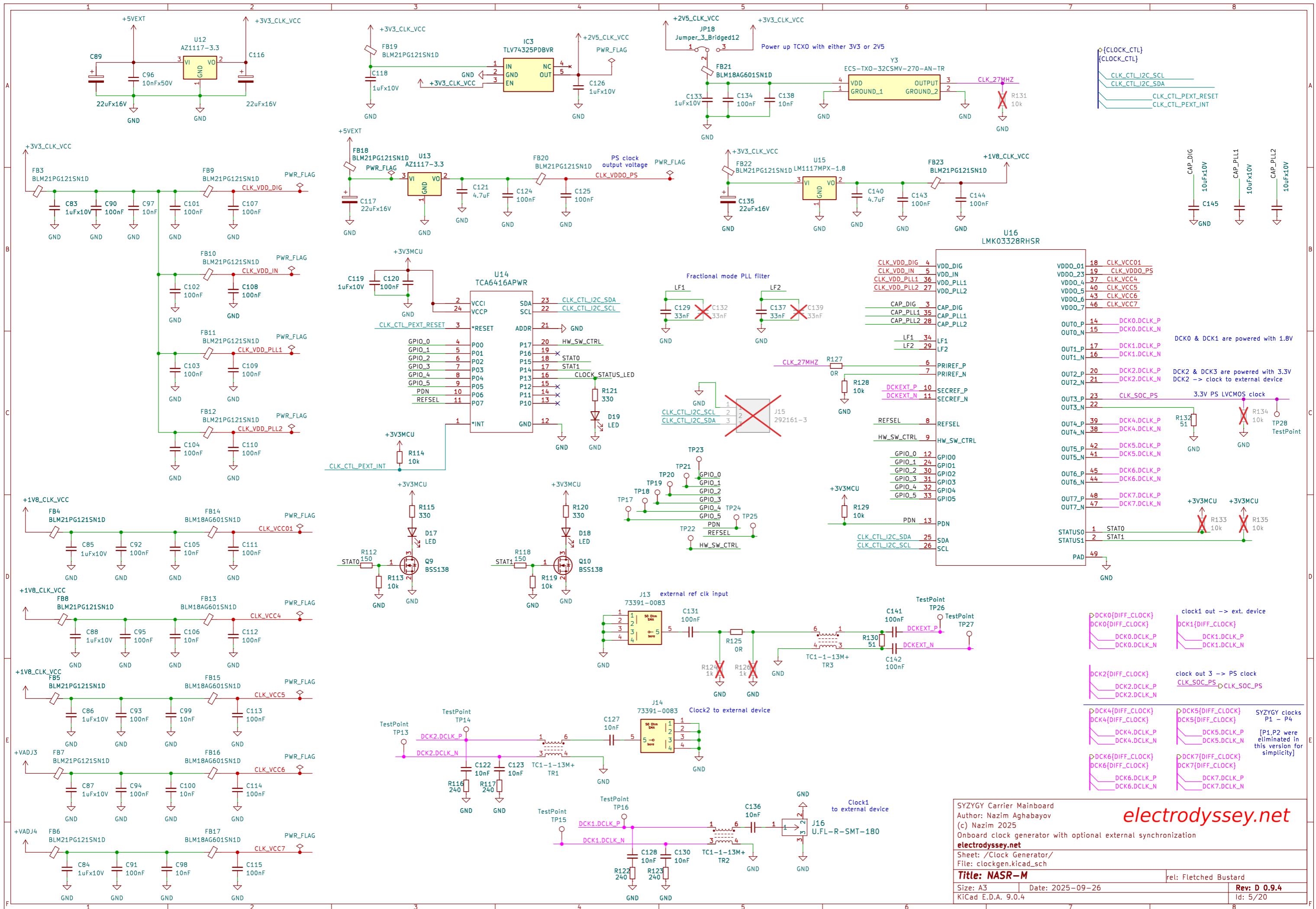




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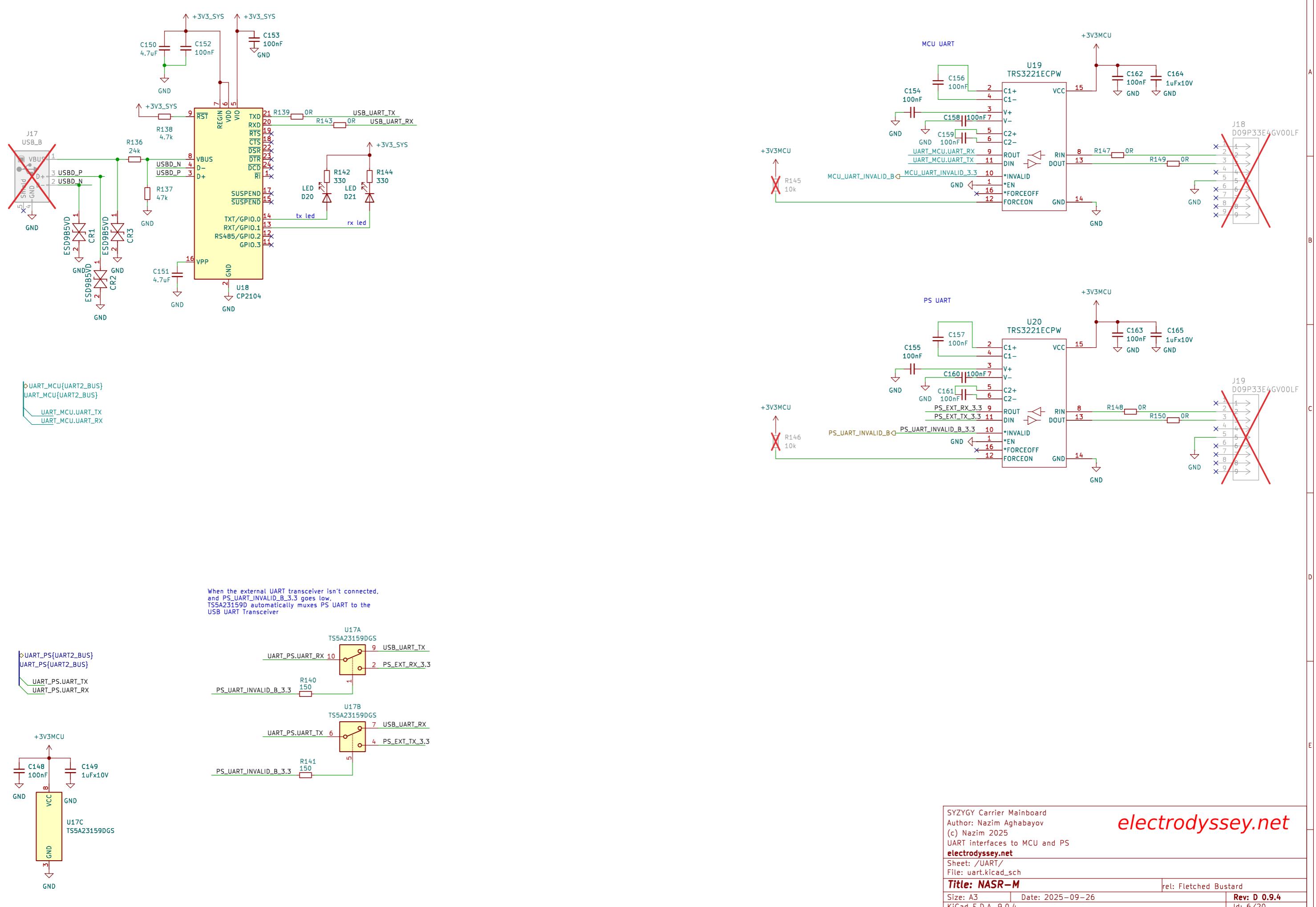
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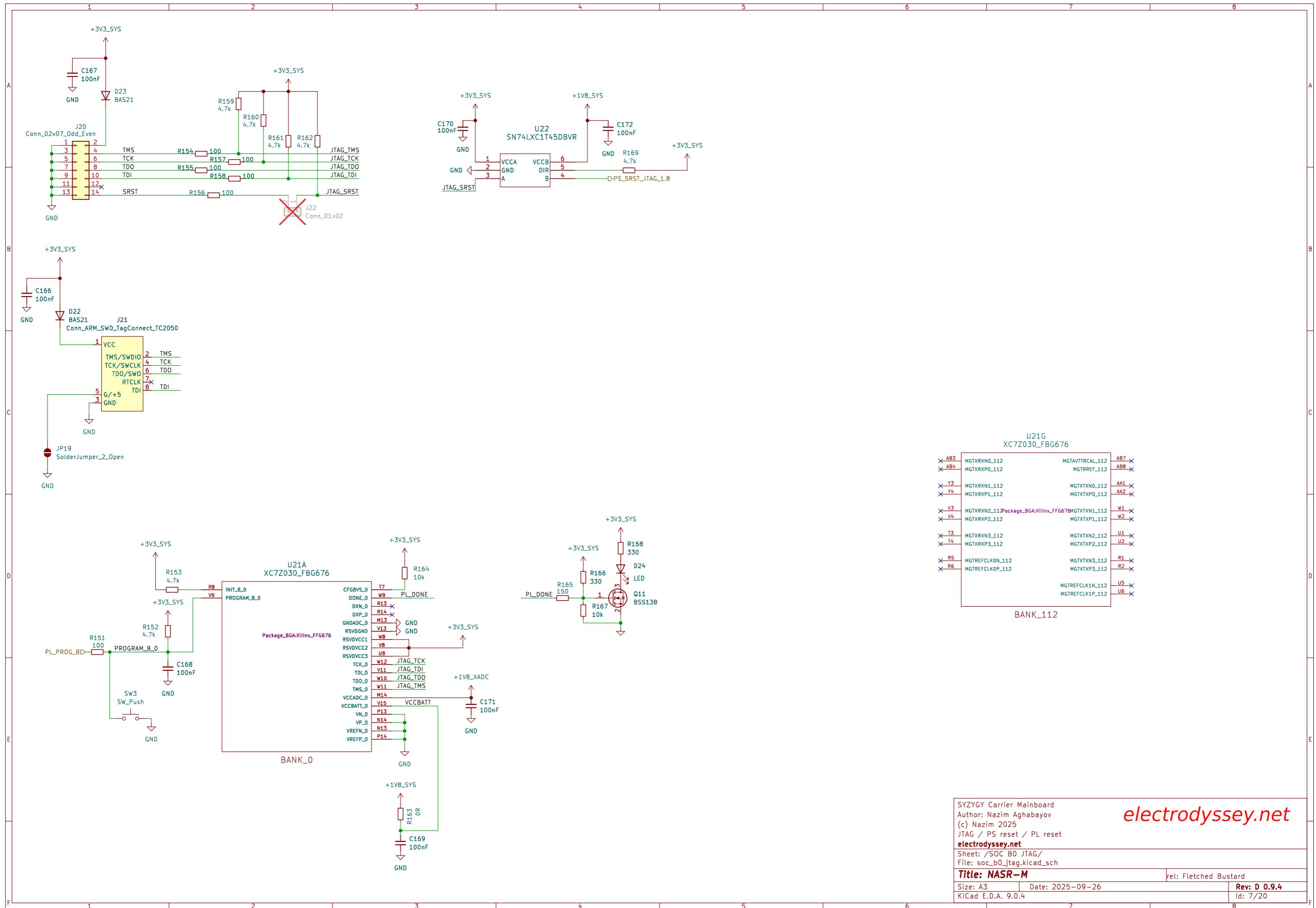


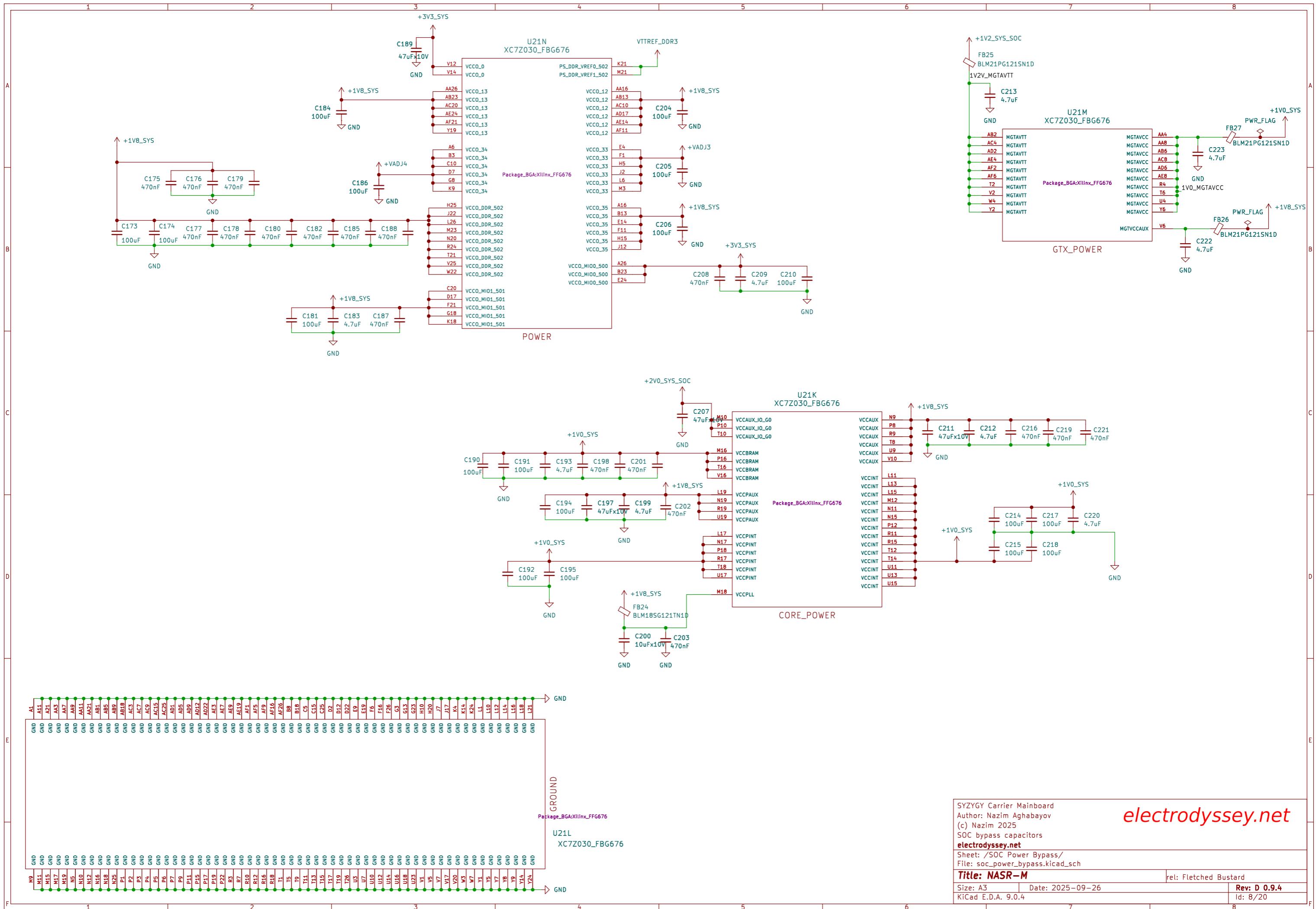
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SYZYGY Carrier Mainboard  
Author: Nazim Aghabayov  
(c) Nazim 2025  
Onboard clock generator with optional external synchronization  
electrodyssey.net  
Sheet: /Clock Generator/  
File: clockgen.kicad\_sch

**Title: NASR-M**  
Size: A3 Date: 2025-09-26  
KiCad E.D.A. 9.0.4 rel: Fletched Bustard  
Rev: D 0.9.4  
Id: 5/20







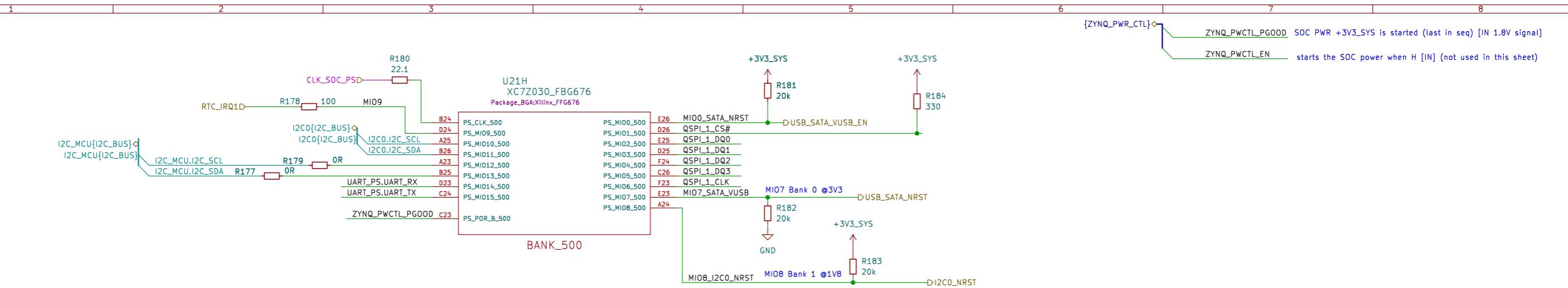
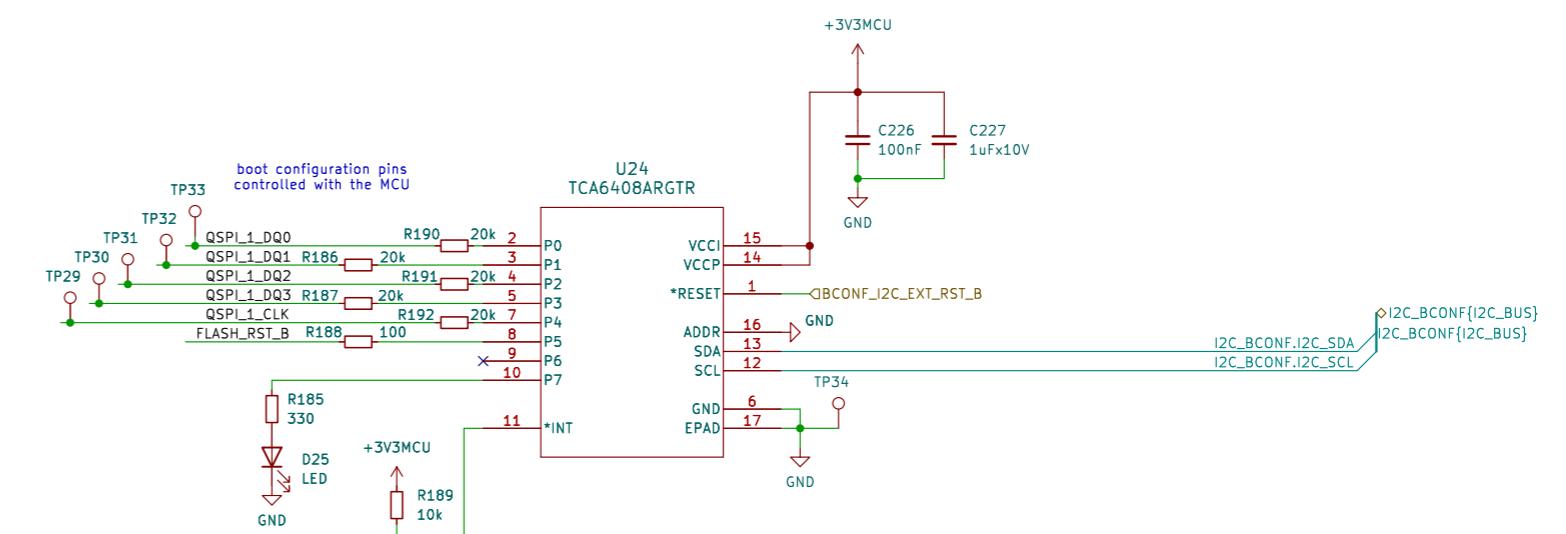
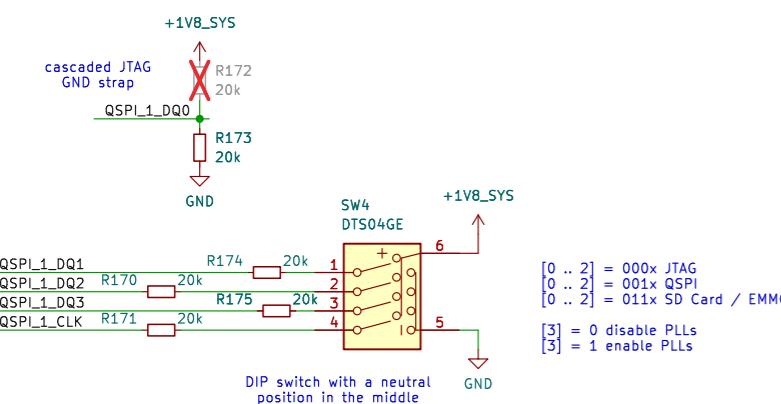
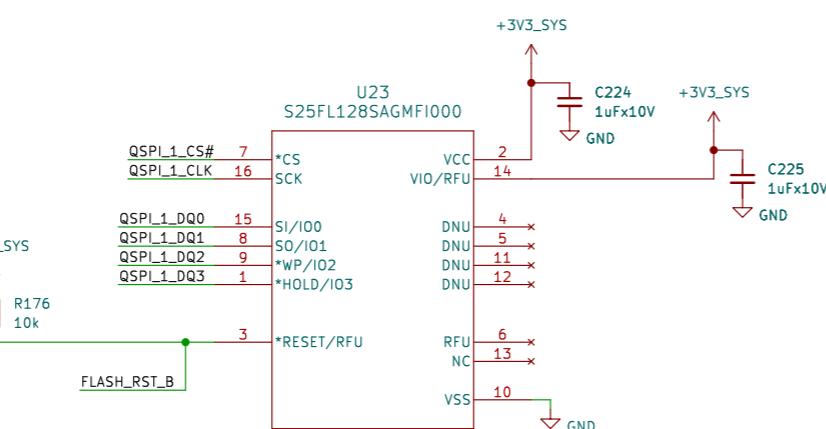


Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]	
	MODE[1]	VINODE[0]	BOOT_MODE[4]	BOOT_MODE[3]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[0]	
<b>Boot Devices</b>								
JTAG Boot Mode; cascaded is most common <sup>[1]</sup>	0	0	0				JTAG Chain Routing <sup>[2]</sup>	
NOR Boot <sup>[3]</sup>	0	0	1				0: Cascade mode 1: Independent mode	
NAND	0	1	0					
Quad-SPI <sup>[3]</sup>	1	0	0					
SD Card	1	1	0					
<b>Mode for all 3 PLLs</b>								
PLL Enabled		0	Hardware waits for PLL to lock, then executes BootROM.					
PLL Bypassed		1	Allows for a wide PS_CLK frequency range.					
<b>MIO Bank Voltage<sup>[4]</sup></b>								
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. 2.5 V, 3.3 V 0 0					
			Voltage Bank 1 includes MIO pins 16 thru 53. 1.8 V 1 1					

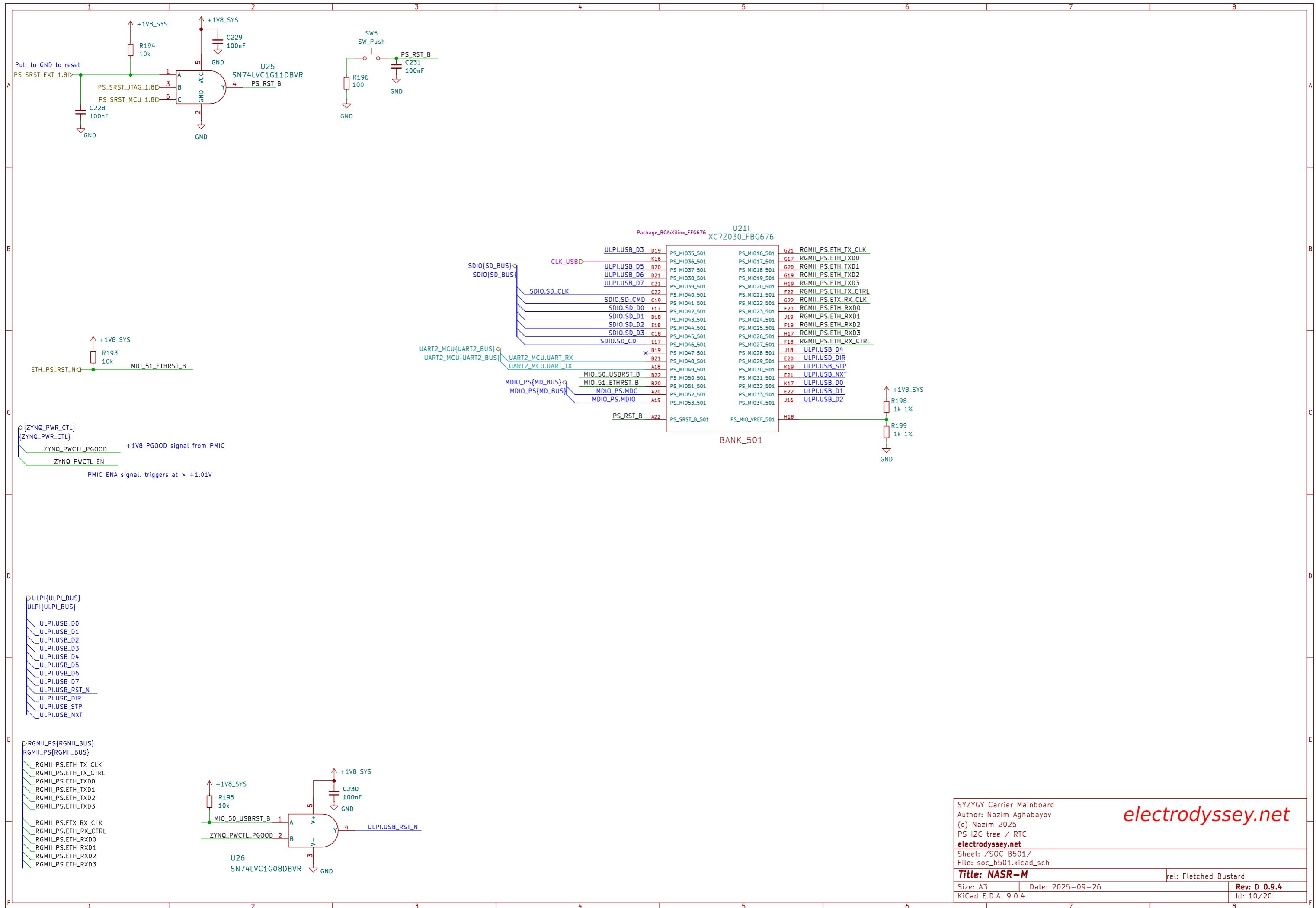
Notes:  
1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.  
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.  
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure).  
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

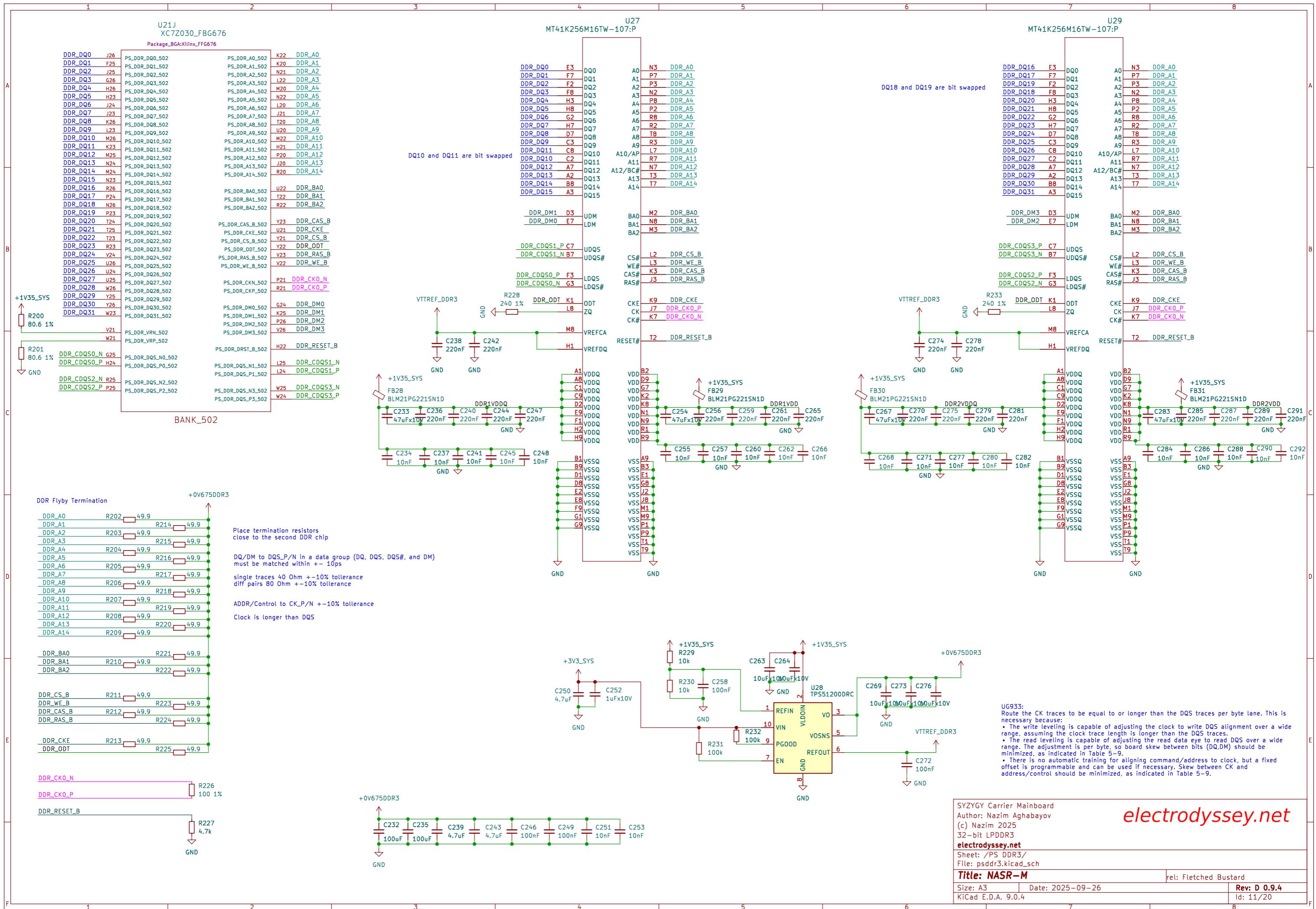


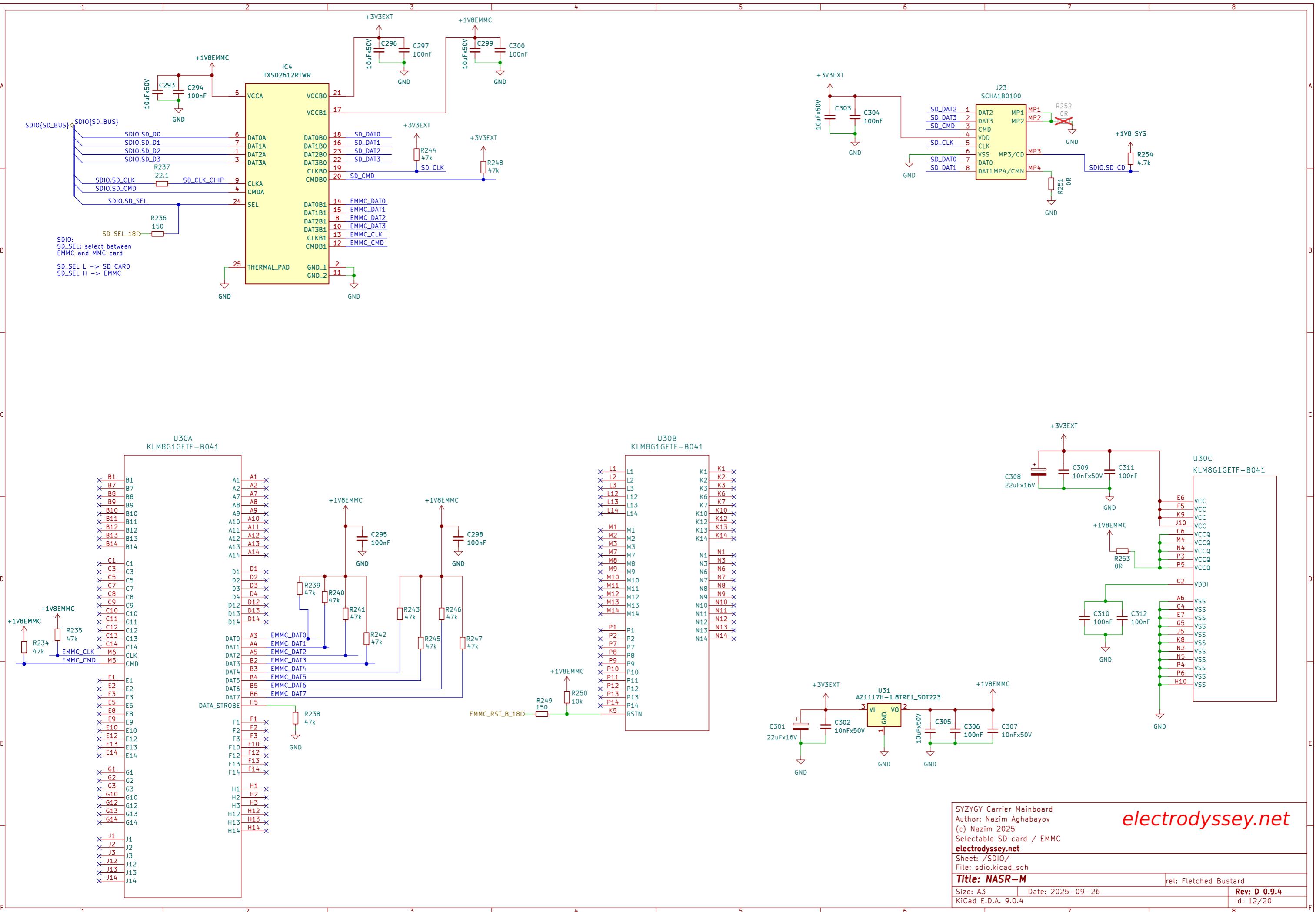
SYZYGY Carrier Mainboard  
Author: Nazim Aghabayov  
(c) Nazim 2025  
Bank 500; QSPI / Boot mode switches / POR  
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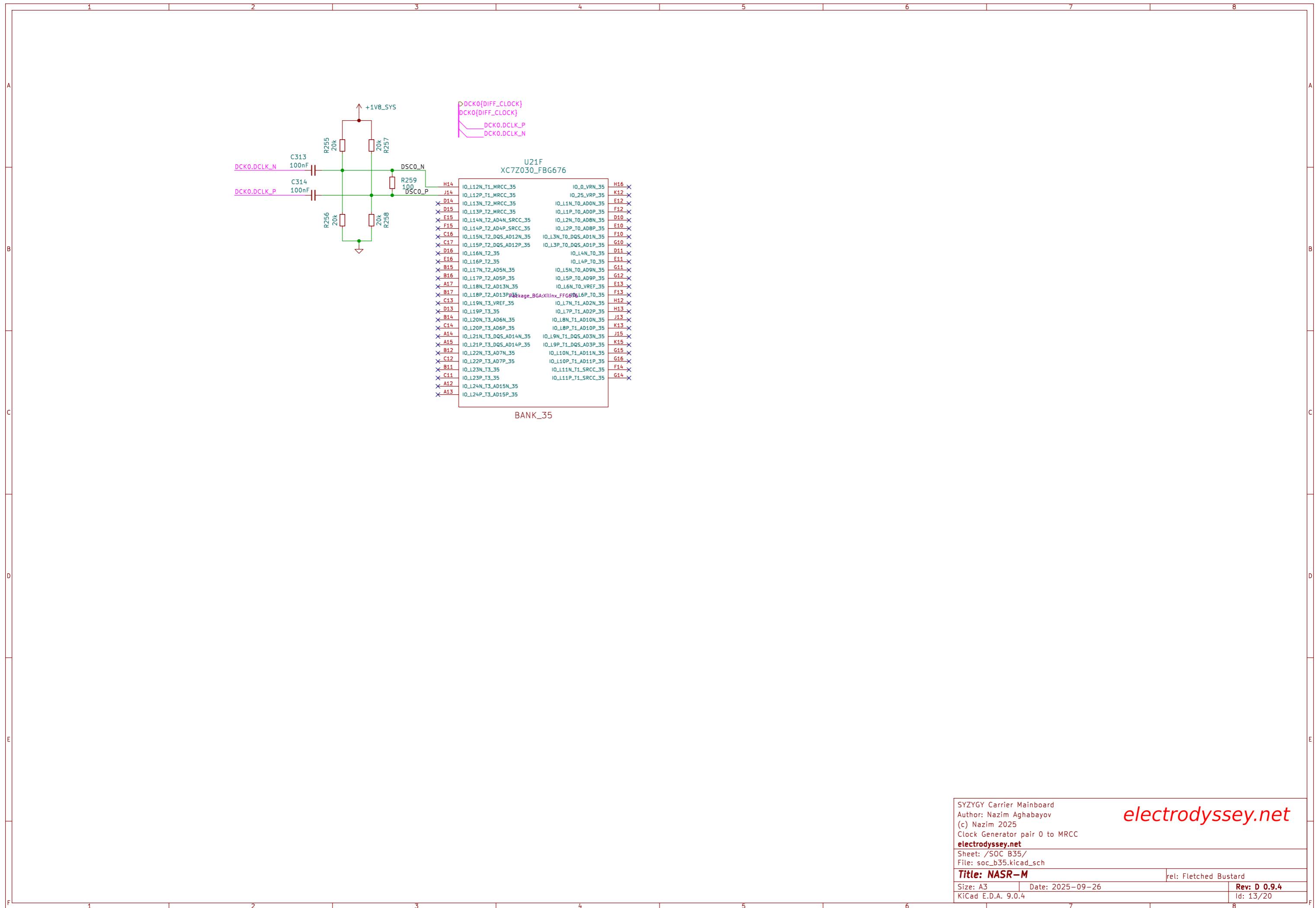
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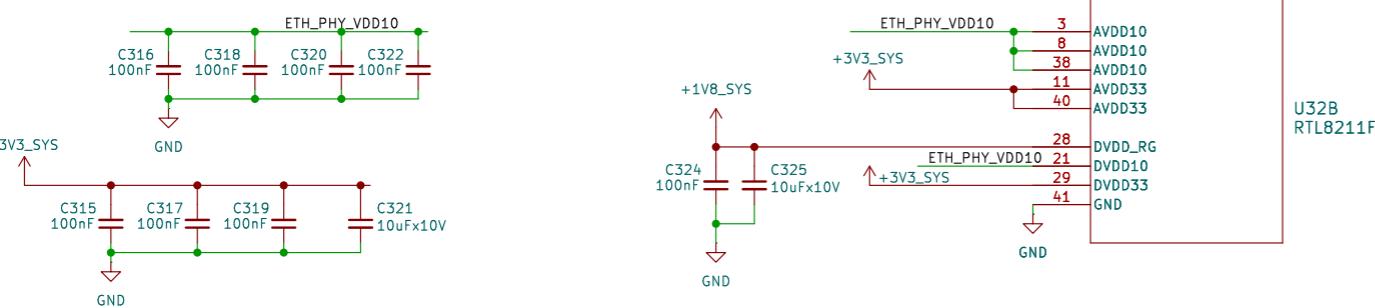
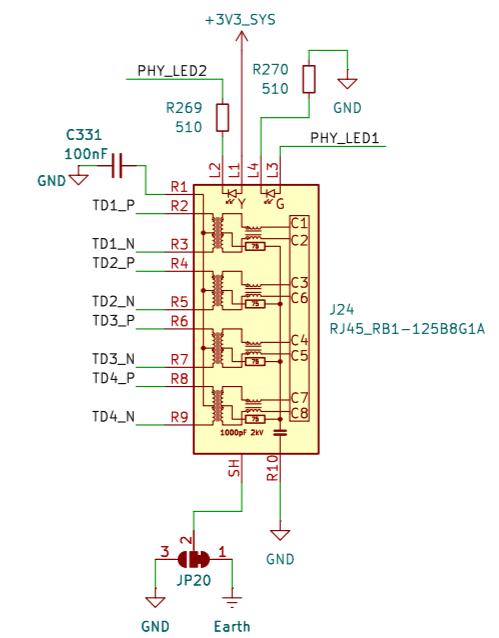
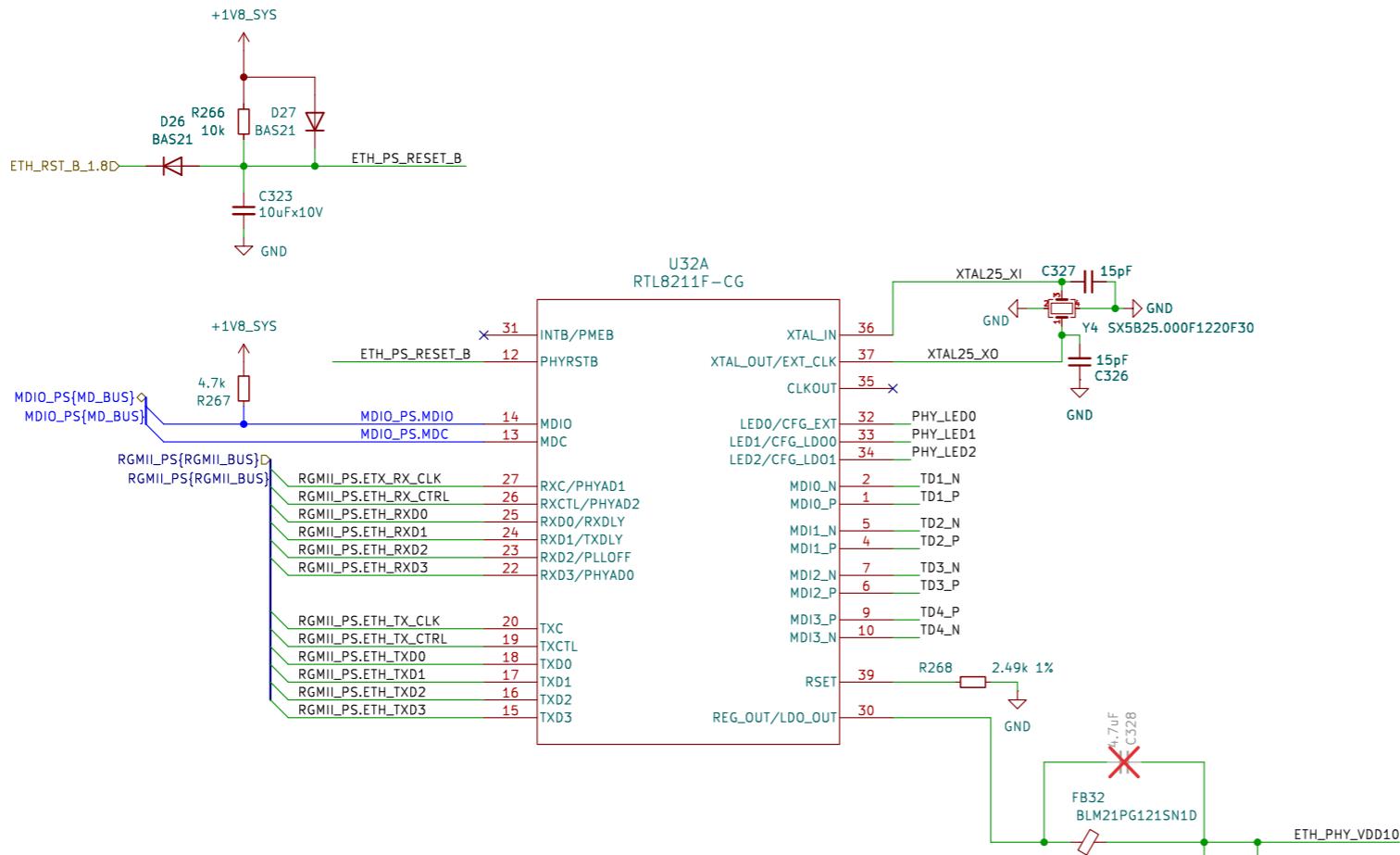
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Size: A3 Date: 2025-09-26  
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Id: 9/20











Configuration straps:  
LED0 CFG\_EXT  
LED1 CFG\_LDO0  
LED2 CFG\_LDO1

32	CFG_EXT	O/LI/PD	IO Pad External Power Source Mode Configuration. Pull up to use the external power source for the IO pad. Pull down to use the integrated LDO to transform the desired voltage for the IO pad.
33	CFG_LDO0	O/LI/PU	LDO Output Voltage Selection for I/O Pad/ External Power Source Voltage Selection for I/O Pad. When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved. 2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V.
34	CFG_LDO1	O/LI/PD	When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for input voltage selection of the external power for IO pad: 2'b00: 3.3V. 2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V.

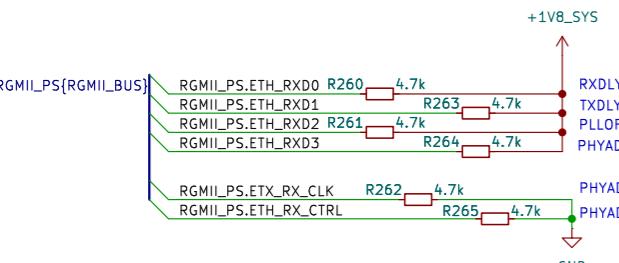


Table 11. Configuration Register Definitions	
Configuration	Description
PHYAD[2:0]	PHY Address. PHYAD sets the PHY address for the device. The RTL8211F(I)/RTL8211FD(I) supports PHY addresses from 00001 to 00111. Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Reg24.13=0 (See Table 37). Note 2: The RTL8211F(I)/RTL8211FD(I) with PHYAD[2:0]=000 can automatically remember the first non-zero PHY address. This function can be enabled by setting Reg24.6 = 1 (See Table 37).
PLLOFF	ALDPS Mode PLL Off Configuration. 1: Stop PLL when entering ALDPS mode (via 4.7k-ohm to DVDD_RG) 0: PLL continue toggling when entering ALDPS mode (via 4.7k-ohm to GND)
TXDLY	RGMII Transmit Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG) 0: No delay (via 4.7k-ohm to GND)
RXDLY	RGMII Receive Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG) 0: No delay (via 4.7k-ohm to GND)
CFG_EXT	I/O Pad External Power Source Mode Configuration. 1: Use the external power source for the IO pad (via 4.7k-ohm to 3.3V) 0: Use the integrated LDO to transform the desired voltage for the IO pad (via 4.7k-ohm to GND)

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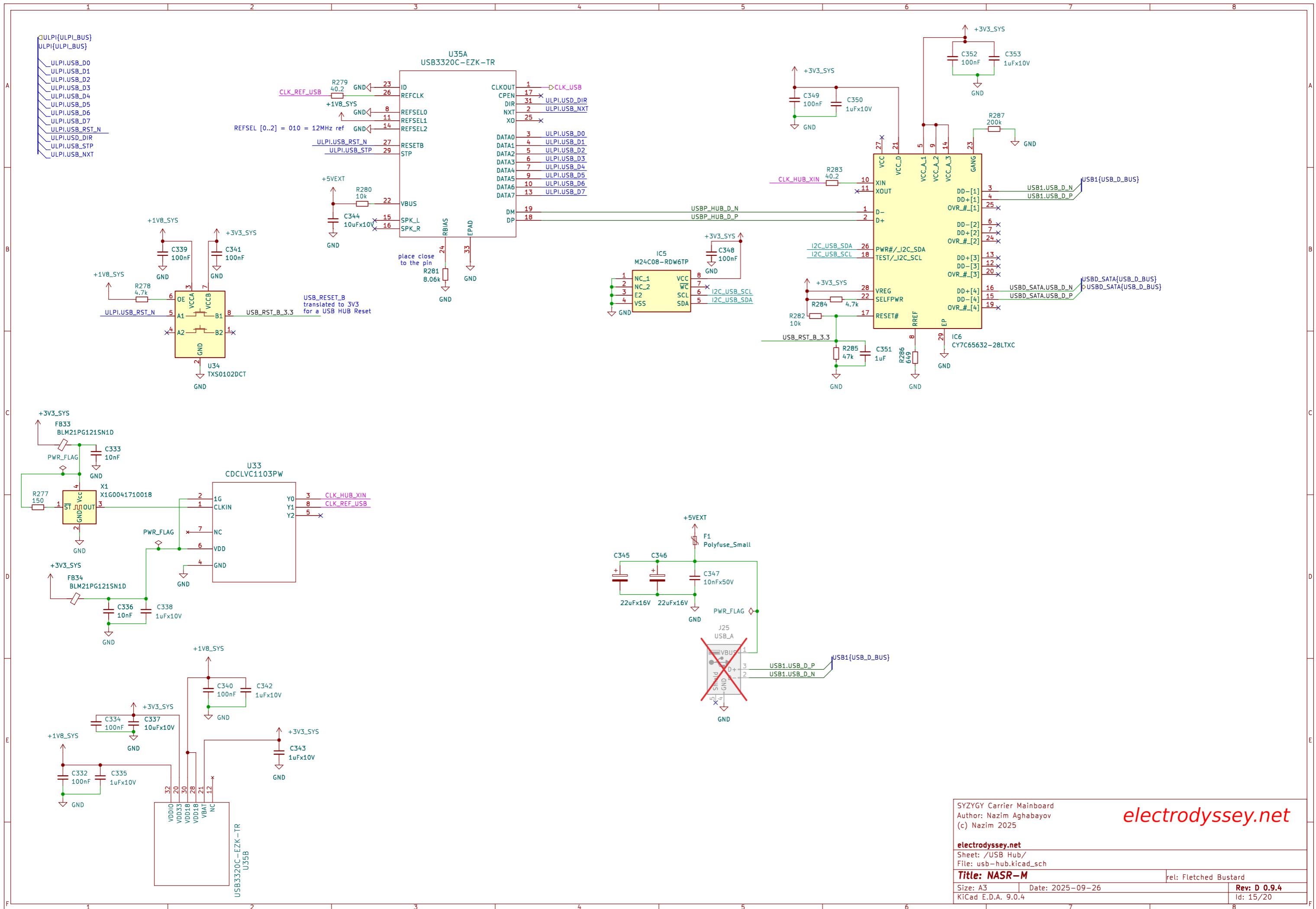
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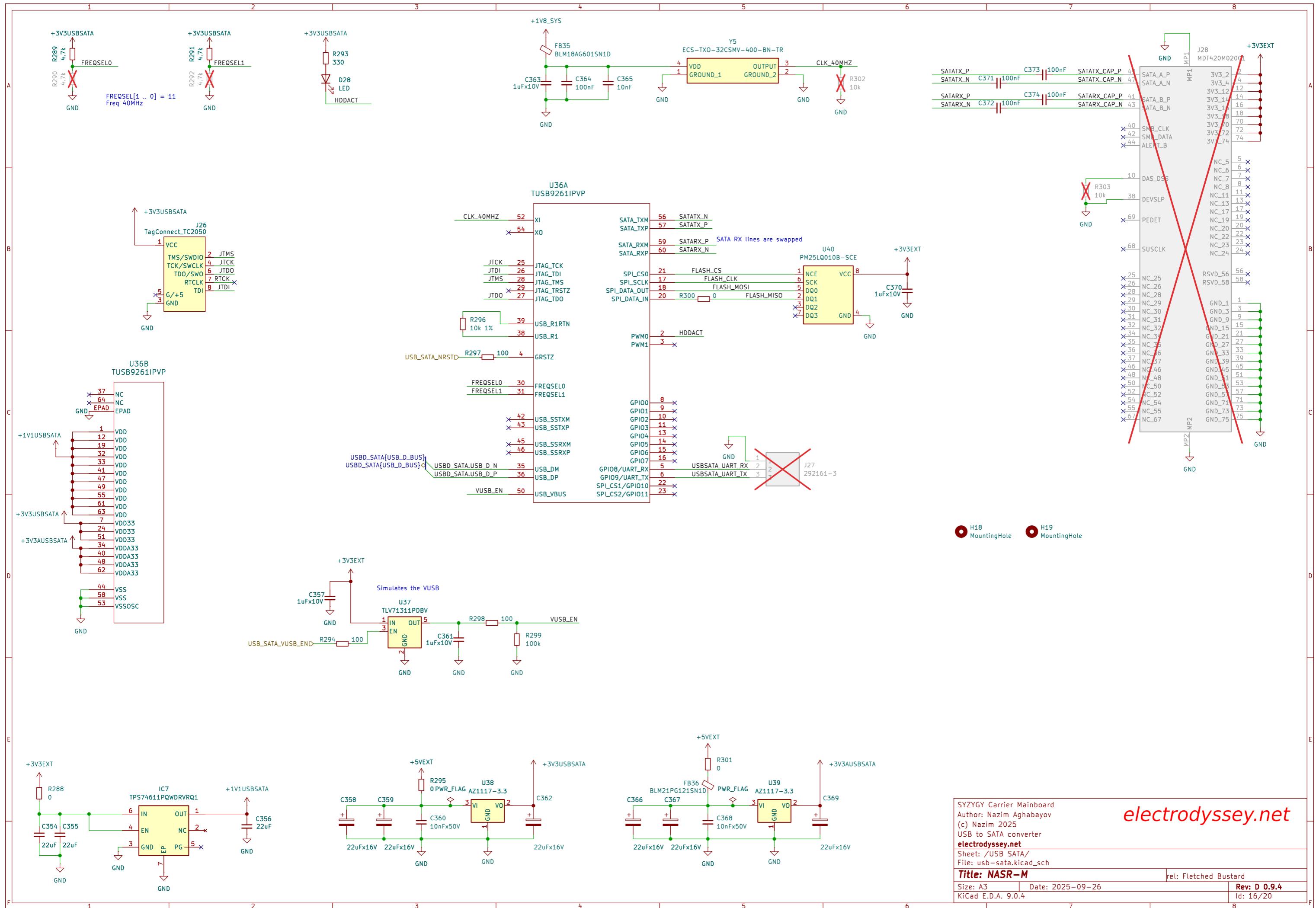
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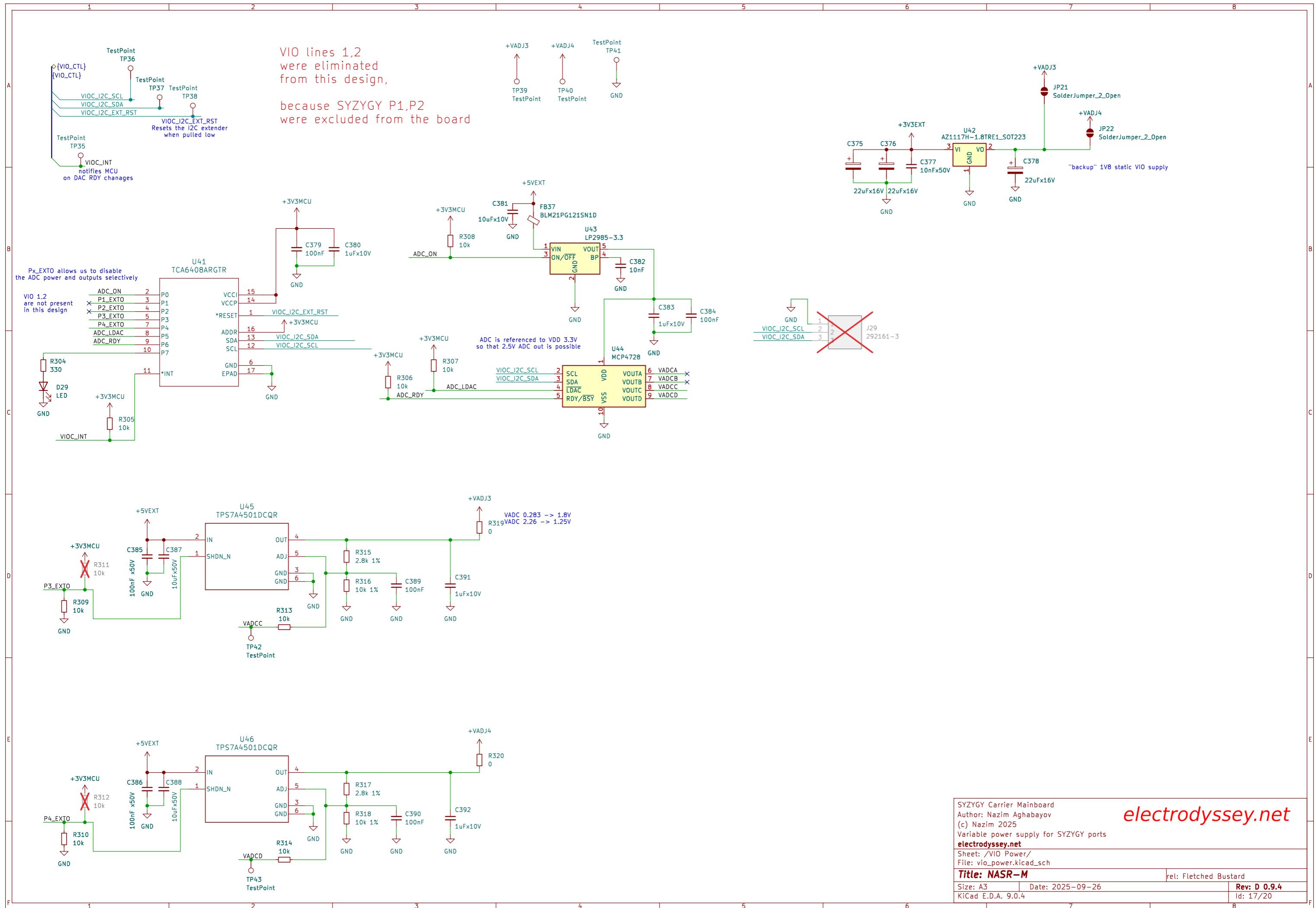
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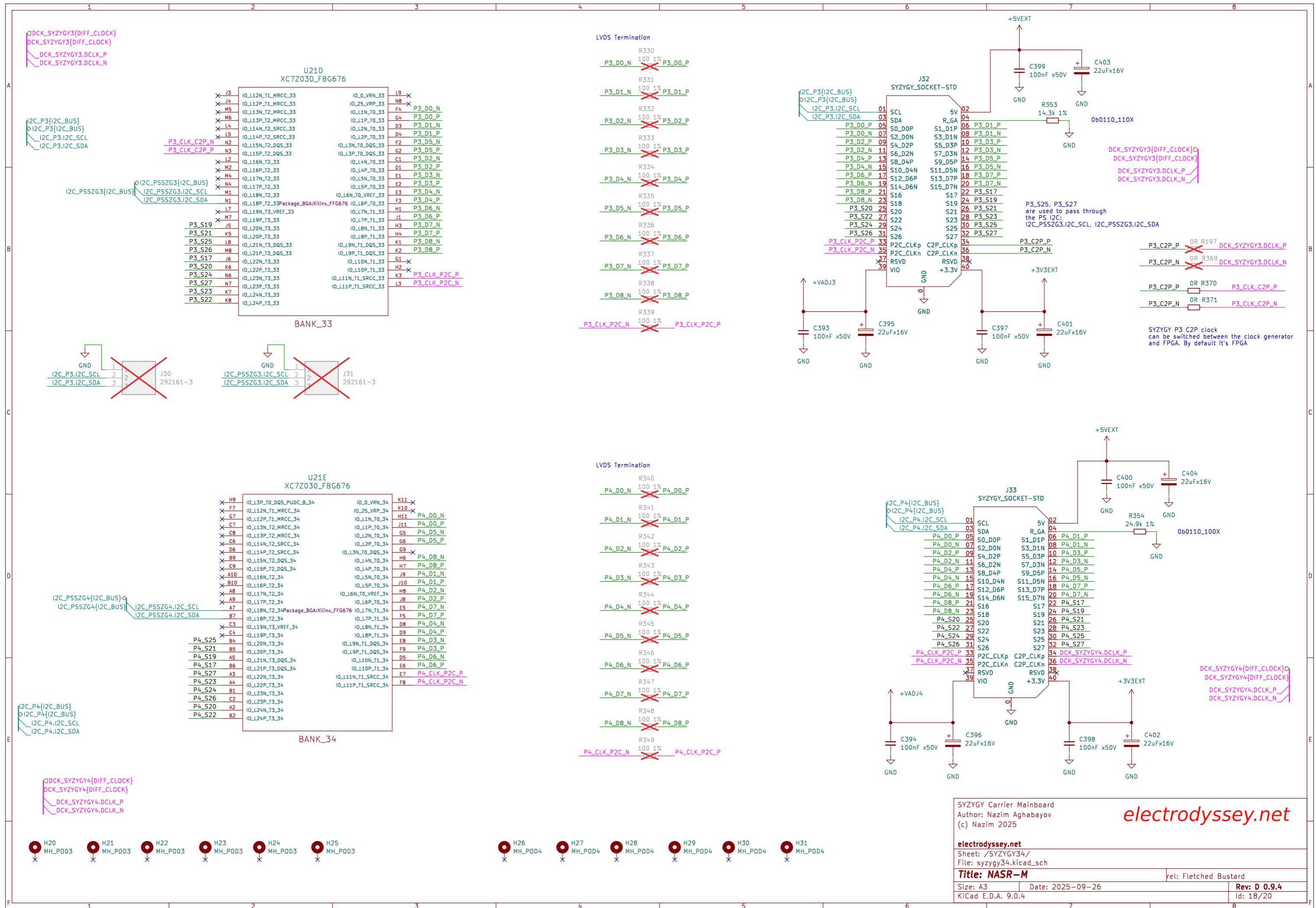
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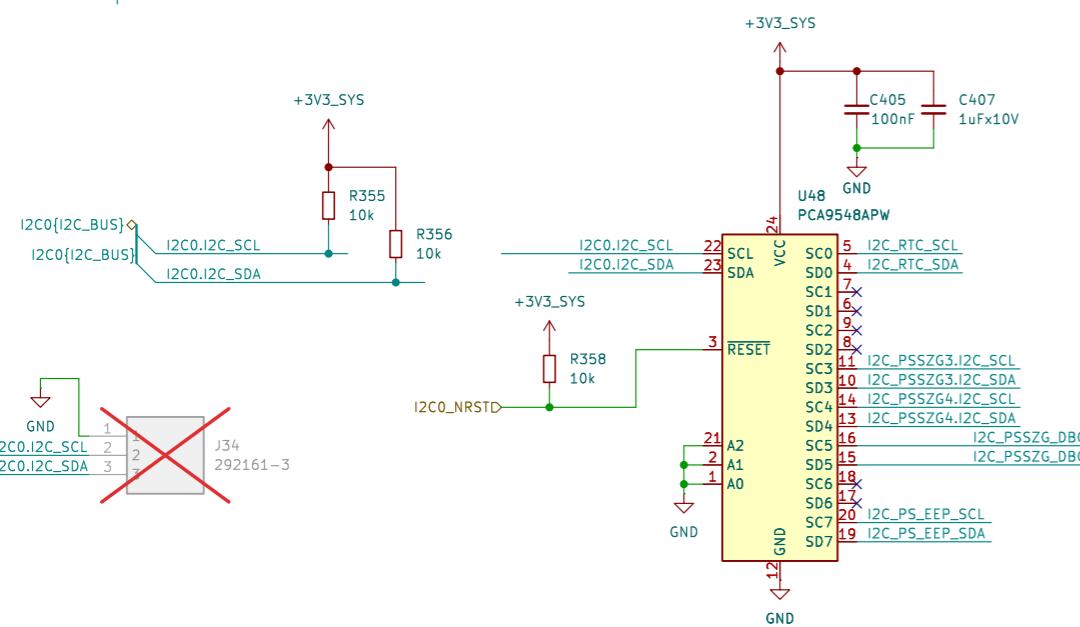




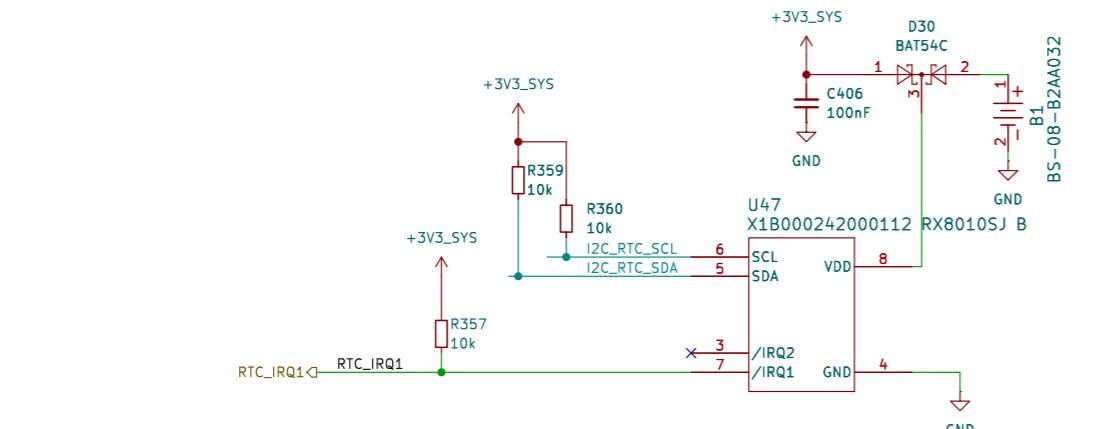
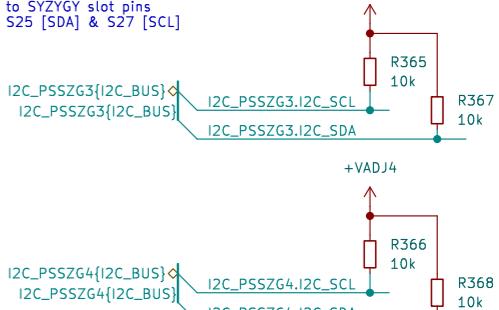


TestPoint  
TP44  
I2C0.I2C\_SCL

TestPoint  
TP45  
I2C0.I2C\_SDA



I2C\_PSSZG3 & I2C\_PSSZG4  
are I2C passthrough  
to SYZYGY slot pins.  
S25 [SDA] & S27 [SCL]



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