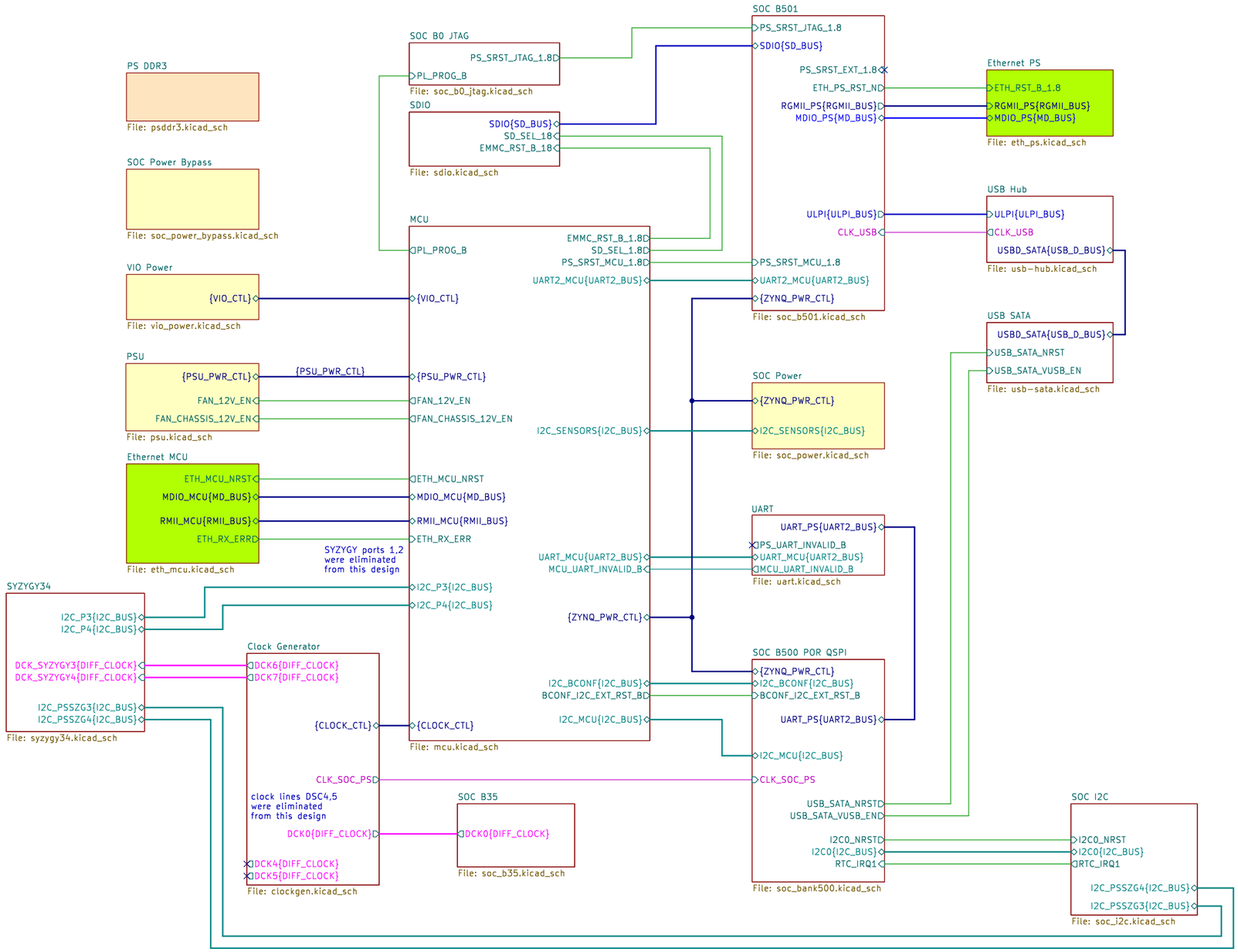


PAGE	DESCRIPTION
1 ROOT PAGE	Block Diagram of the project
2 PSU	ATX PSU connector and filters
3 SOC Power	A secondary power supply for SOC
4 MCU	MCU
5 Clock Generator	Clocks for SOC and SYZYGY, external master sync
6 UART	UART peripherals
7 SOC B0 JTAG	SOC JTAG
8 SOC Power Bypass	SOC bypass capacitors
9 SOC B500 POR QSPI	Power on reset, QSPI, SOC boot config
10 SOC B501	Peripheral resets, ULPI and RGMII buses
11 PS DDR3	DDR3 RAM for SOC PS sybsystem
12 SDIO	SDIO and EMMC shared bus
13 SOC B35	A redundant clock for SOC PS
14 Ethernet PS	RGMII Ethernet peripheral
15 USB Hub	USB ULPI transceiver and hub
16 USB SATA	USB SATA converter and SATA SSD socket
17 VIO Power	Variable IO power for SYZYGY slots
18 SYZYGY34	SYZYGY slots
19 SOC I2C	SOC I2C
20 Ethernet MCU	10/100 RMII Ethernet for MCU

Stackup JLC10161H-2116(1.57mm±10%)

F.Cu, B.Cu:
diff 80Ohm track / spacing: 8.28/6 mil; 0.2103/0.1524 mm
single 40Ohm: 11.23 mil; 0.2852 mm

diff 100Ohm track / spacing: 5.58/8 mil; 0.1417/0.2032 mm
single 50Ohm: 7.36mil; 0.1869 mm

In3, In5, In7 internal layers:
diff 80Ohm: 6.44/8 mil; 0.1636/0.2032 mm
single 40Ohm: 7.03mil; 0.1786 mm

diff 100Ohm: 4.29/11 mil; 0.1090/0.2794 mm
single 50Ohm: 4.54mil; 0.1153 mm

NOTE:
SYZYGY ports 1,2
were eliminated
from this design

H1 MH1_M3
H2 MH2_M3
H3 MH3_M3
H4 MH4_M3
JP1 SolderJumper_2_Open
R1 0R
GND

H5 EARTH_MH_M3
H6 MountingHole
H7 MountingHole
H8 MountingHole
H9 MountingHole
H10 MountingHole
H11 MountingHole
H12 MountingHole
H13 MountingHole
H14 MountingHole
H15 MountingHole
H16 MountingHole
H17 MountingHole

SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Top Level Schema
electrodyssey.net

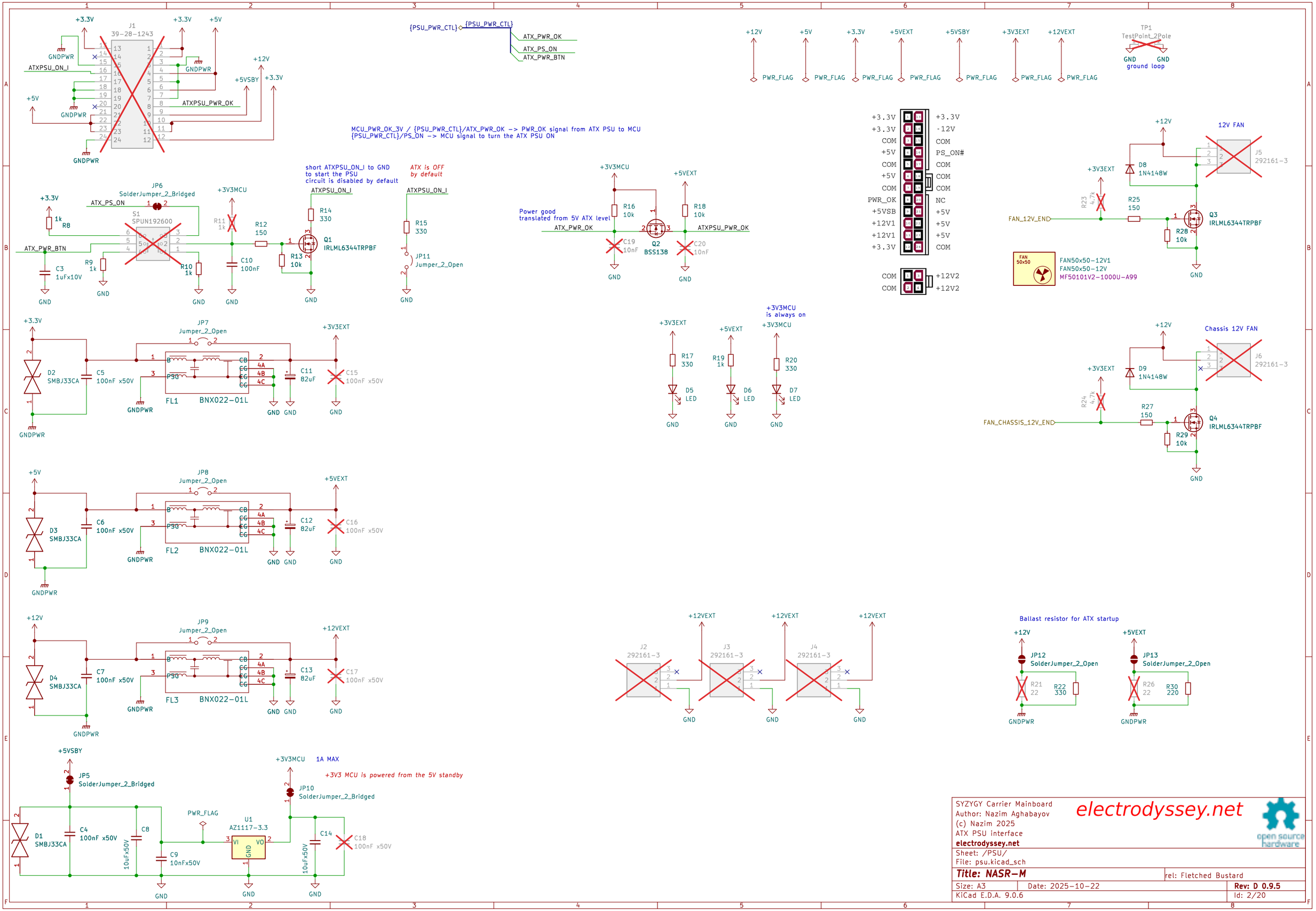
electrodyssey.net

Sheet: /
File: NASR.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**
KiCad E.D.A. 9.0.6 | Id: 1/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
ATX PSU interface
electrodyssey.net

electrodyssey.net

open source hardware

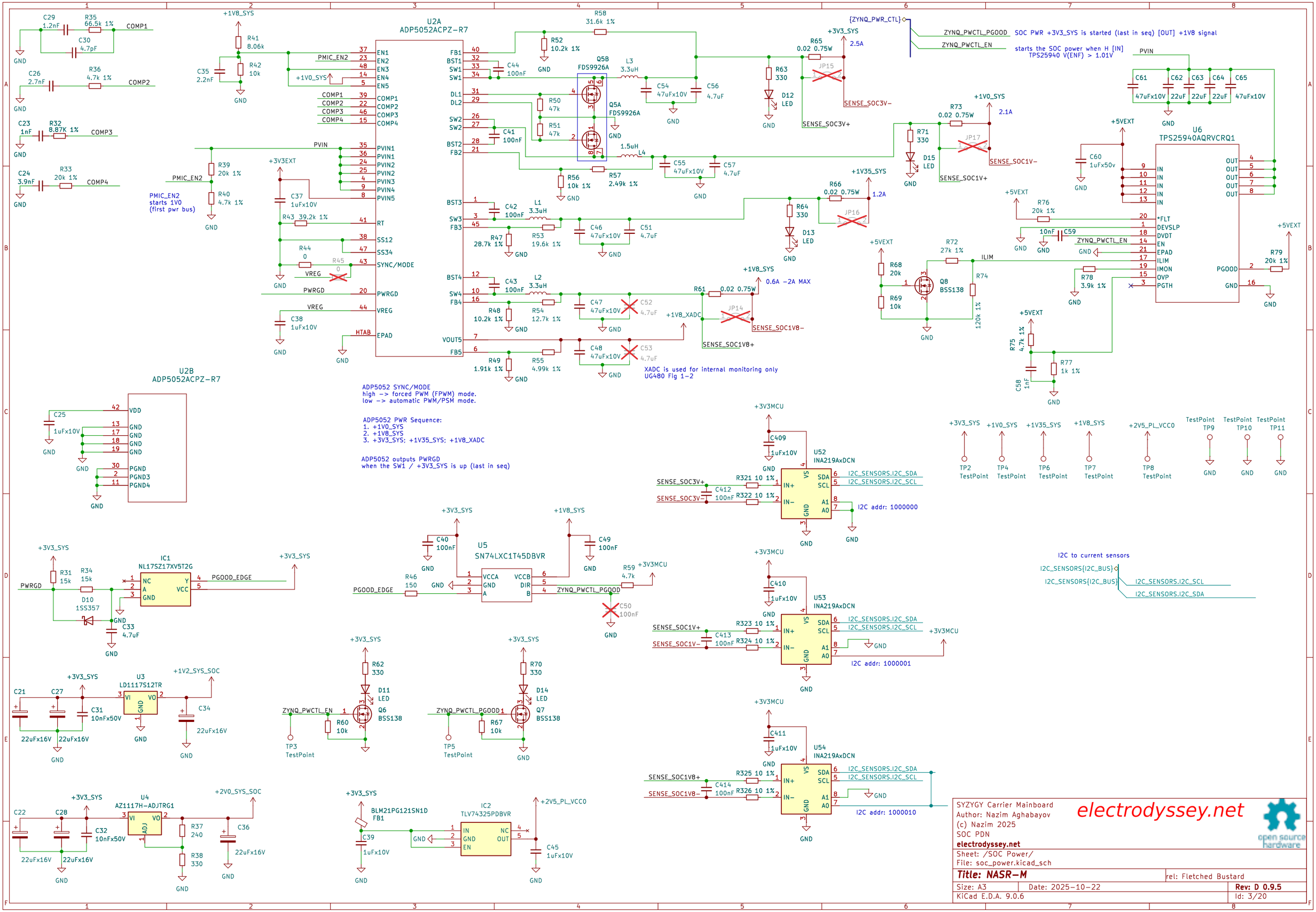
Sheet: /PSU/
File: psu.kicad_sch

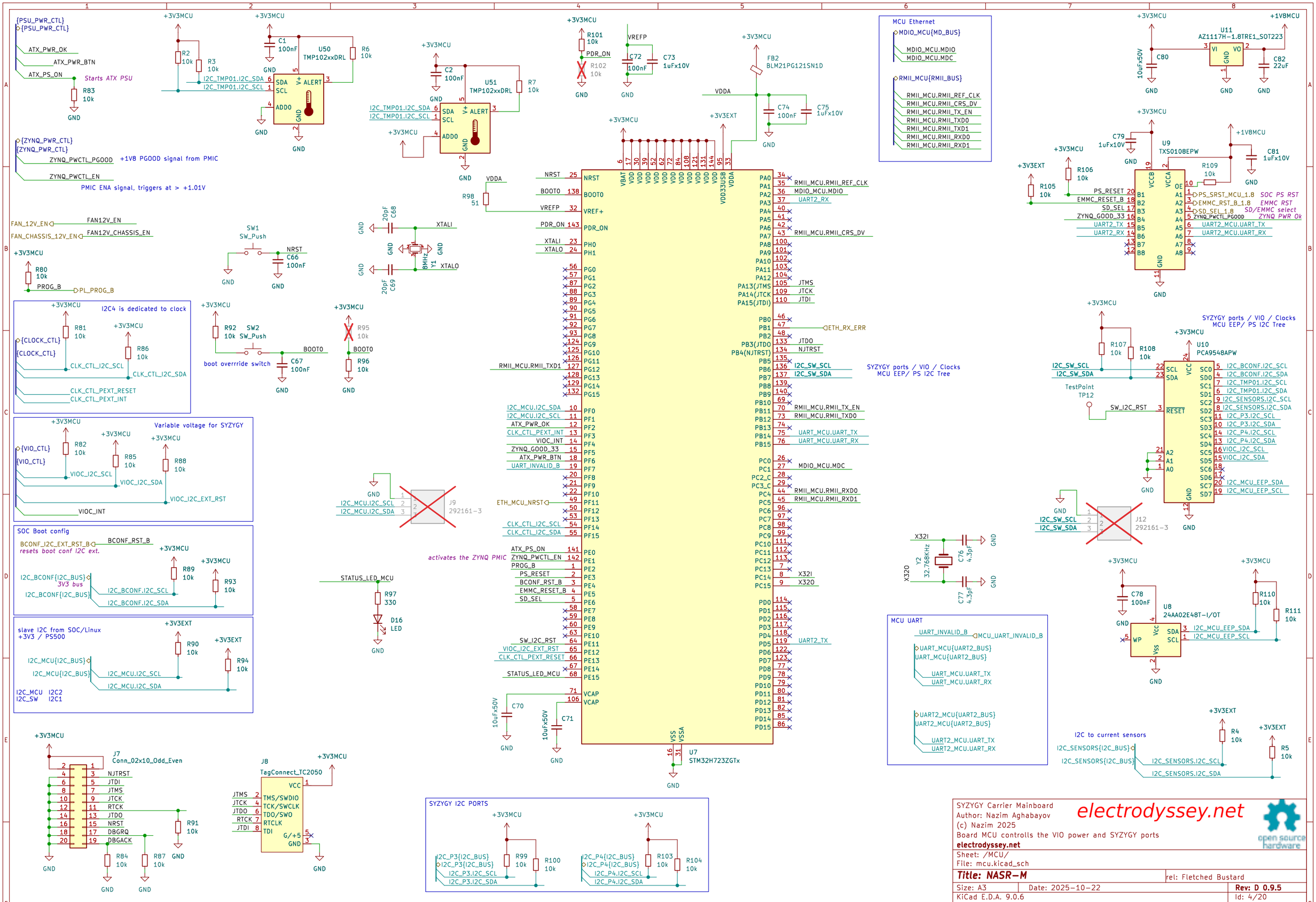
Title: NASR-M

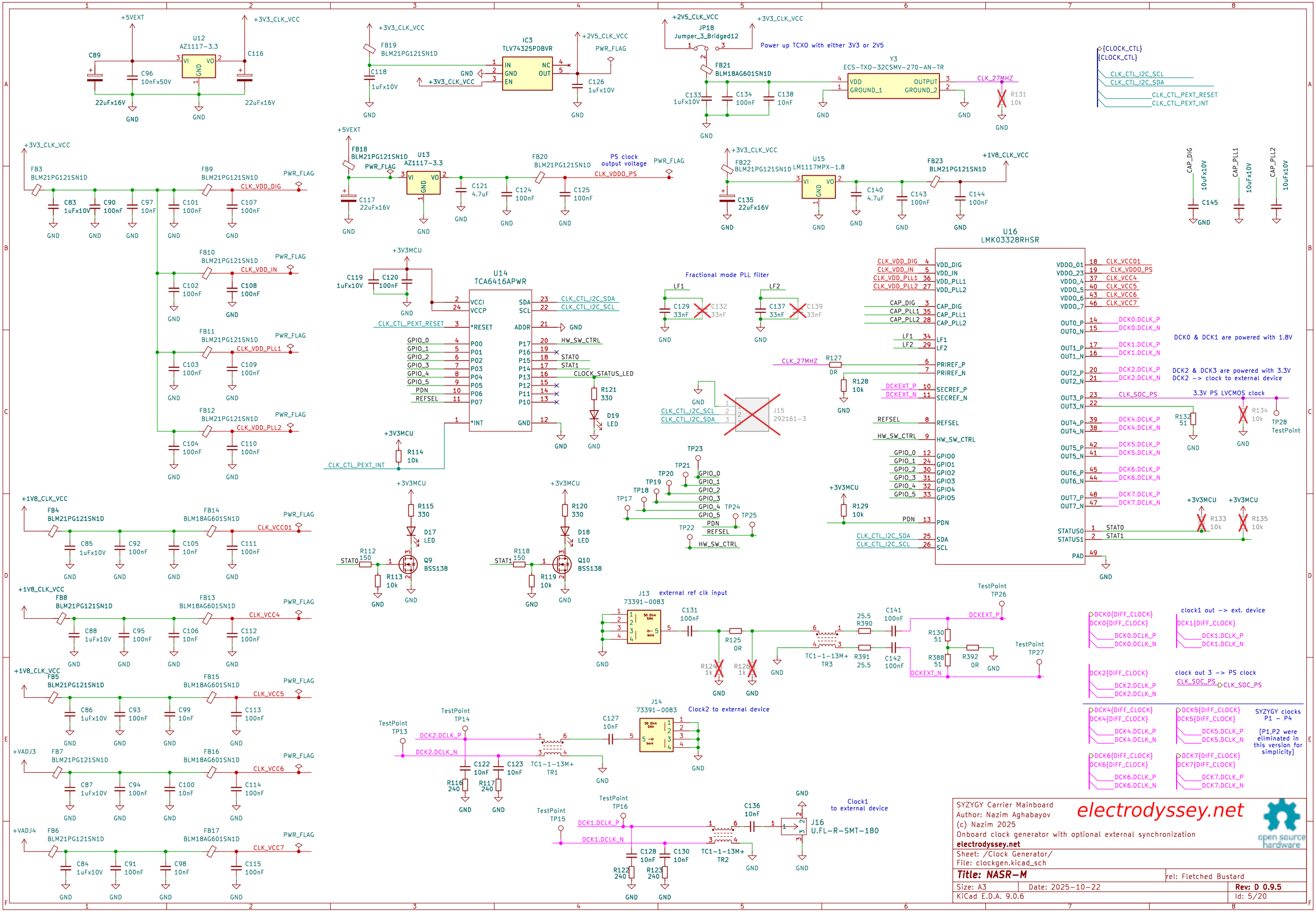
rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**

KiCad E.D.A. 9.0.6 | Id: 2/20


U2A
ADP5052ACPZ-R7
U2B
ADP5052ACPZ-R7
U6
TPS25940AQRVCRQ1
U5
SN74LXC1T45DBVR
U52
INA219AxDCN
U53
INA219AxDCN
U54
INA219AxDCN
U3
LD1117S12TR
U4
AZ1117H-ADJTRG1
IC1
NL17SZ17XV5T2G
IC2
TLV74325PDBVR
Q5B
FDS9926A
Q5A
FDS9926A
Q8
BSS138
Q6
BSS138
Q7
BSS138
{ZYNQ_PWR_CTL}
ZYNQ_PWCTL_PGOOD
ZYNQ_PWCTL_EN
SOC PWR +3V3_SYS is started (last in seq) [OUT] +1V8 signal
starts the SOC power when H [IN]
TPS25940 V(ENF) > 1.01V
PMIC_EN2
starts 1V0
(first pwr bus)
ADP5052 SYNC/MODE
high -> forced PWM (FPWM) mode.
low -> automatic PWM/PSM mode.
ADP5052 PWR Sequence:
1. +1V0_SYS
2. +1V8_SYS
3. +3V3_SYS; +1V35_SYS; +1V8_XADC
ADP5052 outputs PWRGD
when the SW1 / +3V3_SYS is up (last in seq)
XADC is used for internal monitoring only
UG480 Fig 1-2
I2C to current sensors
I2C_SENSORS.I2C_SDA
I2C_SENSORS.I2C_SCL
I2C addr: 1000000
I2C addr: 1000001
I2C addr: 1000010
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
SOC PDN
electrodyssey.net
Sheet: /SOC Power/
File: soc_power.kicad_sch
Title: NASR-M
rel: Fletched Bustard
Size: A3
Date: 2025-10-22
Rev: D 0.9.5
KiCad E.D.A. 9.0.6
Id: 3/20
electrodyssey.net
open source hardware


{PSU_PWR_CTL}
ATX_PWR_OK
ATX_PWR_BTN
ATX_PS_ON
Starts ATX PSU
R83 10k
{ZYNQ_PWR_CTL}
ZYNQ_PWCTL_PGOOD
+1V8 PGOOD signal from PMIC
ZYNQ_PWCTL_EN
PMIC ENA signal, triggers at > +1.01V
FAN_12V_EN
FAN12V_EN
FAN_CHASSIS_12V_EN
FAN12V_CHASSIS_EN
R80 10k
PROG_B
PL_PROG_B
I2C4 is dedicated to clock
{CLOCK_CTL}
CLK_CTL_I2C_SCL
CLK_CTL_I2C_SDA
CLK_CTL_PEXT_RESET
CLK_CTL_PEXT_INT
Variable voltage for SYZYGY
{VIO_CTL}
VIOC_I2C_SCL
VIOC_I2C_SDA
VIOC_I2C_EXT_RST
VIOC_INT
SOC Boot config
BCONF_I2C_EXT_RST_B
BCONF_RST_B
resets boot conf I2C ext.
I2C_BCONF{I2C_BUS}
3V3 bus
I2C_BCONF.I2C_SCL
I2C_BCONF.I2C_SDA
slave I2C from SOC/Linux
+3V3 / PS500
I2C_MCU{I2C_BUS}
I2C_MCU.I2C_SCL
I2C_MCU.I2C_SDA
I2C_MCU I2C2
I2C_SW I2C1
J7
Conn_02x10_Odd_Even
NJTRST
JTDI
JTMS
JTCK
RTCK
JTDO
NRST
DBGRQ
DBGACK
J8
TagConnect_TC2050
TMS/SWDIO
TCK/SWCLK
TDO/SWO
RTCLK
TDI
U50
TMP102xxDRL
U51
TMP102xxDRL
I2C_TMP01.I2C_SDA
I2C_TMP01.I2C_SCL
SW1
SW_Push
SW2
SW_Push
boot overrride switch
BOOT0
XTALI
XTALO
8MHz
Y1
VREFP
VDDA
PDR_ON
FB2
BLM21PG121SN1D
U7
STM32H723ZGTx
NRST
BOOT0
VREF+
PDR_ON
XTALI
XTALO
RMII_MCU.RMII_TXD1
I2C_MCU.I2C_SDA
I2C_MCU.I2C_SCL
ATX_PWR_OK
CLK_CTL_PEXT_INT
VIOC_INT
ZYNQ_GOOD_33
ATX_PWR_BTN
UART_INVALID_B
ETH_MCU_NRST
CLK_CTL_I2C_SCL
CLK_CTL_I2C_SDA
ATX_PS_ON
ZYNQ_PWCTL_EN
PROG_B
PS_RESET
BCONF_RST_B
EMMC_RESET_B
SD_SEL
SW_I2C_RST
VIOC_I2C_EXT_RST
CLK_CTL_PEXT_RESET
STATUS_LED_MCU
activates the ZYNQ PMIC
RMII_MCU.RMII_REF_CLK
MDIO_MCU.MDIO
UART2_RX
RMII_MCU.RMII_CRS_DV
JTMS
JTCK
JTDI
ETH_RX_ERR
JTDO
NJTRST
I2C_SW_SCL
I2C_SW_SDA
RMII_MCU.RMII_TX_EN
RMII_MCU.RMII_TXD0
UART_MCU.UART_TX
UART_MCU.UART_RX
MDIO_MCU.MDC
RMII_MCU.RMII_RXD0
RMII_MCU.RMII_RXD1
UART2_TX
X32I
X32O
SYZYGY ports / VIO / Clocks
MCU EEP/ PS I2C Tree
MCU Ethernet
MDIO_MCU{MD_BUS}
RMII_MCU{RMII_BUS}
RMII_MCU.RMII_REF_CLK
RMII_MCU.RMII_CRS_DV
RMII_MCU.RMII_TX_EN
RMII_MCU.RMII_TXD0
RMII_MCU.RMII_TXD1
RMII_MCU.RMII_RXD0
RMII_MCU.RMII_RXD1
U11
AZ1117H-1.8TRE1_SOT223
+1V8MCU
U9
TXS0108EPW
PS_RESET
EMMC_RESET_B
SD_SEL
ZYNQ_GOOD_33
UART2_TX
UART2_RX
PS_SRST_MCU_1.8
EMMC_RST_B_1.8
SD_SEL_1.8
ZYNQ_PWCTL_PGOOD
SOC PS RST
EMMC RST
SD/EMMC select
ZYNQ PWR Ok
UART2_MCU.UART_TX
UART2_MCU.UART_RX
SYZYGY ports / VIO / Clocks
MCU EEP/ PS I2C Tree
U10
PCA9548APW
TestPoint
TP12
SW_I2C_RST
I2C_BCONF.I2C_SCL
I2C_BCONF.I2C_SDA
I2C_TMP01.I2C_SCL
I2C_TMP01.I2C_SDA
I2C_SENSORS.I2C_SCL
I2C_SENSORS.I2C_SDA
I2C_P3.I2C_SCL
I2C_P3.I2C_SDA
I2C_P4.I2C_SCL
I2C_P4.I2C_SDA
VIOC_I2C_SCL
VIOC_I2C_SDA
I2C_MCU_EEP_SDA
I2C_MCU_EEP_SCL
J9
292161-3
J12
292161-3
Y2
32.768KHz
MCU UART
UART_INVALID_B
MCU_UART_INVALID_B
UART_MCU{UART2_BUS}
UART2_MCU{UART2_BUS}
U8
24AA02E48T-I/OT
I2C_MCU_EEP_SDA
I2C_MCU_EEP_SCL
I2C to current sensors
I2C_SENSORS{I2C_BUS}
I2C_SENSORS.I2C_SCL
I2C_SENSORS.I2C_SDA
SYZYGY I2C PORTS
I2C_P3{I2C_BUS}
I2C_P4{I2C_BUS}
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Board MCU controlls the VIO power and SYZYGY ports
electrodyssey.net
Sheet: /MCU/
File: mcu.kicad_sch
Title: NASR-M
rel: Fletched Bustard
Size: A3
Date: 2025-10-22
Rev: D 0.9.5
KiCad E.D.A. 9.0.6
Id: 4/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Onboard clock generator with optional external synchronization
electrodyssey.net

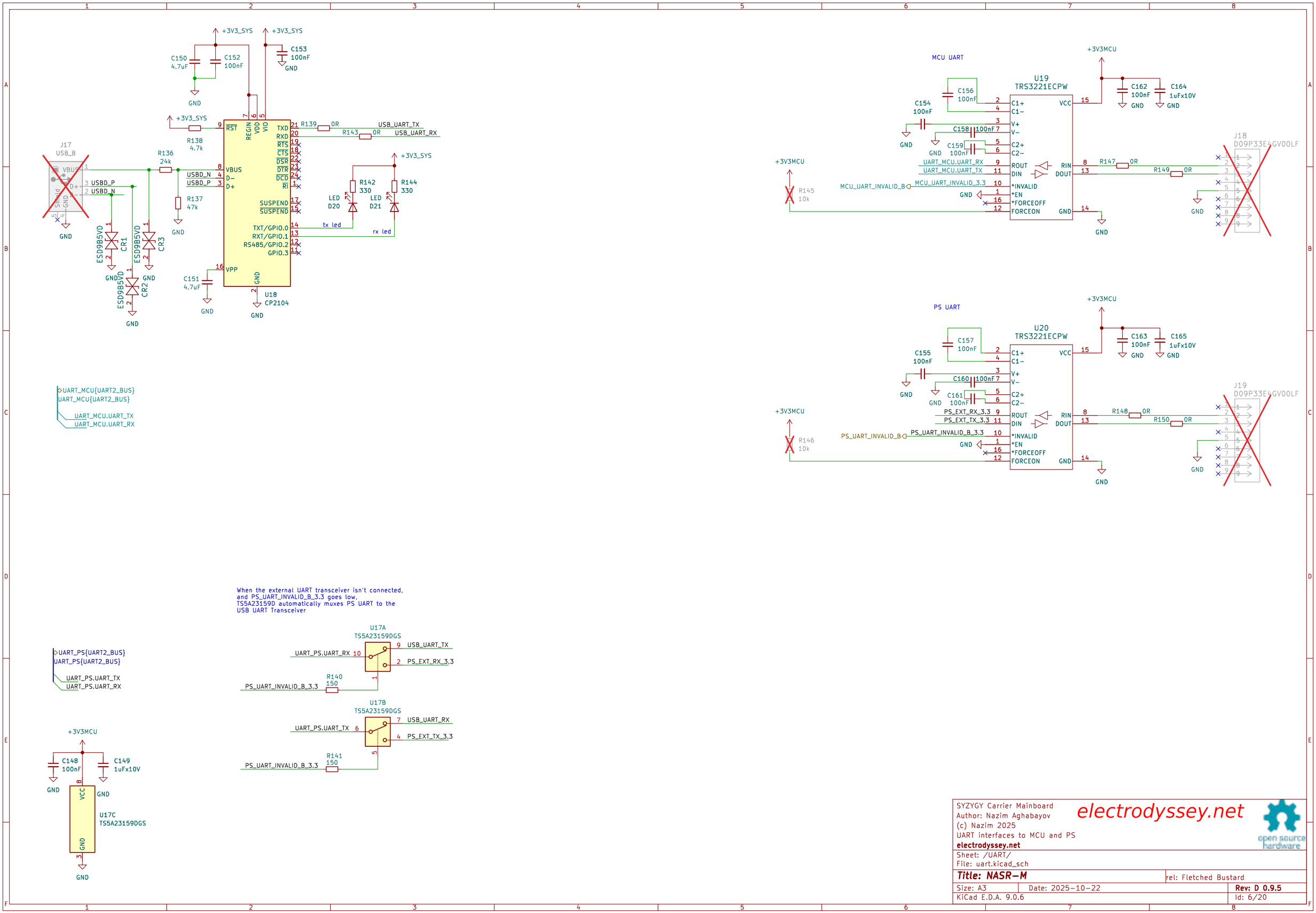
electrodyssey.net

Sheet: /Clock Generator/
File: clockgen.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**
KiCad E.D.A. 9.0.6 | Id: 5/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
UART interfaces to MCU and PS
electrodyssey.net

electrodyssey.net

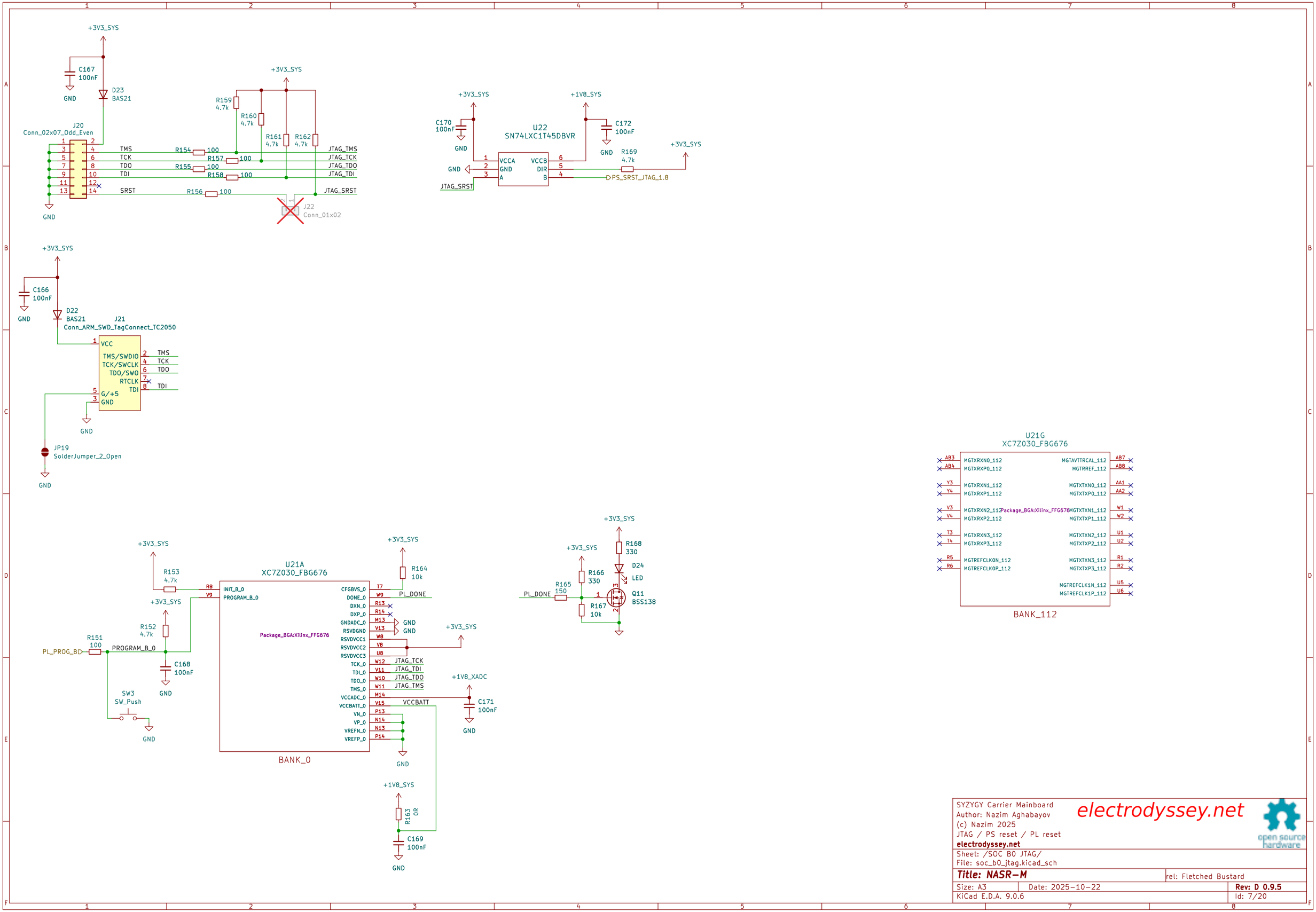
open source hardware

Sheet: /UART/
File: uart.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**
KiCad E.D.A. 9.0.6 | Id: 6/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
JTAG / PS reset / PL reset
electrodyssey.net

electrodyssey.net

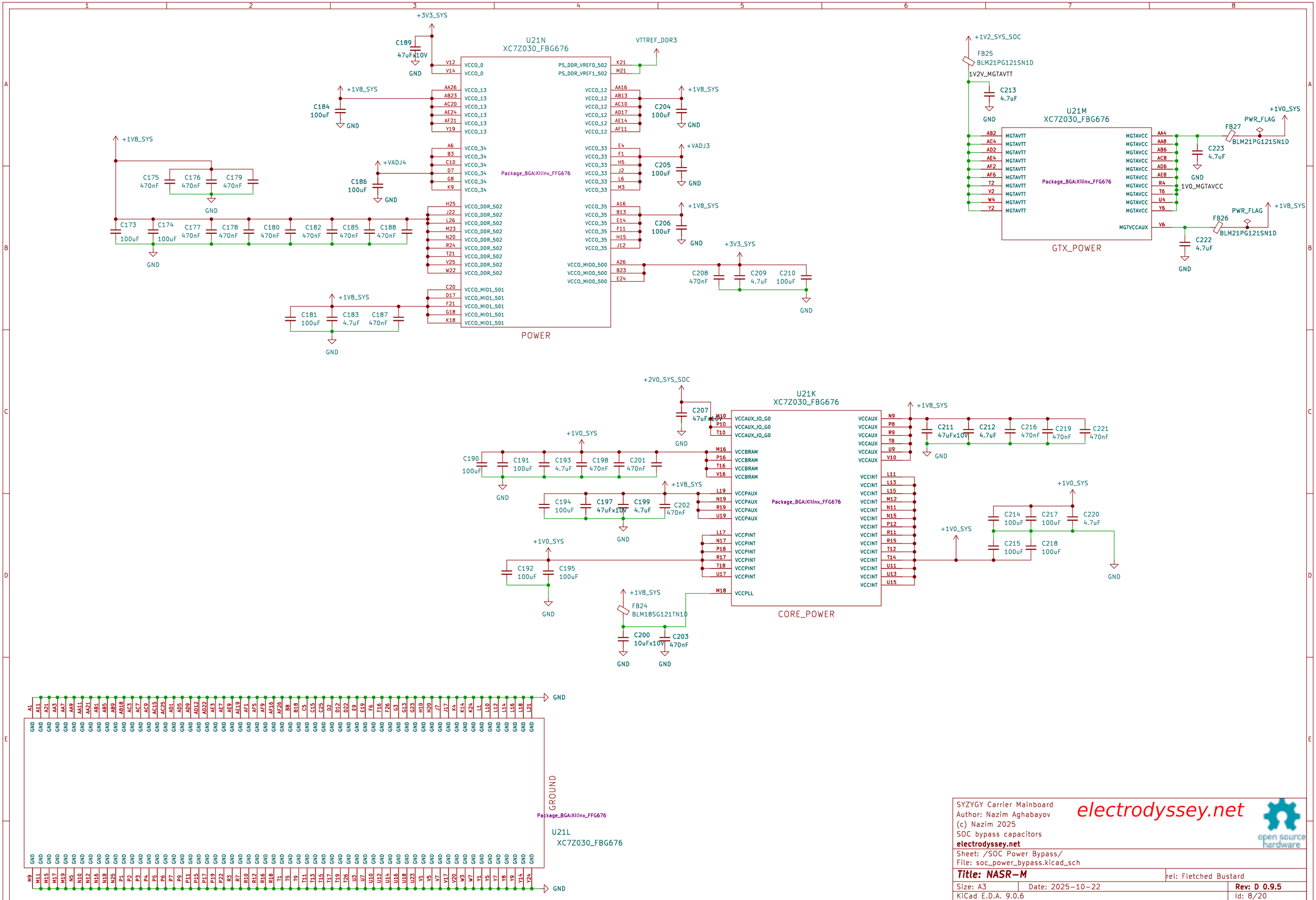
open source hardware

Sheet: /SOC B0 JTAG/
File: soc_b0_jtag.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**
KiCad E.D.A. 9.0.6 | Id: 7/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
SOC bypass capacitors
electrodyssey.net

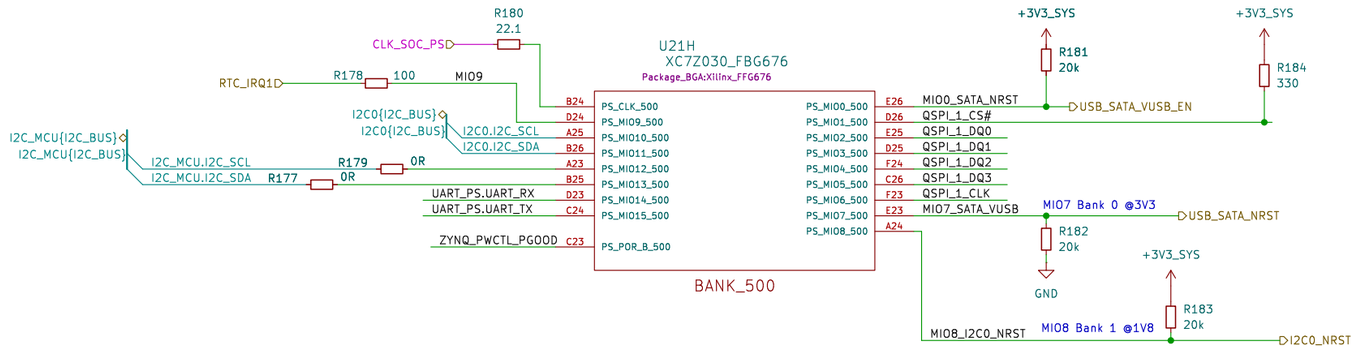
electrodyssey.net

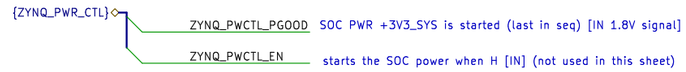
Sheet: /SOC Power Bypass/
File: soc_power_bypass.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**
KiCad E.D.A. 9.0.6 | Id: 8/20





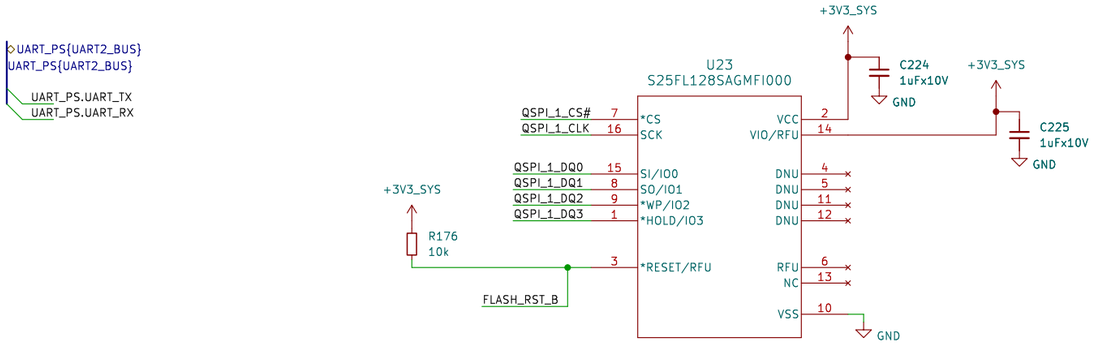
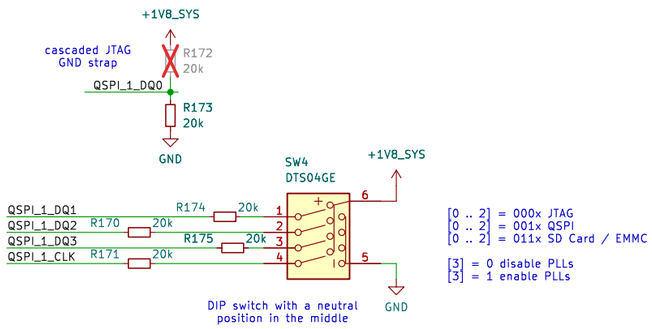


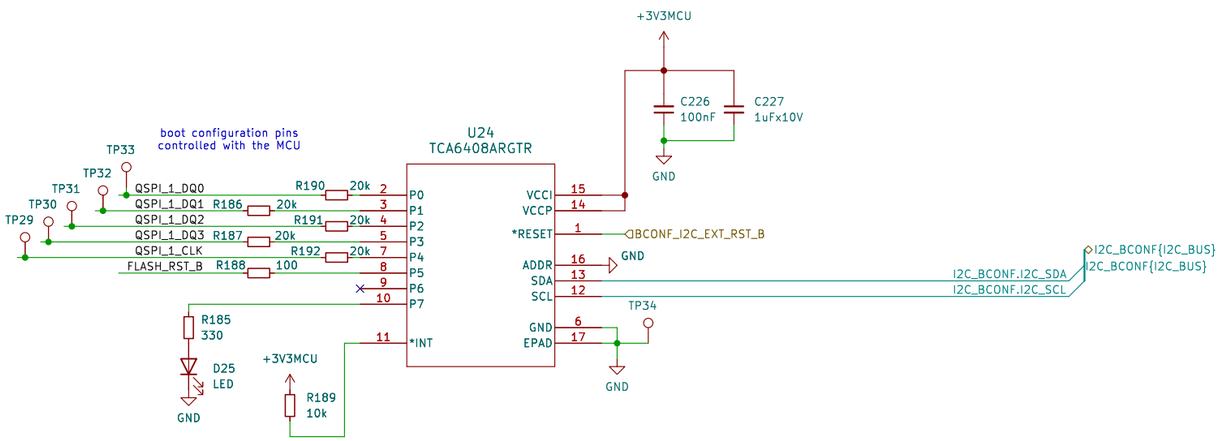
Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common[1]				0	0	0	**JTAG Chain Routing[2]** 0: Cascade mode 1: Independent mode
NOR Boot[3]				0	0	1	
NAND				0	1	0	
Quad-SPI[3]				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage[4]							
	Bank 1	**Bank 0**	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
2.5 V, 3.3 V	0	0					
1.8 V	1	1					

Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.





SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Bank 500; QSPI / Boot mode switches / POR
electrodyssey.net

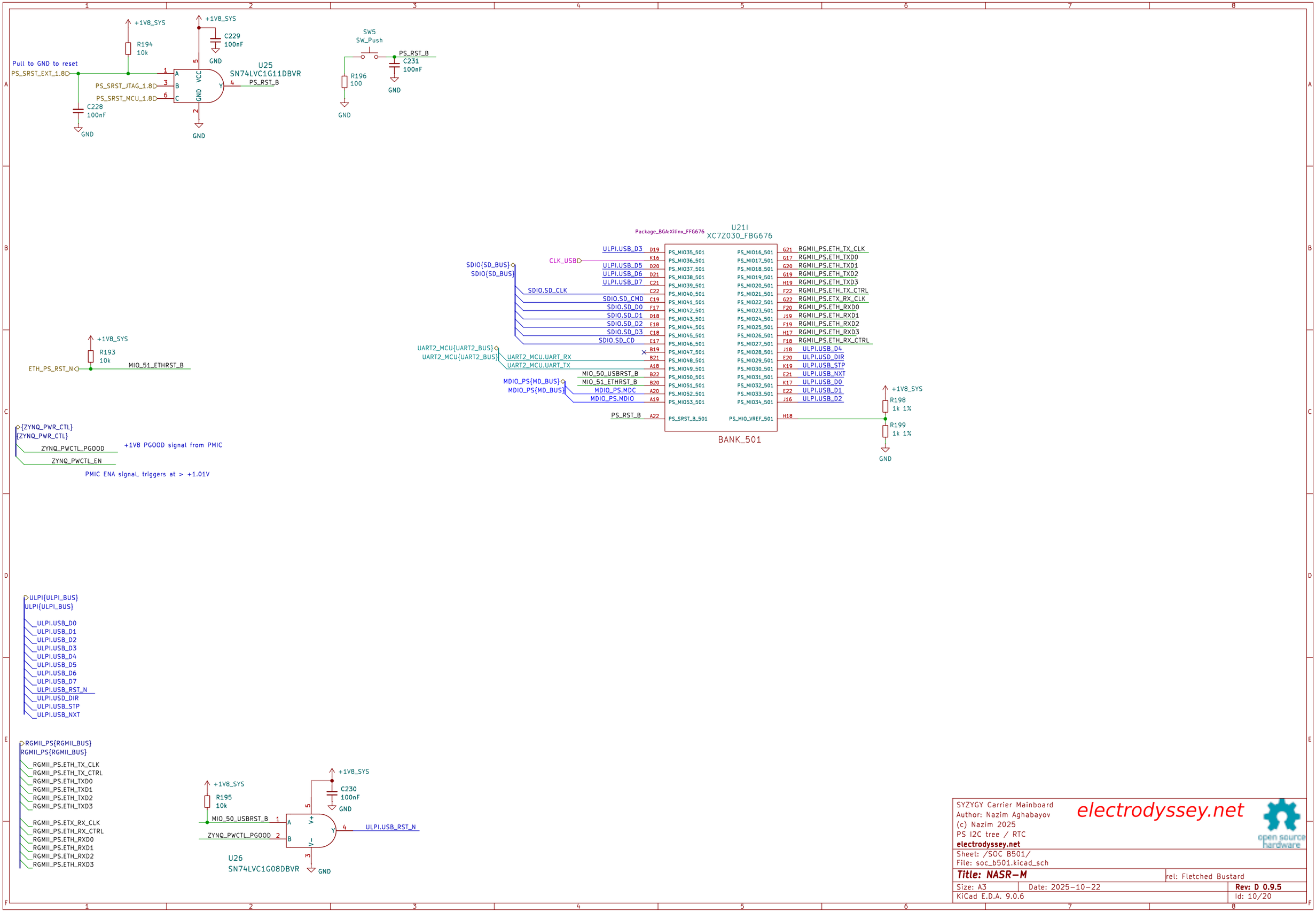
electrodyssey.net

Sheet: /SOC B500 POR QSPI/
File: soc_bank500.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**
KiCad E.D.A. 9.0.6 | Id: 9/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
PS I2C tree / RTC
electrodyssey.net

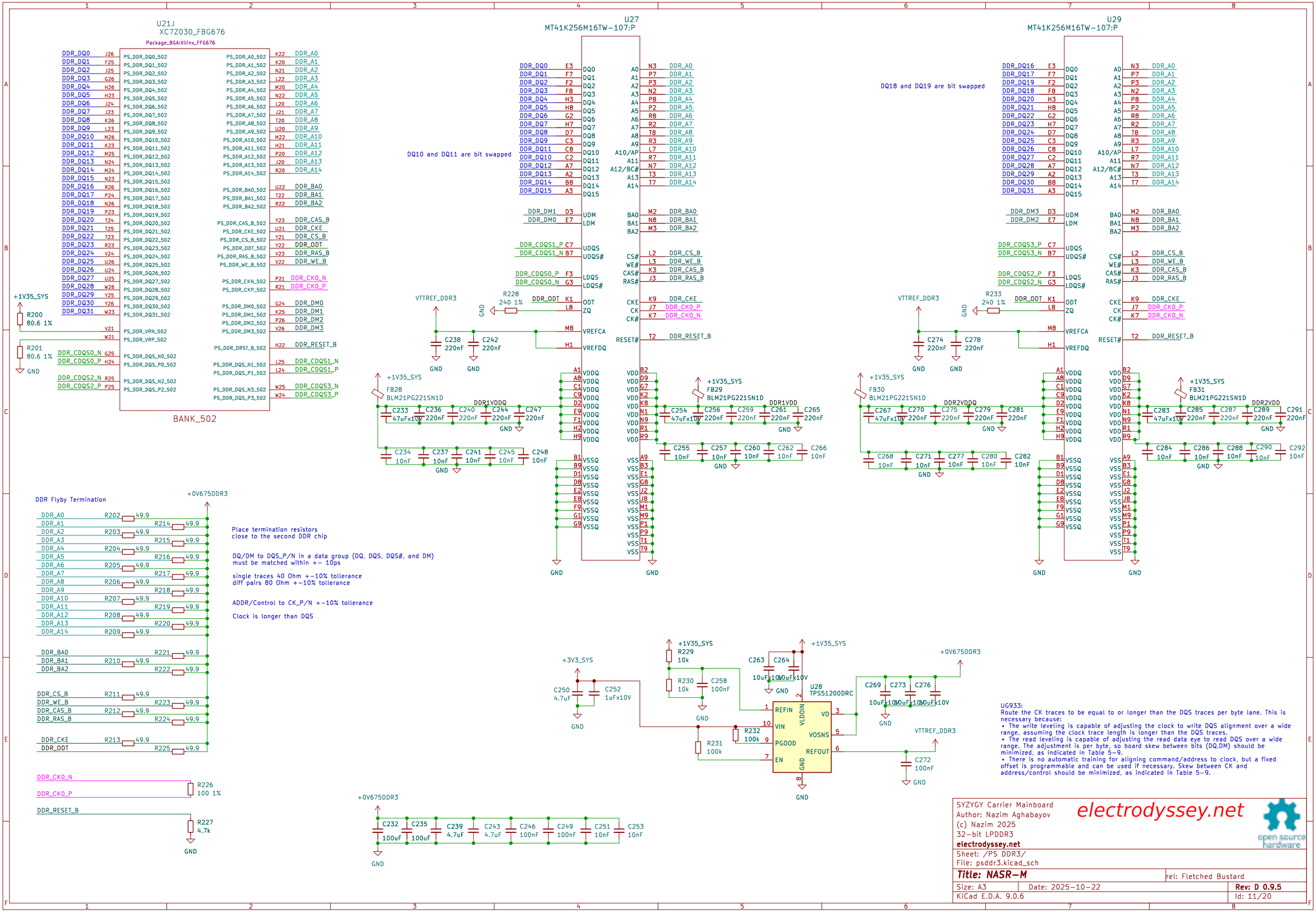
Sheet: /SOC B501/
File: soc_b501.kicad_sch

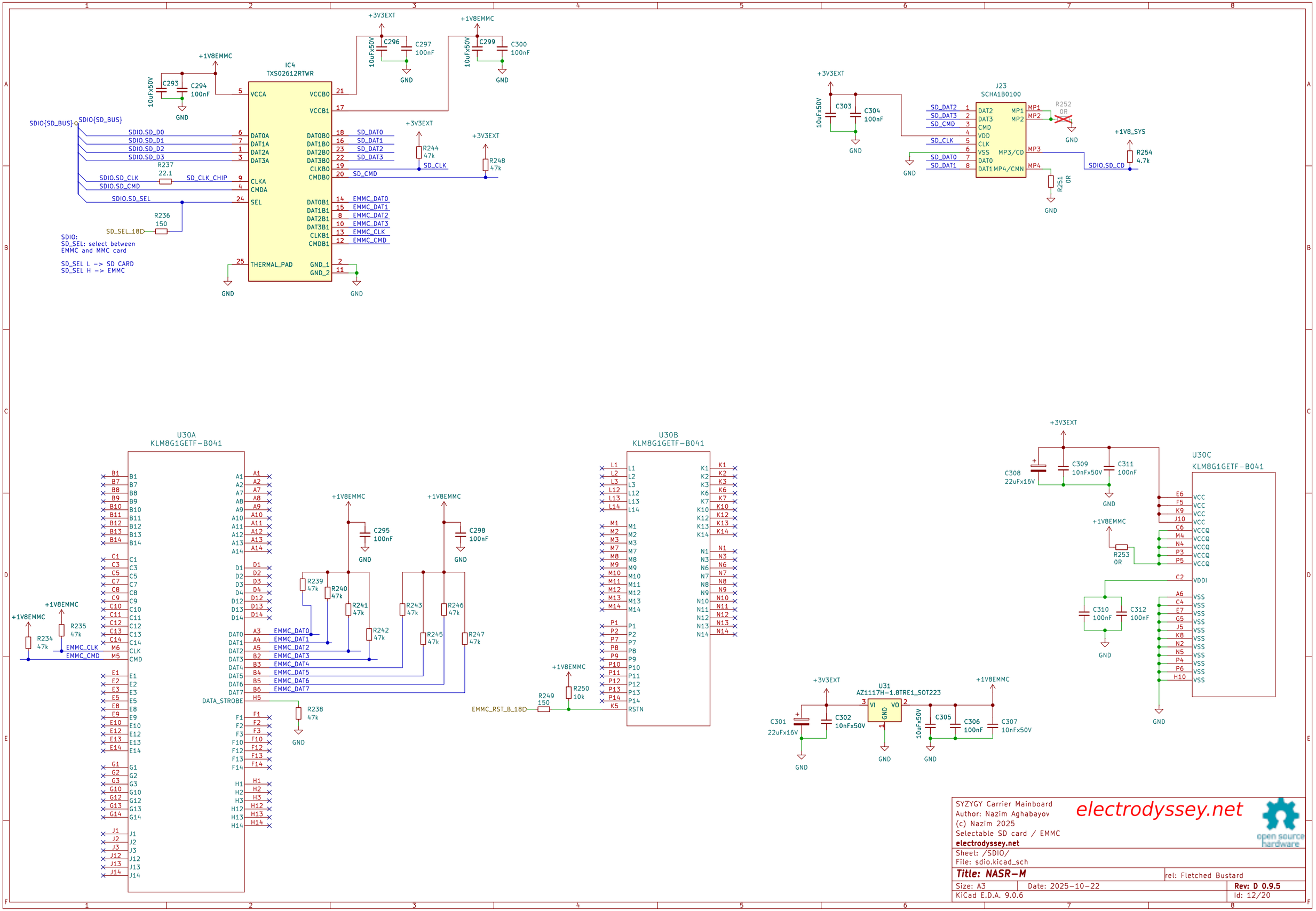
Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**

KiCad E.D.A. 9.0.6 | Id: 10/20


U21J
XC7Z030_FBG676
Package_BGA:Xilinx_FFG676
BANK_502
U27
MT41K256M16TW-107:P
U29
MT41K256M16TW-107:P
DQ10 and DQ11 are bit swapped
DQ18 and DQ19 are bit swapped
DDR Flyby Termination
+0V675DDR3
Place termination resistors
close to the second DDR chip
DQ/DM to DQS_P/N in a data group (DQ, DQS, DQS#, and DM)
must be matched within +- 10ps
single traces 40 Ohm +-10% tollerance
diff pairs 80 Ohm +-10% tollerance
ADDR/Control to CK_P/N +-10% tollerance
Clock is longer than DQS
U28
TPS51200DRC
UG933:
Route the CK traces to be equal to or longer than the DQS traces per byte lane. This is
necessary because:
• The write leveling is capable of adjusting the clock to write DQS alignment over a wide
range, assuming the clock trace length is longer than the DQS traces.
• The read leveling is capable of adjusting the read data eye to read DQS over a wide
range. The adjustment is per byte, so board skew between bits (DQ,DM) should be
minimized, as indicated in Table 5-9.
• There is no automatic training for aligning command/address to clock, but a fixed
offset is programmable and can be used if necessary. Skew between CK and
address/control should be minimized, as indicated in Table 5-9.
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
32-bit LPDDR3
electrodyssey.net
Sheet: /PS DDR3/
File: psddr3.kicad_sch
Title: NASR-M
rel: Fletched Bustard
Size: A3
Date: 2025-10-22
Rev: D 0.9.5
KiCad E.D.A. 9.0.6
Id: 11/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Selectable SD card / EMMC
electrodyssey.net

electrodyssey.net

open source hardware

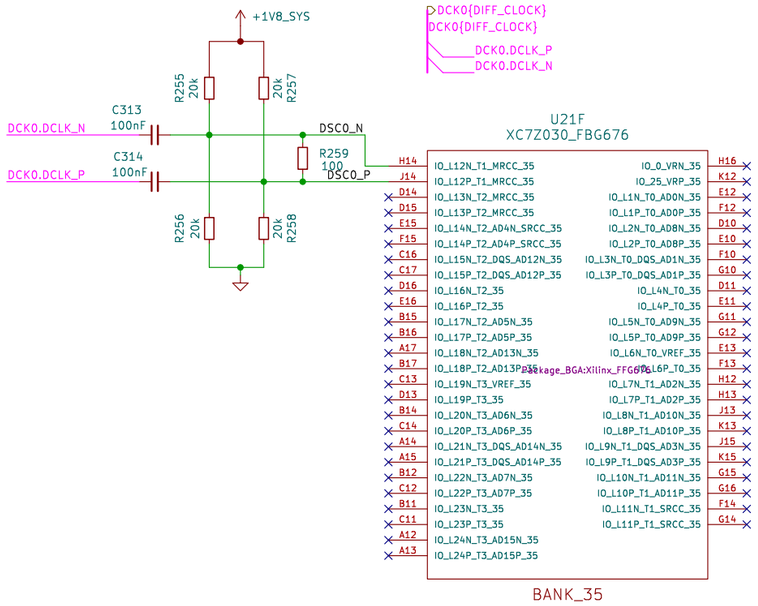
Sheet: /SDIO/
File: sdio.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**

KiCad E.D.A. 9.0.6 | Id: 12/20



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Clock Generator pair 0 to MRCC
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Sheet: /SOC B35/
File: soc_b35.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**

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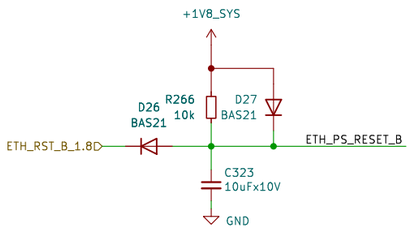

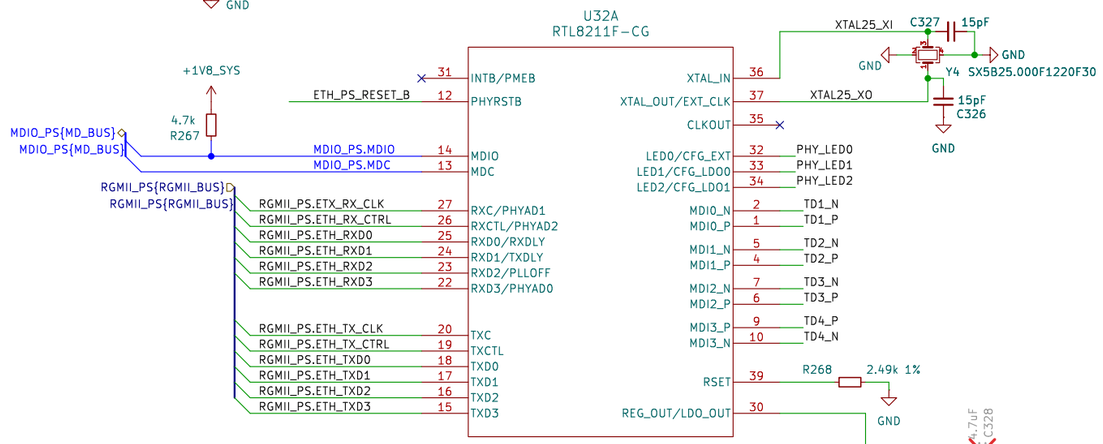

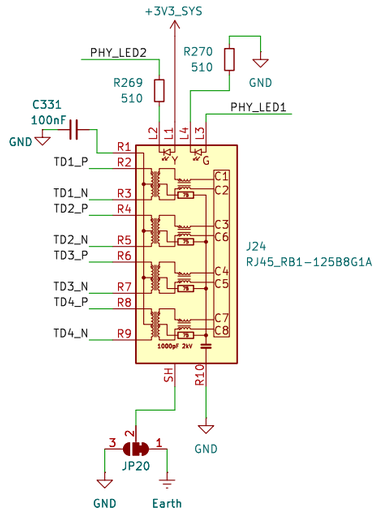

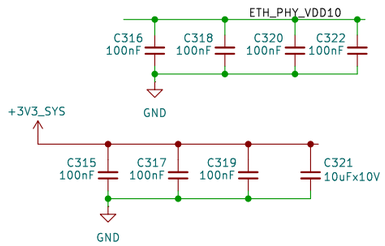

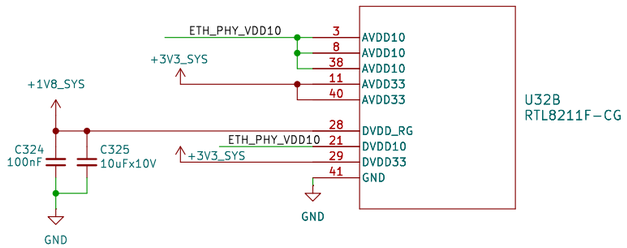

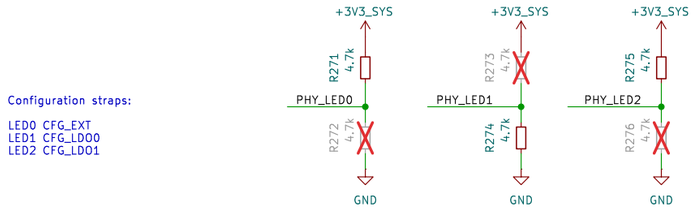

Table 10. CONFIG Pins vs. Configuration Register

CONFIG Pin	Configuration
RXD3	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD2	PLLOFF
RXD1	TXDLY
RXD0	RXDLY
LED0	CFG_EXT
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]

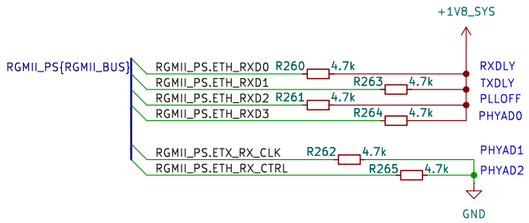

Table 11. Configuration Register Definitions

Configuration	Description
PHYAD[2:0]	PHY Address. PHYAD sets the PHY address for the device. The RTL8211F(I)/ RTL8211FD(I) supports PHY addresses from 00001 to 00111. *Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Reg24.13=0 (See Table 37).* *Note 2: The RTL8211F(I)/ RTL8211FD(I) with PHYAD[2:0]=000 can automatically remember the first non-zero PHY address. This function can be enabled by setting Reg24.6 = 1 (See Table 37).*
PLLOFF	ALDPS Mode PLL Off Configuration. 1: Stop PLL when entering ALDPS mode (via 4.7k-ohm to DVDD_RG) 0: PLL continue toggling when entering ALDPS mode (via 4.7k-ohm to GND)
TXDLY	RGMII Transmit Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG) 0: No delay (via 4.7k-ohm to GND)
RXDLY	RGMII Receive Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG) 0: No delay (via 4.7k-ohm to GND)
CFG_EXT	I/O Pad External Power Source Mode Configuration. 1: Use the external power source for the IO pad (via 4.7k-ohm to 3.3V) 0: Use the integrated LDO to transform the desired voltage for the IO pad (via 4.7k-ohm to GND)

32	CFG_EXT	O/LI/PD	IO Pad External Power Source Mode Configuration. Pull up to use the external power source for the IO pad. Pull down to use the integrated LDO to transform the desired voltage for the IO pad.
33	CFG_LDO0	O/LI/PU	LDO Output Voltage Selection for I/O Pad/
34	CFG_LDO1	O/LI/PD	External Power Source Voltage Selection for I/O Pad. When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved. 2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V. When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for input voltage selection of the external power for IO pad: 2'b00: 3.3V. 2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V.

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Sheet: /Ethernet PS/
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Title: NASR-M rel: Fletched Bustard

Size: A3 Date: 2025-10-22 **Rev: D 0.9.5**
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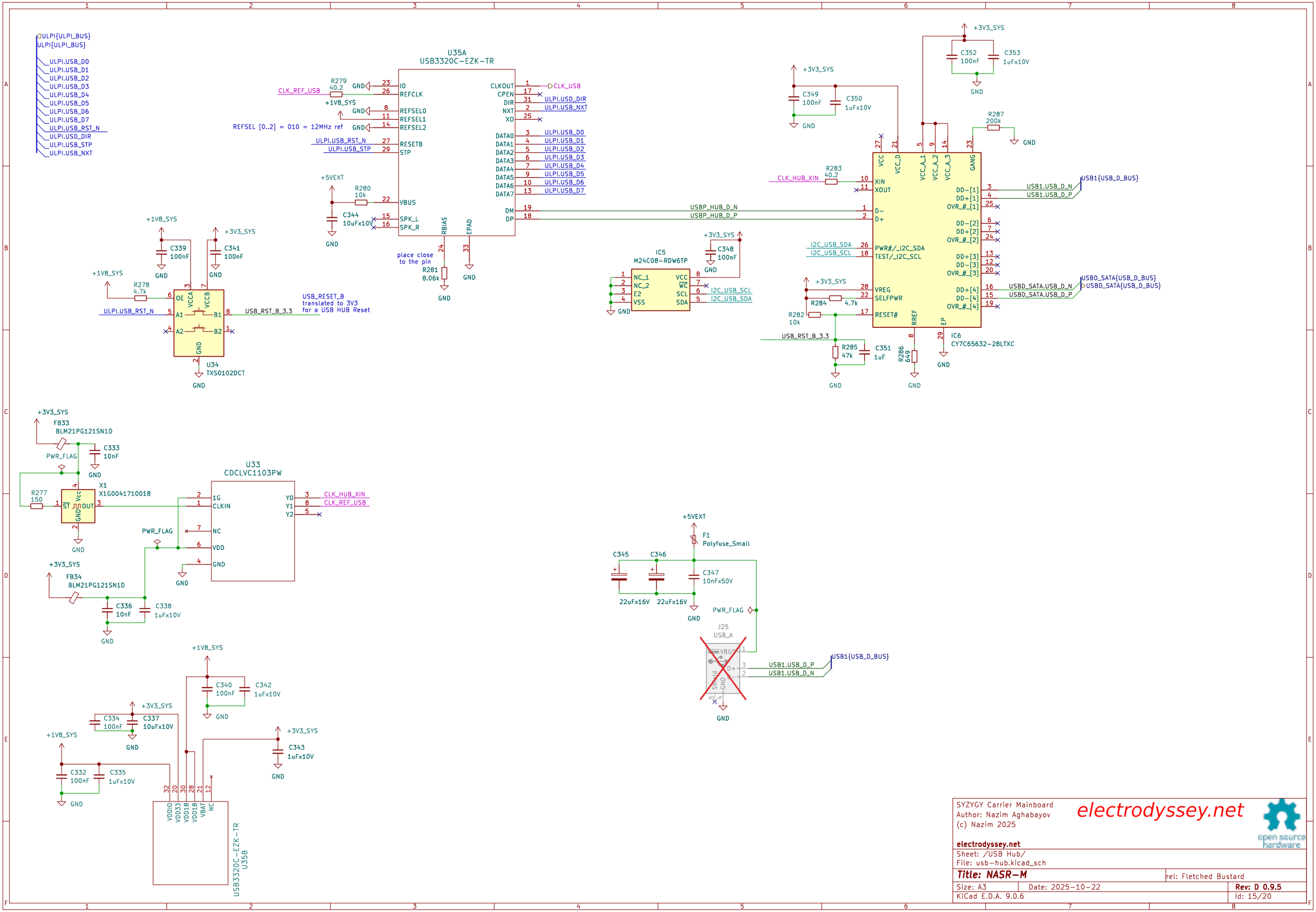

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Sheet: /USB Hub/
File: usb-hub.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**

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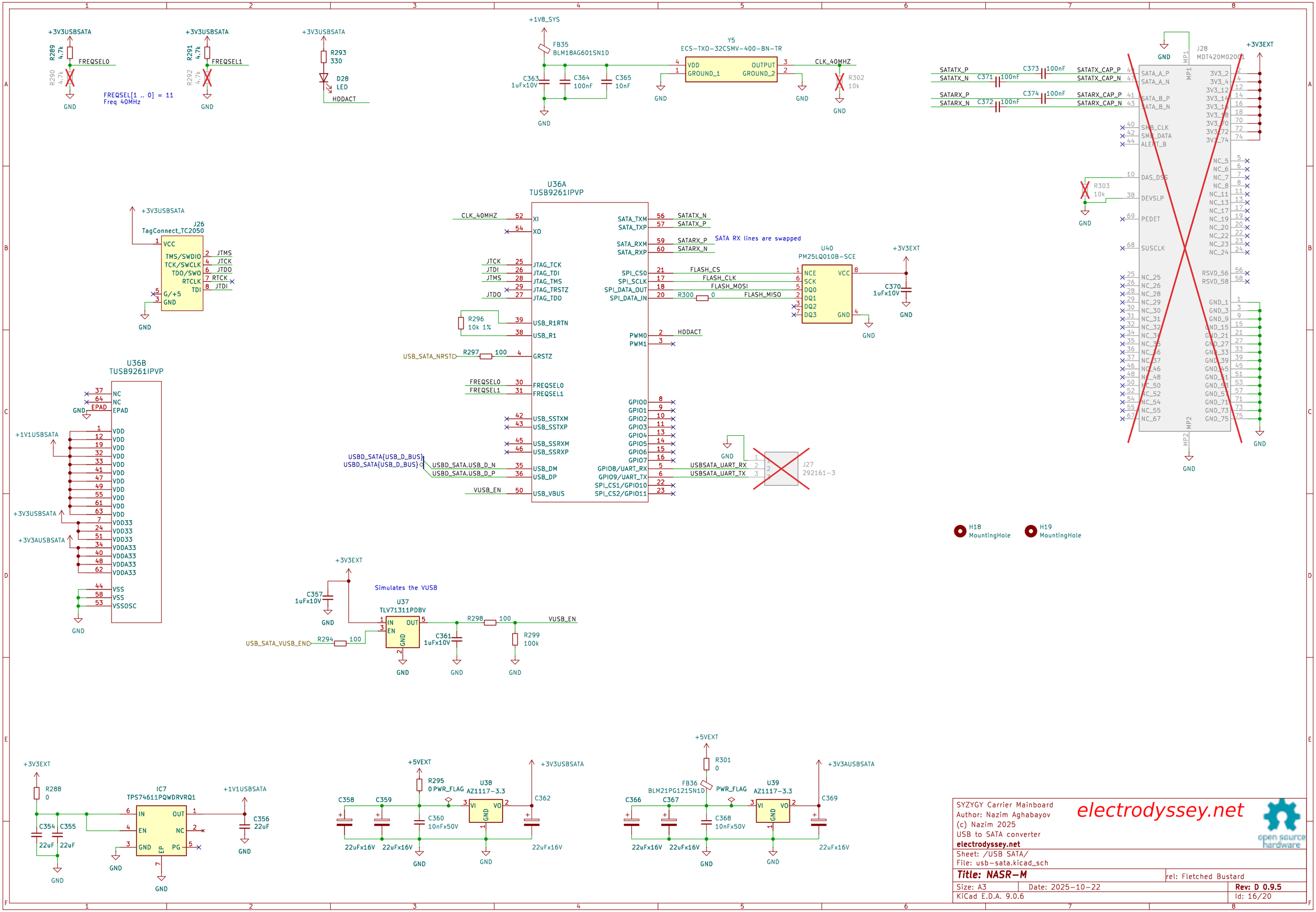
+3V3USBSATA
R289 4.7k
R290 4.7k
FREQSEL0
GND
FREQSEL[1 .. 0] = 11
Freq 40MHz
R291 4.7k
R292 4.7k
FREQSEL1
R293 330
D28 LED
HDDACT
+1V8_SYS
FB35 BLM18AG601SN1D
C363 1uFx10V
C364 100nF
C365 10nF
Y5
ECS-TXO-32CSMV-400-BN-TR
VDD
GROUND_1
OUTPUT
GROUND_2
CLK_40MHZ
R302 10k
SATATX_P
SATATX_N
SATARX_P
SATARX_N
C371 100nF
C372 100nF
C373 100nF
C374 100nF
SATATX_CAP_P
SATATX_CAP_N
SATARX_CAP_P
SATARX_CAP_N
J28
MDT420M02001
+3V3EXT
R303 10k
DEVSLP
PEDET
SUSCLK
DAS_DSS
SMB_CLK
SMB_DATA
ALERT_B
J26
TagConnect_TC2050
VCC
TMS/SWDIO
TCK/SWCLK
TDO/SWO
RTCLK
TDI
G/+5
JTMS
JTCK
JTDO
RTCK
JTDI
U36A
TUSB9261IPVP
CLK_40MHZ
XI
XO
JTAG_TCK
JTAG_TDI
JTAG_TMS
JTAG_TRSTZ
JTAG_TDO
R296 10k 1%
USB_R1RTN
USB_R1
USB_SATA_NRSTD
R297 100
GRSTZ
FREQSEL0
FREQSEL1
USB_SSTXM
USB_SSTXP
USB_SSRXM
USB_SSRXP
USBD_SATA{USB_D_BUS}
USBD_SATA.USB_D_N
USBD_SATA.USB_D_P
USB_DM
USB_DP
VUSB_EN
USB_VBUS
SATA_TXM
SATA_TXP
SATA_RXM
SATA_RXP
SATATX_N
SATATX_P
SATARX_P
SATARX_N
SATA RX lines are swapped
SPI_CS0
SPI_SCLK
SPI_DATA_OUT
SPI_DATA_IN
FLASH_CS
FLASH_CLK
FLASH_MOSI
FLASH_MISO
R300 0
PWM0
PWM1
HDDACT
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8/UART_RX
GPIO9/UART_TX
SPI_CS1/GPIO10
SPI_CS2/GPIO11
USBSATA_UART_RX
USBSATA_UART_TX
J27
292161-3
U40
PM25LQ010B-SCE
NCE
SCK
DQ0
DQ1
DQ2
DQ3
C370 1uFx10V
U36B
TUSB9261IPVP
NC
EPAD
VDD
VDD33
VDDA33
VSS
VSSOSC
+1V1USBSATA
+3V3AUSBSATA
H18 MountingHole
H19 MountingHole
+3V3EXT
C357 1uFx10V
Simulates the VUSB
U37
TLV71311PDBV
IN
EN
OUT
GND
R294 100
USB_SATA_VUSB_END
C361 1uFx10V
R298 100
VUSB_EN
R299 100k
R288 0
IC7
TPS74611PQWDRVRQ1
C354 22uF
C355 22uF
IN
EN
GND
OUT
NC
PG
EP
C356 22uF
+5VEXT
R295 0 PWR_FLAG
U38
AZ1117-3.3
VI
VO
C358 22uFx16V
C359 22uFx16V
C360 10nFx50V
C362 22uFx16V
+3V3USBSATA
R301 0
FB36 BLM21PG121SN1D
PWR_FLAG
U39
AZ1117-3.3
C366 22uFx16V
C367 22uFx16V
C368 10nFx50V
C369 22uFx16V
+3V3AUSBSATA
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
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USB to SATA converter
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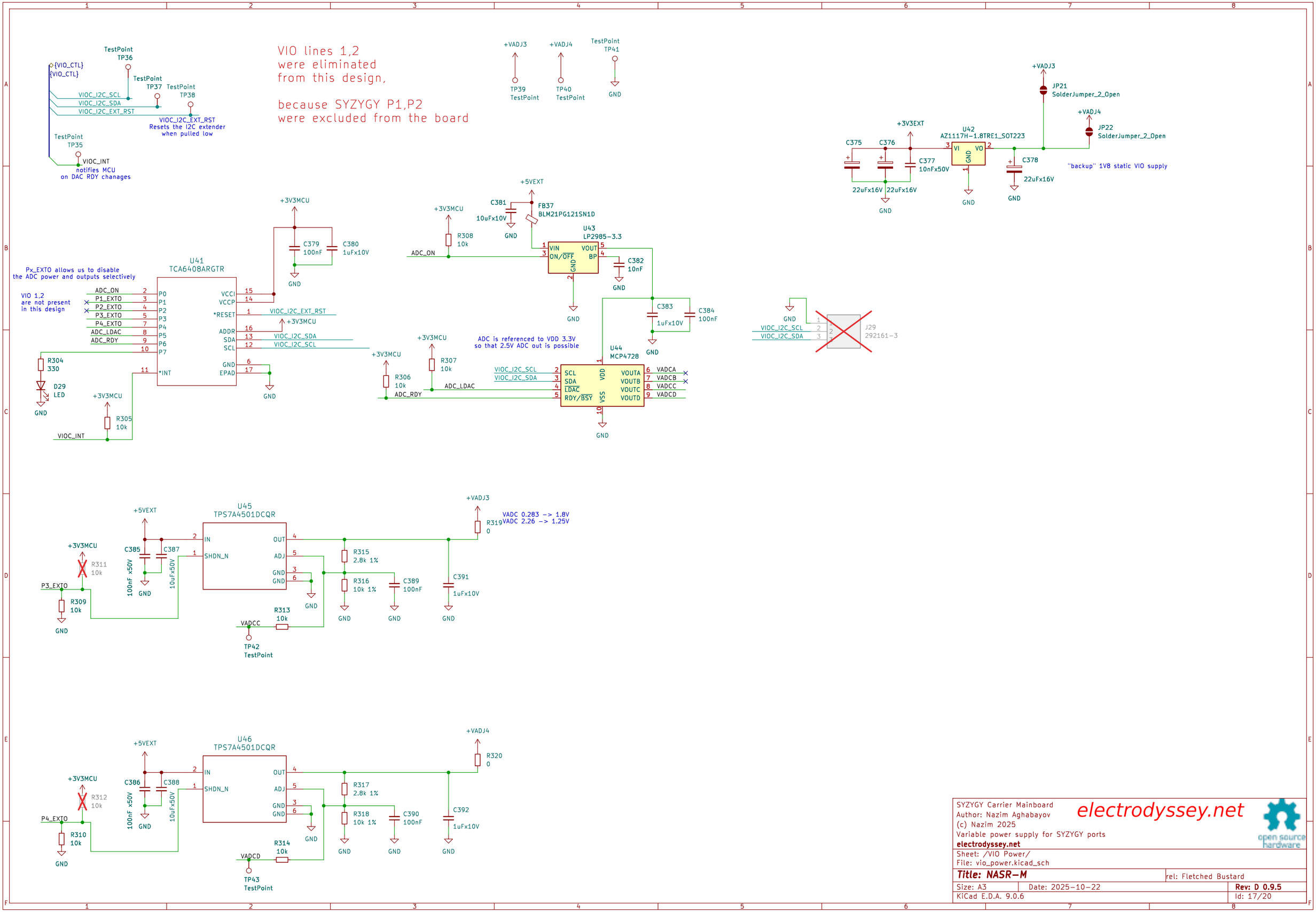
Sheet: /USB SATA/
File: usb-sata.kicad_sch
Title: NASR-M
rel: Fletched Bustard
Size: A3
Date: 2025-10-22
Rev: D 0.9.5
KiCad E.D.A. 9.0.6
Id: 16/20


VIO lines 1,2
were eliminated
from this design,
because SYZYGY P1,P2
were excluded from the board
{VIO_CTL}
{VIO_CTL}
TestPoint
TP36
TestPoint
TP37
TestPoint
TP38
VIOC_I2C_SCL
VIOC_I2C_SDA
VIOC_I2C_EXT_RST
VIOC_I2C_EXT_RST
Resets the I2C extender
when pulled low
TestPoint
TP35
VIOC_INT
notifies MCU
on DAC RDY chanages
+VADJ3
TP39
TestPoint
+VADJ4
TP40
TestPoint
TestPoint
TP41
GND
+VADJ3
JP21
SolderJumper_2_Open
+VADJ4
JP22
SolderJumper_2_Open
+3V3EXT
U42
AZ1117H-1.8TRE1_SOT223
C375
C376
C377
10nFx50V
22uFx16V
22uFx16V
C378
22uFx16V
"backup" 1V8 static VIO supply
+5VEXT
C381
10uFx10V
FB37
BLM21PG121SN1D
U43
LP2985-3.3
VIN
ON/OFF
GND
VOUT
BP
C382
10nF
+3V3MCU
R308
10k
ADC_ON
+3V3MCU
C379
100nF
C380
1uFx10V
U41
TCA6408ARGTR
Px_EXTO allows us to disable
the ADC power and outputs selectively
VIO 1,2
are not present
in this design
ADC_ON
P1_EXTO
P2_EXTO
P3_EXTO
P4_EXTO
ADC_LDAC
ADC_RDY
P0
P1
P2
P3
P4
P5
P6
P7
*INT
VCCI
VCCP
*RESET
ADDR
SDA
SCL
GND
EPAD
VIOC_I2C_EXT_RST
+3V3MCU
VIOC_I2C_SDA
VIOC_I2C_SCL
R304
330
D29
LED
+3V3MCU
R305
10k
VIOC_INT
C383
1uFx10V
C384
100nF
ADC is referenced to VDD 3.3V
so that 2.5V ADC out is possible
U44
MCP4728
+3V3MCU
R306
10k
ADC_RDY
+3V3MCU
R307
10k
ADC_LDAC
VIOC_I2C_SCL
VIOC_I2C_SDA
SCL
SDA
LDAC
RDY/BSY
VDD
VSS
VOUTA
VOUTB
VOUTC
VOUTD
VADCA
VADCB
VADCC
VADCD
J29
292161-3
U45
TPS7A4501DCQR
+5VEXT
+3V3MCU
C385
100nF x50V
C387
10uFx50V
R311
10k
P3_EXTO
R309
10k
IN
SHDN_N
OUT
ADJ
GND
GND
+VADJ3
VADC 0.283 -> 1.8V
VADC 2.26 -> 1.25V
R319
0
R315
2.8k 1%
R316
10k 1%
C389
100nF
C391
1uFx10V
R313
10k
VADCC
TP42
TestPoint
U46
TPS7A4501DCQR
+5VEXT
+3V3MCU
C386
100nF x50V
C388
10uFx50V
R312
10k
P4_EXTO
R310
10k
IN
SHDN_N
OUT
ADJ
GND
GND
+VADJ4
R320
0
R317
2.8k 1%
R318
10k 1%
C390
100nF
C392
1uFx10V
R314
10k
VADCD
TP43
TestPoint
SYZYGY Carrier Mainboard
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Variable power supply for SYZYGY ports
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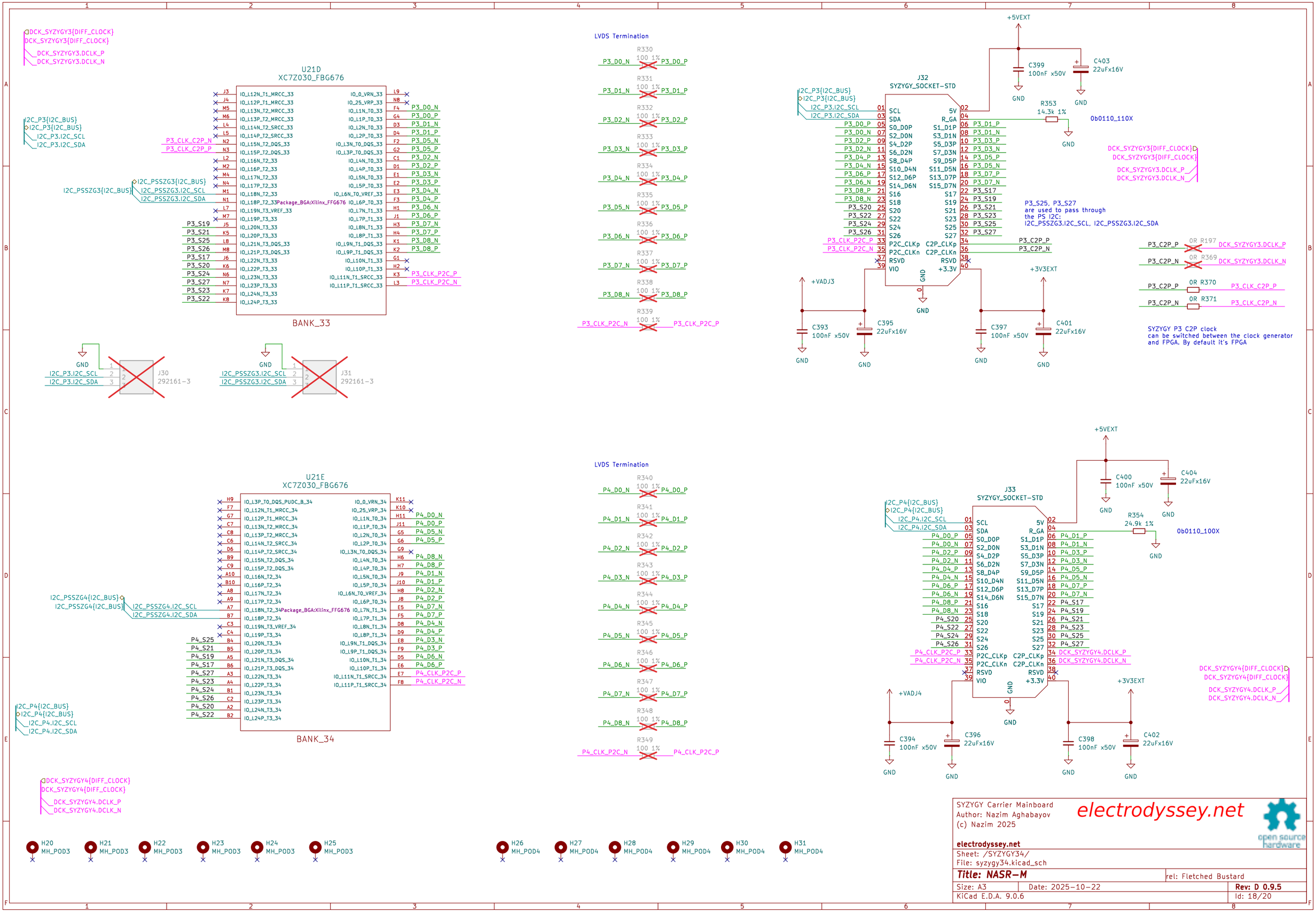
Sheet: /VIO Power/
File: vio_power.kicad_sch
Title: NASR-M
rel: Fletched Bustard
Size: A3
Date: 2025-10-22
Rev: D 0.9.5
KiCad E.D.A. 9.0.6
Id: 17/20



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Sheet: /SYZYGY34/
File: syzygy34.kicad_sch

Title: NASR-M | rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**
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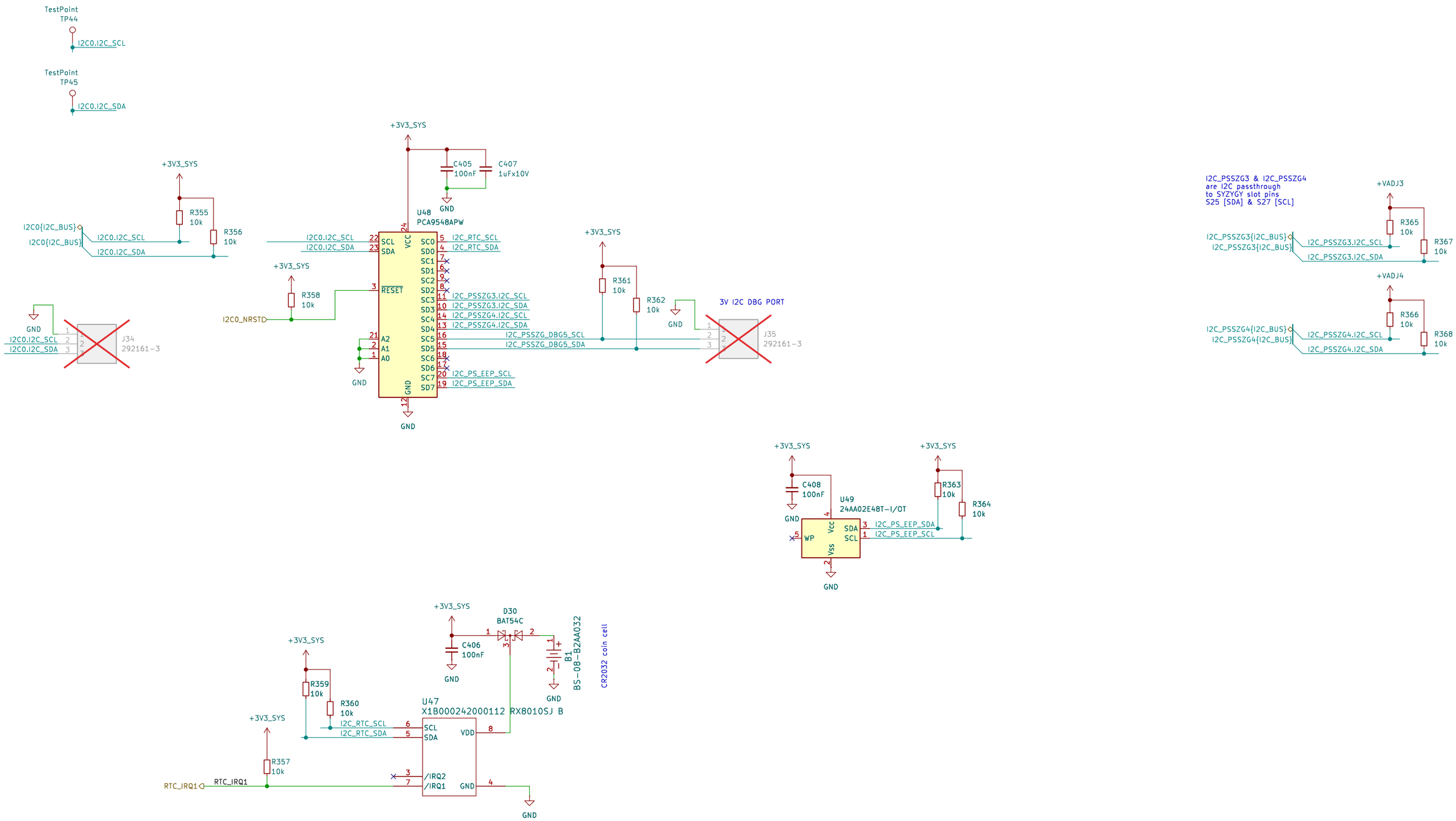

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Sheet: /SOC I2C/
File: soc_i2c.kicad_sch

Title: NASR-M

rel: Fletched Bustard

Size: A3 | Date: 2025-10-22 | **Rev: D 0.9.5**

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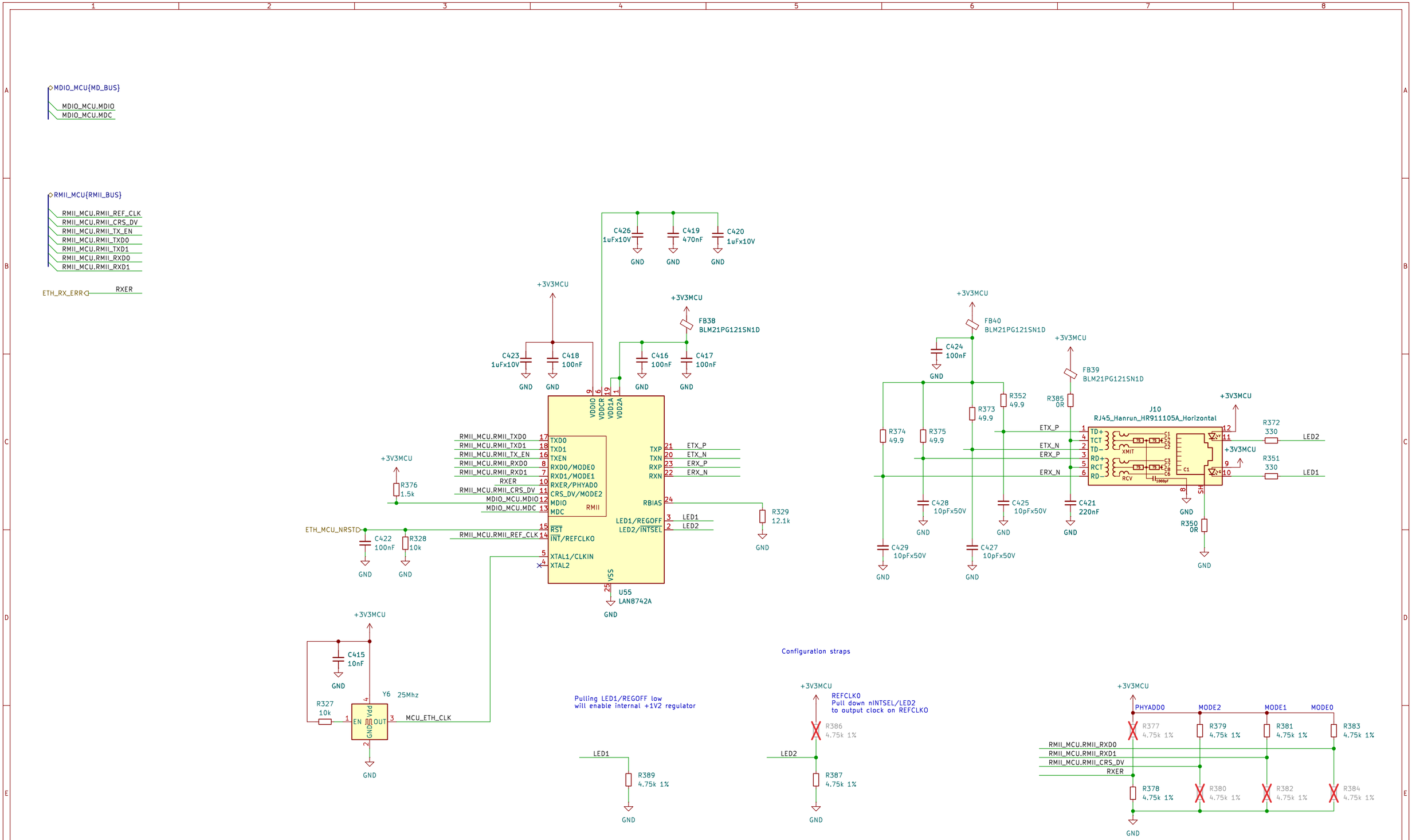

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Sheet: /Ethernet MCU/
File: eth_mcu.kicad_sch

Title: NASR-M		rel: Fletched Bustard
Size: A3	Date: 2025-10-22	**Rev: D 0.9.5**
KiCad E.D.A. 9.0.6		Id: 20/20