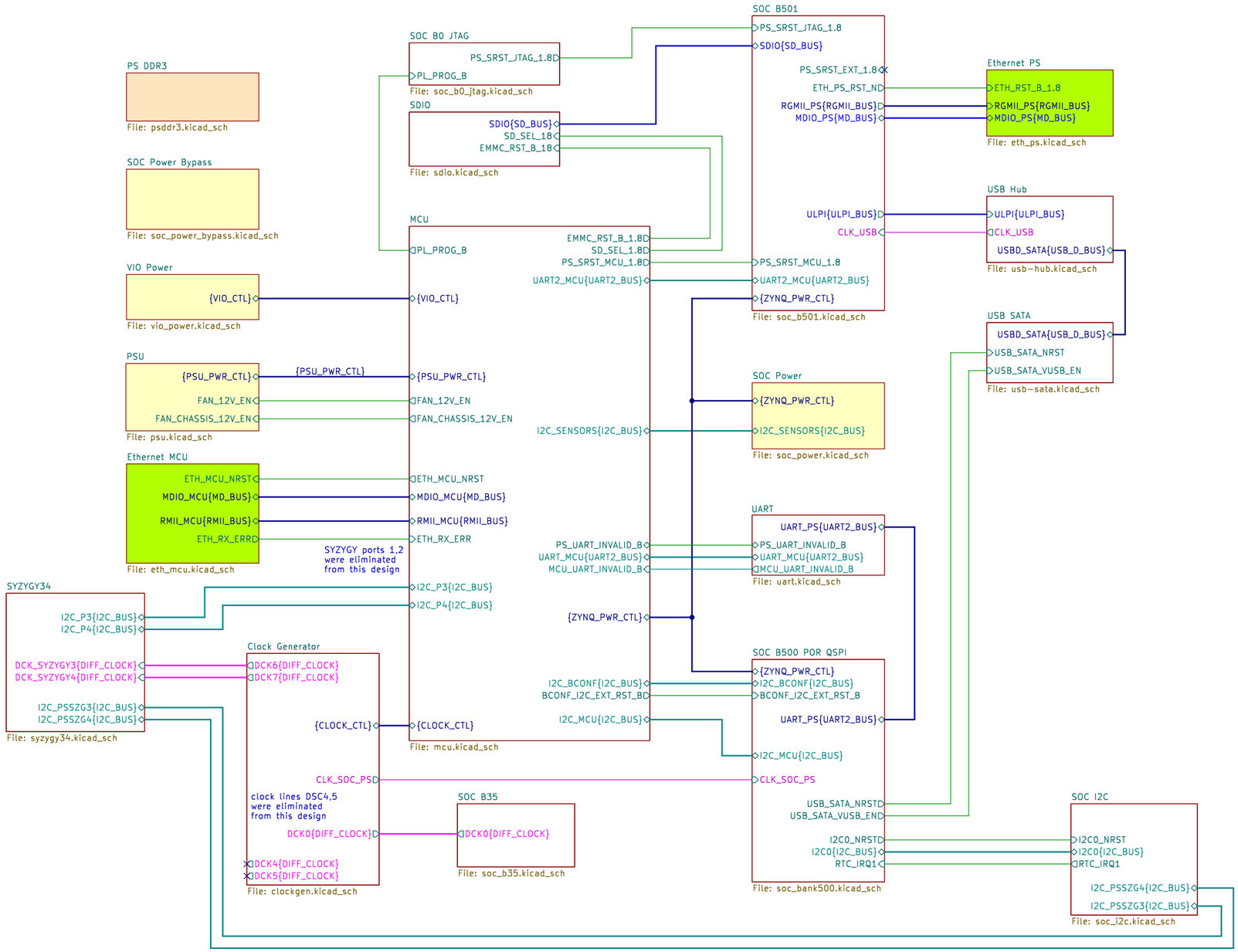


PAGE	DESCRIPTION
1 ROOT PAGE	Block Diagram of the project
2 PSU	ATX PSU connector and filters
3 SOC Power	A secondary power supply for SOC
4 MCU	MCU
5 Clock Generator	Clocks for SOC and SYZYGY, external master sync
6 UART	UART peripherals
7 SOC B0 JTAG	SOC JTAG
8 SOC Power Bypass	SOC bypass capacitors
9 SOC B500 POR QSPI	Power on reset, QSPI, SOC boot config
10 SOC B501	Peripheral resets, ULPI and RGMII buses
11 PS DDR3	DDR3 RAM for SOC PS sybsystem
12 SDIO	SDIO and EMMC shared bus
13 SOC B35	A redundant clock for SOC PS
14 Ethernet PS	RGMII Ethernet peripheral
15 USB Hub	USB ULPI transceiver and hub
16 USB SATA	USB SATA converter and SATA SSD socket
17 VIO Power	Variable IO power for SYZYGY slots
18 SYZYGY34	SYZYGY slots
19 SOC I2C	SOC I2C
20 Ethernet MCU	10/100 RMII Ethernet for MCU

Stackup JLC10161H-2116(1.57mm±10%)

F.Cu, B.Cu:
diff 80Ohm track / spacing: 8.28/6 mil; 0.2103/0.1524 mm
single 40Ohm: 11.23 mil; 0.2852 mm

diff 100Ohm track / spacing: 5.58/8 mil; 0.1417/0.2032 mm
single 50Ohm: 7.36mil; 0.1869 mm

In3, In5, In7 internal layers:
diff 80Ohm: 6.44/8 mil; 0.1636/0.2032 mm
single 40Ohm: 7.03mil; 0.1786 mm

diff 100Ohm: 4.29/11 mil; 0.1090/0.2794 mm
single 50Ohm: 4.54mil; 0.1153 mm

NOTE:
SYZYGY ports 1,2
were eliminated
from this design

H1 MH1_M3
H2 MH2_M3
H3 MH3_M3
H4 MH4_M3
H34 MH4_M3
H35 MH4_M3
JP1 SolderJumper_2_Open
R1 0R
GND

H5 EARTH_MH_M3
H6 MountingHole
H7 MountingHole
H8 MountingHole
H9 MountingHole
H10 MountingHole
H11 MountingHole
H12 MountingHole
H13 MountingHole
H14 MountingHole
H15 MountingHole
H16 MountingHole
H17 MountingHole
H32 MountingHole
H33 MountingHole

SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Top Level Schema
electrodyssey.net

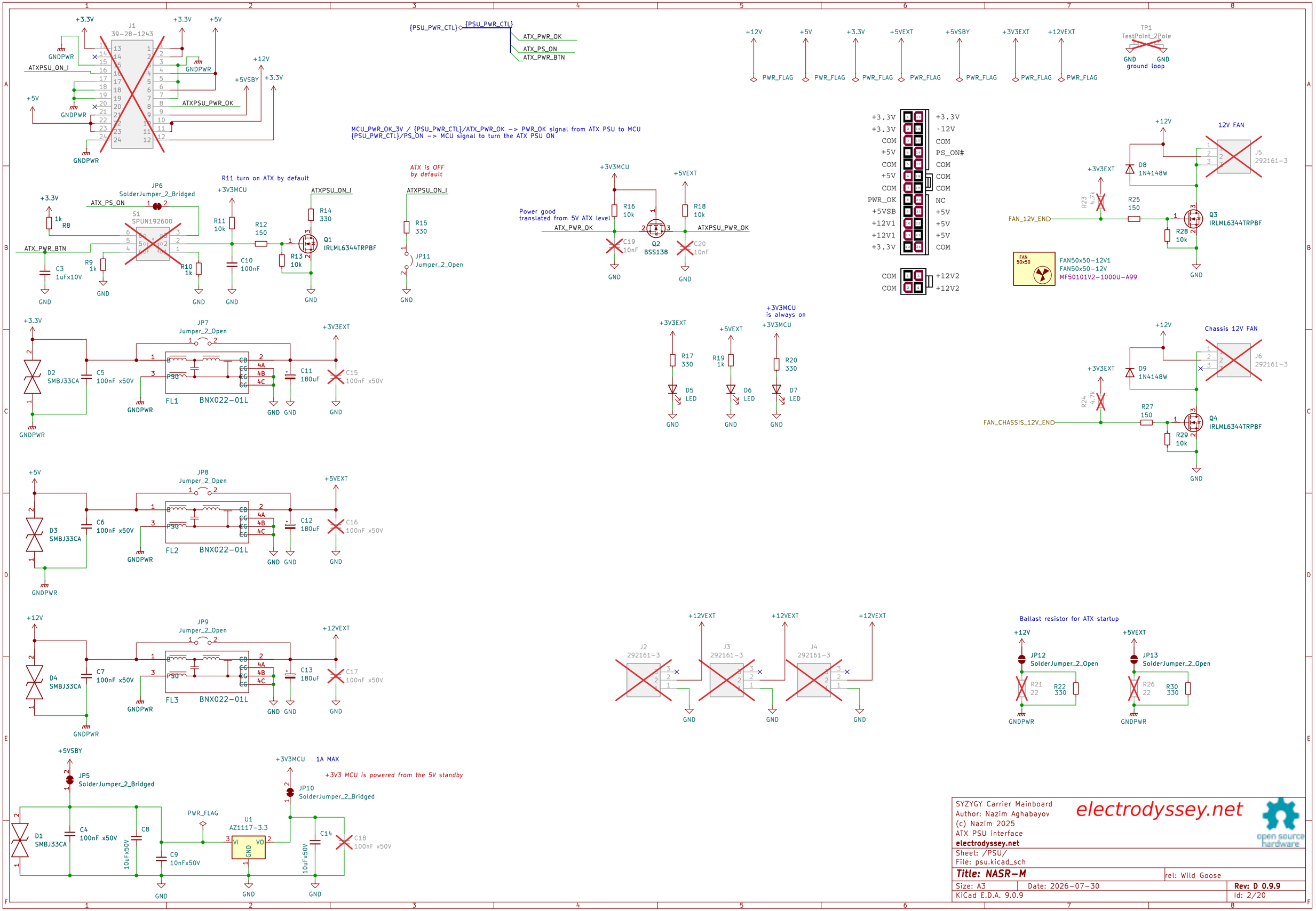
electrodyssey.net

Sheet: /
File: NASR.kicad_sch

Title: NASR-M

rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**
KiCad E.D.A. 9.0.9 | Id: 1/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
ATX PSU interface
electrodyssey.net

electrodyssey.net

open source hardware

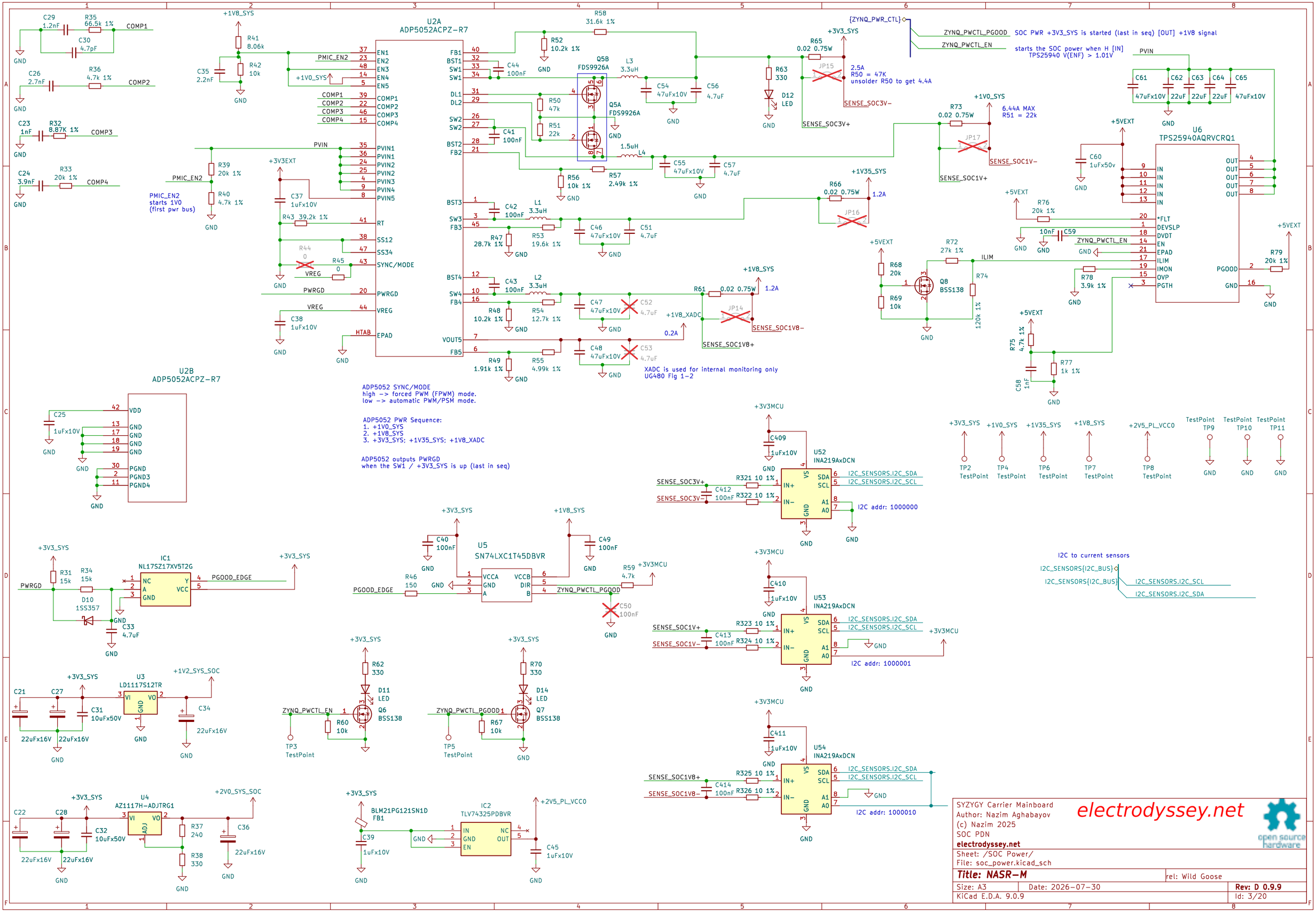
Sheet: /PSU/
File: psu.kicad_sch

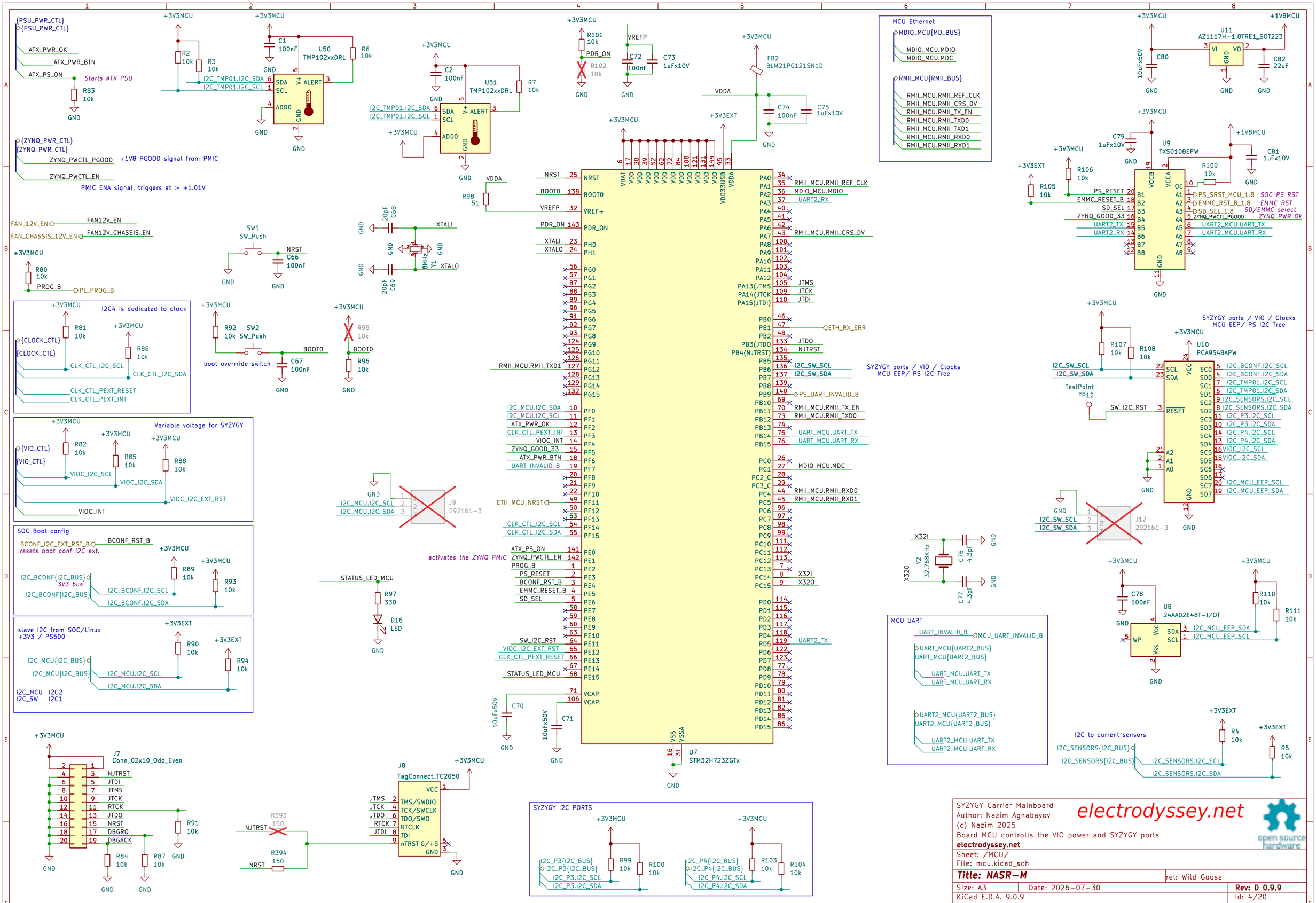
Title: NASR-M

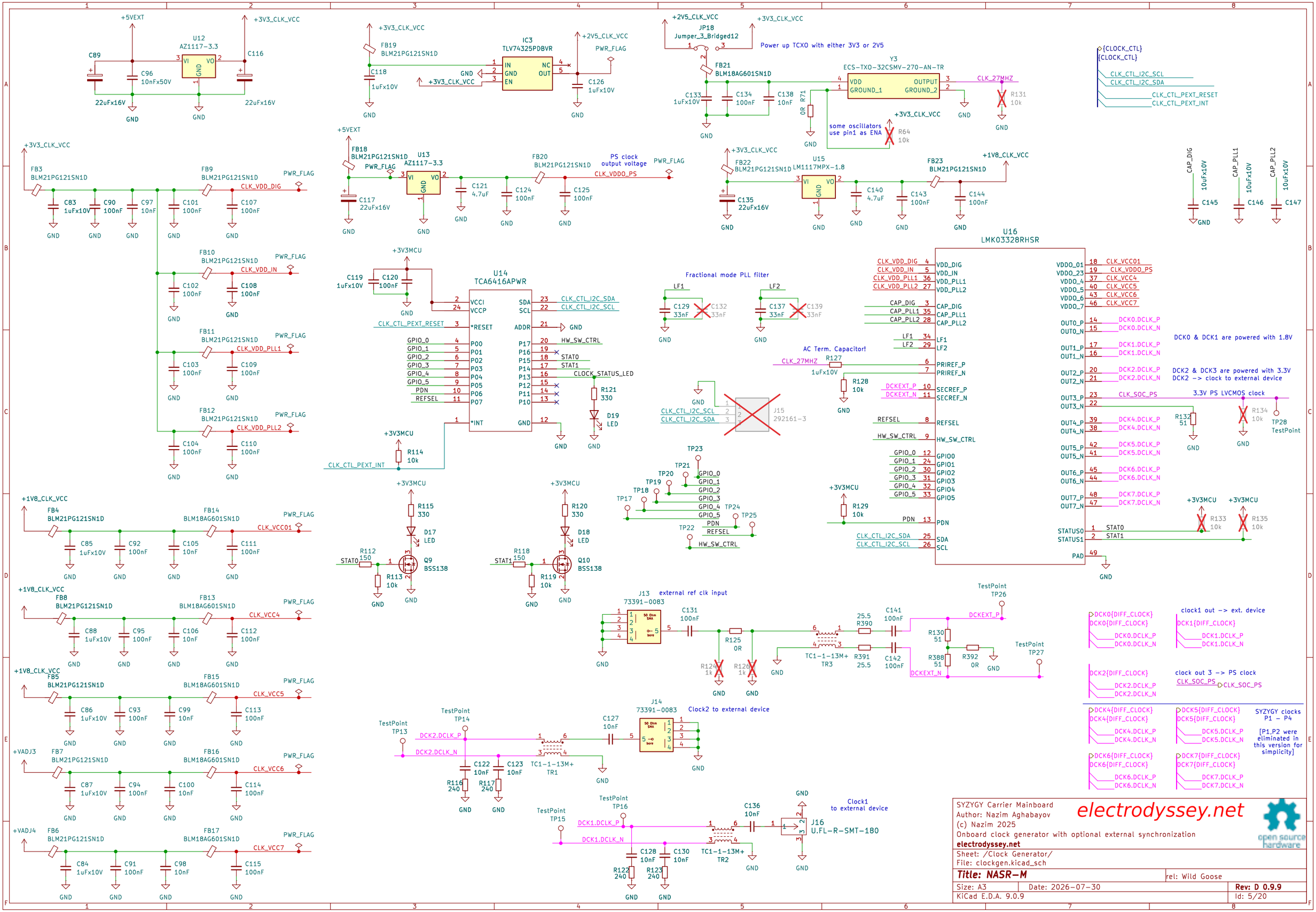
rel: Wild Goose

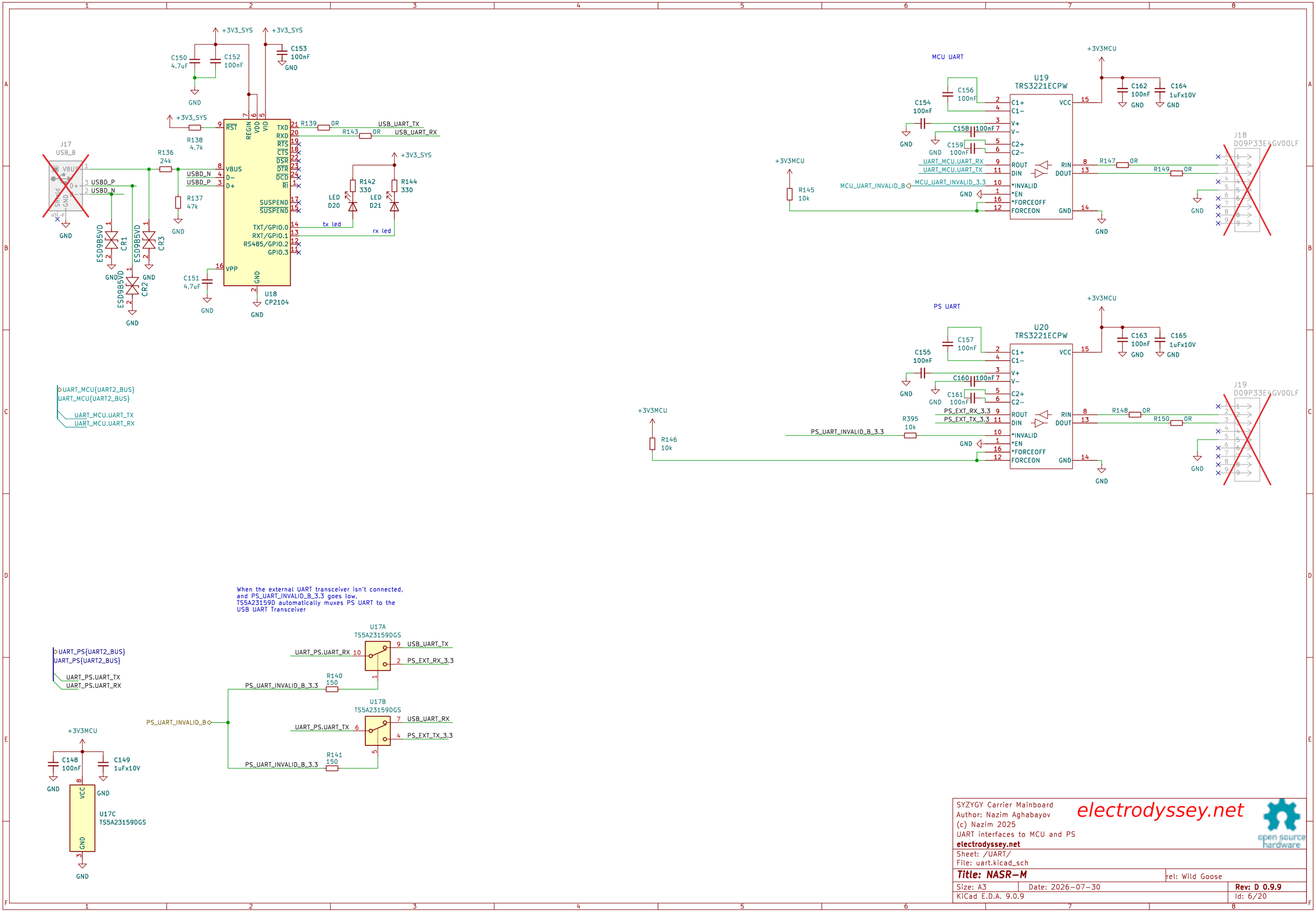
Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**

KiCad E.D.A. 9.0.9 | Id: 2/20


U2A
ADP5052ACPZ-R7
U2B
ADP5052ACPZ-R7
U6
TPS25940AQRVCRQ1
U5
SN74LXC1T45DBVR
U52
INA219AxDCN
U53
INA219AxDCN
U54
INA219AxDCN
U3
LD1117S12TR
U4
AZ1117H-ADJTRG1
IC1
NL17SZ17XV5T2G
IC2
TLV74325PDBVR
Q5B
FDS9926A
Q5A
FDS9926A
Q8
BSS138
Q6
BSS138
Q7
BSS138
D12
LED
D10
1SS357
D11
LED
D14
LED
ADP5052 SYNC/MODE
high -> forced PWM (FPWM) mode.
low -> automatic PWM/PSM mode.
ADP5052 PWR Sequence:
1. +1V0_SYS
2. +1V8_SYS
3. +3V3_SYS; +1V35_SYS; +1V8_XADC
ADP5052 outputs PWRGD
when the SW1 / +3V3_SYS is up (last in seq)
PMIC_EN2
starts 1V0
(first pwr bus)
XADC is used for internal monitoring only
UG480 Fig 1-2
{ZYNQ_PWR_CTL}
ZYNQ_PWCTL_PGOOD
SOC PWR +3V3_SYS is started (last in seq) [OUT] +1V8 signal
ZYNQ_PWCTL_EN
starts the SOC power when H [IN]
TPS25940 V(ENF) > 1.01V
2.5A
R50 = 47K
unsolder R50 to get 4.4A
6.44A MAX
R51 = 22k
I2C to current sensors
I2C_SENSORS{I2C_BUS}
I2C_SENSORS.I2C_SCL
I2C_SENSORS.I2C_SDA
I2C addr: 1000000
I2C addr: 1000001
I2C addr: 1000010
TP2 TestPoint
TP4 TestPoint
TP6 TestPoint
TP7 TestPoint
TP8 TestPoint
TP3 TestPoint
TP5 TestPoint
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
SOC PDN
electrodyssey.net
Sheet: /SOC Power/
File: soc_power.kicad_sch
Title: NASR-M
rel: Wild Goose
Size: A3
Date: 2026-07-30
Rev: D 0.9.9
KiCad E.D.A. 9.0.9
Id: 3/20


{PSU_PWR_CTL}
ATX_PWR_OK
ATX_PWR_BTN
ATX_PS_ON
Starts ATX PSU
R83 10k
{ZYNQ_PWR_CTL}
ZYNQ_PWCTL_PGOOD
+1V8 PGOOD signal from PMIC
ZYNQ_PWCTL_EN
PMIC ENA signal, triggers at > +1.01V
FAN_12V_EN
FAN12V_EN
FAN_CHASSIS_12V_EN
FAN12V_CHASSIS_EN
R80 10k
PROG_B
PL_PROG_B
I2C4 is dedicated to clock
{CLOCK_CTL}
CLK_CTL_I2C_SCL
CLK_CTL_I2C_SDA
CLK_CTL_PEXT_RESET
CLK_CTL_PEXT_INT
Variable voltage for SYZYGY
{VIO_CTL}
VIOC_I2C_SCL
VIOC_I2C_SDA
VIOC_I2C_EXT_RST
VIOC_INT
SOC Boot config
BCONF_I2C_EXT_RST_B
BCONF_RST_B
resets boot conf I2C ext.
I2C_BCONF{I2C_BUS}
3V3 bus
I2C_BCONF.I2C_SCL
I2C_BCONF.I2C_SDA
slave I2C from SOC/Linux
+3V3 / PS500
I2C_MCU{I2C_BUS}
I2C_MCU.I2C_SCL
I2C_MCU.I2C_SDA
I2C_MCU I2C2
I2C_SW I2C1
U50 TMP102xxDRL
U51 TMP102xxDRL
I2C_TMP01.I2C_SDA
I2C_TMP01.I2C_SCL
SW1 SW_Push
NRST
C66 100nF
SW2 SW_Push
boot overrride switch
BOOT0
C67 100nF
R95 10k
R96 10k
XTALI
XTALO
8MHz Y1
20pF C68
20pF C69
VREFP
C72 100nF
C73 1uFx10V
R101 10k
PDR_ON
R102 10k
FB2 BLM21PG121SN1D
VDDA
C74 100nF
C75 1uFx10V
+3V3EXT
R98 51
J9 292161-3
I2C_MCU.I2C_SCL
I2C_MCU.I2C_SDA
ETH_MCU_NRST
activates the ZYNQ PMIC
STATUS_LED_MCU
R97 330
D16 LED
U7 STM32H723ZGTx
C70 10uFx50V
C71 10uFx50V
J7 Conn_02x10_Odd_Even
NJTRST
JTDI
JTMS
JTCK
RTCK
JTDO
NRST
DBGRQ
DBGACK
R91 10k
R84 10k
R87 10k
J8 TagConnect_TC2050
VCC
TMS/SWDIO
TCK/SWCLK
TDO/SWO
RTCLK
TDI
nTRST G/+5
R393 150
R394 150
MCU Ethernet
MDIO_MCU{MD_BUS}
MDIO_MCU.MDIO
MDIO_MCU.MDC
RMII_MCU{RMII_BUS}
RMII_MCU.RMII_REF_CLK
RMII_MCU.RMII_CRS_DV
RMII_MCU.RMII_TX_EN
RMII_MCU.RMII_TXD0
RMII_MCU.RMII_TXD1
RMII_MCU.RMII_RXD0
RMII_MCU.RMII_RXD1
SYZYGY ports / VIO / Clocks
MCU EEP/ PS I2C Tree
PS_UART_INVALID_B
UART_MCU.UART_TX
UART_MCU.UART_RX
UART2_TX
X321
X320
Y2 32.768KHz
C76 4.3pF
C77 4.3pF
MCU UART
UART_INVALID_B
MCU_UART_INVALID_B
UART_MCU{UART2_BUS}
UART2_MCU{UART2_BUS}
UART2_MCU.UART_TX
UART2_MCU.UART_RX
SYZYGY I2C PORTS
I2C_P3{I2C_BUS}
I2C_P3.I2C_SCL
I2C_P3.I2C_SDA
I2C_P4{I2C_BUS}
I2C_P4.I2C_SCL
I2C_P4.I2C_SDA
R99 10k
R100 10k
R103 10k
R104 10k
U11 AZ1117H-1.8TRE1_SOT223
C80 10uFx50V
C82 22uF
+1V8MCU
C79 1uFx10V
U9 TXS0108EPW
C81 1uFx10V
R106 10k
R105 10k
R109 10k
PS_RESET
EMMC_RESET_B
SD_SEL
ZYNQ_GOOD_33
PS_SRST_MCU_1.8
EMMC_RST_B_1.8
SD_SEL_1.8
ZYNQ_PWCTL_PGOOD
SOC PS RST
EMMC RST
SD/EMMC select
ZYNQ PWR Ok
SYZYGY ports / VIO / Clocks
MCU EEP/ PS I2C Tree
U10 PCA9548APW
R107 10k
R108 10k
I2C_SW_SCL
I2C_SW_SDA
TestPoint TP12
SW_I2C_RST
J12 292161-3
C78 100nF
U8 24AA02E48T-I/OT
R110 10k
R111 10k
I2C_MCU_EEP_SDA
I2C_MCU_EEP_SCL
I2C to current sensors
I2C_SENSORS{I2C_BUS}
I2C_SENSORS.I2C_SCL
I2C_SENSORS.I2C_SDA
R4 10k
R5 10k
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Board MCU controlls the VIO power and SYZYGY ports
electrodyssey.net
Sheet: /MCU/
File: mcu.kicad_sch
Title: NASR-M
rel: Wild Goose
Size: A3
Date: 2026-07-30
Rev: D 0.9.9
KiCad E.D.A. 9.0.9
Id: 4/20


U12 AZ1117-3.3
+5VEXT
+3V3_CLK_VCC
C89 22uFx16V
C96 10nFx50V
C116 22uFx16V
GND
IC3 TLV74325PDBVR
FB19 BLM21PG121SN1D
C118 1uFx10V
C126 1uFx10V
PWR_FLAG
+2V5_CLK_VCC
JP18 Jumper_3_Bridged12
Power up TCXO with either 3V3 or 2V5
FB21 BLM18AG601SN1D
Y3 ECS-TXO-32CSMV-270-AN-TR
C133 1uFx10V
C134 100nF
C138 10nF
R71 0R
CLK_27MHZ
R131 10k
some oscillators use pin1 as ENA
R64 10k
{CLOCK_CTL}
CLK_CTL_I2C_SCL
CLK_CTL_I2C_SDA
CLK_CTL_PEXT_RESET
CLK_CTL_PEXT_INT
FB3 BLM21PG121SN1D
FB9 BLM21PG121SN1D
CLK_VDD_DIG
C83 1uFx10V
C90 100nF
C97 10nF
C101 100nF
C107 100nF
FB18 BLM21PG121SN1D
U13 AZ1117-3.3
C117 22uFx16V
C121 4.7uF
C124 100nF
C125 100nF
FB20 BLM21PG121SN1D
PS clock output voltage
CLK_VDDO_PS
FB22 BLM21PG121SN1D
U15 LM1117MPX-1.8
C135 22uFx16V
C140 4.7uF
C143 100nF
C144 100nF
FB23 BLM21PG121SN1D
+1V8_CLK_VCC
CAP_DIG 10uFx10V C145
CAP_PLL1 10uFx10V C146
CAP_PLL2 10uFx10V C147
FB10 BLM21PG121SN1D
CLK_VDD_IN
C102 100nF
C108 100nF
FB11 BLM21PG121SN1D
CLK_VDD_PLL1
C103 100nF
C109 100nF
FB12 BLM21PG121SN1D
CLK_VDD_PLL2
C104 100nF
C110 100nF
+3V3MCU
C119 1uFx10V
C120 100nF
U14 TCA6416APWR
VCCI
VCCP
*RESET
P00
P01
P02
P03
P04
P05
P06
P07
*INT
SDA
SCL
ADDR
P17
P16
P15
P14
P13
P12
P11
P10
GND
CLK_CTL_I2C_SDA
CLK_CTL_I2C_SCL
HW_SW_CTRL
STAT0
STAT1
CLOCK_STATUS_LED
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
PDN
REFSEL
R121 330
D19 LED
R114 10k
Fractional mode PLL filter
LF1
LF2
C129 33nF
C132 33nF
C137 33nF
C139 33nF
AC Term. Capacitor!
R127 1uFx10V
R128 10k
J15 292161-3
TP23
TP21
TP20
TP19
TP18
TP17
TP24
TP25
TP22
U16 LMK03328RHSR
VDD_DIG
VDD_IN
VDD_PLL1
VDD_PLL2
CAP_DIG
CAP_PLL1
CAP_PLL2
LF1
LF2
PRIREF_P
PRIREF_N
SECREF_P
SECREF_N
REFSEL
HW_SW_CTRL
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
PDN
SDA
SCL
PAD
VDDO_01
VDDO_23
VDDO_4
VDDO_5
VDDO_6
VDDO_7
CLK_VCC01
CLK_VDDO_PS
CLK_VCC4
CLK_VCC5
CLK_VCC6
CLK_VCC7
OUT0_P
OUT0_N
OUT1_P
OUT1_N
OUT2_P
OUT2_N
OUT3_P
OUT3_N
OUT4_P
OUT4_N
OUT5_P
OUT5_N
OUT6_P
OUT6_N
OUT7_P
OUT7_N
DCK0.DCLK_P
DCK0.DCLK_N
DCK1.DCLK_P
DCK1.DCLK_N
DCK2.DCLK_P
DCK2.DCLK_N
DCK4.DCLK_P
DCK4.DCLK_N
DCK5.DCLK_P
DCK5.DCLK_N
DCK6.DCLK_P
DCK6.DCLK_N
DCK7.DCLK_P
DCK7.DCLK_N
DCKEXT_P
DCKEXT_N
STATUS0
STATUS1
DCK0 & DCK1 are powered with 1.8V
DCK2 & DCK3 are powered with 3.3V
DCK2 -> clock to external device
3.3V PS LVCMOS clock
CLK_SOC_PS
R132 51
R134 10k
TP28 TestPoint
R133 10k
R135 10k
R129 10k
FB4 BLM21PG121SN1D
FB14 BLM18AG601SN1D
CLK_VCC01
C85 1uFx10V
C92 100nF
C105 10nF
C111 100nF
R115 330
D17 LED
R120 330
D18 LED
R112 150
Q9 BSS138
R113 10k
R118 150
Q10 BSS138
R119 10k
FB8 BLM21PG121SN1D
FB13 BLM18AG601SN1D
CLK_VCC4
C88 1uFx10V
C95 100nF
C106 10nF
C112 100nF
FB5 BLM21PG121SN1D
FB15 BLM18AG601SN1D
CLK_VCC5
C86 1uFx10V
C93 100nF
C99 10nF
C113 100nF
+VADJ3
FB7 BLM21PG121SN1D
FB16 BLM18AG601SN1D
CLK_VCC6
C87 1uFx10V
C94 100nF
C100 10nF
C114 100nF
+VADJ4
FB6 BLM21PG121SN1D
FB17 BLM18AG601SN1D
CLK_VCC7
C84 1uFx10V
C91 100nF
C98 10nF
C115 100nF
J13 73391-0083
external ref clk input
C131 100nF
R125 0R
R124 1k
R126 1k
25.5 R390
C141 100nF
TC1-1-13M+ TR3
R391 25.5
C142 100nF
R130 51
R388 51
R392 0R
TestPoint TP26
TestPoint TP27
DCKEXT_P
DCKEXT_N
DCK0{DIFF_CLOCK}
DCK0.DCLK_P
DCK0.DCLK_N
clock1 out -> ext. device
DCK1{DIFF_CLOCK}
DCK1.DCLK_P
DCK1.DCLK_N
DCK2{DIFF_CLOCK}
DCK2.DCLK_P
DCK2.DCLK_N
clock out 3 -> PS clock
CLK_SOC_PS
DCK4{DIFF_CLOCK}
DCK4.DCLK_P
DCK4.DCLK_N
DCK5{DIFF_CLOCK}
DCK5.DCLK_P
DCK5.DCLK_N
SYZYGY clocks P1 - P4
[P1,P2 were eliminated in this version for simplicity]
DCK6{DIFF_CLOCK}
DCK6.DCLK_P
DCK6.DCLK_N
DCK7{DIFF_CLOCK}
DCK7.DCLK_P
DCK7.DCLK_N
TestPoint TP13
TestPoint TP14
DCK2.DCLK_P
DCK2.DCLK_N
C122 10nF
C123 10nF
TC1-1-13M+ TR1
R116 240
R117 240
J14 73391-0083
Clock2 to external device
C127 10nF
TestPoint TP15
TestPoint TP16
DCK1.DCLK_P
DCK1.DCLK_N
C128 10nF
C130 10nF
TC1-1-13M+ TR2
R122 240
R123 240
C136 10nF
Clock1 to external device
J16 U.FL-R-SMT-180
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
Onboard clock generator with optional external synchronization
electrodyssey.net
electrodyssey.net
open source hardware
Sheet: /Clock Generator/
File: clockgen.kicad_sch
Title: NASR-M
rel: Wild Goose
Size: A3
Date: 2026-07-30
Rev: D 0.9.9
KiCad E.D.A. 9.0.9
Id: 5/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
UART interfaces to MCU and PS
electrodyssey.net

electrodyssey.net

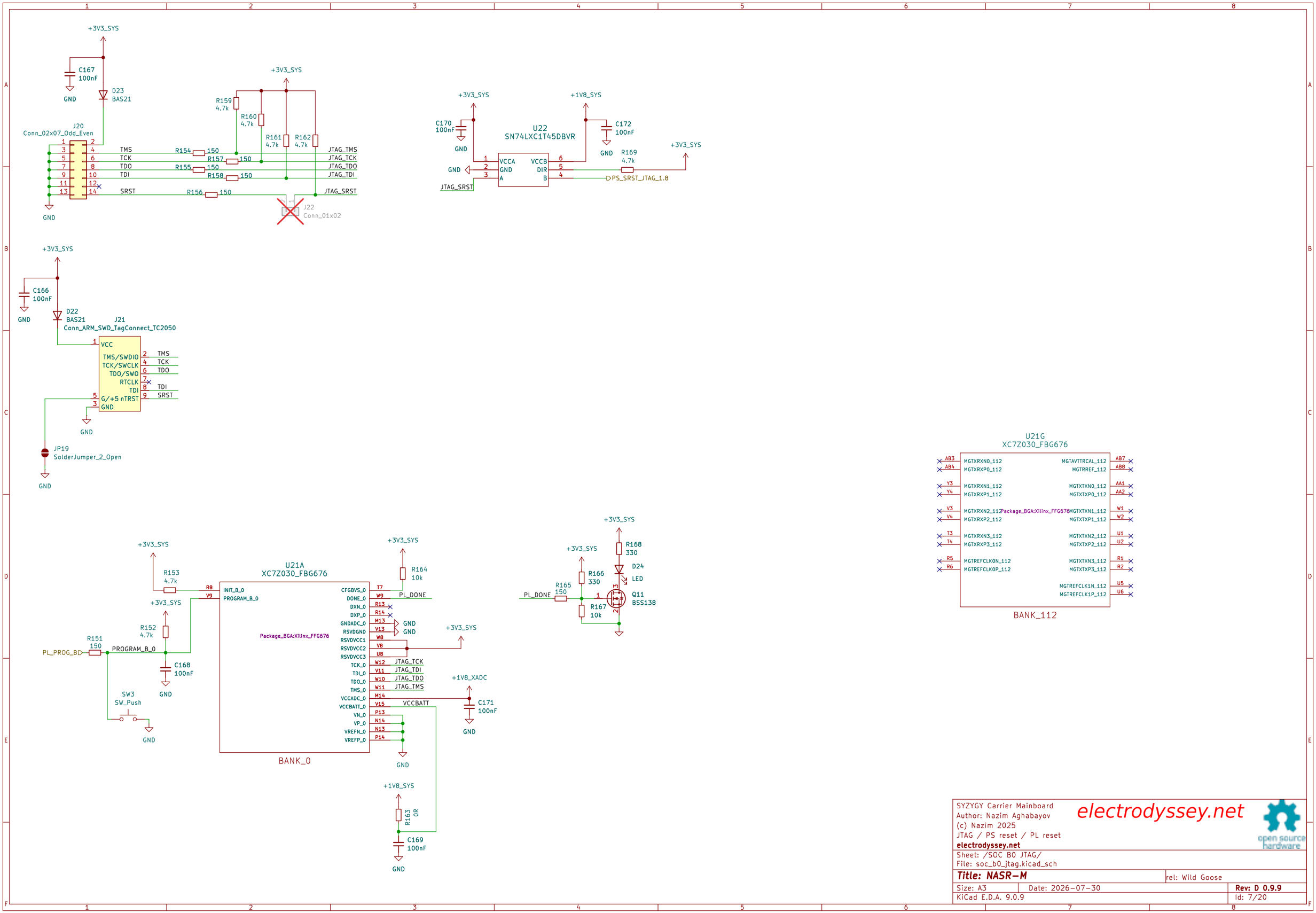
open source hardware

Sheet: /UART/
File: uart.kicad_sch

Title: NASR-M

rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**
KiCad E.D.A. 9.0.9 | Id: 6/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
JTAG / PS reset / PL reset
electrodyssey.net

electrodyssey.net

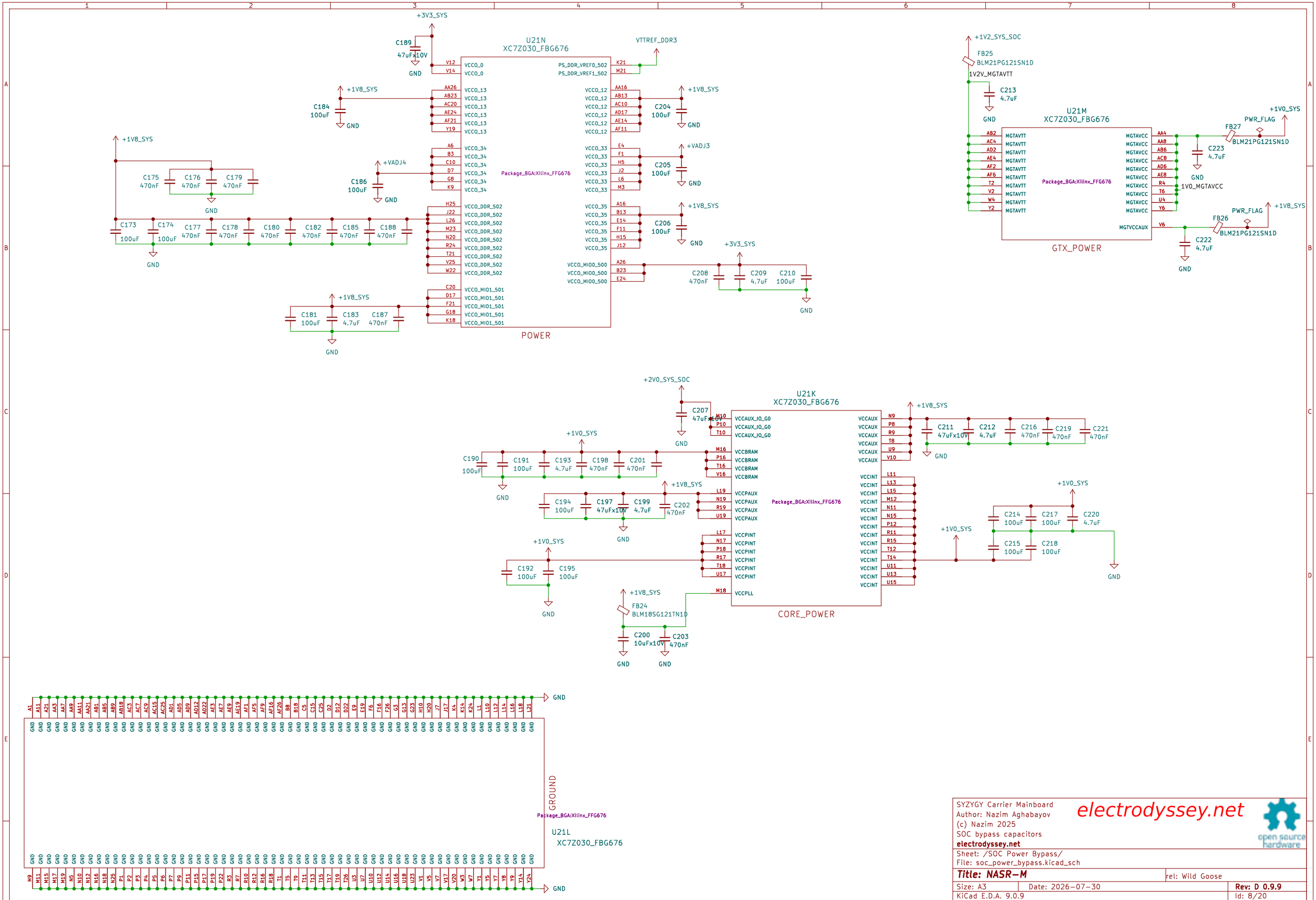
open source hardware

Sheet: /SOC B0 JTAG/
File: soc_b0_jtag.kicad_sch

Title: NASR-M

rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**
KiCad E.D.A. 9.0.9 | Id: 7/20



SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
(c) Nazim 2025
SOC bypass capacitors
electrodyssey.net

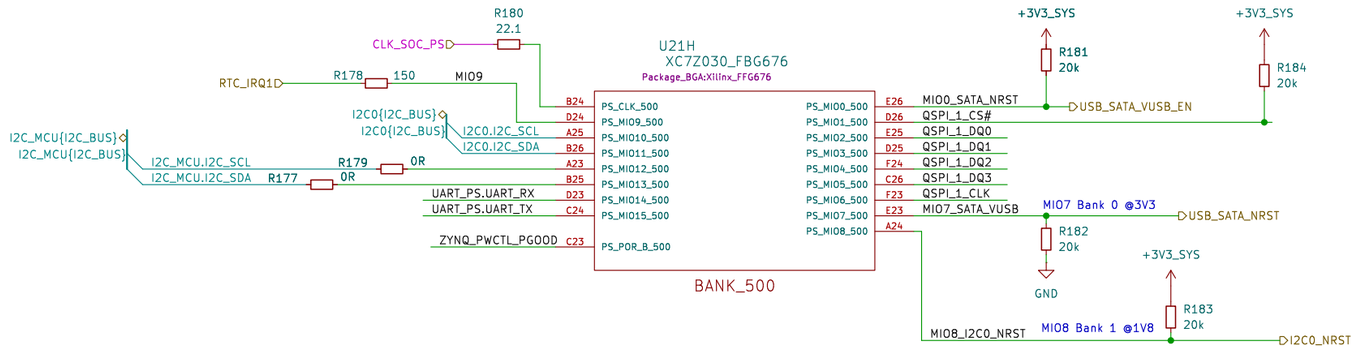
electrodyssey.net

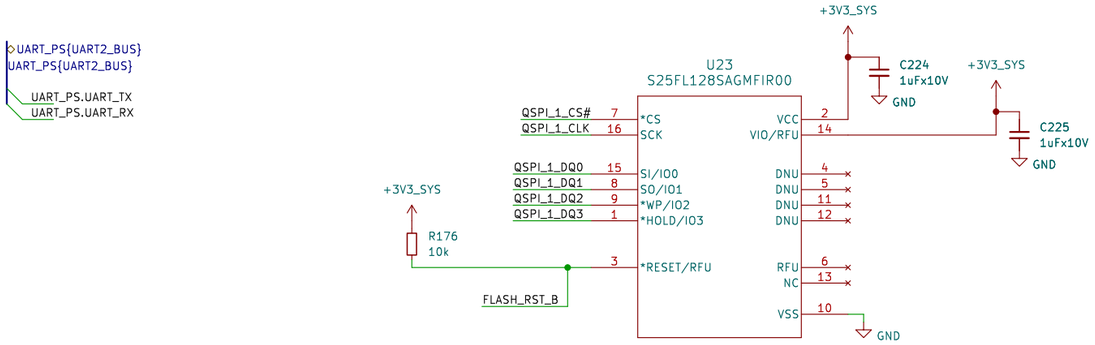
Sheet: /SOC Power Bypass/
File: soc_power_bypass.kicad_sch

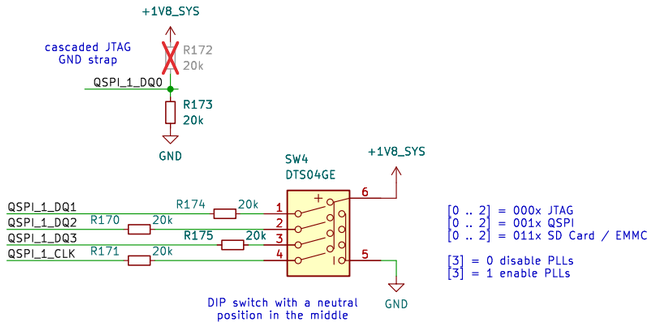
Title: NASR-M

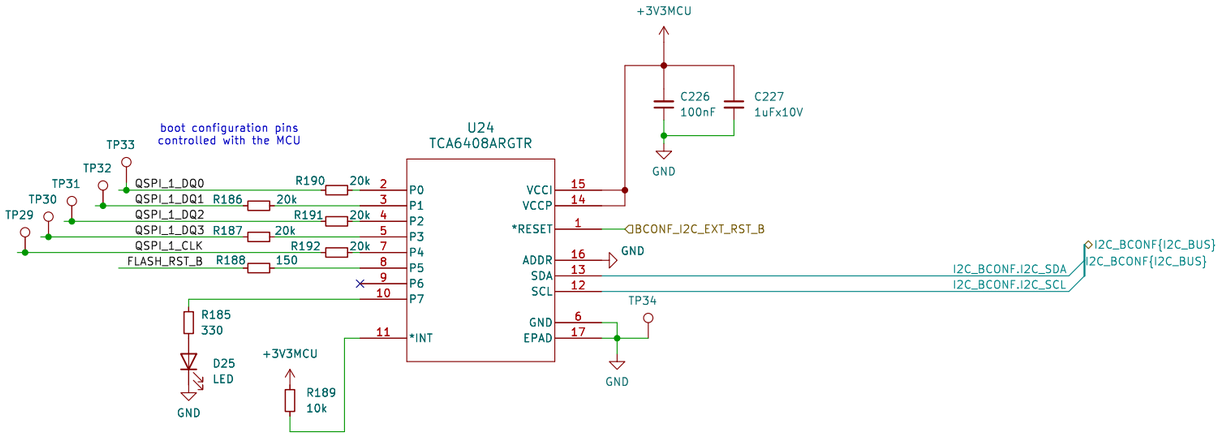
rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**
KiCad E.D.A. 9.0.9 | Id: 8/20









{ZYNQ_PWR_CTL}

- ZYNQ_PWCTL_PGOOD — SOC PWR +3V3_SYS is started (last in seq) [IN 1.8V signal]
- ZYNQ_PWCTL_EN — starts the SOC power when H [IN] (not used in this sheet)

Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common[1]				0	0	0	**JTAG Chain Routing[2]** 0: Cascade mode 1: Independent mode
NOR Boot[3]				0	0	1	
NAND				0	1	0	
Quad-SPI[3]				1	0	0	
SD Card				1	1	0	
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage[4]							
	Bank 1	**Bank 0**	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.				
2.5 V, 3.3 V	0	0					
1.8 V	1	1					

Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

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Bank 500; QSPI / Boot mode switches / POR
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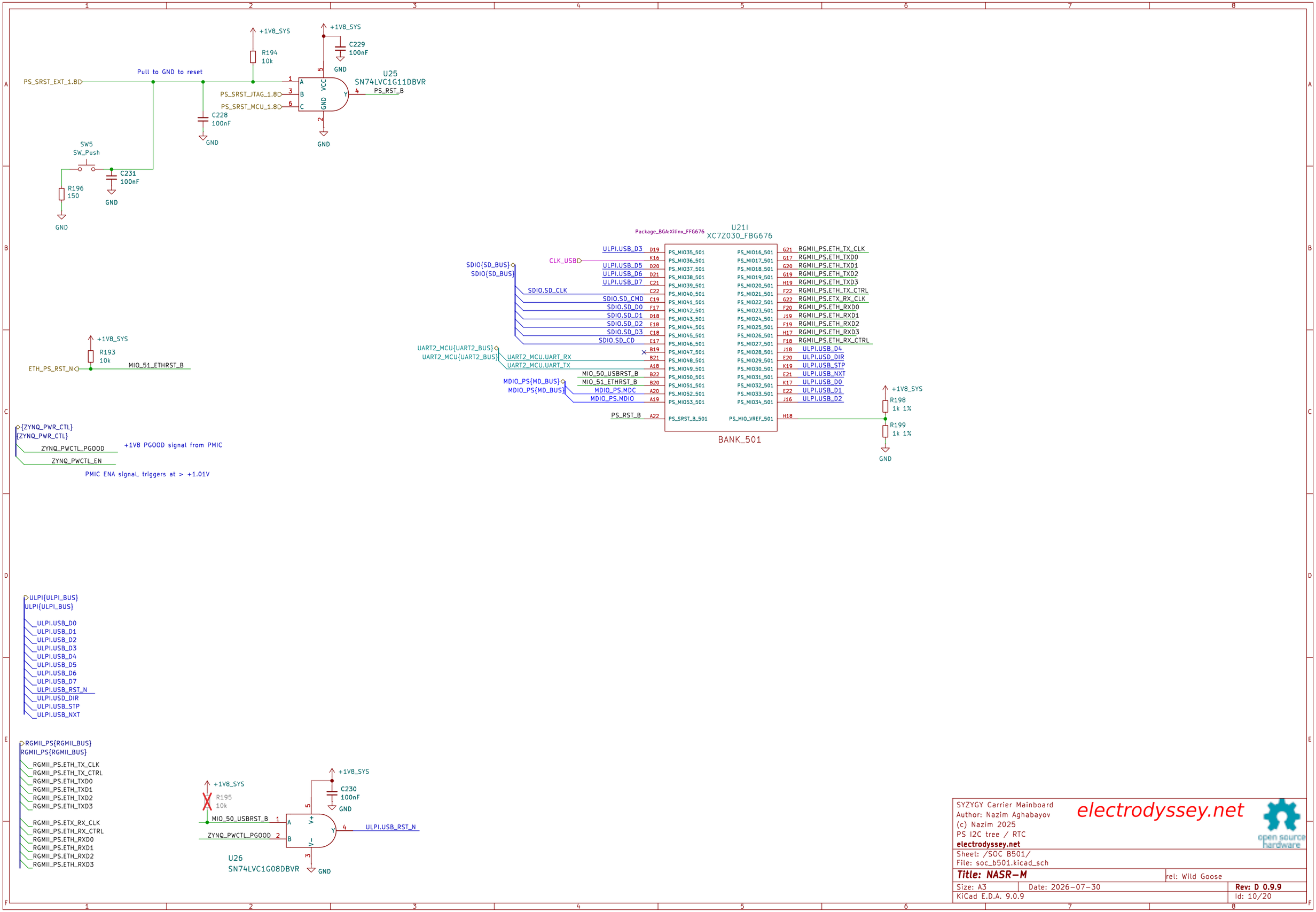
Sheet: /SOC B500 POR QSPI/
File: soc_bank500.kicad_sch

Title: NASR-M | rel: Wild Goose

Size: A3	Date: 2026-07-30	**Rev: D 0.9.9**
KiCad E.D.A. 9.0.9		Id: 9/20



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PS I2C tree / RTC
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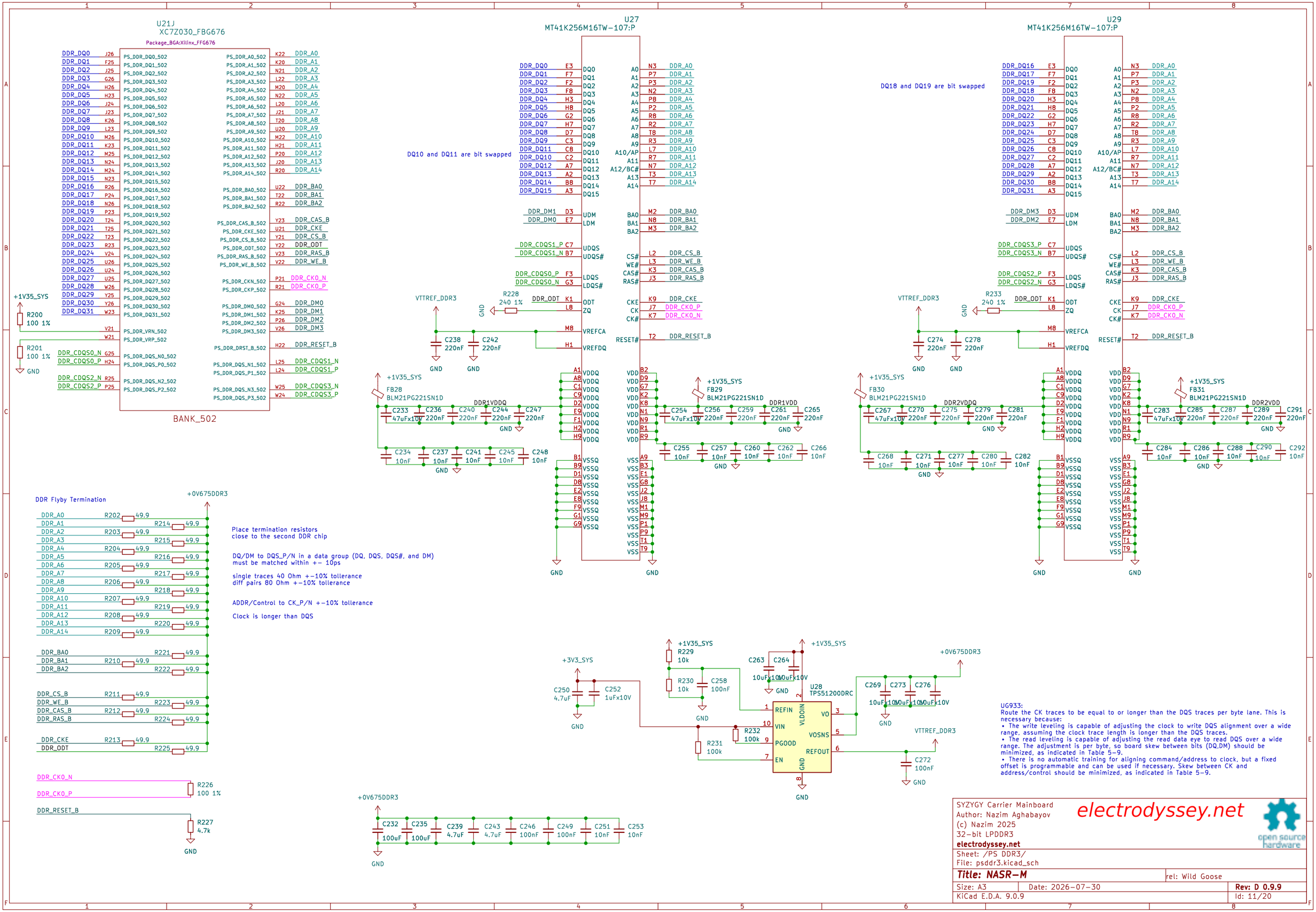
Sheet: /SOC B501/
File: soc_b501.kicad_sch

Title: NASR-M rel: Wild Goose

Size: A3 Date: 2026-07-30 **Rev: D 0.9.9**
KiCad E.D.A. 9.0.9 Id: 10/20


U21J
XC7Z030_FBG676
Package_BGA:Xilinx_FFG676
BANK_502
U27
MT41K256M16TW-107:P
U29
MT41K256M16TW-107:P
DQ10 and DQ11 are bit swapped
DQ18 and DQ19 are bit swapped
DDR Flyby Termination
+0V675DDR3
Place termination resistors
close to the second DDR chip
DQ/DM to DQS_P/N in a data group (DQ, DQS, DQS#, and DM)
must be matched within +- 10ps
single traces 40 Ohm +-10% tollerance
diff pairs 80 Ohm +-10% tollerance
ADDR/Control to CK_P/N +-10% tollerance
Clock is longer than DQS
U28
TPS51200DRC
UG933:
Route the CK traces to be equal to or longer than the DQS traces per byte lane. This is
necessary because:
• The write leveling is capable of adjusting the clock to write DQS alignment over a wide
range, assuming the clock trace length is longer than the DQS traces.
• The read leveling is capable of adjusting the read data eye to read DQS over a wide
range. The adjustment is per byte, so board skew between bits (DQ,DM) should be
minimized, as indicated in Table 5-9.
• There is no automatic training for aligning command/address to clock, but a fixed
offset is programmable and can be used if necessary. Skew between CK and
address/control should be minimized, as indicated in Table 5-9.
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32-bit LPDDR3
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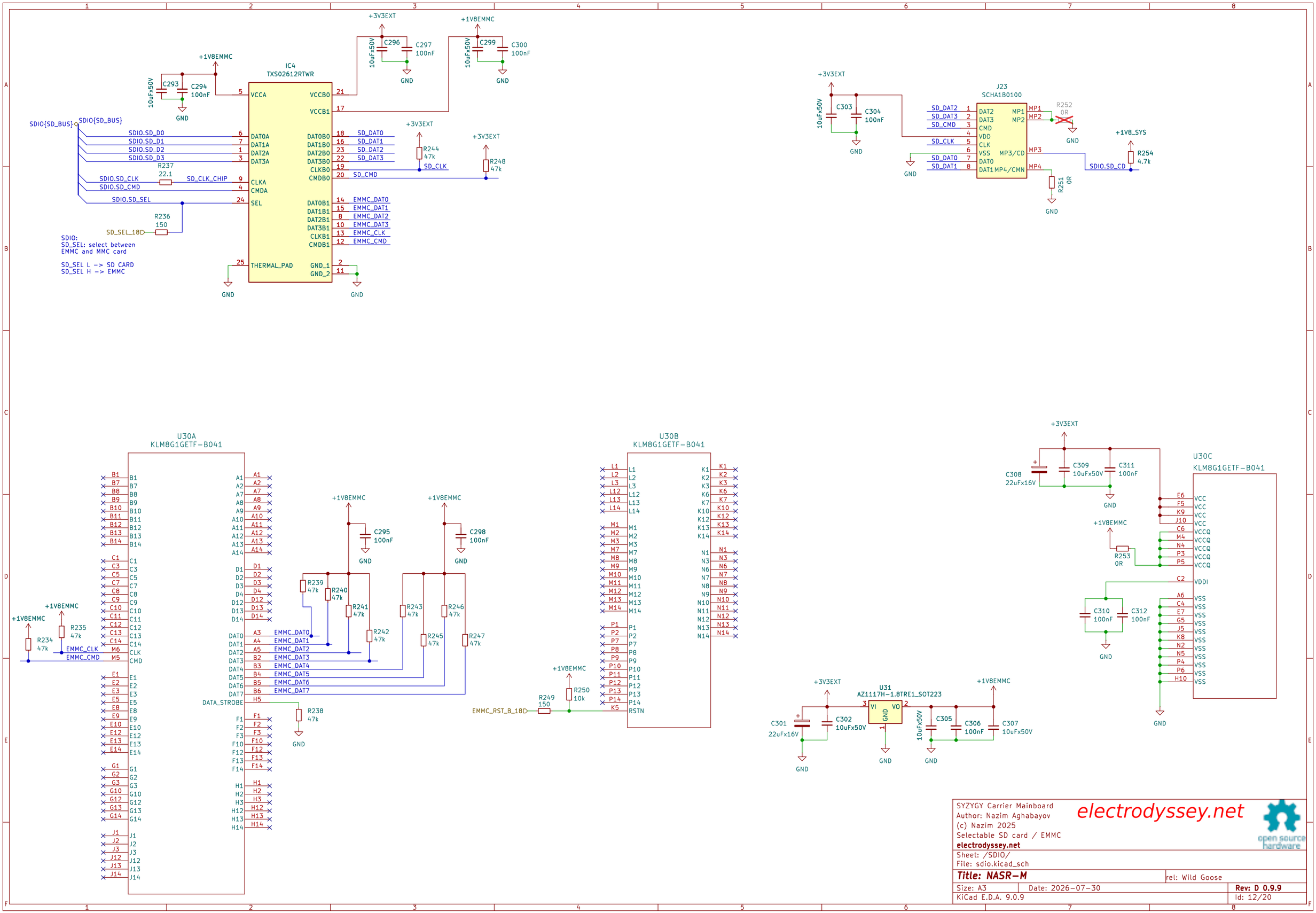
Sheet: /PS DDR3/
File: psddr3.kicad_sch
Title: NASR-M
rel: Wild Goose
Size: A3
Date: 2026-07-30
Rev: D 0.9.9
KiCad E.D.A. 9.0.9
Id: 11/20



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Selectable SD card / EMMC
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Sheet: /SDIO/
File: sdio.kicad_sch

Title: NASR-M

rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**

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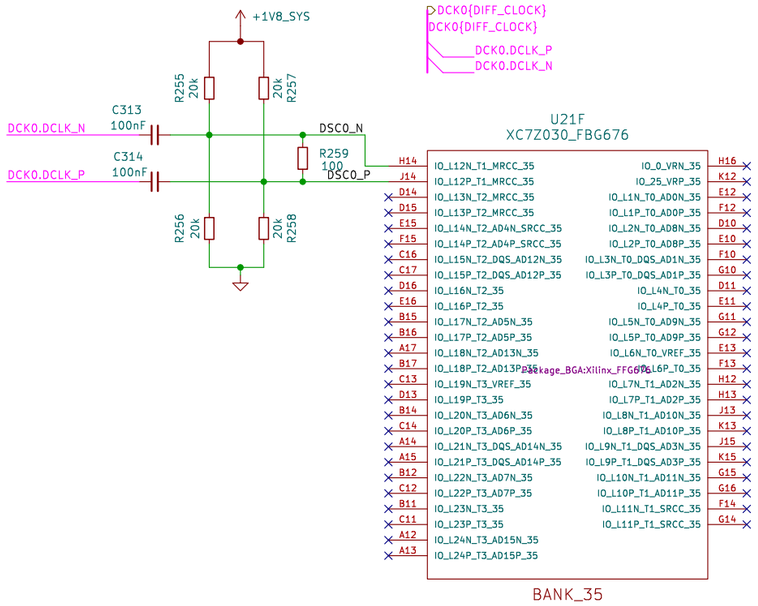

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Clock Generator pair 0 to MRCC
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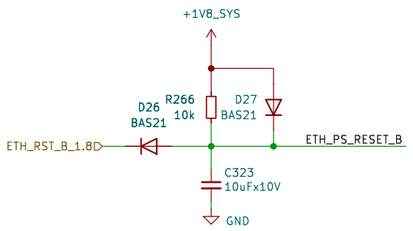
Sheet: /SOC B35/
File: soc_b35.kicad_sch

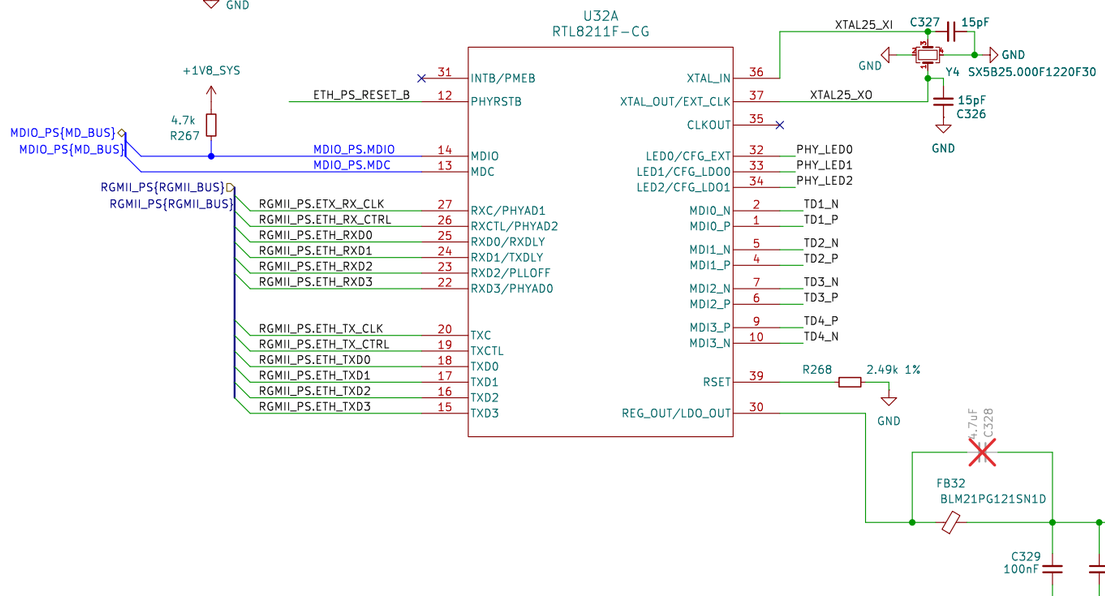
Title: NASR-M

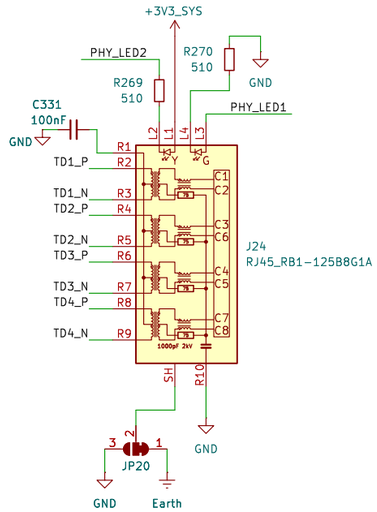
rel: Wild Goose

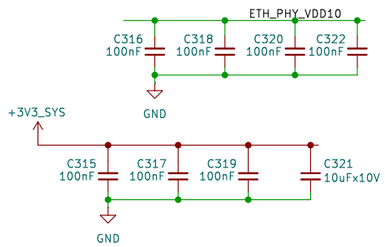
Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**

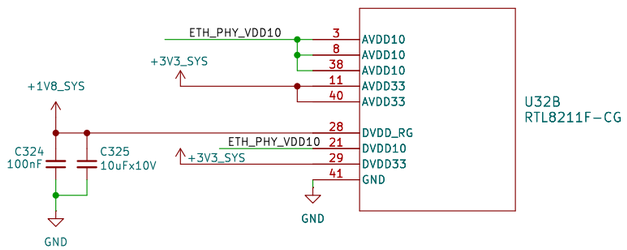
KiCad E.D.A. 9.0.9 | Id: 13/20











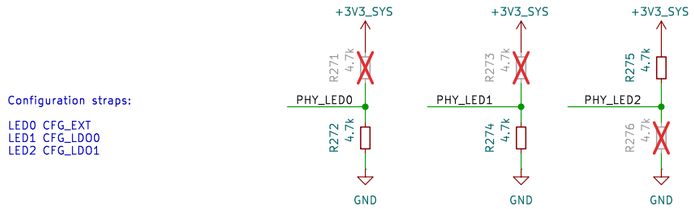


Table 10. CONFIG Pins vs. Configuration Register

CONFIG Pin	Configuration
RXD3	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD2	PLLOFF
RXD1	TXDLY
RXD0	RXDLY
LED0	CFG_EXT
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]

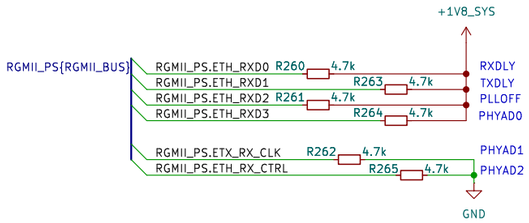


Table 11. Configuration Register Definitions

Configuration	Description
PHYAD[2:0]	PHY Address. PHYAD sets the PHY address for the device. The RTL8211F(I)/ RTL8211FD(I) supports PHY addresses from 00001 to 00111. *Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Reg24.13=0 (See Table 37).* *Note 2: The RTL8211F(I)/ RTL8211FD(I) with PHYAD[2:0]=000 can automatically remember the first non-zero PHY address. This function can be enabled by setting Reg24.6 = 1 (See Table 37).*
PLLOFF	ALDPS Mode PLL Off Configuration. 1: Stop PLL when entering ALDPS mode (via 4.7k-ohm to DVDD_RG) 0: PLL continue toggling when entering ALDPS mode (via 4.7k-ohm to GND)
TXDLY	RGMII Transmit Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG) 0: No delay (via 4.7k-ohm to GND)
RXDLY	RGMII Receive Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to DVDD_RG) 0: No delay (via 4.7k-ohm to GND)
CFG_EXT	I/O Pad External Power Source Mode Configuration. 1: Use the external power source for the IO pad (via 4.7k-ohm to 3.3V) 0: Use the integrated LDO to transform the desired voltage for the IO pad (via 4.7k-ohm to GND)

32	CFG_EXT	O/LI/PD	IO Pad External Power Source Mode Configuration. Pull up to use the external power source for the IO pad. Pull down to use the integrated LDO to transform the desired voltage for the IO pad.
33	CFG_LDO0	O/LI/PU	LDO Output Voltage Selection for I/O Pad/
34	CFG_LDO1	O/LI/PD	External Power Source Voltage Selection for I/O Pad. When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved. 2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V. When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for input voltage selection of the external power for IO pad: 2'b00: 3.3V. 2'b01: 2.5V. 2'b10: 1.8V. 2'b11: 1.5V.

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Sheet: /Ethernet PS/
File: eth_ps.kicad_sch

Title: NASR-M rel: Wild Goose

Size: A3 Date: 2026-07-30 **Rev: D 0.9.9**
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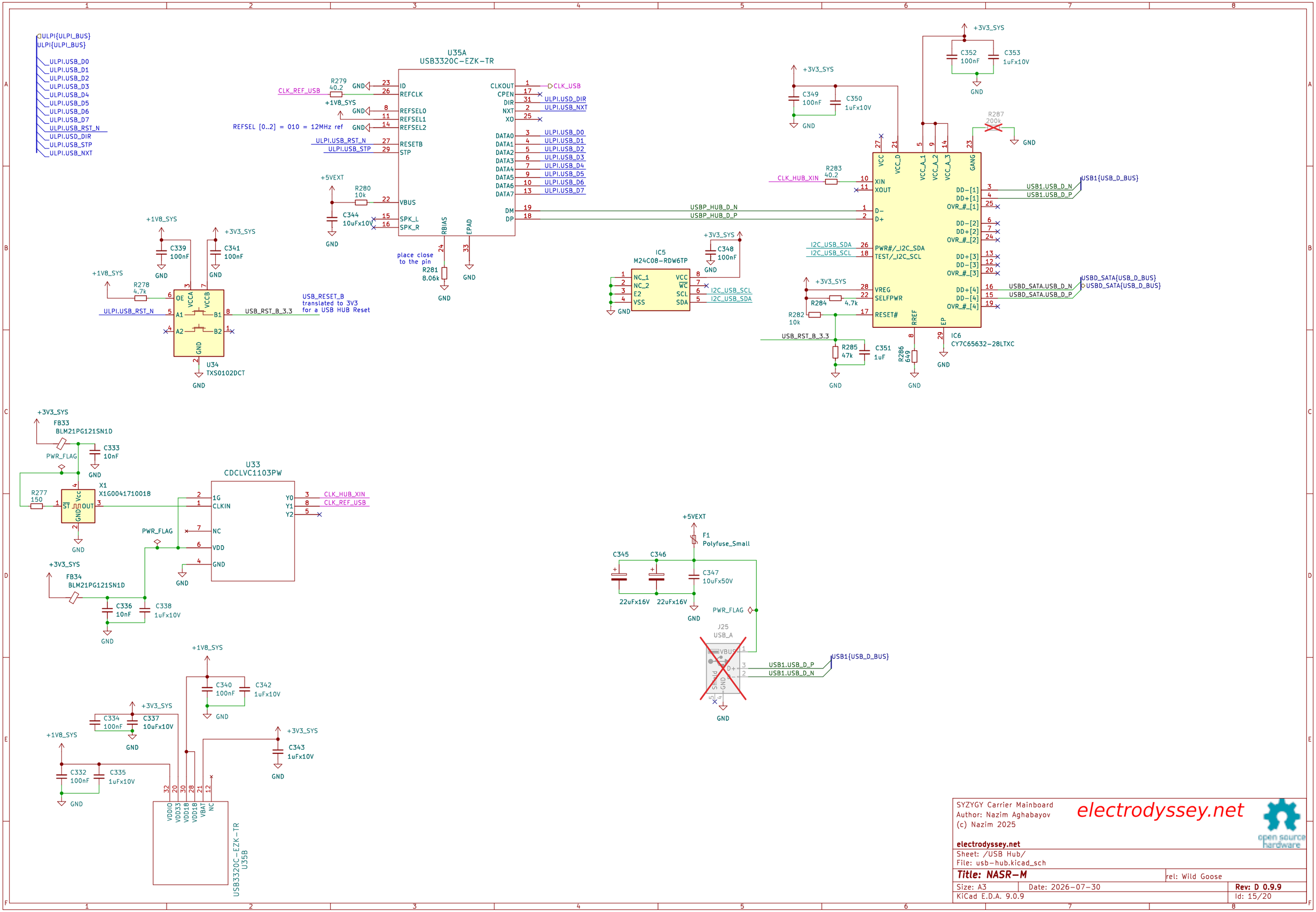

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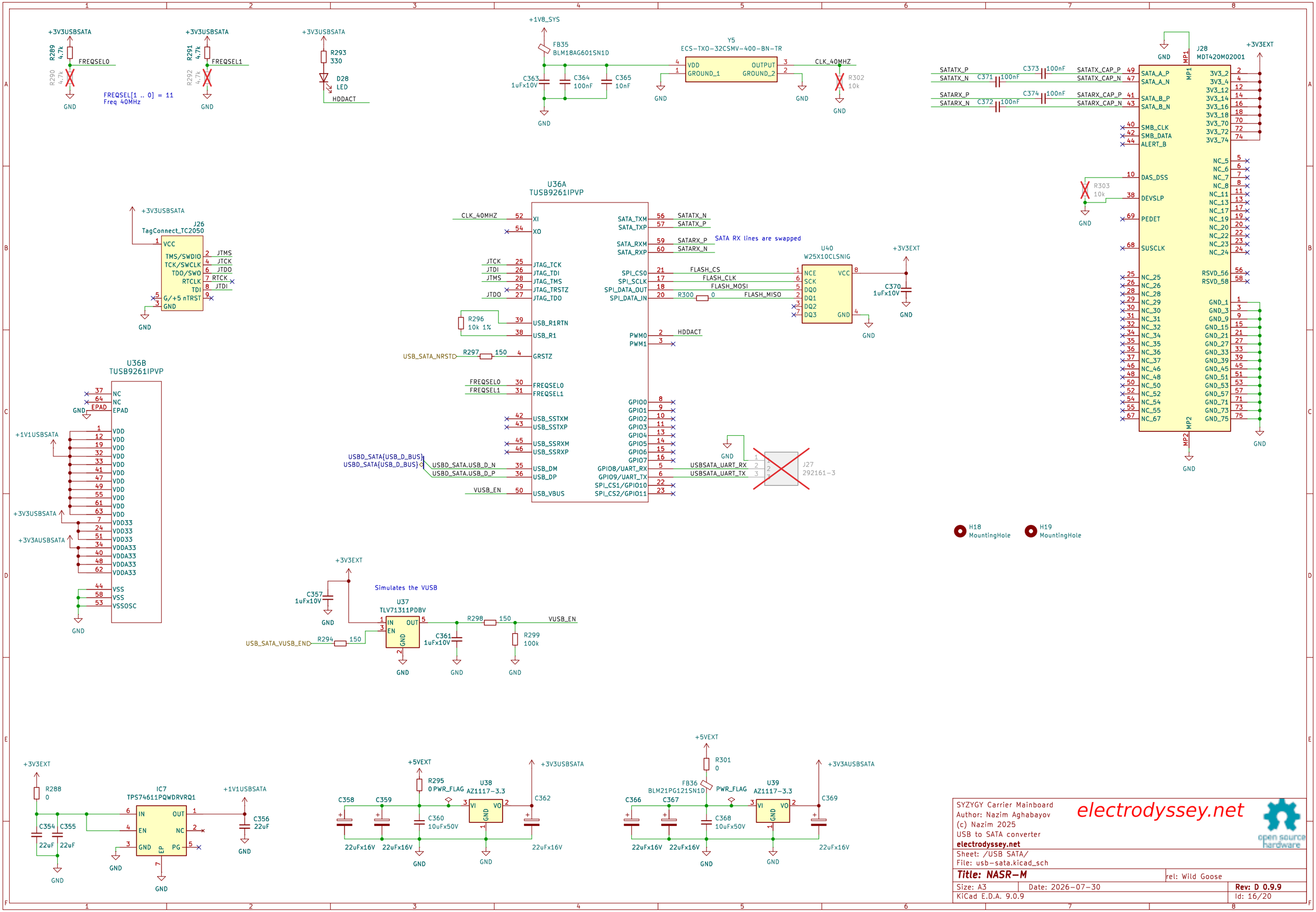
Sheet: /USB Hub/
File: usb-hub.kicad_sch

Title: NASR-M

rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**

KiCad E.D.A. 9.0.9 | Id: 15/20



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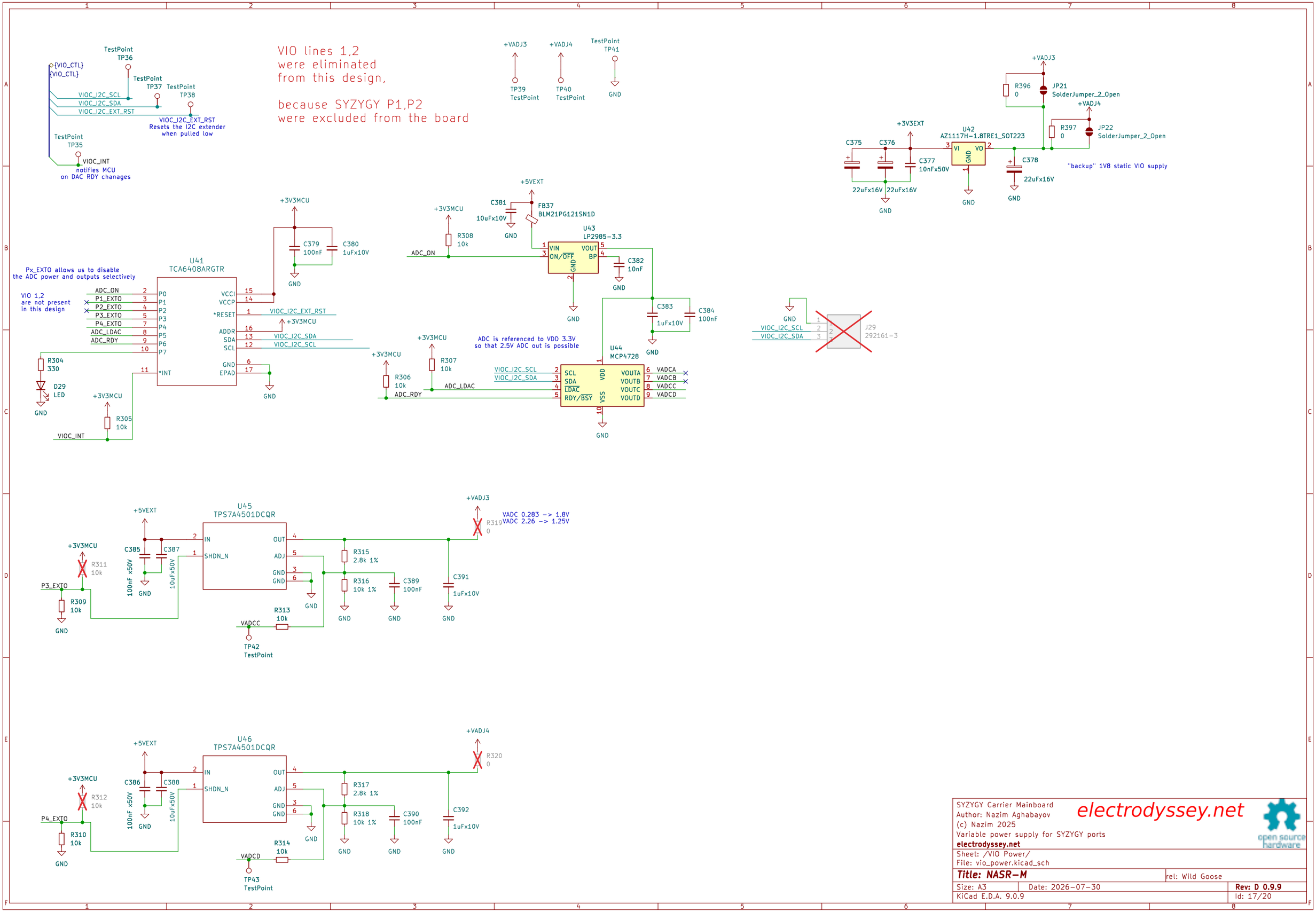
open source hardware

Sheet: /USB SATA/
File: usb-sata.kicad_sch

Title: NASR-M | rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**
KiCad E.D.A. 9.0.9 | Id: 16/20


VIO lines 1,2
were eliminated
from this design,
because SYZYGY P1,P2
were excluded from the board
{VIO_CTL}
{VIO_CTL}
TestPoint
TP36
TestPoint
TP37
TestPoint
TP38
VIOC_I2C_SCL
VIOC_I2C_SDA
VIOC_I2C_EXT_RST
VIOC_I2C_EXT_RST
Resets the I2C extender
when pulled low
TestPoint
TP35
VIOC_INT
notifies MCU
on DAC RDY chanages
+VADJ3
TP39
TestPoint
+VADJ4
TP40
TestPoint
TestPoint
TP41
GND
+VADJ3
R396
0
JP21
SolderJumper_2_Open
+VADJ4
R397
0
JP22
SolderJumper_2_Open
+3V3EXT
U42
AZ1117H-1.8TRE1_SOT223
VI
VO
GND
C375
C376
C377
10nFx50V
C378
22uFx16V
22uFx16V
22uFx16V
GND
"backup" 1V8 static VIO supply
+5VEXT
C381
10uFx10V
FB37
BLM21PG121SN1D
U43
LP2985-3.3
VIN
ON/OFF
GND
VOUT
BP
C382
10nF
+3V3MCU
R308
10k
ADC_ON
C383
1uFx10V
C384
100nF
+3V3MCU
C379
100nF
C380
1uFx10V
Px_EXTO allows us to disable
the ADC power and outputs selectively
VIO 1,2
are not present
in this design
U41
TCA6408ARGTR
ADC_ON
P1_EXTO
P2_EXTO
P3_EXTO
P4_EXTO
ADC_LDAC
ADC_RDY
P0
P1
P2
P3
P4
P5
P6
P7
*INT
VCCI
VCCP
*RESET
ADDR
SDA
SCL
GND
EPAD
VIOC_I2C_EXT_RST
+3V3MCU
VIOC_I2C_SDA
VIOC_I2C_SCL
R304
330
D29
LED
+3V3MCU
R305
10k
VIOC_INT
ADC is referenced to VDD 3.3V
so that 2.5V ADC out is possible
U44
MCP4728
SCL
SDA
LDAC
RDY/BSY
VDD
VSS
VOUTA
VOUTB
VOUTC
VOUTD
VADCA
VADCB
VADCC
VADCD
+3V3MCU
R307
10k
+3V3MCU
R306
10k
ADC_LDAC
ADC_RDY
GND
VIOC_I2C_SCL
VIOC_I2C_SDA
J29
292161-3
U45
TPS7A4501DCQR
+5VEXT
+3V3MCU
R311
10k
C385
100nF x50V
C387
10uFx50V
P3_EXTO
R309
10k
IN
SHDN_N
OUT
ADJ
GND
GND
+VADJ3
R319
0
VADC 0.283 -> 1.8V
VADC 2.26 -> 1.25V
R315
2.8k 1%
R316
10k 1%
C389
100nF
C391
1uFx10V
R313
10k
VADCC
TP42
TestPoint
U46
TPS7A4501DCQR
+5VEXT
+3V3MCU
R312
10k
C386
100nF x50V
C388
10uFx50V
P4_EXTO
R310
10k
IN
SHDN_N
OUT
ADJ
GND
GND
+VADJ4
R320
0
R317
2.8k 1%
R318
10k 1%
C390
100nF
C392
1uFx10V
R314
10k
VADCD
TP43
TestPoint
SYZYGY Carrier Mainboard
Author: Nazim Aghabayov
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Variable power supply for SYZYGY ports
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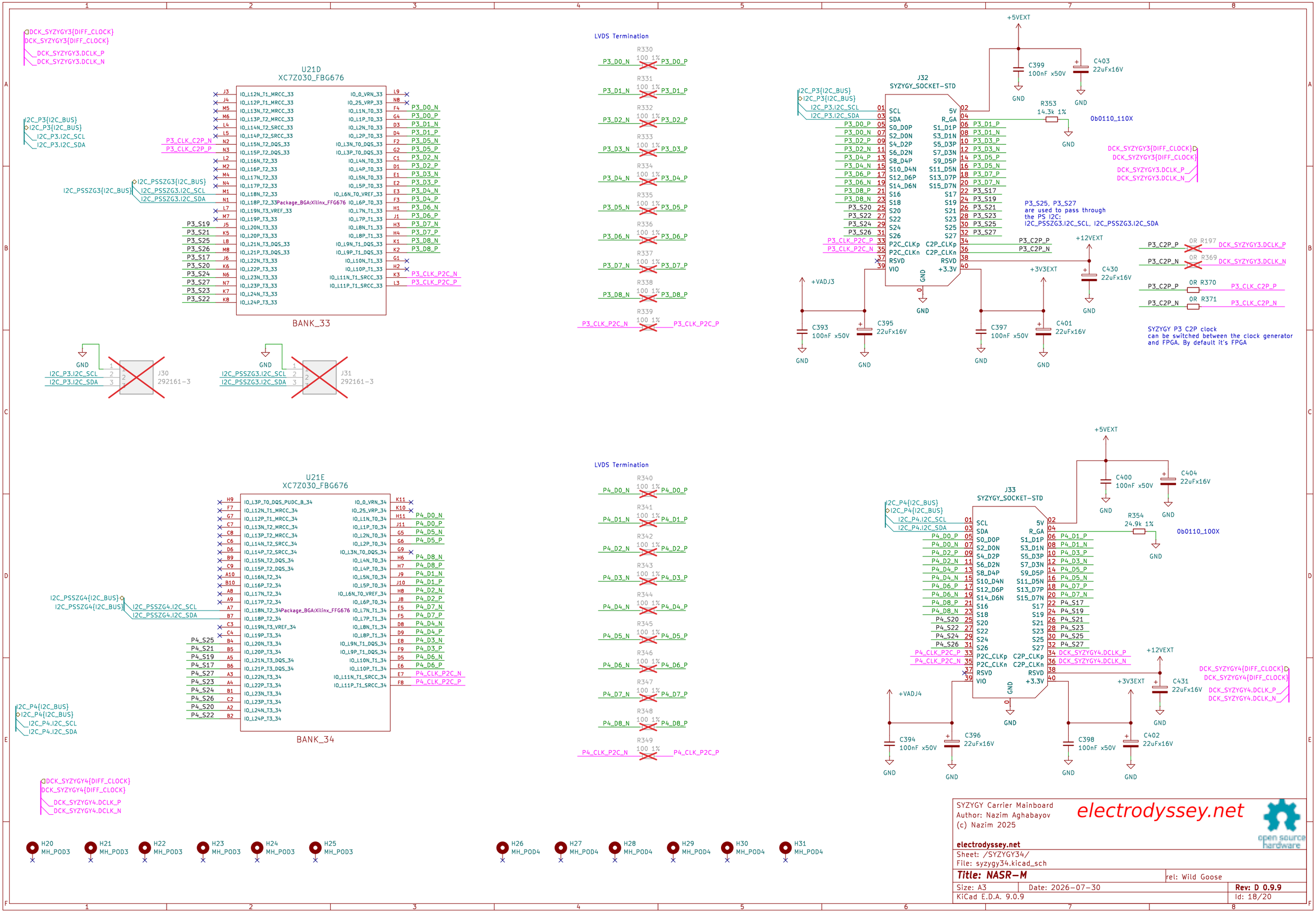
open source hardware
Sheet: /VIO Power/
File: vio_power.kicad_sch
Title: NASR-M
rel: Wild Goose
Size: A3
Date: 2026-07-30
Rev: D 0.9.9
KiCad E.D.A. 9.0.9
Id: 17/20



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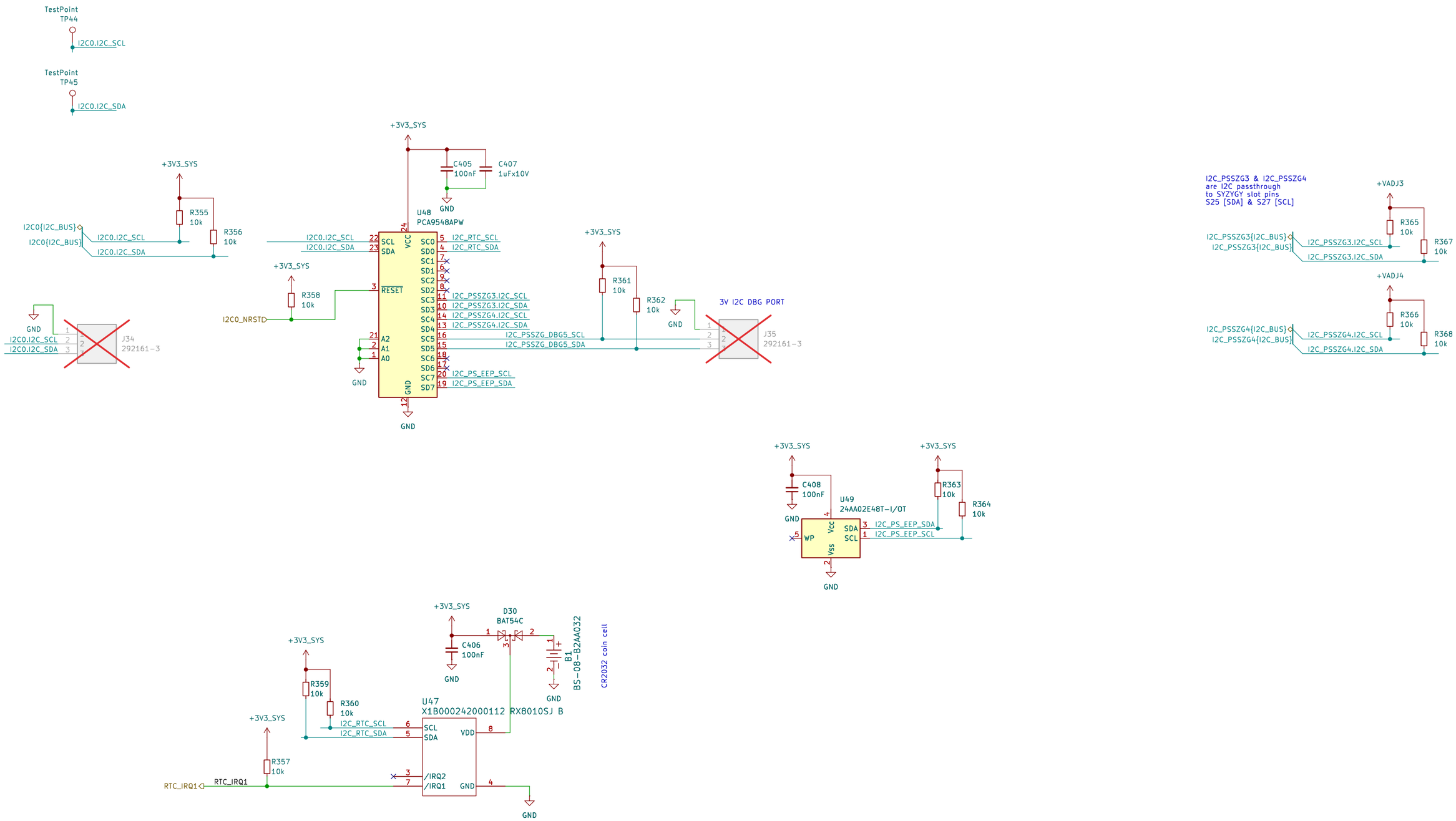
Sheet: /SYZYGY34/
File: syzygy34.kicad_sch

Title: NASR-M

rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**
KiCad E.D.A. 9.0.9 | Id: 18/20



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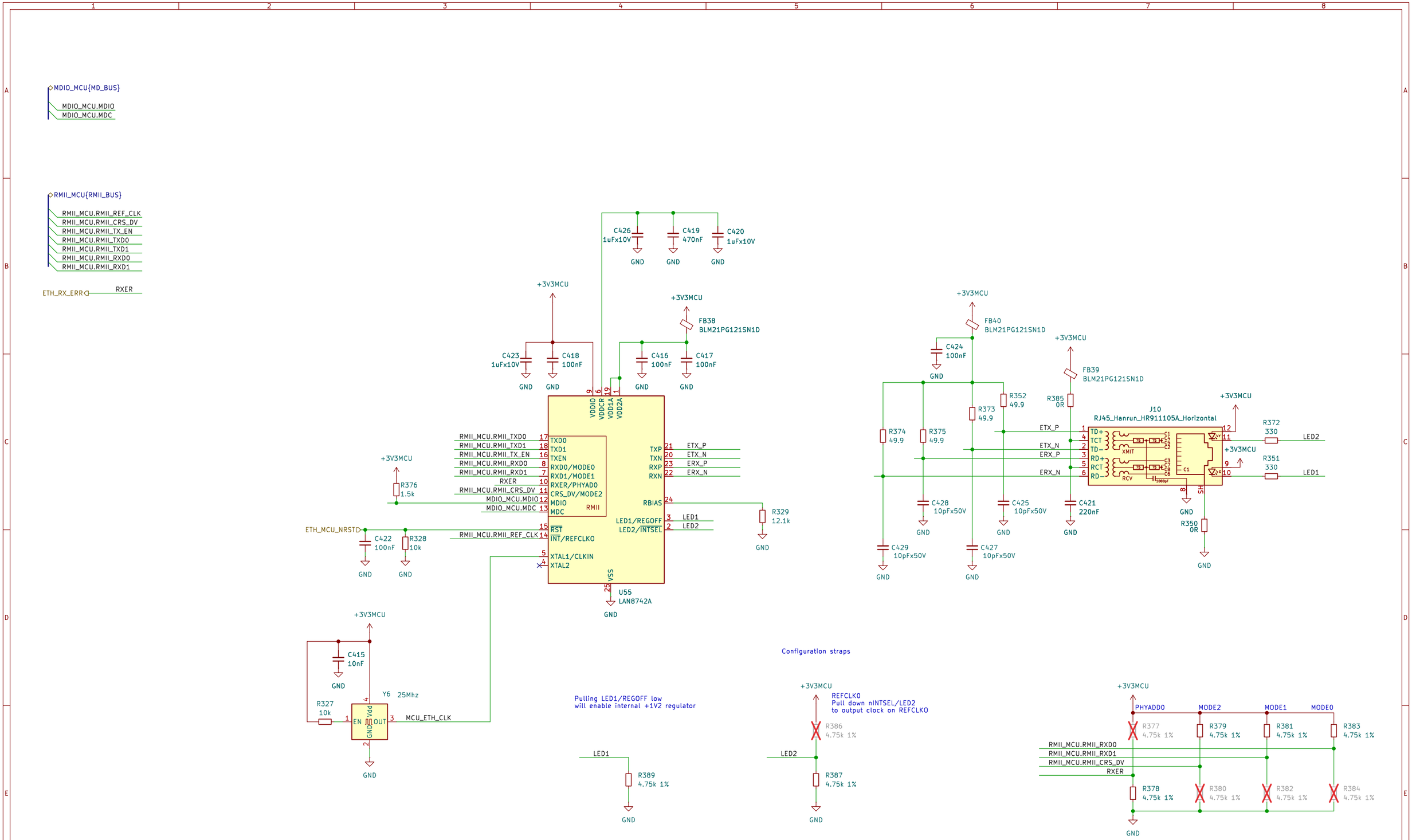
Sheet: /SOC I2C/
File: soc_i2c.kicad_sch

Title: NASR-M

rel: Wild Goose

Size: A3 | Date: 2026-07-30 | **Rev: D 0.9.9**

KiCad E.D.A. 9.0.9 | Id: 19/20



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Sheet: /Ethernet MCU/
File: eth_mcu.kicad_sch

Title: NASR-M		rel: Wild Goose
Size: A3	Date: 2026-07-30	**Rev: D 0.9.9**
KiCad E.D.A. 9.0.9		Id: 20/20