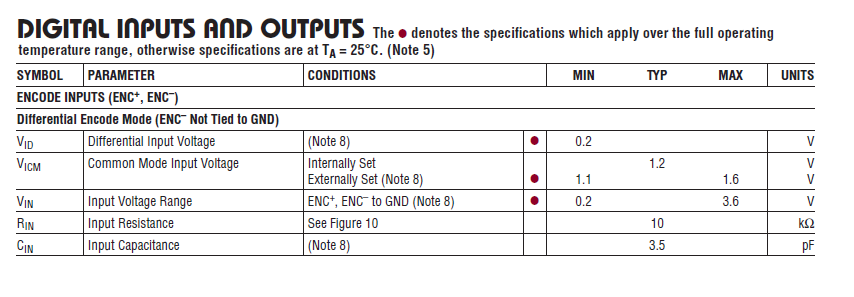
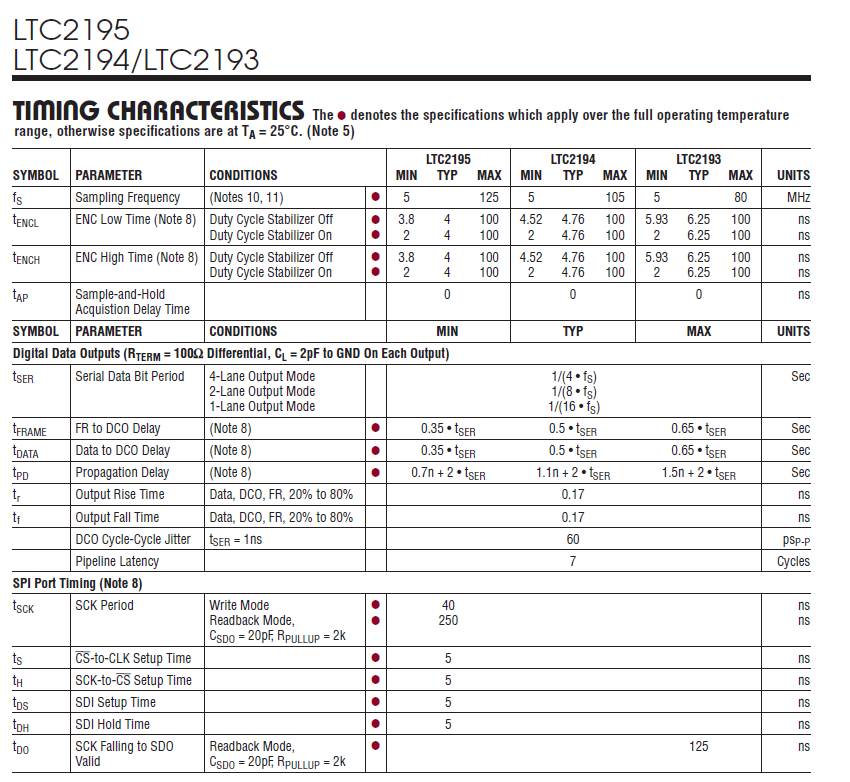
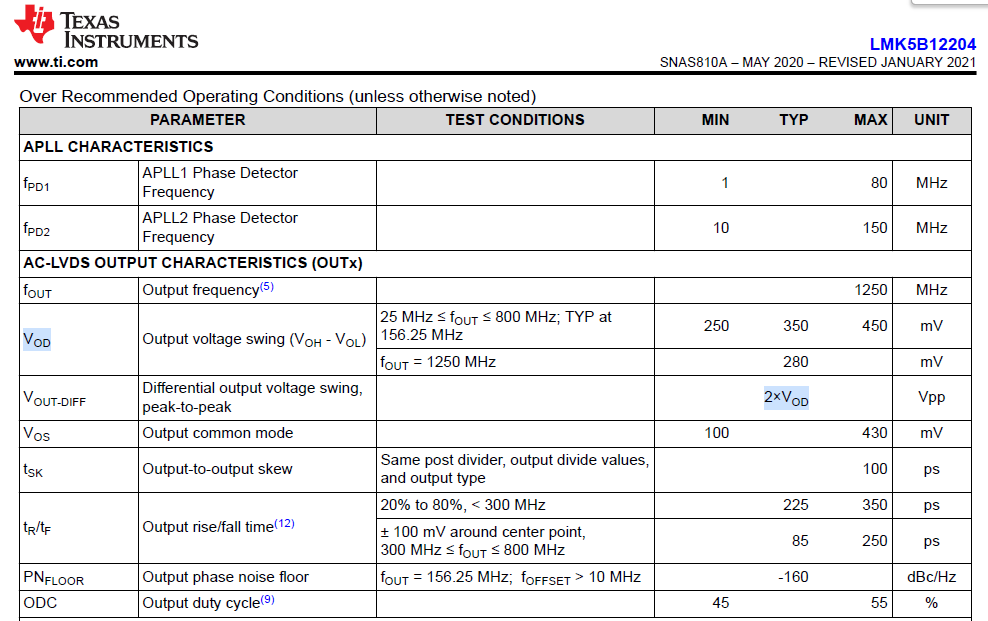
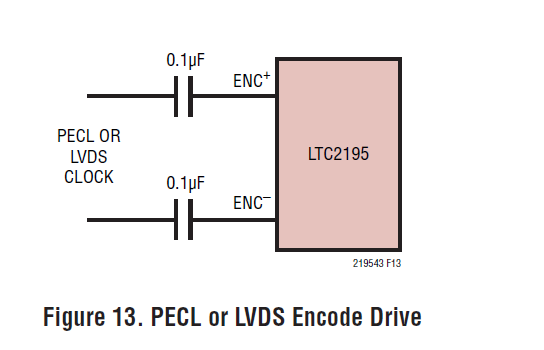
**LTC2193 ADC ENC Input:****--**







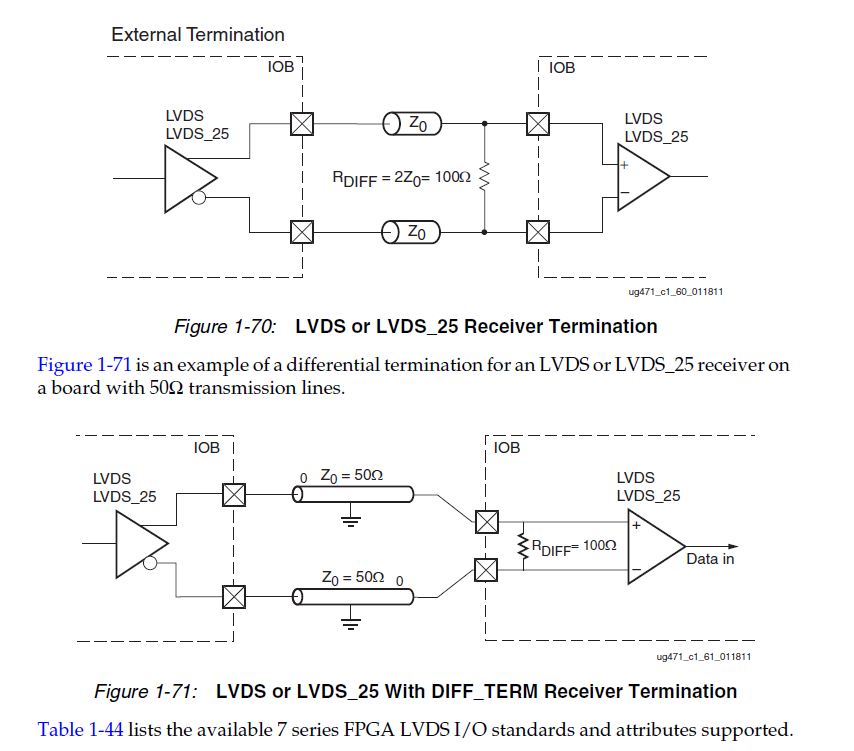
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**Artix-7 HR bank LVDS Receiver Termination**

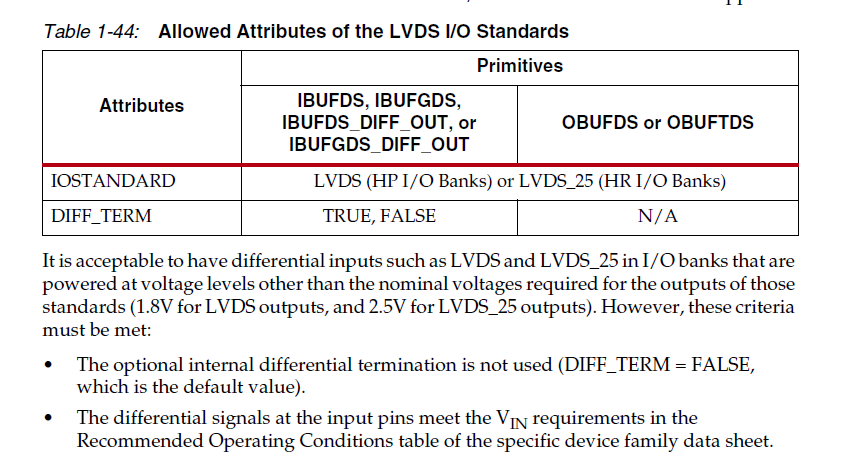
Bank is powered with 2.5V

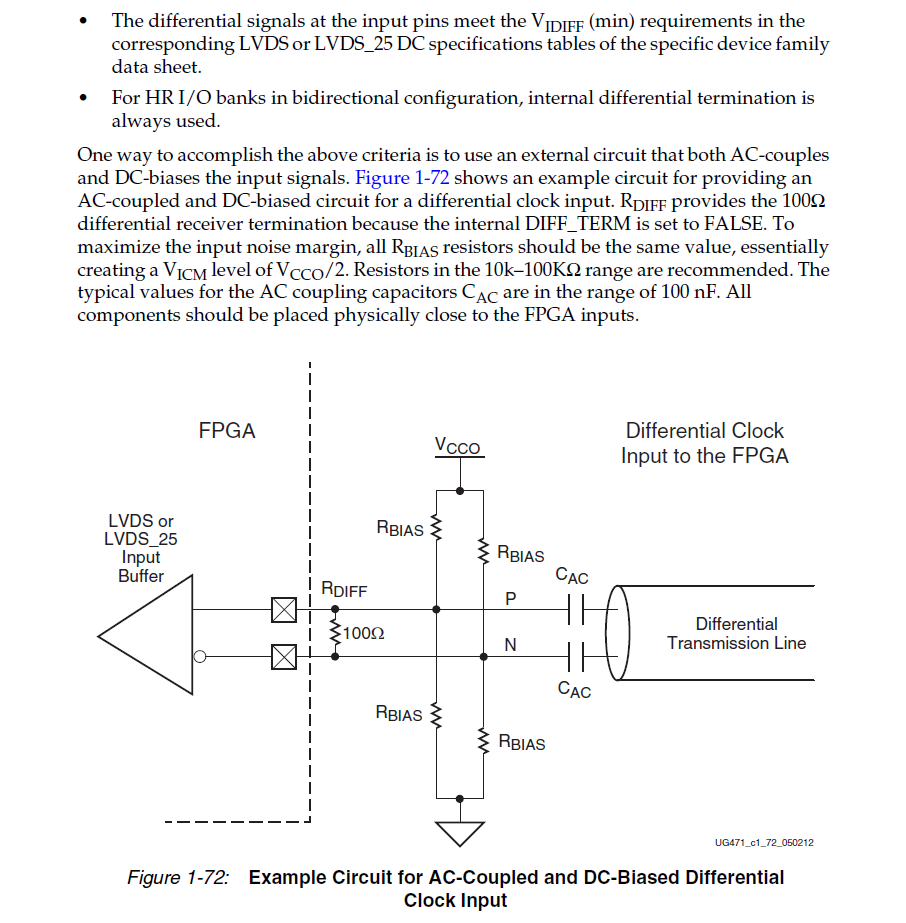
Figure 1-70 is an example of differential termination for an LVDS or LVDS\_25 receiver on a

board with 50Ω transmission lines.



**FPGA clock input**





https://support.xilinx.com/s/question/0D52E00006iHsBqSAK/offchip-input-differential-termination-needed-for-lvds25-input-in-artix7xc7a35t?language=en\_US