HIGH-VOLTAGE MIXED-SIGNAL IC

UC1604

65x192 STN Controller-Driver

ES Specifications
Datasheet Revision: 0.6

IC Version: c_A
July 22, 2010

ULTRA CHIP

The Coolest LCD Driver, Ever!

Table of Content

UC1604

Single-Chip, Ultra-Low Power
65COM by 192SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1604c is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip ’s unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power column and row drivers, the IC contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

? Cellular Phones, Smart Phones, PDA, and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

? Single chip controller-driver support 65x192 graphics STN LCD panels.

? Support both row ordered and column ordered display buffer RAM access.

? A software-readable ID pin to support configurable vender identification.

? Support both row-ordered and column-ordered display buffer RAM access.

? Support industry standard 8-bit parallel bus (8080 or 6800 mode), 4-wire and 3-wire serial buses (S8 and S9), and 2-wire I^2C serial interface.

? Ultra-low power consumption under all display patterns.

? Fully programmable Mux Rate, partial display, Bias Ratio and Frame Rate allow many flexible power management options.

? Software programmable frame rates at 76, 95, 132 and 168 Hz.

? Four software programmable temperature compensation coefficients.

? 7-x internal charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.

? On-chip Power-ON Reset makes RST pin optional.

? Very low pin count (10-pin) allows exceptional image quality in COG format on conventional ITO glass.

? Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.

? V_{DD} (digital) range (Typ.): 1.8V ~ 3.3V
V_{DD} (analog) range (Typ.): 2.7V ~ 3.3V
V_{LCD} range: 4.8V ~ 11.5V

? Available in gold bump dies

? COM/SEG bump information
Bump pitch: 27.6 μM
Bump gap: 12 μM
Bump surface: 2028 μM^2

ORDERING INFORMATION

Part Number	MTP	I²C	Description
UC1604cGAA Yes		Yes	Gold Bumped Die

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I²C

The implementation of I²C is already included and tested in all silicon.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

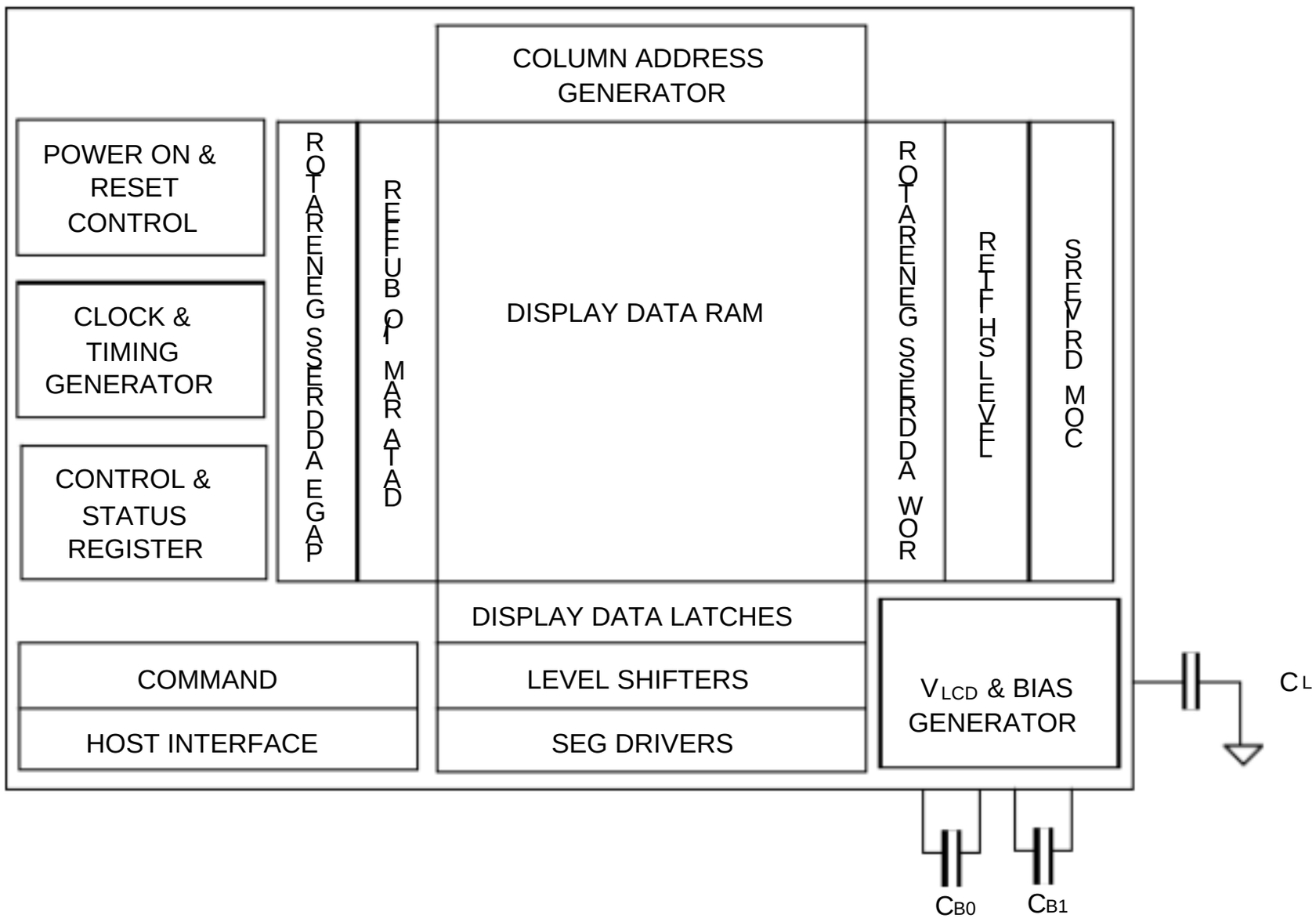
CONTENT DISCLAIMER

CONTACT DETAILS

UltraChip Inc. (Headquarter)
4F, No. 618, Recom Road,
Neihu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

BLOCK DIAGRAM

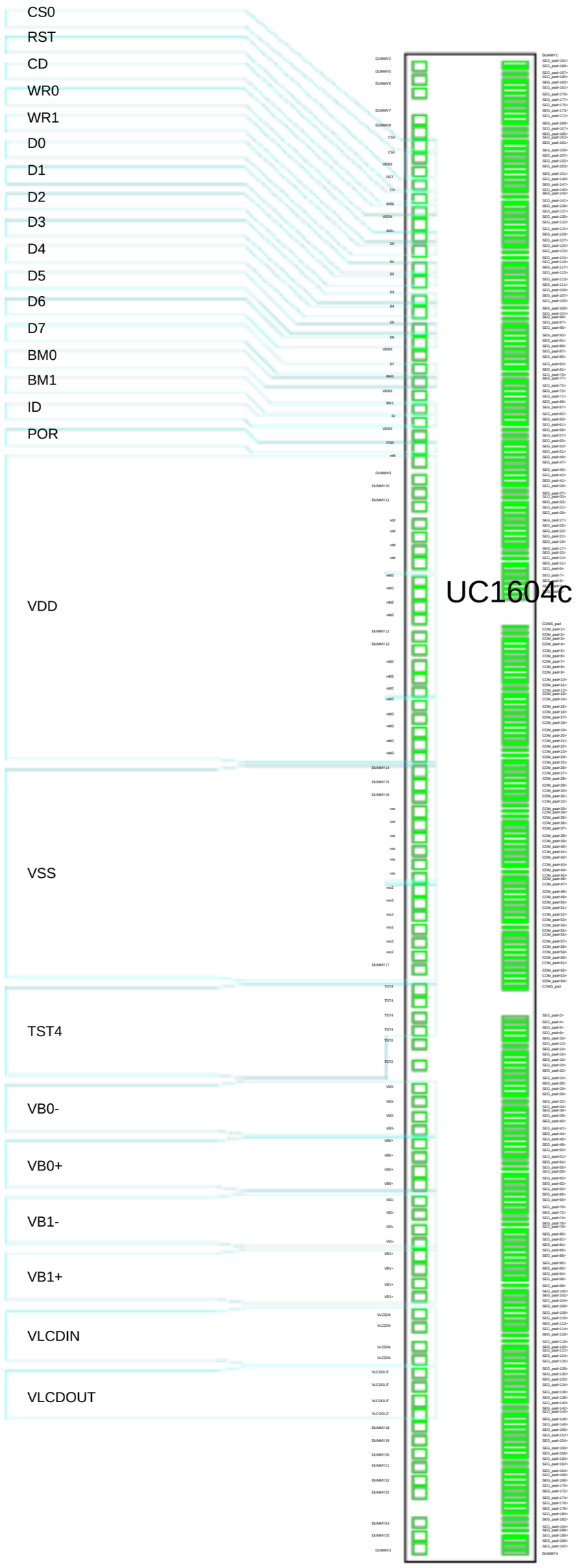


PIN DESCRIPTION

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">MAIN POWER SUPPLY</td></tr>
<tr><td>V_{DD}
V_{DD2}
V_{DD3}</td><td>PWR</td><td>5
7
5</td><td>V_{DD} supplies for Display Data RAM and digital logic, V_{DD2} supplies for V_{LCD} and V_D generator, V_{DD3} supplies for V_{BIAS} and other analog circuits.
V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}.
Please maintain the following relationship:
$V_{DD}+1.3V$ $V_{DD2/3}$ V_{DD}
ITO trace resistance needs to be minimized for V_{DD2}/V_{DD3}.</td></tr>
<tr><td>V_{SS}
V_{SS2}</td><td>GND</td><td>6
6</td><td>Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. In COG applications, minimize the ITO resistance for both V_{SS} and V_{SS2}.</td></tr>
<tr><td colspan="4">LCD POWER SUPPLY & VOLTAGE CONTROL</td></tr>
<tr><td>V_{B1+}
V_{B1-}
V_{B0+}
V_{B0-}</td><td>PWR</td><td>4
4
4
4</td><td>LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. See the “LCD Voltage Setting” section for more details.
In COG application, the resistance of these ITO traces directly affects the SEG driving strength of the resulting LCD module. Minimize these trace resistance is critical in achieving high quality image.</td></tr>
<tr><td>V_{LCDIN}
V_{LCDOUT}</td><td>PWR</td><td>4
4</td><td>Main LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} source is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open.
Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance around 70 ?.</td></tr>
<tr><td colspan="4">? Recommended capacitor values:
C_B: 2.2 μF/5V or 300x(LCD load capacitance), whichever is higher.
C_L: 330nF/25V is appropriate for most applications.</td></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and D[7] by the following relationship:
<table>
<tr><th>BM[1:0]</th><th>D[7]</th><th>Mode</th><th>Remark</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td><td></td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td><td></td></tr>
<tr><td>00</td><td>--</td><td>4-wire SPI w/ 8-bit token</td><td>(S8: conventional)</td></tr>
<tr><td>01</td><td>0</td><td>3-wire SPI w/ 9-bit token</td><td>(S9: conventional)</td></tr>
<tr><td>01</td><td>1</td><td>2-wire serial (I^2C)</td><td></td></tr>
</table></td></tr>
<tr><td>CS1/A3
CS0/A2</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=“H” and CS0 =“L”. When the chip is not selected, D[7:0] will be of high impedance.
In I^2C mode, these two pins specifies bits 3~2 of UC1604c’ device address (A[3:2]).</td></tr>
<tr><td>RST I</td><td></td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1604c has built-in Power-On Reset, the RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD I</td><td></td><td>1</td><td>Select Control data or Display data for read/write operation. In S9, CD pin is not used. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID I 1</td><td></td><td></td><td>ID may be used for production identification.
Connect ID to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
</table>

<table>
<tr><th colspan="2">Name Type</th><th>Pins</th><th>Description</th></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details.
In parallel mode, the meaning of WR[1:0] depends on which interface it is in, 6800 or 8080 mode. In serial interface modes, these two pins are not used, Connect them to V_{SS}.</td></tr>
<tr><td>D7~D0</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[5:3] to SDA.
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>8-bit (BM=1x)</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>s8 (BM=00)</td><td>--</td><td>--</td><td>SDA *</td><td>SDA *</td><td>SDA</td><td>--</td><td>--</td><td>SCK</td></tr>
<tr><td>S9 (BM=01)</td><td>0</td><td>--</td><td>SDA *</td><td>SDA *</td><td>SDA</td><td>--</td><td>--</td><td>SCK</td></tr>
<tr><td>I^2C (BM=01)</td><td>1</td><td>--</td><td>SDA *</td><td>SDA *</td><td>SDA</td><td>--</td><td>--</td><td>SCK</td></tr>
</table>
* D[5:3] : SDA-read; D[3] : SDA-write
For better drive ability, connect D[5:3] together when using read function.
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
<tr><td colspan="4">HIGH VOLTAGE LCD DRIVER OUTPUT</td></tr>
<tr><td>SEG1 ~ SEG192</td><td>HV 192</td><td></td><td>SEG (column) driver outputs. Support up to 192 pixels.
Leave unused SEG drivers open-circuit.</td></tr>
<tr><td>COM1 ~ COM64</td><td>HV 64</td><td></td><td>COM (row) driver outputs. Support up to 64 rows.
When designing LCM, always start from COM1. If the LCM has N pixel rows and N is less than 64, set CEN to be N-1, and leave COM drivers [N+1 ~ 64] open-circuit.</td></tr>
<tr><td>CIC</td><td>HV</td><td>2</td><td>Icon driver outputs. Leave it open if not used.</td></tr>
<tr><td colspan="4">MISC. PINS</td></tr>
<tr><td>V_{DDX}</td><td></td><td>5</td><td>Auxiliary V_{DD}. This pin is connected to the main V_{DD} bus within the IC. It's provided to facilitate chip configurations in COG application.
There's no need to connect V_{DDX} to main V_{DD} externally and it should NOT be used to provide V_{DD} power to the chip.</td></tr>
<tr><td>TST4</td><td>I</td><td>4</td><td>TST4 is used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50 ?.</td></tr>
<tr><td>TST2</td><td>I/O</td><td>2</td><td>Test I/O pins. Leave these pins open during normal use.</td></tr>
<tr><td>POR</td><td></td><td>1</td><td>Power-ON Reset control.
Connect the POR pin to V_{DD} for "H"; to Vss for "L" to control the POR register.
"L": Power-ON Reset Enable.
"H": Power-ON Reset Disabled.</td></tr>
<tr><td>Dummy</td><td></td><td>25</td><td>Dummy pins are NOT connected inside the IC.</td></tr>
<tr><td colspan="4">Note: Several control registers will specify "0 based index" for COM and SEG electrodes. In those situations, SEG X will correspond to index X-1, and the value range for those index register will be 0~63 for COM and 0~191 for SEG.</td></tr>
</table>

RECOMMENDED COG LAYOUT



NOTES FOR VDD WITH COG:

The operation condition, V_{DD}=1.8V (typical), should be satisfied under all operating conditions. UC1604c's D_{D} peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1604c's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1604c contains registers, which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, Command Table and Command Description.

Name: The Symbolic reference of the register. Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in Bold font are default values after Power-Up-Reset and System-Reset.

Name	Bits	Default	Description
SL 6		00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (64). Setting SL outside of this range causes undefined effect on the displayed image.
CA 8		00H	Display Data RAM Column Address. Value range is 0 ~ 191. (Used in Host to Display Data RAM access)
PA 4		0H	Display Data Page Row Address. Value range is 0 ~ 8. (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_D. 00b: 6 01b: 7 10b: 8 11b: 9
TC	2	0H	Temperature Compensation (per ^oC) 00b: -0.00% 01b: -0.05% 10b: -0.10% 11b: -0.15%
PM	8	49H	Electronic Potentiometer to fine tune V_D and V_{LCD}
PMO 6		00H	PM offset.
PC	3	6H	Power Control. PC[1:0]: low pump charge current select 00b: 0.6mA 01b: 1.0mA 10b: 1.4mA 11b: 2.3mA PC[2]: to program the build-in charge pump stages 0b: External V_{LCD} 1b: Internal V_{LCD} (7x charge pump)
AC	3	1H	Address Control: AC[0]: WA: Automatic column/row Wrap Around (Default 1: ON) AC[1]: Auto-Increment order 0: Column (CA) first 1: Page (PA) first AC[2]: RID: RA (row address) auto increment direction (L:+1 H:-1)
DC 3		0H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default 0: OFF) DC[1]: APO: All Pixels ON (Default 0: OFF) DC[2]: Display ON/OFF (Default 0: OFF)
LC	6	08H	LCD Control: LC[0]: Reserved (always set to 0) LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: 0:OFF) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: 0:OFF) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 76 fps 01b: 95 fps 10b: 132 fps 11b: 168 fps LC[5] : Partial Display. 0b: Disabled . Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled. Mux-Rate = DEN-DST+1

Name	Bits	Default	Description
CEN DST DEN	6 6 6	3FH 00H 3FH	COM scanning end (last COM with full line cycle, 0-based index) Display start (first COM with active scan pulse, 0-based index) Display end (last COM with active scan pulse, 0-based index) Please maintain the following relationship: CEN = “ the actual number of pixel rows on the LCD ” – 1 CEN DEN DST+ 9
MTPC	5	00H	MTP Programming Control: MTPC[2:0] : MTP command 000 : Idle 001 : Read 010 : Erase 011 : Program 1XX : For UltraChip debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore 1: Use
MTPM	6	00H	MTP Write Mask. For each bit, Bit =1: program, Bit=0: no action.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
ID	1	PIN	Access the connected status of ID pins.
POR	1	PIN	Power-ON Reset control. Controlled by the POR pin. “ L ”: Power-ON Reset Enable. “ H”: Power-ON Reset Disabled.

COMMAND TABLE

The following is a list of host commands supported by UC1604c

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

Useful Data bits – Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	ID	MX	MY	WA	DE	WS	MD	MS	Get Status PMO[5:0]	N/A
				VER	POR	#	#	#	#	#	#		
4.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0
	Set Column Address MSB 0		0	0	0	0	1	#	#	#	#	Set CA [7:4]	0
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	110b
7.	Set Adv. Program Control (double-byte command)	0 0		0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0~3	N/A
				#	#	#	#	#	#	#	#		
8.	Set Scroll Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
9.	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
10.	Set V_{BIAS} Potentiometer (double-byte command)	0 0		1	0	0	0	0	0	0	1	Set PM[7:0]	49H
				#	#	#	#	#	#	#	#		
11.	Set Partial Display Control 0		0	1	0	0	0	0	1	0	#	Set LC[5]	0b
12.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13.	Set Frame Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	01b
14.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
15.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
16.	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
17.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	0	Set LC[2:1]	00b
18.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
19.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
20.	Set Test Control (double-byte command)	0 0		1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
				#	#	#	#	#	#	#	#		
21.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
22.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[5:0]	63D
				--	--	#	#	#	#	#	#		
23.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[5:0]	0
				--	--	#	#	#	#	#	#		
24.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[5:0]	63D
				--	--	#	#	#	#	#	#		
25.	Set MTP Operation Control	0	0	1	1	1	1	1	0	0	0	Set MTPC[4:0]	00H
				--	--	--	#	#	#	#	#		
26.	Set MTP Write Mask	0	0	1	1	1	1	1	0	0	1	Set MTPM[5:0]	0
				--	--	#	#	#	#	#	#		
27.	Set V_{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Set VMTP1[7:0]	N/A
				#	#	#	#	#	#	#	#		
28.	Set V_{MTP2} Potentiometer	0	0	1	1	1	1	0	1	0	1	Set VMTP2[7:0]	N/A
				#	#	#	#	#	#	#	#		
29.	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0	Set MTPWT[7:0]	N/A
				#	#	#	#	#	#	#	#		
30.	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1	Set MTPRT[7:0]	N/A
				#	#	#	#	#	#	#	#		
Serial Read Command (Enabled only in S8/S9 mode)													
31.	Get Status	0	0	1	1	1	1	1	1	1	0	Get Status PMO[5:0]	N/A
		0 1		ID	MX	MY		WA	DE	WS	MD	MS	
				VER	POR	#	#	#	#	#	#		

Any bit pattern other than those listed above may result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte to Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data write to SRAM							

2. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data read from SRAM							

Write/Read Data Byte (Command 1,2) access Display Data RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing Set Page Address and Set Column Address commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of the page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches the end of the page, CA will be reset to 0 and PA will increase or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM, PA will be wrapped around to the other end of RAM and continue.

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	ID	MX MY	WA DE WS	MD MS				
	0 1		VER	POR PMO5		PMO4	PMO3	PMO2	PMO1	PMO0

Status1 definitions:

ID: Provide access to ID pins connection status.

MX : Status of register LC[1], mirror X.

MY : Status of register LC[2], mirror Y.

WA: Status of register AC[0]. Automatic column/row wrap around.

DE : Display Enable flag. DE=1 when display is enabled.

WS: MTP Operation succeeded

MD: MTP Option (1 for MTP version, 0 for non-MTP version)

MS: MTP action status

Status2 definitions:

Ver: IC Version, 0 ~ 1.

POR: Power-ON Reset control.

PMO[5:0]: PM offset value. Default: 00H

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0 0 0 0				CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	0 0 0 1				CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA value range: 0 ~191

5. Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.00%/ ^{o}C 01b = -0.05%/ ^{o}C 10b = -0.10%/ ^{o}C 11b = -0.15%/ ^{o}C

6. Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Power Control PC[2:0]	0	0	0	0	1			PC2	PC1	PC0

PC[1:0] : to select low-pump charge current

00b: 0.6mA 01b: 1.0mA 10b: 1.4mA 11b: 2.3mA

Set PC[2] : to program the build-in charge pump stages.

0b: External V_{LCD} 1b: Internal V_{LCD} (7x charge pump)

7. Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control APC[R][7:0]	0 0		0	0	1	1	0	0	R	R
(Double-byte command)	0 0	APC7		APC6	APC5	APC4	APC3	APC2	APC1	APC0

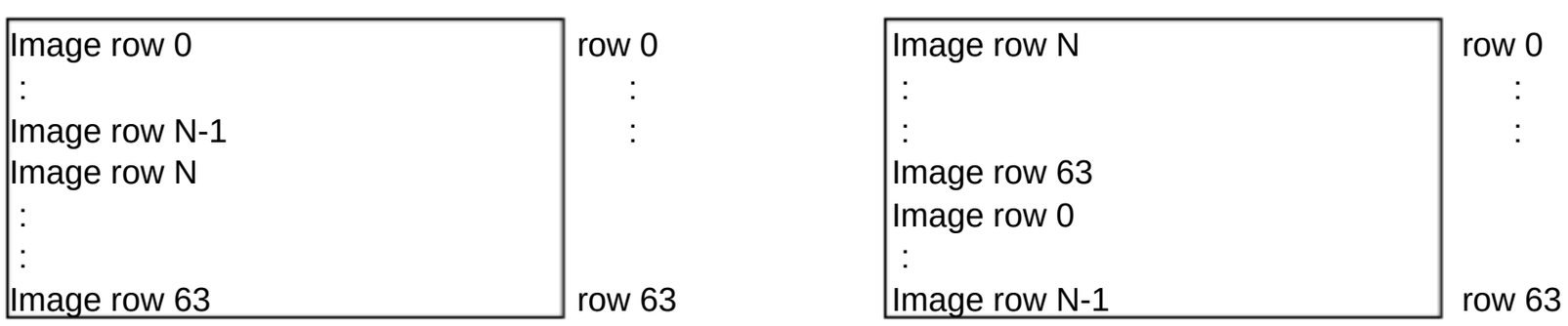
For UltraChip only. Please Do NOT use.

8. Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line SL[5:0]	0	0	0	1		SL5	SL4	SL3	SL2	SL1 SL0

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. Icon output CIC will not be affected by Set Scroll Line command.



9. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA[3:0]	0	0	1	0	1	1	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output CIC.

Possible value = 0~8.

10. Set V_{BIAS} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V BIAS Potentiometer PM [7:0]	0 0		1 0 0 0 0 0 0 1							
(Double-byte command)	0	0	PM7 PM6 PM5 PM4 PM3 PM2 PM1 PM0							

Program V BIAS Potentiometer (PM[7:0]). See section LCD Voltage Setting for more detail.

Effective range: 0 ~ 255 (Default: 49H)

11. Set Partial Display Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [5]	0	0	1 0 0 0 0 1 0							LC5

This command is used to enable partial display function.

LC[5] : 0b: Disable Partial Display , Mux-Rate = CEN+1 (DST, DEN not used.)
1b: Enable Partial Display, Mux-Rate = DEN-DST+1

12. Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1 0 0 0 1					AC2	AC1	AC0

Program registers AC[2:0] for RAM address control. It controls the auto-increment behavior of CA and PA.

AC[0] – WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and CA or PA will increase by one.

AC[1] – Auto-Increment order
0 : column (CA) increasing (+1) first until CA reach CA boundary, then PA will increase by (+/-1).
1 : page (PA) increasing (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2] – PID, page address (PA) auto increment direction (0/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether page address will be adjusted by +1 or -1.

13. Set Frame Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Frame Rate LC [4:3]	0	0	1 0 1 0 0 0						LC4	LC3

Program LC [3] for frame rate setting

00b: 76 fps 01b: 95 fps 10b: 132 fps 11b: 168 fps
(fps: frame-per-second)

14. Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1 0 1 0 0 1 0							DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.
(Default: 0)

15. Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM. (Default: 0)

16. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[2]	0	0	1	0	1	0	1	1	1	DC2

This command is for programming register DC[2]. When DC[2] is set to 1, UC1604c will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers. (Default: 0)

17. Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Control LC[2:1]	0	0	1	1	0	0	0	MY	MX	0

Set LC[2:1] for COM (row) mirror (MY), SEG (column) mirror (MX). (Default: 00b)

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 63-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

18. System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

19. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for “ no operation ”.

20. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	1	1	1	0	0	1	TT	
(Double byte command)	0	0	For test only							

This command is used for UltraChip production testing. Please do NOT use.

21. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:

00b= 6 01b = 7 10b = 8 11b= 9

22. Set COM End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [5:0]	0 0		1 1 1 1	0 0 0 1						
(Double-byte command)	0 0		-	-	CEN register parameter					

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 64 pixel rows, the LCM designer should set CEN to N-1 (where N is the number of pixel rows) and use COM1 through COM-N as COM driver electrodes. (Default: 63)

23. Set Partial Display Start

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [5:0]	0 0		1 1 1 1	0 0 1 0						
(Double-byte command)	0 0		-	-	DST register parameter					

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

24. Set Partial Display End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [5:0]	0 0		1 1 1 1	0 0 1 1						
(Double-byte command)	0 0		-	- DEN	register parameter					

This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

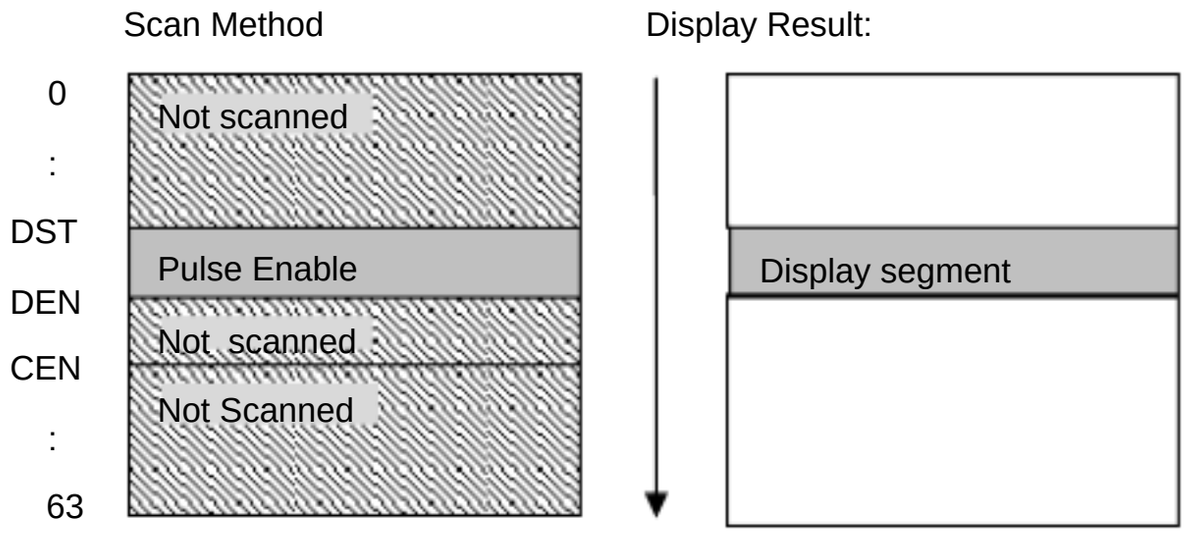
CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

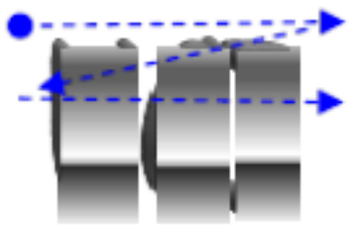
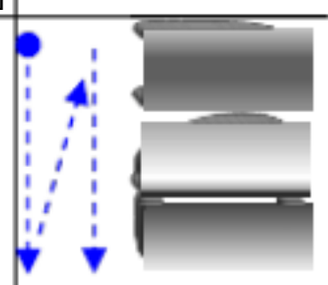
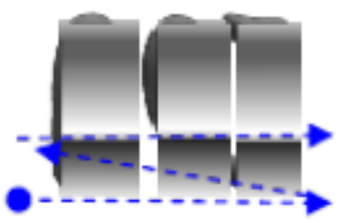
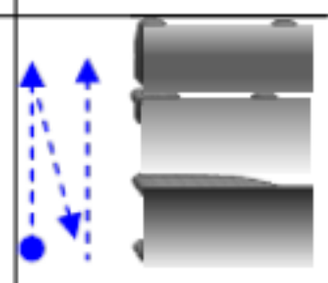
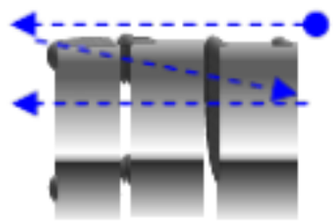
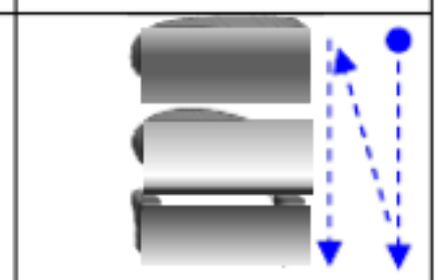
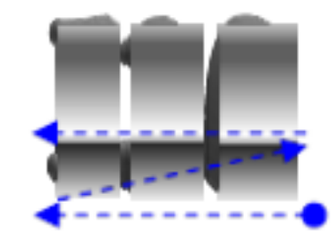
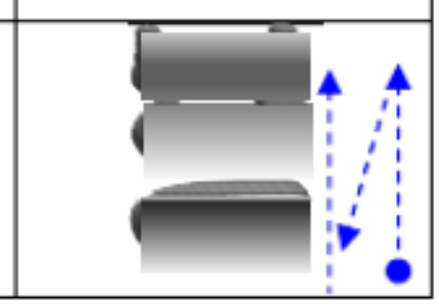
When LC[5]=1b, the Mux-Rate is narrowed down to DEN – DST + 1. When MUX rate is reduced, reduce the frame rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

For minimum power consumption, set LC[5]=1b, set (DST, DEN, CEN) to minimize Mux rate, use slowest frame rate which satisfies the flicker requirement, set PC[0]=0b, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 16, it is recommended to set BR=6 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.

Keep CEN DEN DST+ 9



Display Data Direction	Function Setting			Image in DDRAM (Physical origin: upper left corner)	Display Data Direction	Function Setting			Image in DDRAM (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	RID AC[2]			AIO AC[1]	MX LC[1]	RID AC[2]	
Normal 0 0 0					X-Y Exchange	1 0 0			
Y-mirror 0		0	1		X-Y Exchange Y-mirror	1 0 1			
X-mirror 0		1	0		X-Y Exchange X-mirror	1 1 0			
X-mirror Y-mirror	0 1 1				X-Y Exchange X-mirror Y-mirror	1 1 1			

25. Set MTP Operation Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC [4:0]	0 0		1 1 1 1	1 0 0 0						
(Double-byte command)	0 0		-	-	-	MTPC4	MTPC3	MTPC2	MTPC1	MTPC0

This command is for MTP operation control: (MTPC[4:0] : default: D0H)

MTPC[2:0] : MTP command
000 : Sleep 001 : MTP Read 010 : MTP Erase 011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (set H to active MTP value)

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

26. Set MTP Write Mask

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM [5:0] (Double-byte command)	0 0		1 1 1 1 1 0 0 1							
	0 0		-	-	MTPM[5:0]					

This command enables Write to each of the individual MTP bits. When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no Write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[5:0] : Set PMO value (Default: 00H)

27. Set V_{MTP1} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set VMTP1 [7:0] (Double-byte command)	0 0		1 1 1 1 0 1 0 0							
	0 0		VMTP1[7:0]							

This command is for fine tuning V_{OPT1} setting (with BR=00).

28. Set V_{MTP2} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set VMTP2 [7:0] (Double-byte command)	0 0		1 1 1 1 0 1 0 1							
	0 0		VMTP2[7:0]							

This command is for fine tuning V_{MTP2} setting (with BR=11).

29. Set MTP Write Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPWT [7:0] (Double-byte command)	0 0		1 1 1 1 0 1 1 0							
	0 0		MTPWT[7:0]							

This command is only valid when MTPC[3]=1.

30. Set MTP Read Timer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPRT [7:0] (Double-byte command)	0 0		1 1 1 1 0 1 1 1							
	0 0		MTPRT[7:0]							

This command is only valid when MTPC[3]=1.

Serial Read Command (Enable only in S8/S9 mode):

31. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0 0		1 1 1 1 1 1 1 0							
	0	1	ID	MX MY	WA DE WS MD MS					
	0 1		VER	POR PMO5		PMO4	PMO3	PMO2	PMO1	PMO0

See command 3.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1604c via registers CEN, DST, DEN, and partial display control flags LC[5].

Combined with low power partial display mode and a low bias ratio of 6, UC1604c can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (BR) is defined as the ratio between V_{LCD} and V_D, i.e.

$$BR = V_{LCD} / V_D,$$

where $V_D = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum Bias Ratio can be estimated by $\sqrt{Mux} + 1$. BR of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

UC1604c supports four BR as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6 7 8			9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	– 0.00	– 0.05	– 0.10	– 0.15

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: BR (Bias Ratio), PM (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{o}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

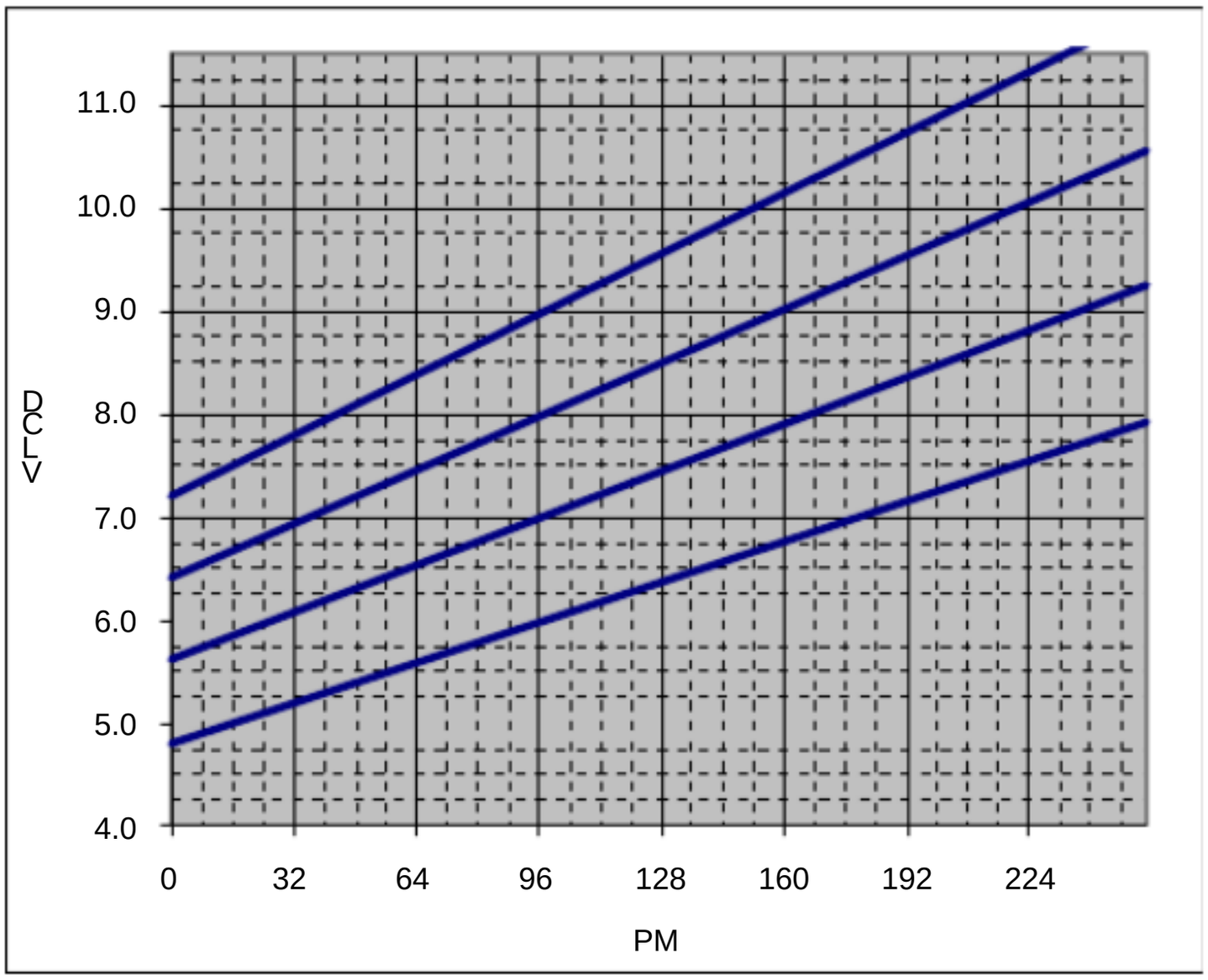
Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment or MTP is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1604c is designed to handle LCD panels with loading up to ~24nF using 20- ? /Sq ITO glass with $V_{DD2/3}$ 2.6V. For larger LCD panels, use lower resistance ITO glass packaging.

VLCD QUICK REFERENCE



VLCD Programming Curve.

BR	CV0 (V)	CPM (mV)	PM	VLCD Range (V)
6 4.800		12.24	0 4.80	
			255 7.92	
7 5.600		14.28	0 5.60	
			255 9.24	
8 6.400		16.32	0 6.40	
			255 10.56	
9 7.200		18.36	0 7.20	
			234 11.50	

Note:

1. For good product reliability, keep V LCD under 11.5V over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

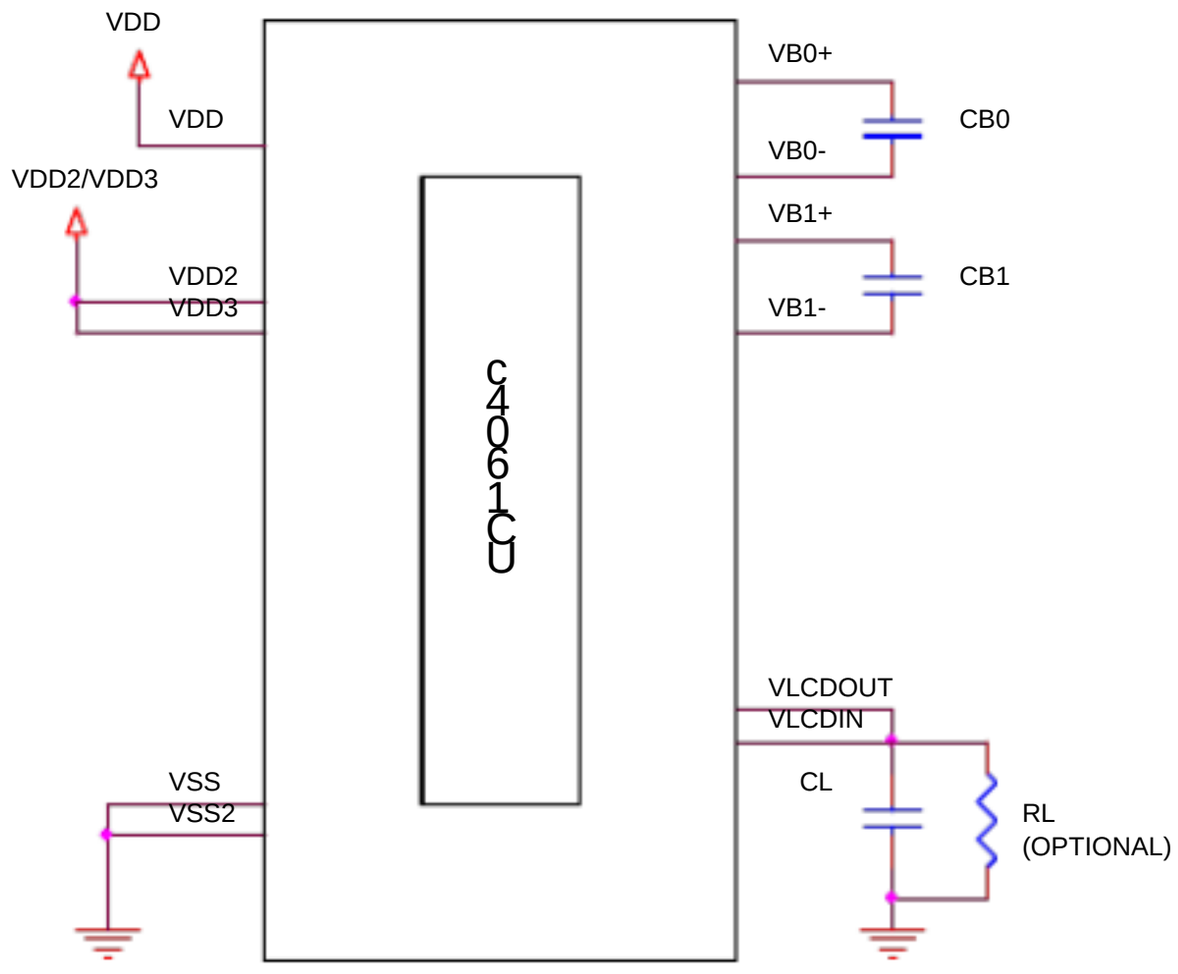


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_{Bx} : 2.2 μF/5V or 300x LCD load capacitance, whichever is higher.

C_L : 330nF(25V) is appropriate for most applications.

R_L: 3.3M~10M ? to act as a draining circuit when V_{DD} is shut down abruptly .

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1604c contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

4 different frame rates are provided for system design flexibility. The frame rate is controlled by register LC[4:3]. When Mux-Rate is above 45, Frame rate: 76fps, 95fps, 132fps, and 168 fps.

When Mux-Rate is lowered to 44, 33, 22, and 17, frame rate will be scaled down automatically by 1.5, 2, 3, and 4 times to reduce power consumption.

Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM x, where x = 1~64, refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via Set Display Enable command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1604c will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1",and UC1604c will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL DISPLAY

UC1604c provides flexible control of Mux Rate and active display area. Please refer to commands Set COM End, Set Partial Display Start, and Set Partial Display End for more detail.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1604c can be as short as 91 μ S, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 9.23\ \mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$|RC_{MAX} - RC_{MIN}| < 2.76\ \mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 6.30\ \mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / (# of column), where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, and crosstalk will increase.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/65	1/9	13.3%	10.6%	9.6%
1/65	1/8	13.1%	10.5%	9.5%

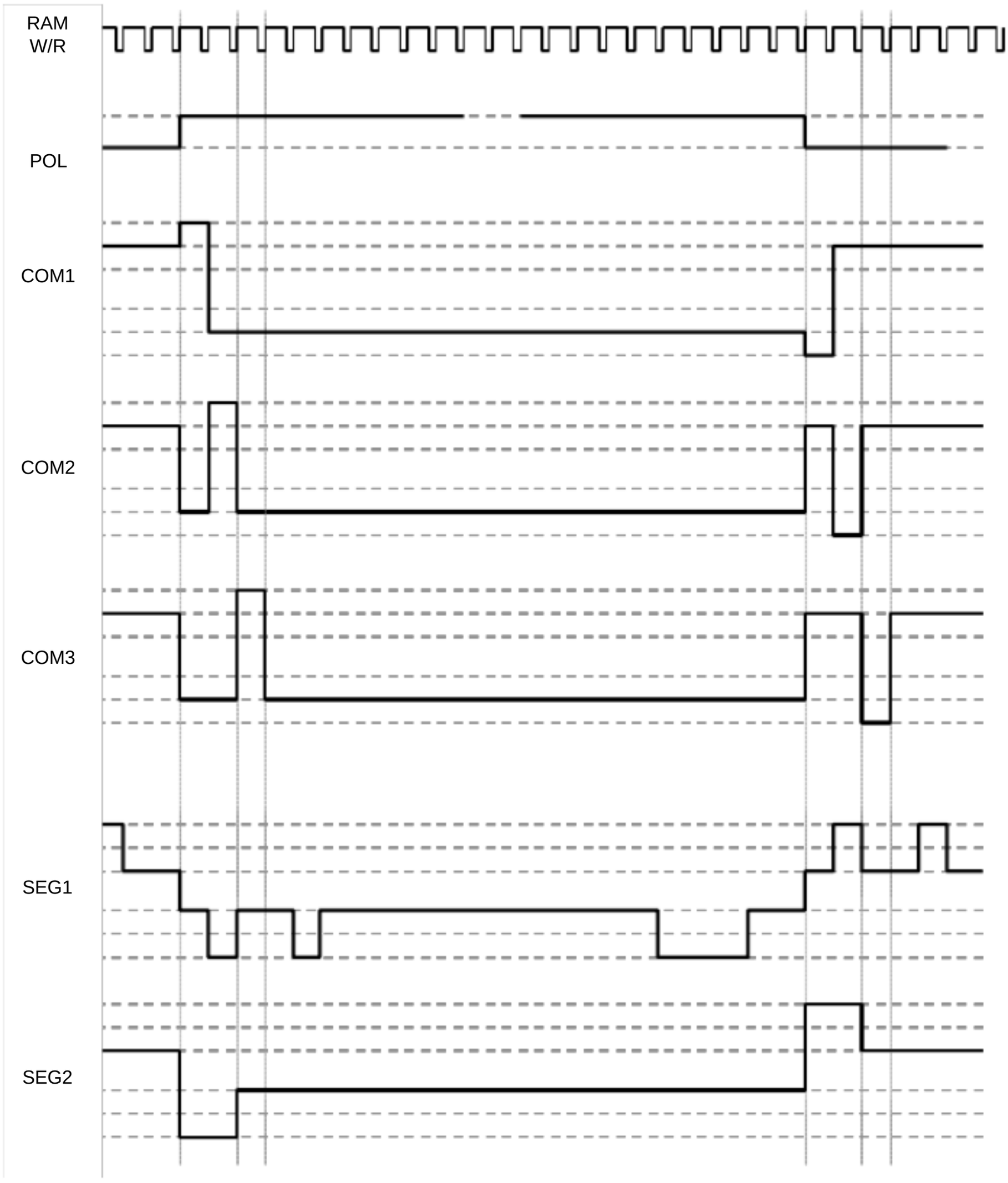


FIGURE 2: COM and SEG Electrode Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1604c supports 2 8-bit parallel bus protocols and 3 serial bus protocols. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

		Bus Type				
		8080	6800	S8(4-wire)	S9(3-wire)	I^2C(2-wire)
Width 8-bit			8-bit	Serial		
Access		Read / Write		Read (status) / Write		R / W
Serial & Parallel I/F	BM[1:0]	10 11 00 01 01				
	D[7] Data		Data	--	0	1
	CS[1:0] Chip	Select				A[3:2]
	CD Control/Data				0	
	WR0	$\overline{WR}$	$\overline{R/W}$	0		
	WR1	$\overline{RD}$	EN	0		
	D[6,2,1] Data			--		
	D[5:3], D[0]	Data		D[5:3]=SDA, D[0]=SCK		

Connect unused control pins and data bus pins to V_{DD} for "H" or V_{SS} for "L".

	CS Disable Bus Interface	CS Init. Bus State	RESET Init. Bus State
8-bit	9	–	9
S8 or S9	9	9	9
I^2C	–	–	9

? CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.

? RESET can be pin reset / soft reset / power on reset.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1604c internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, by either Set CA or Set PA command, a dummy read cycle need to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

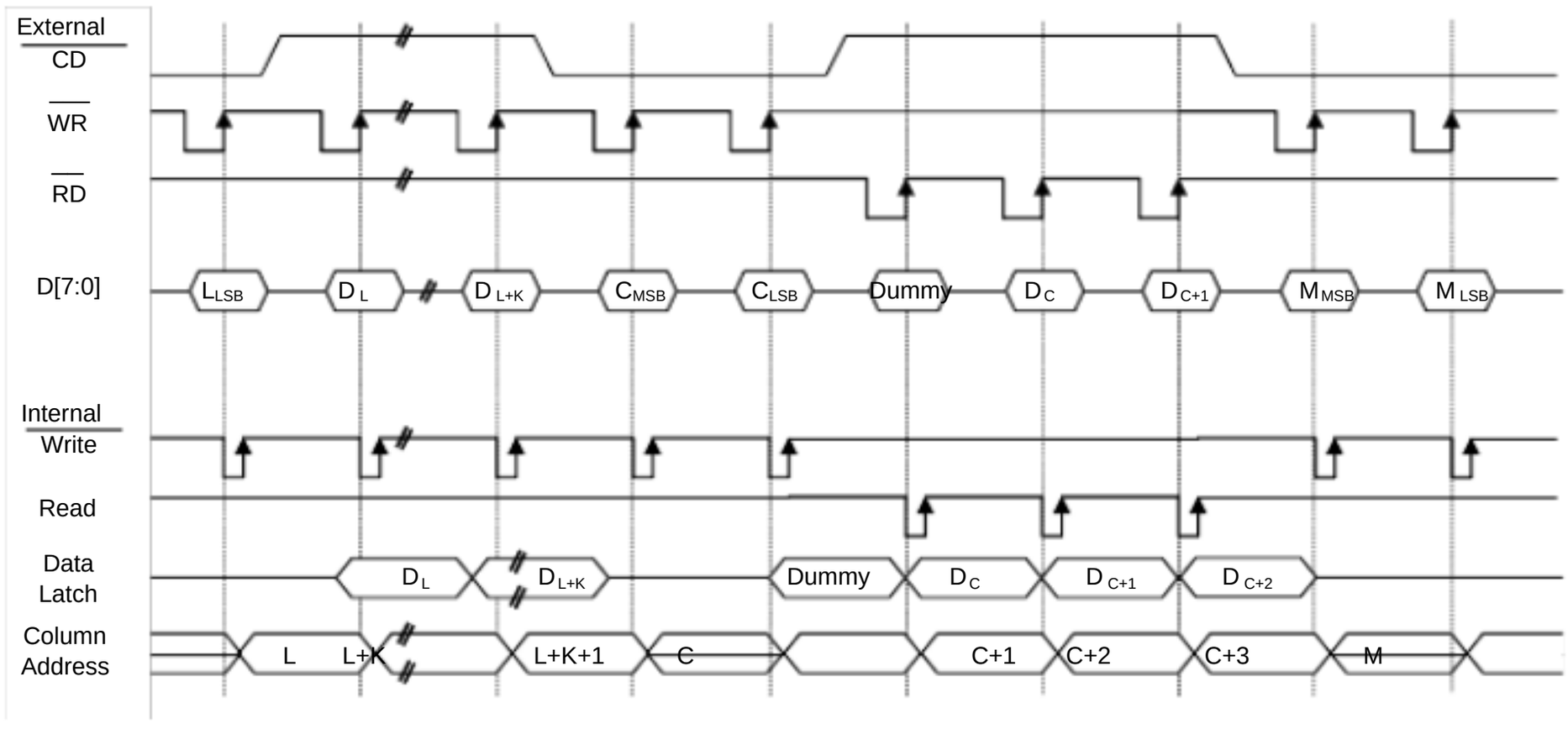


Figure 3: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1604c supports three serial modes, one 4-wire SPI mode (S8), one 3-wire SPI mode (S9) and one 2-wire SPI mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0] and D[7]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, these 8 bits will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

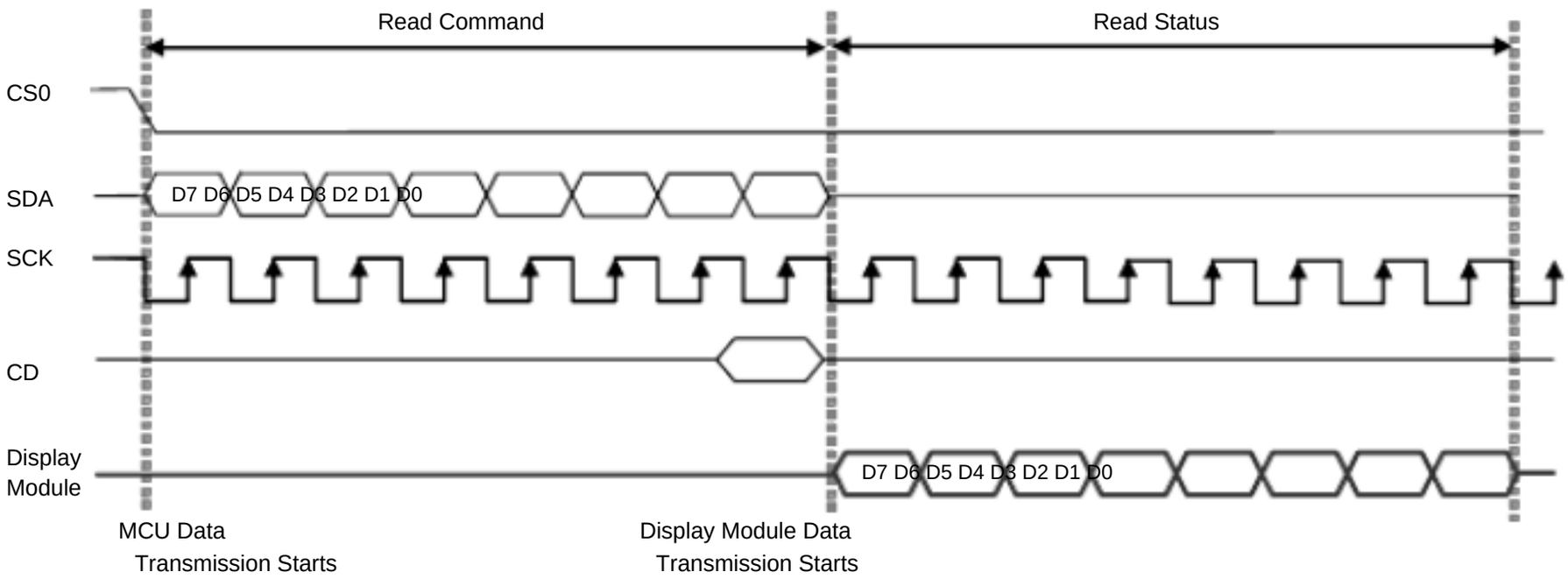


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

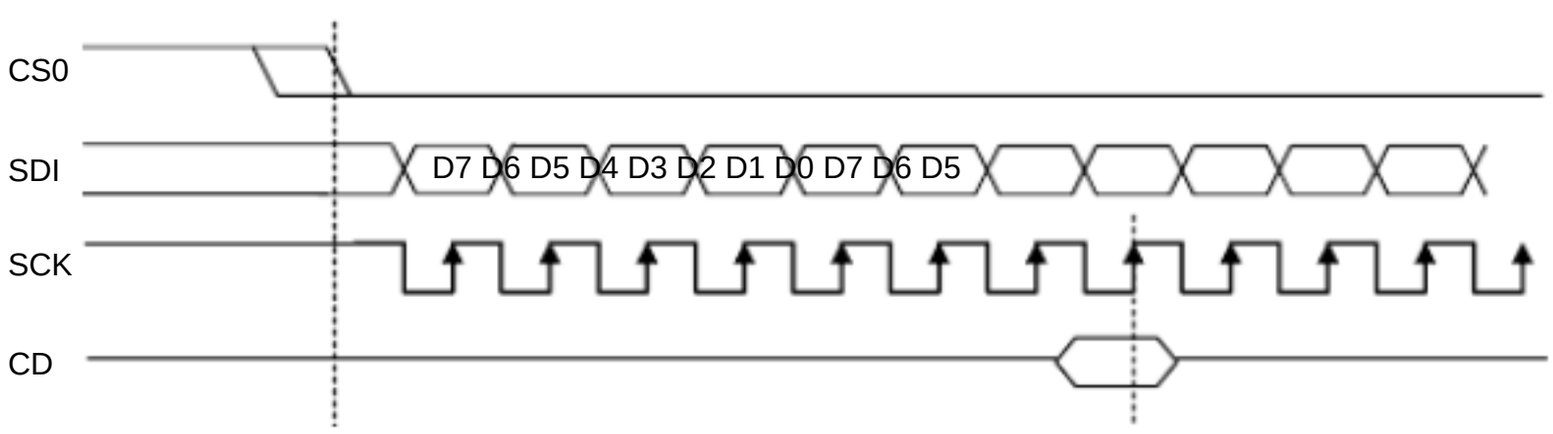


Figure 4.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIER) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

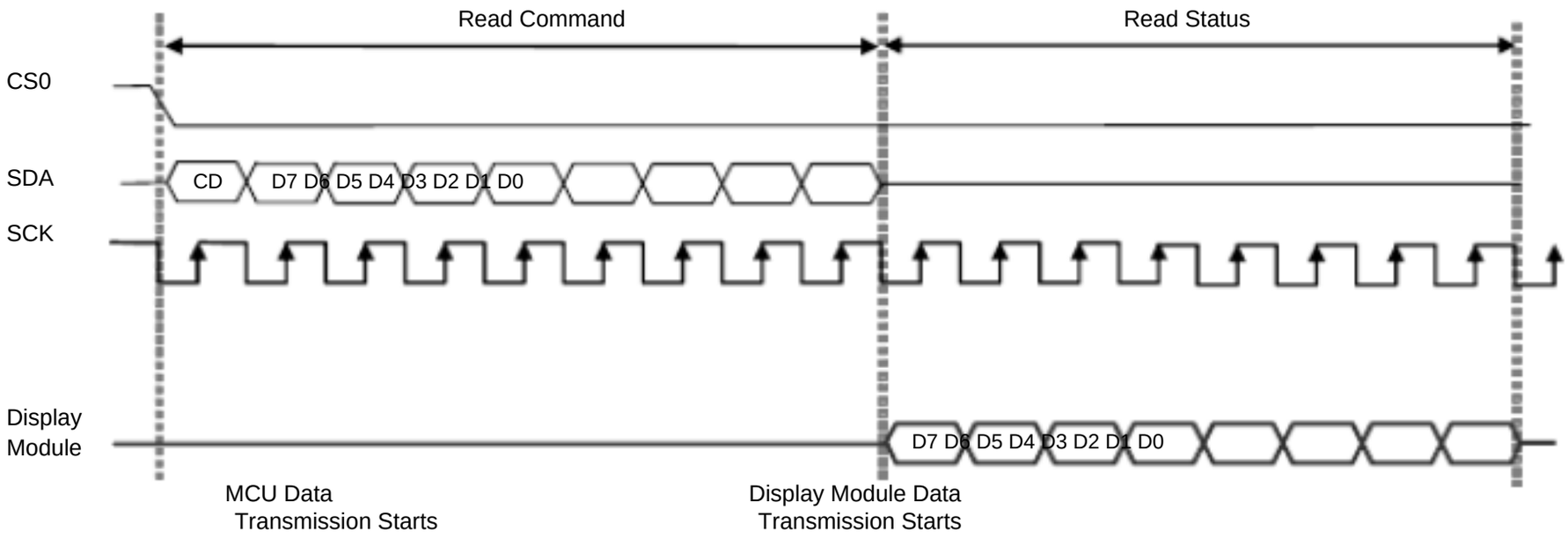


FIGURE 5.a: 3-wire Serial Interface (S9) – Read

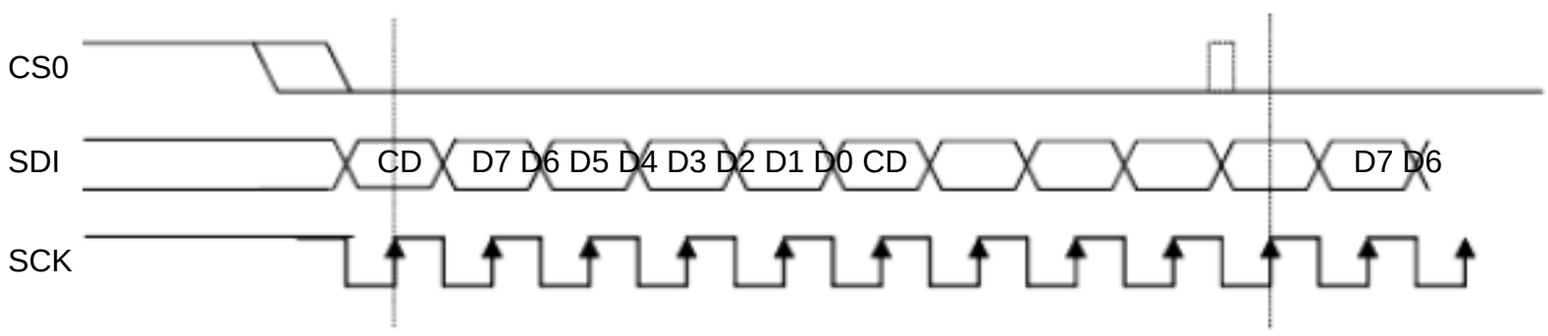


Figure 5.b: 3-wire Serial Interface (S9) – Write

I2C (2-WIRE) INTERFACE

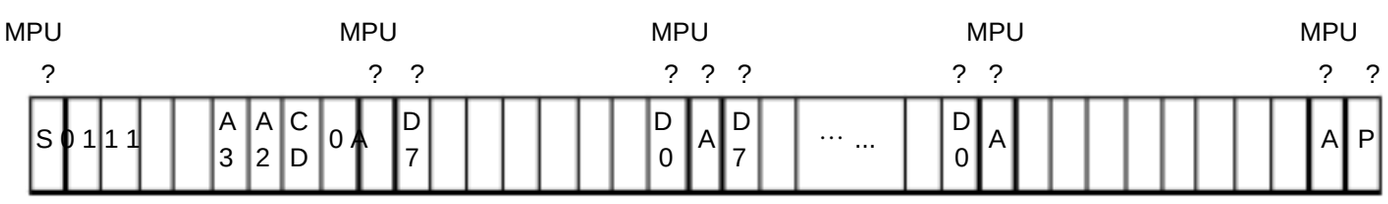
When BM[1:0] is set to "LH" and D[7:6] is set to "HH", UC1604c is configured as an I2C bus signaling protocol compliant slave device. Please refer to I2C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1604c's device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I2C mode.

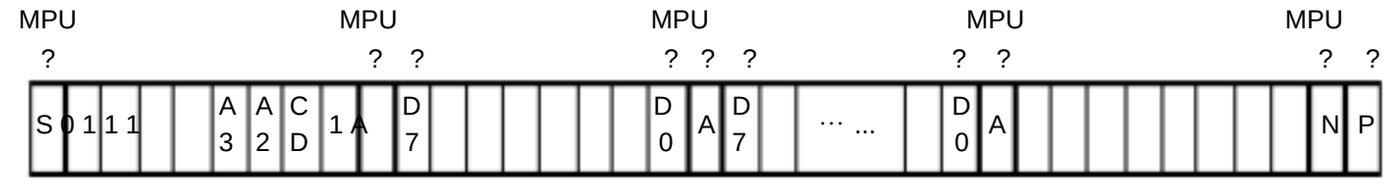
Each UC1604c I2C interface sequence starts with a "S" (Start) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I2C mode and should be connected to V_{SS}.

Write Mode



Read Mode

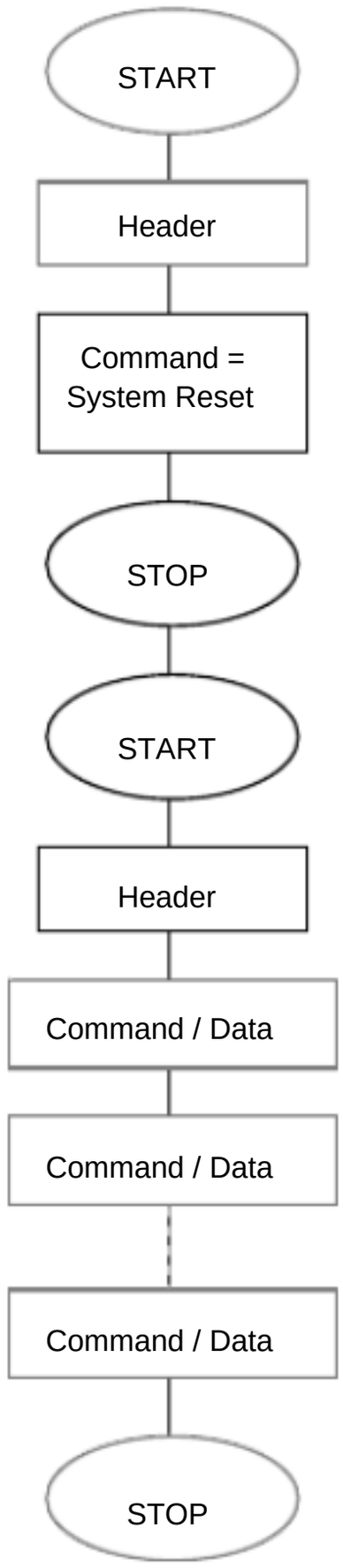


The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R ù W) or the content type (C ù D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1604c will send out a "A" (Acknowledge signal, pull to "L"). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1604c) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE mode), or an N (Not Acknowledged, in READ mode) is sent by the bus master.

When using I²C serial mode, if command "System Reset" is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

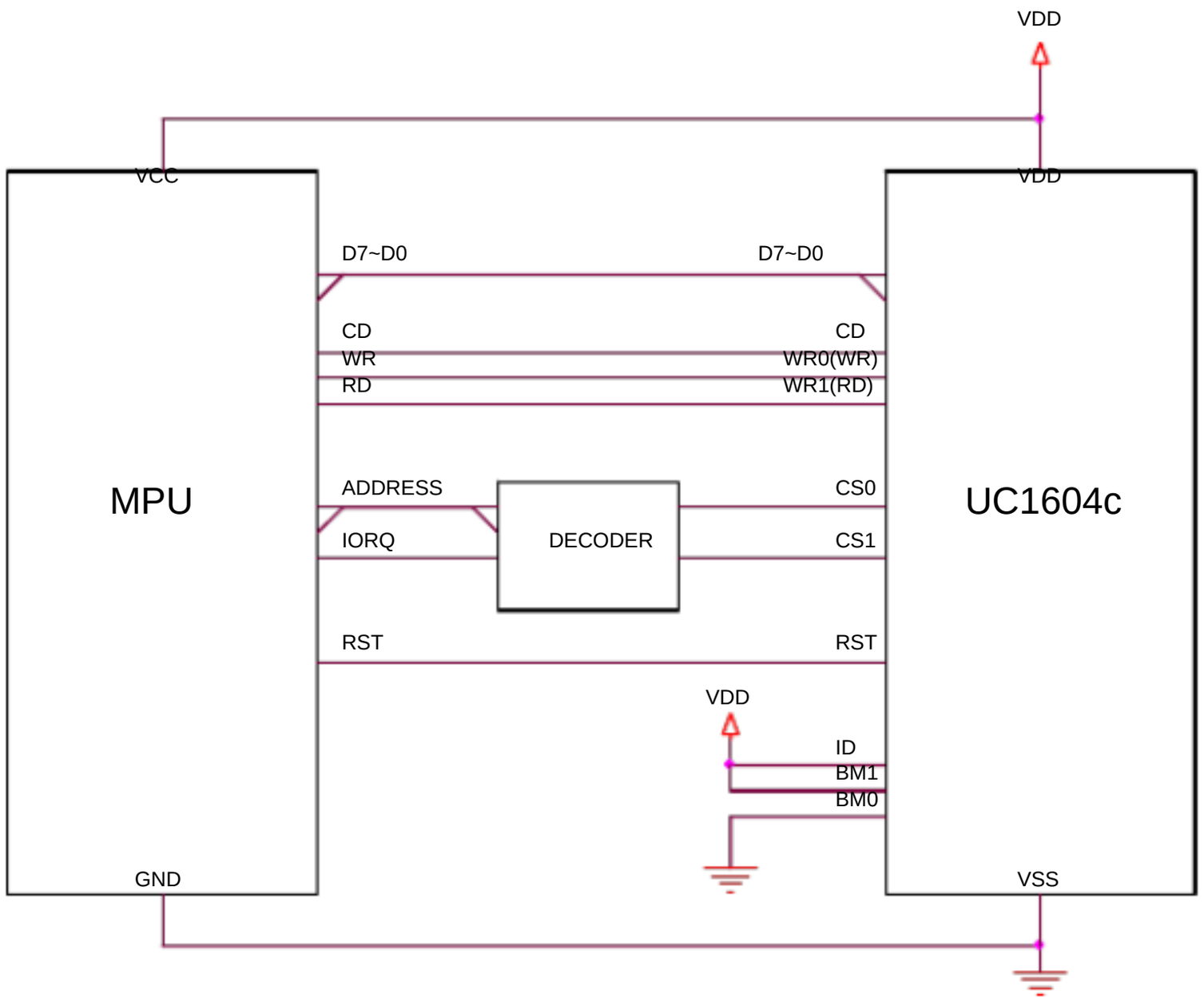


FIGURE 6: 8080/8bit parallel mode reference circuit

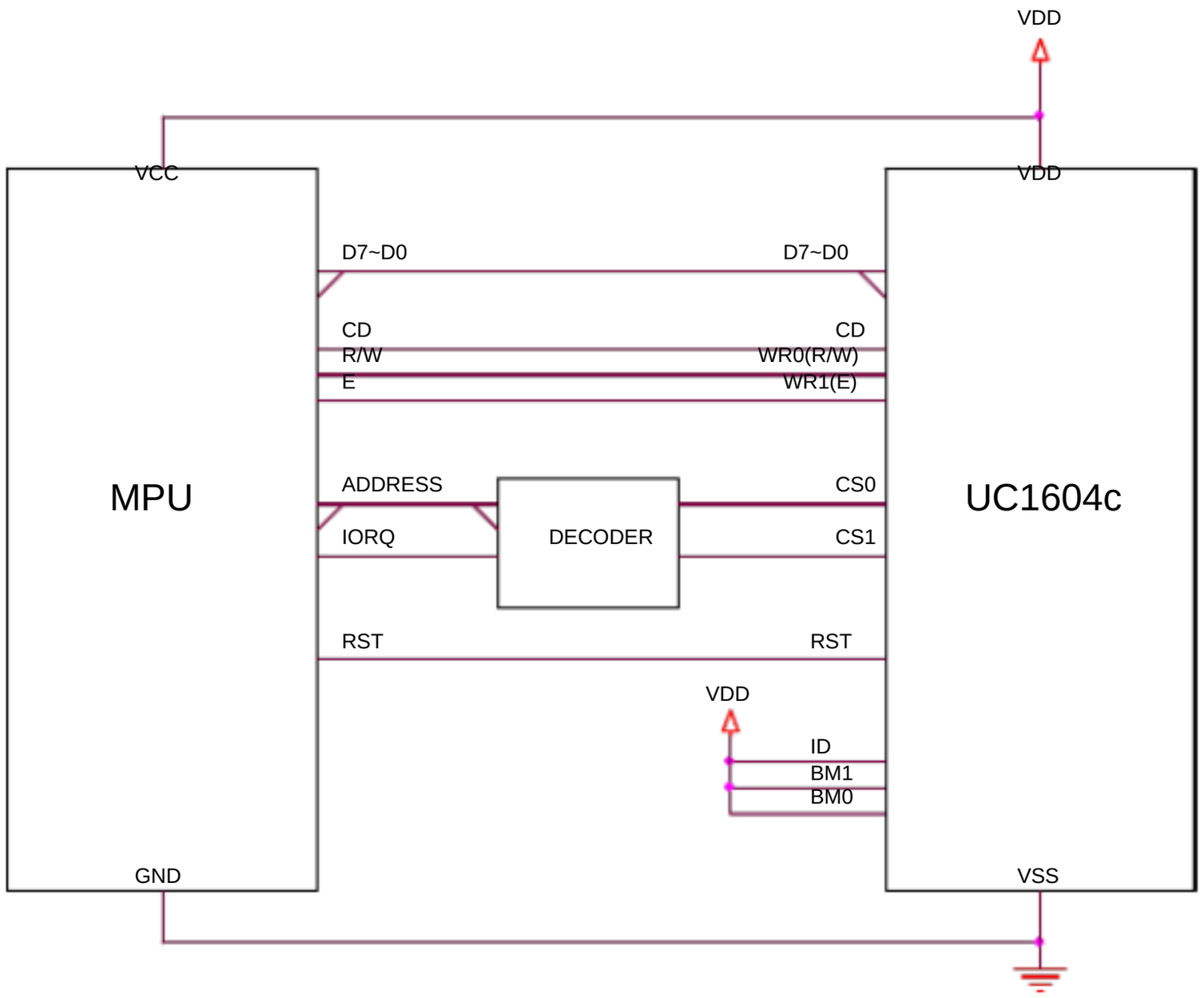


FIGURE 7: 6800/8bit parallel mode reference circuit

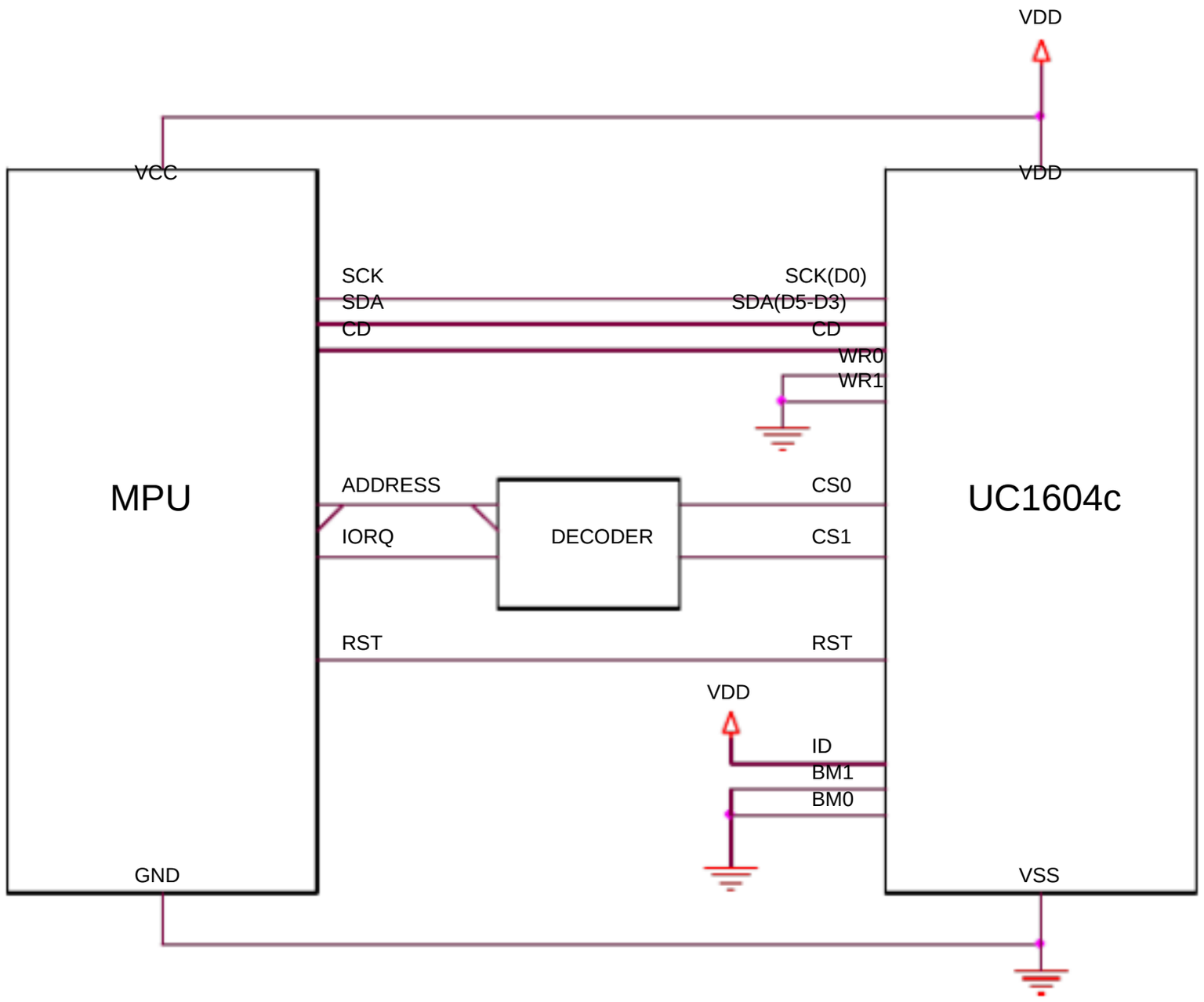


FIGURE 8: Serial-8 serial mode reference circuit

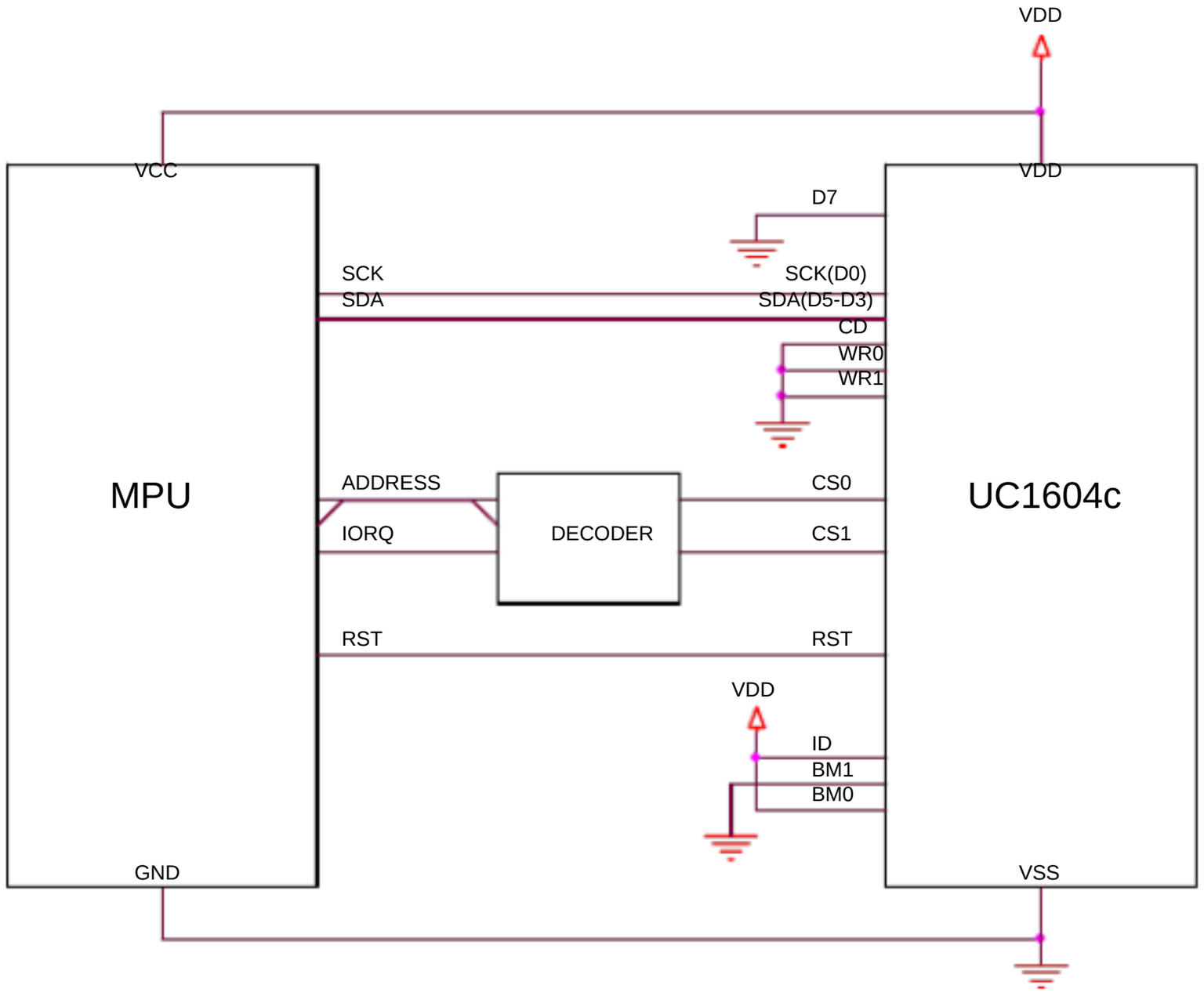


FIGURE 9: Serial-9 serial mode reference circuit

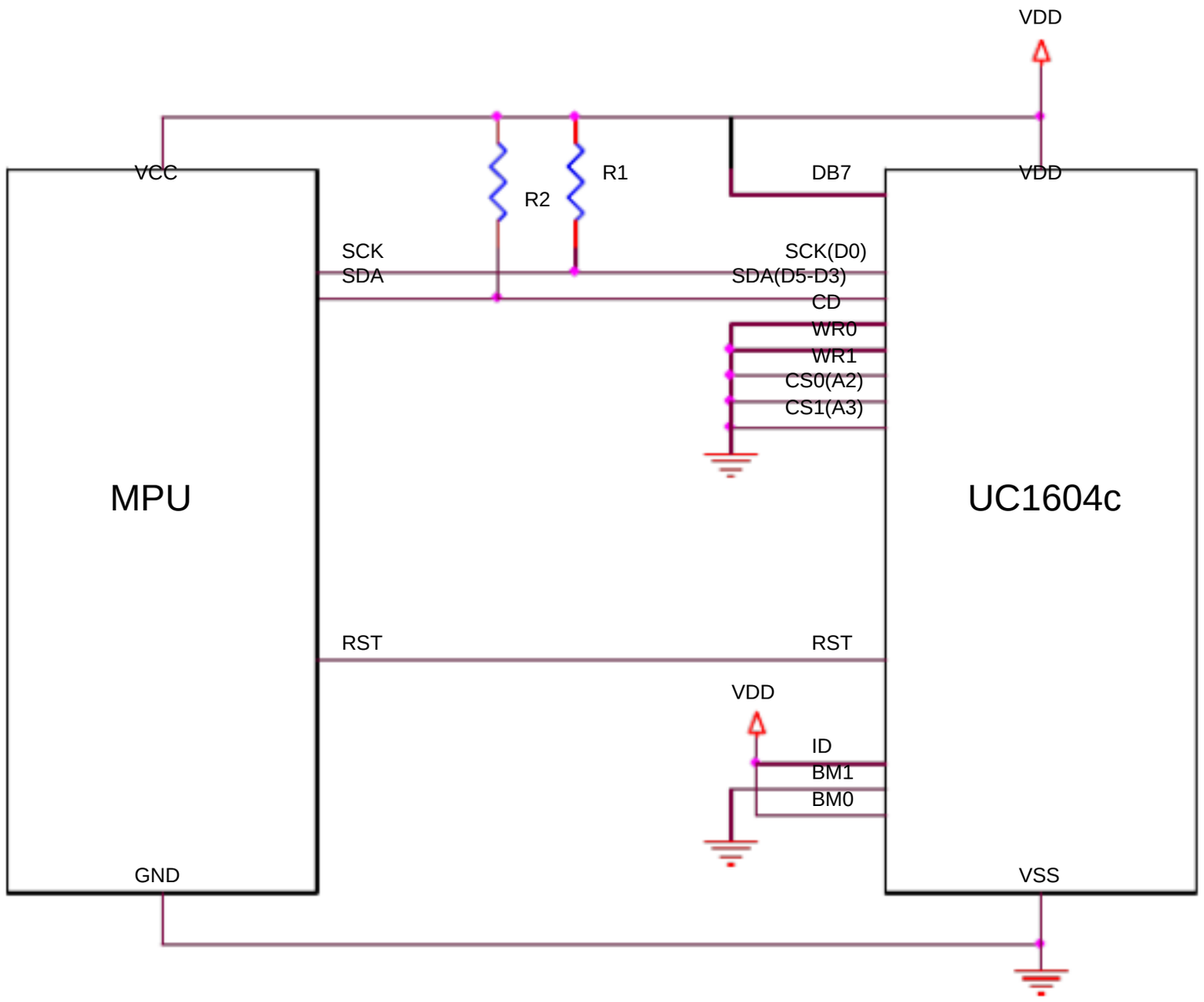


FIGURE 10: I2C serial mode reference circuit

Note

? The ID pins are for production control. The connection will affect the content of D[7] of the 1-st byte of the Get Status command. Connect to VDD for "H" or VSS for "L".

? RST pin is optional. When the RST pin is not used, connect it to VDD.

? When using I2C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.

? R1, R2: 2k ~ 10k ? , use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.

DISPLAY DATA RAM (DDRAM)

DATA ORGANIZATION

The input display data is stored to a dual port static DDRAM (DDRAM, for Display Data RAM) organized as 65x192.

After setting CA and RA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing Set Row Address and Set Column Address commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (191), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increase or decrease, depending on the setting of row Increment Direction (RID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 7), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (191 – CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[2]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by SL rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed Rm scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1-st line period of each field
Line = SL
Otherwise
Line = Mod(Line +1, 64)

Where Mod is the modular operator, and Line is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above Line generation formula produce the “loop around” effect as it effectively resets Line to 0 when Line+1 reaches 64.

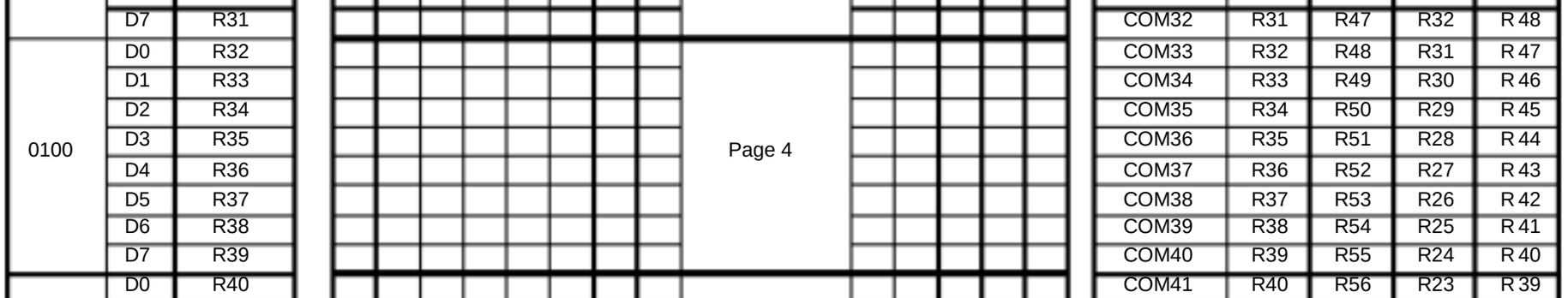
MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(SL + MR -1 , 64)
Otherwise
Line = Mod(Line-1 , 64)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

PA[3:0]	0	Line Address	Panel Location	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
0000	D0	R0	COM1	R0	R16	R63	R 15
	D1	R1	COM2	R1	R17	R62	R 14
	D2	R2	COM3	R2	R18	R61	R 13
	D3	R3	COM4	R3	R19	R60	R 12
	D4	R4	COM5	R4	R20	R59	R 11
	D5	R5	COM6	R5	R21	R58	R 10
	D6	R6	COM7	R6	R22	R57	R9
	D7	R7	COM8	R7	R23	R56	R8
0001	D0	R8	COM9	R8	R24	R55	R7
	D1	R9	COM10	R9	R25	R54	R6
	D2	R10	COM11	R10	R26	R53	R5
	D3	R11	COM12	R11	R27	R52	R4
	D4	R12	COM13	R12	R28	R51	R3
	D5	R13	COM14	R13	R29	R50	R2
	D6	R14	COM15	R14	R30	R49	R1
	D7	R15	COM16	R15	R31	R48	R0
0010	D0	R16	COM17	R16	R32	R47	R 63
	D1	R17	COM18	R17	R33	R46	R 62
	D2	R18	COM19	R18	R34	R45	R 61
	D3	R19	COM20	R19	R35	R44	R 60
	D4	R20	COM21	R20	R36	R43	R 59
	D5	R21	COM22	R21	R37	R42	R 58
	D6	R22	COM23	R22	R38	R41	R 57
	D7	R23	COM24	R23	R39	R40	R 56
0011	D0	R24	COM25	R24	R40	R39	R 55
	D1	R25	COM26	R25	R41	R38	R 54
	D2	R26	COM27	R26	R42	R37	R 53
	D3	R27	COM28	R27	R43	R36	R 52
	D4	R28	COM29	R28	R44	R35	R 51
	D5	R29	COM30	R29	R45	R34	R 50
	D6	R30	COM31	R30	R46	R33	R 49
	D7	R31	COM32	R31	R47	R32	R 48
0100	D0	R32	COM33	R32	R48	R31	R 47
	D1	R33	COM34	R33	R49	R30	R 46
	D2	R34	COM35	R34	R50	R29	R 45
	D3	R35	COM36	R35	R51	R28	R 44
	D4	R36	COM37	R36	R52	R27	R 43
	D5	R37	COM38	R37	R53	R26	R 42
	D6	R38	COM39	R38	R54	R25	R 41
	D7	R39	COM40	R39	R55	R24	R 40
0101	D0	R40	COM41	R40	R56	R23	R 39
	D1	R41	COM42	R41	R57	R22	R 38
	D2	R42	COM43	R42	R58	R21	R 37
	D3	R43	COM44	R43	R59	R20	R 36
	D4	R44	COM45	R44	R60	R19	R 35
	D5	R45	COM46	R45	R61	R18	R 34
	D6	R46	COM47	R46	R62	R17	R 33
	D7	R47	COM48	R47	R63	R16	R 32
0110	D0	R48	COM49	R48	R0	R15	R 31
	D1	R49	COM50	R49	R1	R14	R 30
	D2	R50	COM51	R50	R2	R13	R 29
	D3	R51	COM52	R51	R3	R12	R 28
	D4	R52	COM53	R52	R4	R11	R 27
	D5	R53	COM54	R53	R5	R10	R 26
	D6	R54	COM55	R54	R6	R9	R 25
	D7	R55	COM56	R55	R7	R8	R 24
0111	D0	R56	COM57	R56	R8	R7	R 23
	D1	R57	COM58	R57	R9	R6	R 22
	D2	R58	COM59	R58	R10	R5	R 21
	D3	R59	COM60	R59	R11	R4	R 20
	D4	R60	COM61	R60	R12	R3	R 19
	D5	R61	COM62	R61	R13	R2	R 18
	D6	R62	COM63	R62	R14	R1	R 17
	D7	R63	COM64	R63	R15	R0	R 16
1000	D0	R64	CIC	R64	R64	R64	R 64



Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

? Page 0 SEG 1 (D7-D0) : 0001 1111b
? Page 0 SEG 2 (D7-D0) : 1100 1100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1604c has two different types of Reset:

Power-ON-Reset and System-Reset .

Power-ON-Reset is performed right after V_{DD} is connected to power. Power-On-Reset will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the System Reset .

System Reset can also be activated by connecting the RST pin to ground.

In the following discussions, Reset means System Reset .

The differences between pin reset and software reset are

Procedure (Restoring to default value)	Pin Reset (Power On Reset)	Software Reset
Column Address : CA[7:0]=0	V	V
Page Address : PA[3:0]=0	V	V
RAM Address Control : AC[2:0]=001b	V	V
Temp. Compensation : TC[1:0]=00b	V	X
Power Control : PC[2:0]=110b	V	X
Scroll Line : SL[5:0]=0	V	X
Vbias Potentiometer : PM[7:0]=49h	V	X
Partial Display Control : LC[5]=0b	V	X
Frame Rate : LC[4:3]	V	X
All-Pixel-On : DC[1]=0b	V	X
Inverse Display : DC[0]=0b	V	X
Display Enable : DC[2]=0b	V	X
LCD Mapping Control : LC[2:1]=00b	V	X
Test Control	V	X
LCD Bias Ratio : BR[1:0]=11b	V	X
COM End : CEN[6:0]=63d	V	X
Partial Display Command	V	X
MTP Function Control	V	X

RESET STATUS

When UC1604c enters RESET sequence:

? Operation mode will be “ Reset ”

? All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1604c has three operating modes (OM):
Reset, Sleep, Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM 00		10	11
Host Interface	Active	Active	Active
Clock OFF		OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:
Set Display Enable , and System Reset .

When DC[2] is modified by Set Display Enable , OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1604c internal clock. To ensure consistent system states, wait at least 10 µS after issuing the Set Display Enable command or triggering System Reset .

Action	Mode	OM
RST_ pin pulled "L" Power ON reset	Reset 00	
Set Driver Enable to "0" Sleep		10
Set Driver Enable to "1" Normal		11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

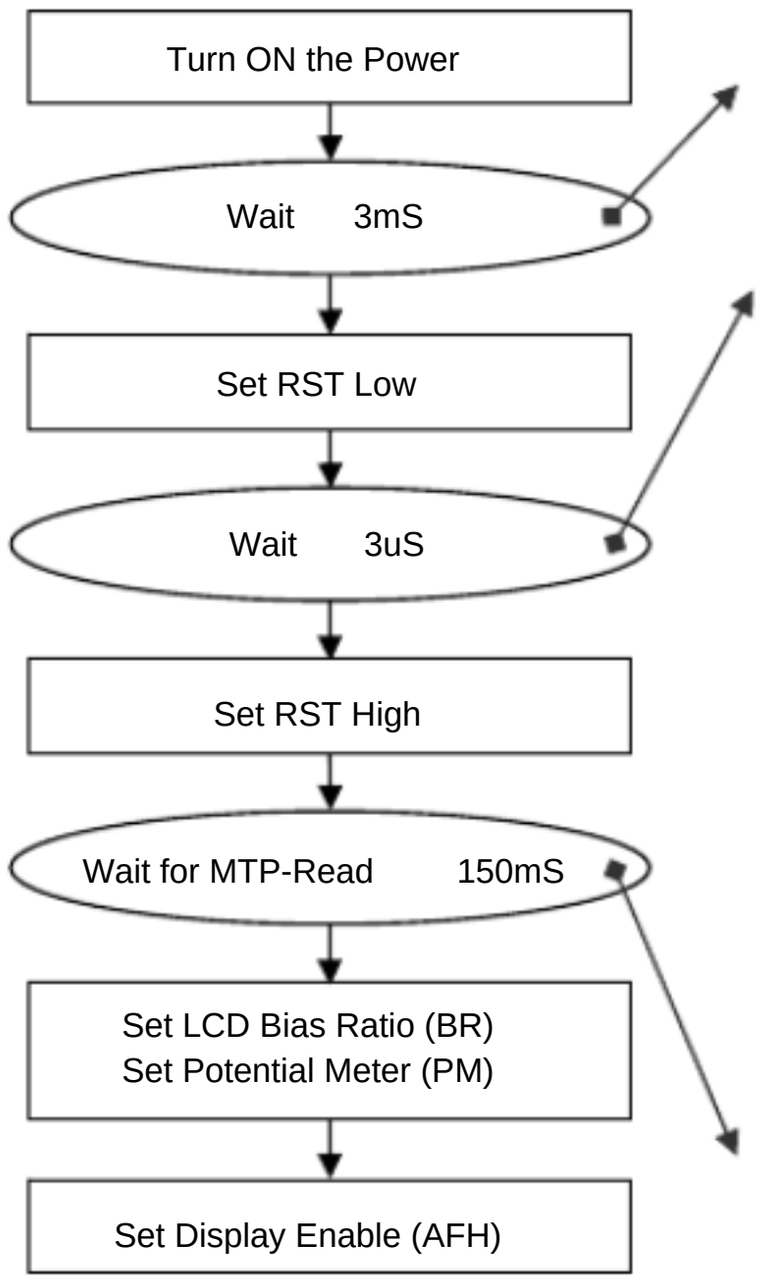
The difference between Sleep mode and Reset mode is that Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1604c consumes very little energy in Sleep mode (typically under 5 µA).

EXITING SLEEP MODE

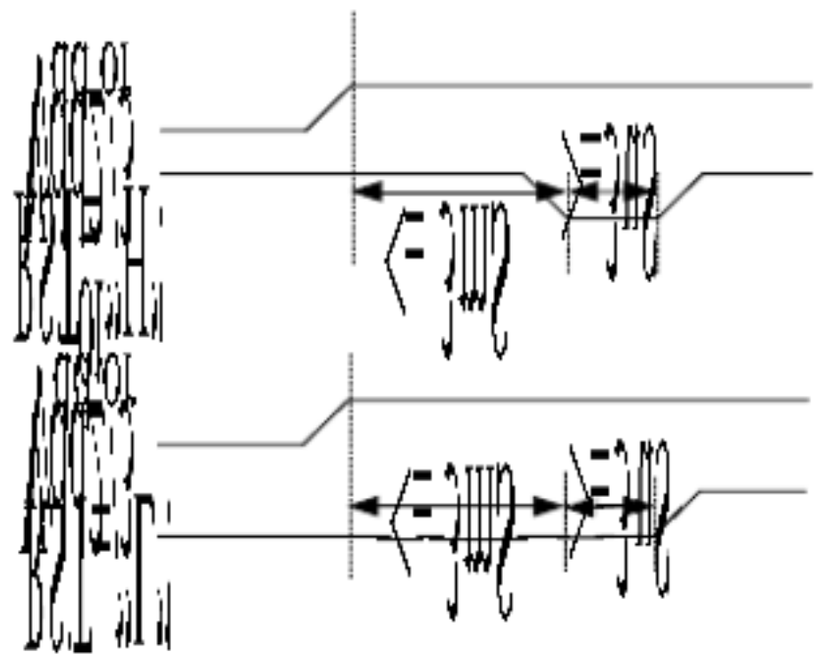
UC1604c contains internal logic to check whether V_{LCD} and V_D are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1604c internal voltage sources are restored to their proper values.

POWER -UP SEQUENCE



Wait 3 mS : After each power-up, a Pin Reset, which is set in 3mS, is required.

Wait 3 uS :



If V_{DD} and $V_{DD2/3}$ are turned ON separately, each one needs to be followed by a RST in 3mS.

Wait 150mS : The system program is required to wait for only 150mS before starting to issue commands to UC1604c. No additional waits are required thereafter.

FIGURE 11: Reference Power-Up Sequence

There ’s no delay needed while turning ON V_{DD} and $V_{DD2/3}$, and either one can be turned ON first.

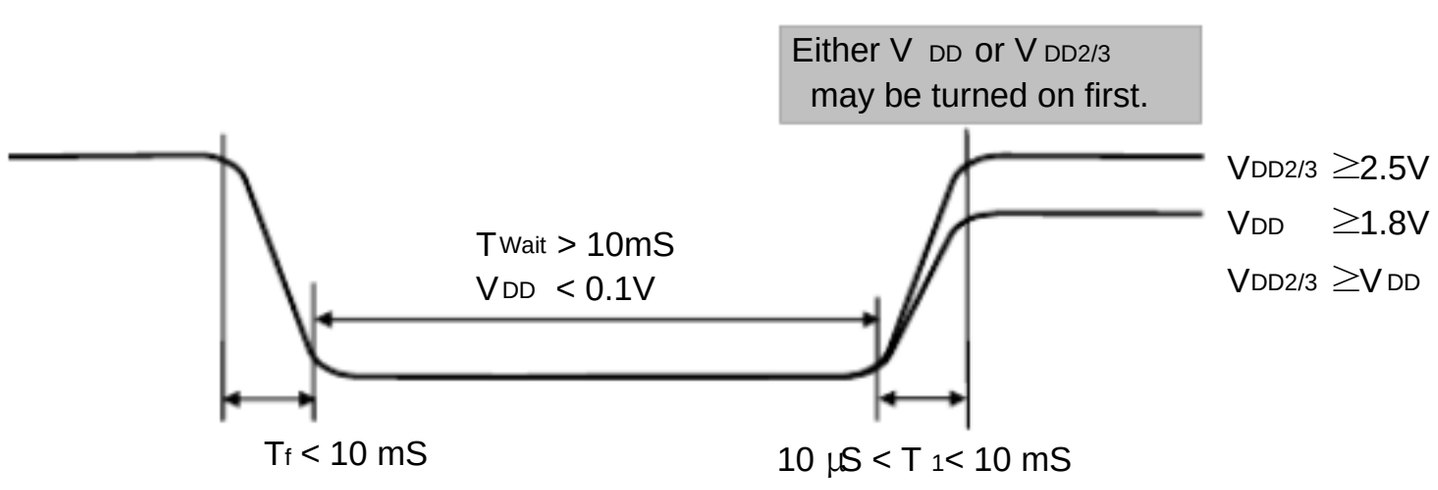


Figure 12: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1604c enters Sleep mode from Display mode by issuing Set Display OFF command. To exit Sleep mode, Set Display ON.

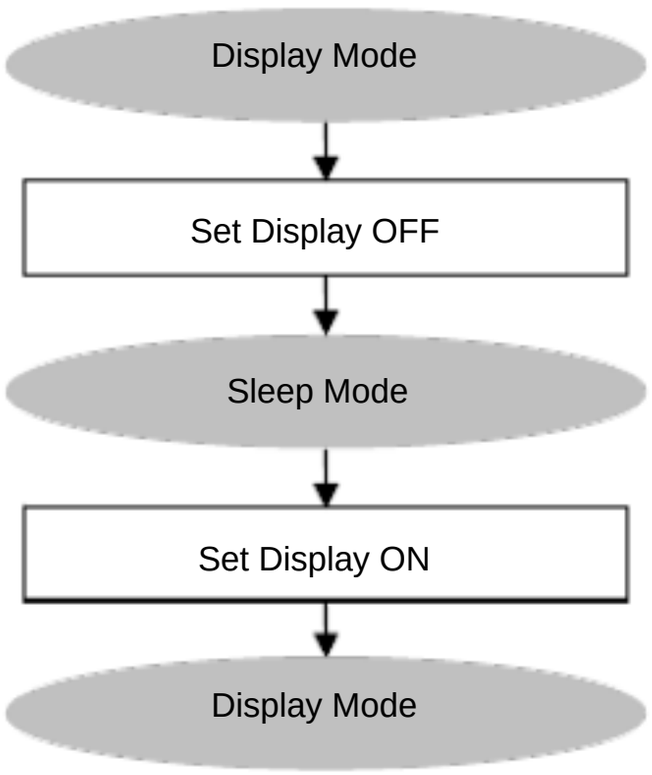


Figure 13 : Enter/Exit Sleep Mode Sequence

Power-Down Sequence

To prevent the charge stored in capacitor C_L causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

When internal V_{LCD} is not used, UC1604c will NOT drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

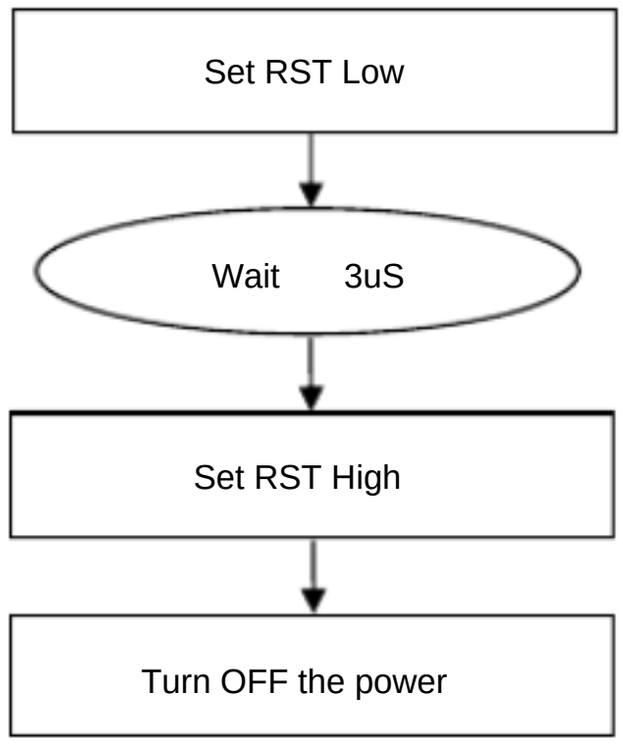


FIGURE 14: Reference Power-Down Sequence

MULTI-TIME PROGRAM NV MEMORY

OVERVIEW

MTP feature is available for UC1604c such that LCM makers can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1604c:

MTP-Erase, MTP-Program, MTP-Read.

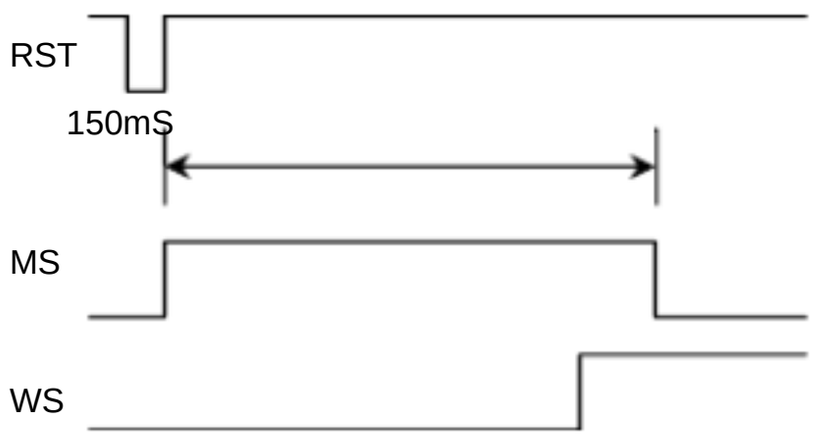
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1604c, no external power source is required, and it is performed automatically after hardware RESET (power-ON and pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1604c, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the Read Status commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}? {1,0}? {1,1} ? {0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use Read Status command in a polling loop to make sure {MS, WS}={0, 1} before proceeding with the normal operations, however, it may be simpler to just issue Set Display Enable command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above "Periodical re-initializing" approach is also an effective safeguard against accidental display off events such as

- ? ESD strikes
- ? Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software RESET command. This enables the Ics to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software RESET for normal operation control purpose and hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

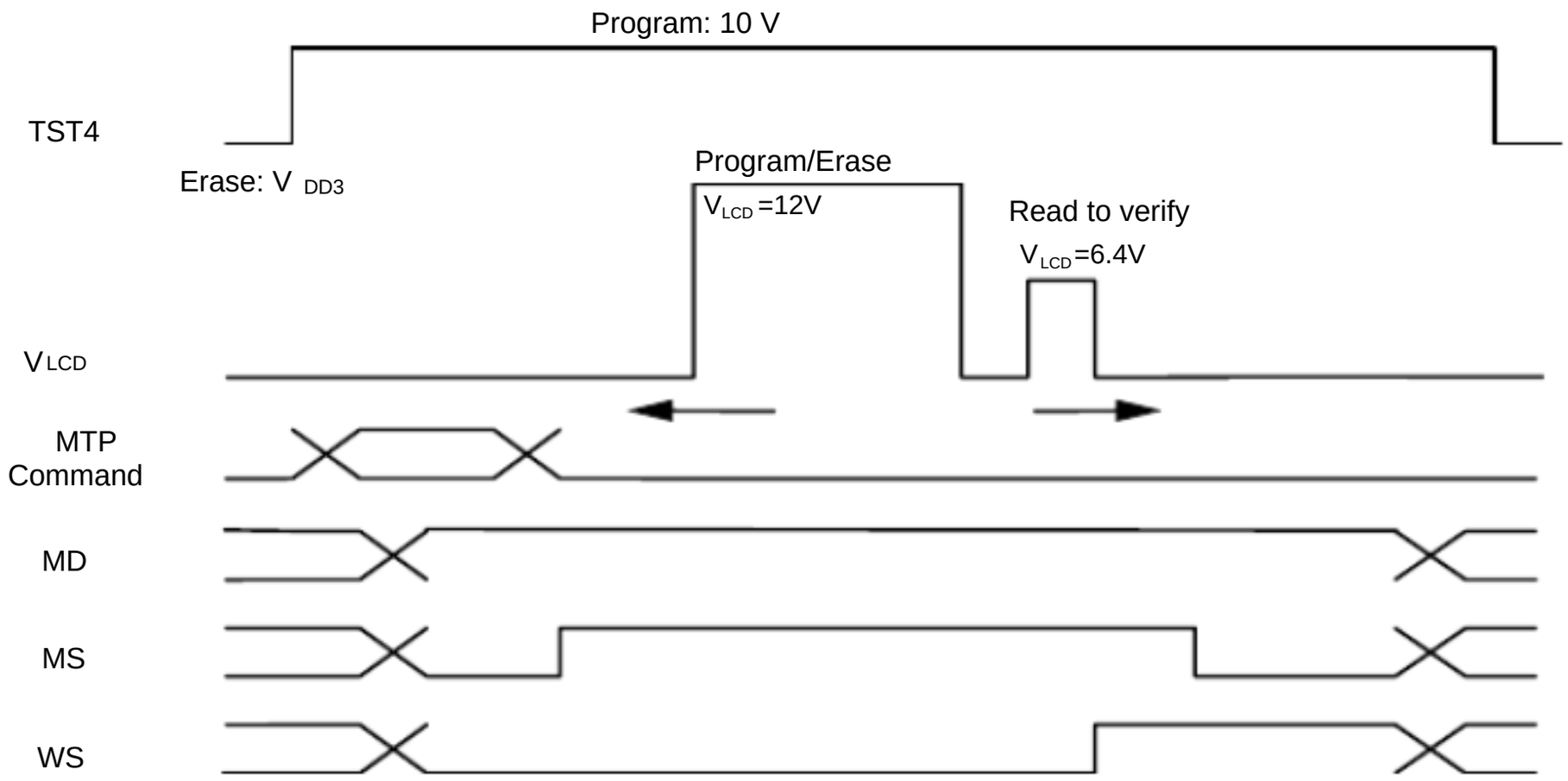
No external power source is required for MTP Erase and Read operation. For these MTP operations, TST4 should be open, or connected to V_{DD3}.

	V_{LCD}	TST4 (external input)
Program	MTP3 : FFh (12V)	10V (1mA per bit)
Erase	MTP3 : FFh (12V)	Floating or V_{DD3}
Read	MTP2 : 64h (6.4V)	Floating or V_{DD3}

Note: Do Erase before Program and program one bit at a time.

2. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

3. MTP Cell Value Usage

There are 6 MTP cell bits. They are divided into two groups for different purpose.

MTP[5:0] : V_{LCD} Trim
When PMO[5]=1: PM with trim = PM – PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R											Set RST pin Low	Wait 3uS after RST is Low
R											Set RST pin High	Wait 150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3] 11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R	0	0	0	1	1	0	0	1	0	0		MTP2: 64h(6.4V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R	0	0	1	1	1	1	1	1	1	1		MTP3: FFh(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	0	0	0	0	1	0		MTP4: 02h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	0	1	0		MTP5: 02h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	0	0	0	0	0	0	0	1	MTPM	Ex: To program MTPM[0] to be 1, set the value to 00000001b *
R												Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3] 1
R	0	0	-			-	0	0	1	1		Set MTPC[2:0] 011
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R												Remove TST4 voltage
R								=			V_{DD} 0V Power	OFF

* It is recommended that users program one bit at a time.

MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Set RST pin Low	Wait 3uS after RST is Low
R											Set RST pin High	Wait 150mS
R 0		0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3] 11b
R 0		0	1	1	1	0	1		0	0	Set V_{MTP1} Potentiometer	Set MTP V_{LCD}
R 0		0	0	1	1	0	0	1	0	0		MTP2: 64h(6.4V)
R 0		0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP V_{LCD}
R 0		0	1	1	1	1	1	1	1	1		MTP3: FFh(12V)
R 0		0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R 0		0	0	0	0	0	0	0	1	0		MTP4: 02h(100mS)
R 0		0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R 0		0	0	0	0	0	0	0	1	0		MTP5: 02h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C 0		0	0	0	0	1	1		1	1	MTPM1	Ex: To erase MTPM[3:0], set the value to 00001111b
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R 0		0	-		-	0	0	1	0			Set MTPC[2:0] 010
R	0	1	-	-	-	-	-		WS	-	MS	Get Status & PM	Check MTP Status until MS=0 WS=1
R									=			V_{DD} 0V Power	OFF

Note: It is recommended that users clear first all the bits to be programmed.

SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R											Wait <= 3 mS	
R											Set RST pin Low	Wait 3 uS after RST is Low
R											Set RST pin High	Wait 150mS after RST is High
C 0		0	0	1	0	0	1	#		#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
R 0		0	1	1	0	0	0	#		#	Set LCD Mapping Control	
A 0		0	1	0	1	0	0	0		#	Set Frame Rate	Fine tune for power, flicker, contrast.
R 0		0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
R	0 0	0 0	1 0	0 0	1 0	1 1	1 1	0 0	0 0	0 1	Set MTP function	Set MTP use & MTP read
R											Wait <= 50 mS	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R 0		0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Set RST pin Low	Wait 3 uS after RST is Low
R											Set RST pin High	
R											Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R 0		0	1	0	1	0	1	1	1	0	Set Display Disable	
C 1	1	0	#	#	#	#	#	#	#	#	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R 0		0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is, therefore, highly recommended that LCM makers strictly follow the “JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices” when manufacturing LCM.

The following pins in UC1604c require special “ESD Sensitivity” consideration in particular:

Pins \ Test Mode		Machine Mode		Human Body Mode	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		150V	150V	1.5KV	1.5KV
LCM Digital Interface		300V 300V		3.0KV	3.0KV
LCM HV Interface	TST1/2/4	300V 250V		3.0KV	3.0KV
	C_B pins	300V 300V		3.0KV	3.0KV
	V_{LCDIN}	200V 200V		3.0KV	3.0KV
	V_{LCDOUT}	300V 300V		3.0KV	3.0KV
PWR/GND -			300V	-	3.0KV

According to UltraChip’s Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 – notes 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$ --		1.2	V
V_{LCD}	LCD Generated voltage	-0.3	+13.2	V
V_{IN} / V_{OUT} Any	input/output	-0.4 V	$_{DD}$ + 0.3	V
T_{OPR} Operating	temperature range	-30	+85	^{o}C
T_{STR} Storage	temperature	-55 +125		^{o}C

Notes

1. V_{DD} is based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65	1.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.6	2.7~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ 2.4V, 25 °C	4.8~11.5		11.5	V
V_D	LCD data voltage	$V_{DD2/3}$ 2.4V, 25 °C	0.80 1.32			V
V_{IL}	Input logic LOW				0.1V_{DD} V	
V_{IH}	Input logic HIGH		0.9V_{DD}			V
V_{OL}	Output logic LOW				0.2V_{DD} V	
V_{OH}	Output logic HIGH		0.8V_{DD}			V
I_{IL}	Input leakage current				1.5	µA
I_{SB} Standby current		V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85 °C			50	µA
C_{IN} Input capacitance				5	10	PF
C_{OUT} Output capacitance				5	10	PF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11.5V		2000	3000	?
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11.5V		2000	3000	?
F_{FR}	Average Frame Rate	LC[4:3] = 01b	-10%	95	+10%	Hz

POWER CONSUMPTION

V_{DD} = 2.7V,
V_{LCD} = 8.54V
Mux Rate = 65,
Temperature = 25 °C, C

Bias Ratio = 11b,
Frame Rate = 01b,
Bus mode =6800,
$_L$ = 330nF,

PM = 73,
PMO = 00H,
C_B = 2.2 µF,
All outputs are open circuit.

Display Pattern	Conditions	Typ.	Max.
All-ON	Bus = idle	175	(TBD)
All-OFF	Bus = idle	175	(TBD)
2-pixel checker	Bus = idle	196	(TBD)
-	Bus = idle (standby current)	-	5

AC CHARACTERISTICS

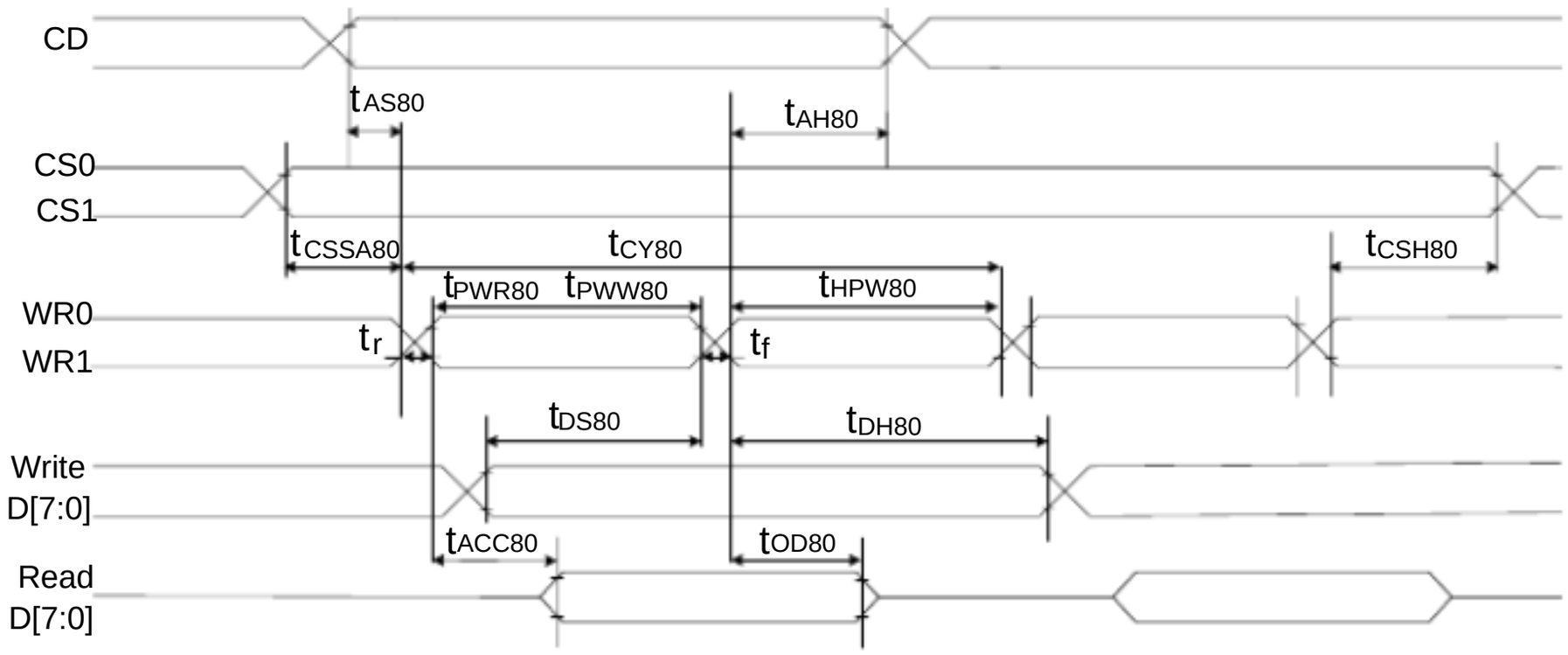


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= −30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	–	nS
t_{CSSA80} t_{CSH80}	CS1, CS0	Chip select setup time Chip select hold time		5 5	– nS	
t_{CY80} t_{PWR80} / t_{PWW80} t_{HPW80}	WR0, WR1	System Cycle time Pulse width High pulse width		120 / 80 60 / 40 60 / 40	–	nS
t_{DS80} t_{DH80}	D7~D0 (Write)	Data setup time Data hold time		30 0	– nS	
t_{ACC80} t_{OD80}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= −30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	–	nS
t_{CSSA80} t_{CSH80}	CS1, CS0	Chip select setup time Chip select hold time		5 5	– nS	
t_{CY80} t_{PWR80} / t_{PWW80} t_{HPW80}	WR0, WR1	System cycle time Pulse width High pulse width		240 / 160 120 / 80 120 / 80	–	nS
t_{DS80} t_{DH80}	D7~D0 (Write)	Data setup time Data hold time		60 0	– nS	
t_{ACC80} t_{OD80}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 15	60 30	nS

Note: tr (rising time), tf (falling time) : 15nS

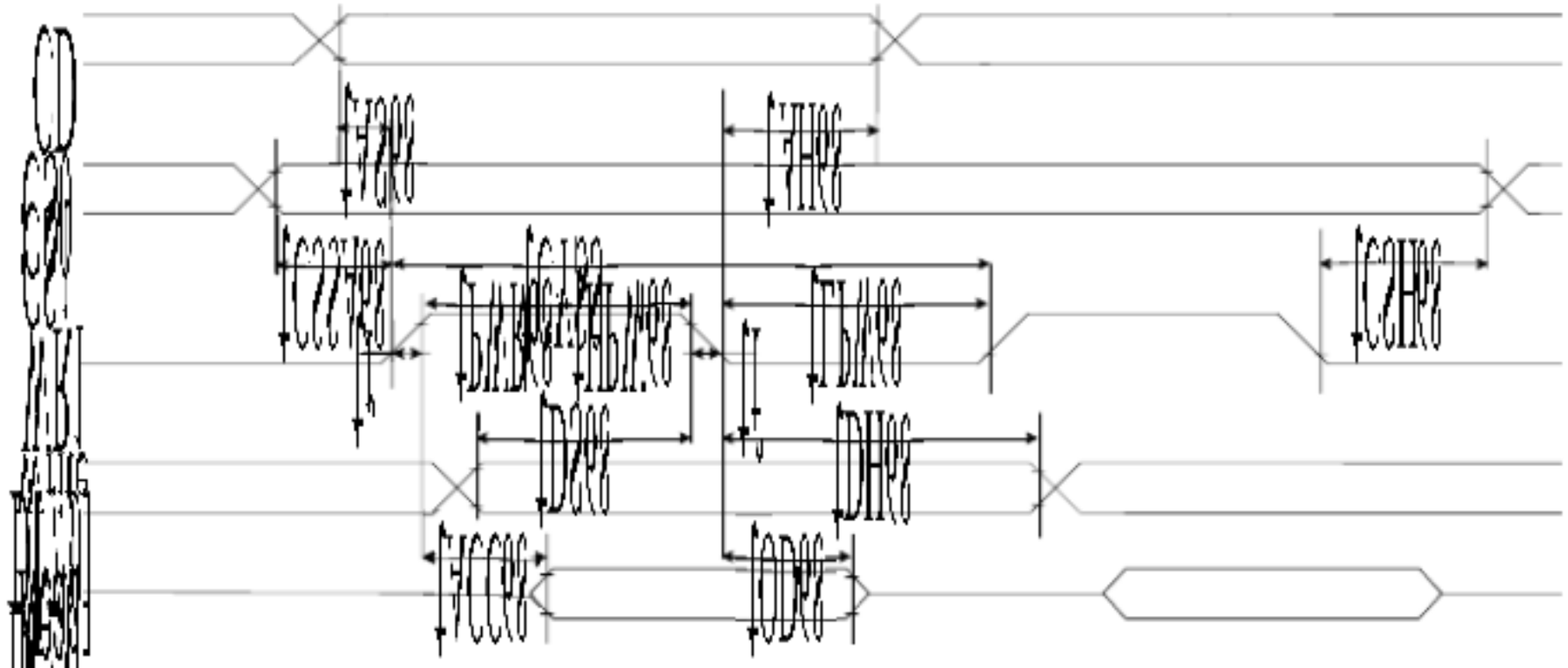


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= – 30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	–	nS
t_{CSSA68} t_{CSH68}	CS1, CS0	Chip select setup time Chip select hold time		5 5	– nS	
t_{CY68} t_{PWR68} / t_{PWW68} t_{HPW68}	WR1	System cycle time Pulse width High pulse width		120 / 80 60 / 40 60 / 40	–	nS
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		30 0	– nS	
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= – 30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	–	nS
t_{CSSA68} t_{CSH68}	CS1, CS0	Chip select setup time Chip select hold time		5 5	– nS	
t_{CY68} t_{PWR68} / t_{PWW68} t_{HPW68}	WR1	System cycle time Pulse width High pulse width		240 / 160 120 / 80 120 / 80	–	nS
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		60 0	– nS	
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– 15	60 30	nS

Note: tr (Rising time), tf (falling time) : 15nS

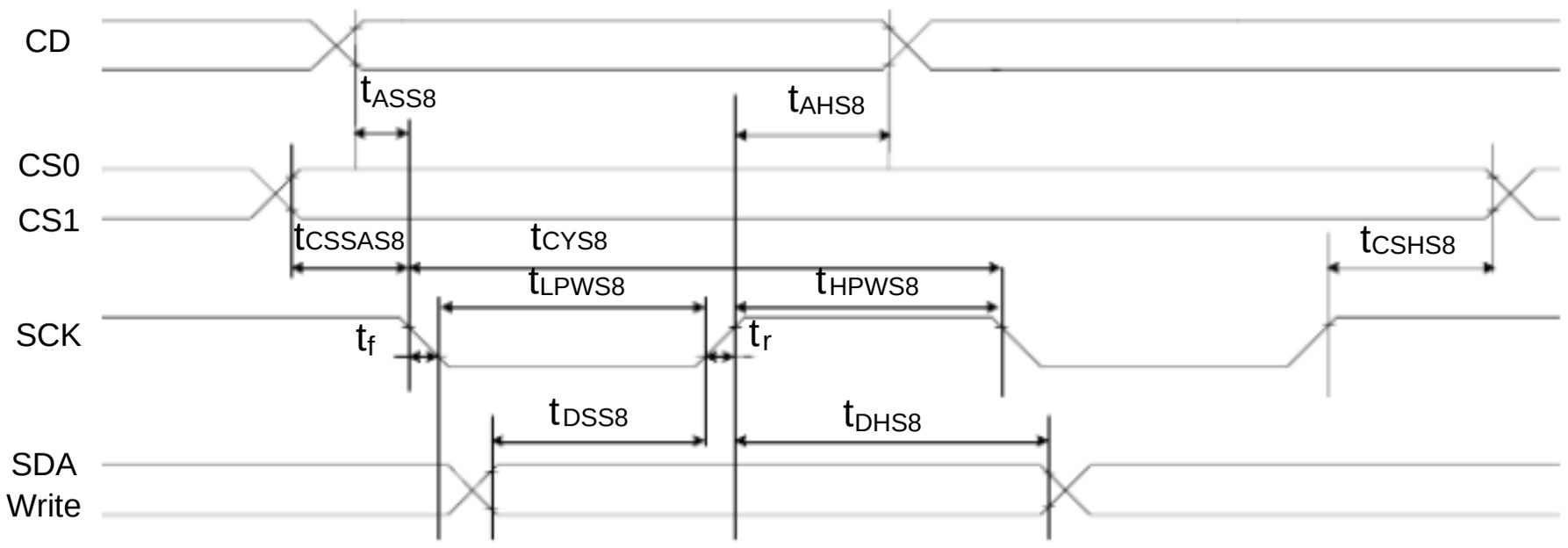


FIGURE 17: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= −30 to +85°C)				(Read / Write)		
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		10		
t_{CSSAS8}	CS1, CS0	Chip select setup time		5	– nS	
t_{CSHS8}		Chip select hold time		5		
t_{CYS8}	SCK	System Cycle time		100 / 30	–	nS
t_{LPWS8}		Low pulse width		50 / 15		
t_{HPWS8}		High pulse width		50 / 15		
t_{DSS8}	SDA (Write)	Data setup time		12	– nS	
t_{DHS8}		Data hold time		0		
(1.65V ≤ V_{DD} < 2.5V, Ta= −30 to +85°C)				(Read / Write)		
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		10		
t_{CSSAS8}	CS1, CS0	Chip select setup time		10	– nS	
t_{CSHS8}		Chip select hold time		10		
t_{CYS8}	SCK	System Cycle time		130 / 60	–	nS
t_{LPWS8}		Low pulse width		65 / 30	–	nS
t_{HPWS8}		High pulse width		65 / 30	–	nS
t_{DSS8}	SDA (Write)	Data setup time		24	– nS	
t_{DHS8}		Data hold time		0		

Note: tr (Rising time), tf (falling time) : 15nS

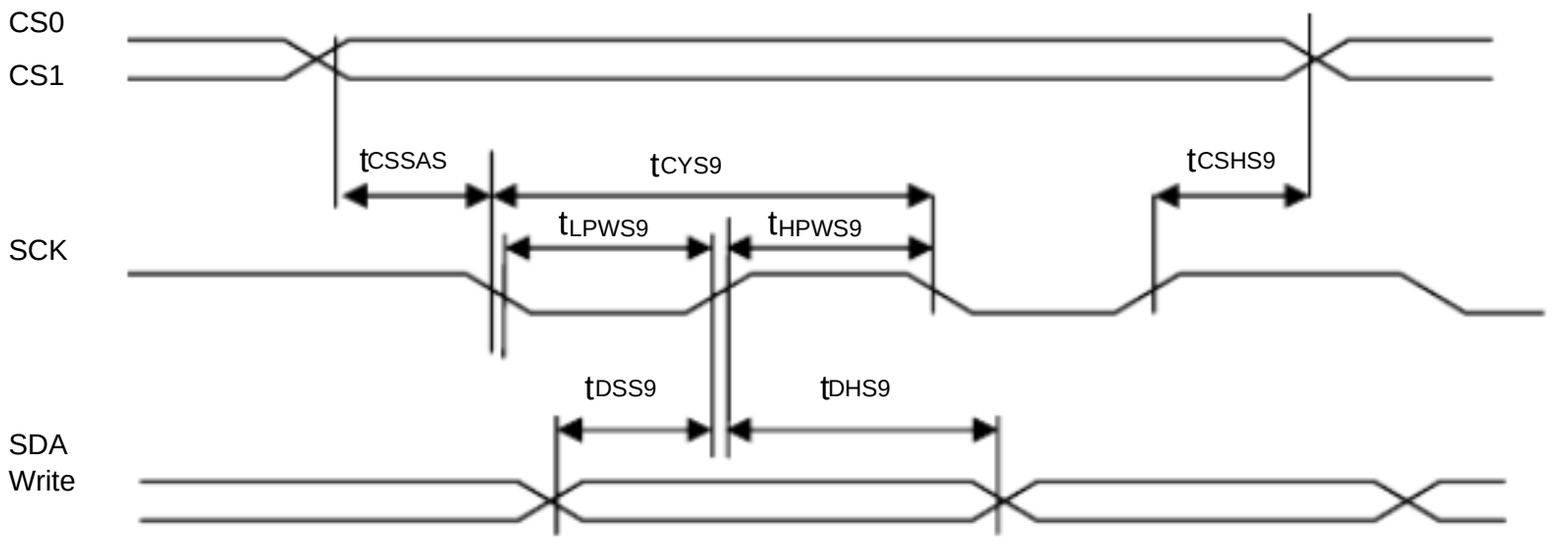


FIGURE 18: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= – 30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1, CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		100 / 30 50 / 15 50 / 15	– nS	
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		12 0	–	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= – 30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1, CS0	Chip select setup time		10 10	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		130 / 60 50 / 30 50 / 30	– nS	
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		24 0	–	nS

Note: tr (Rising time), tf (falling time) : 15nS

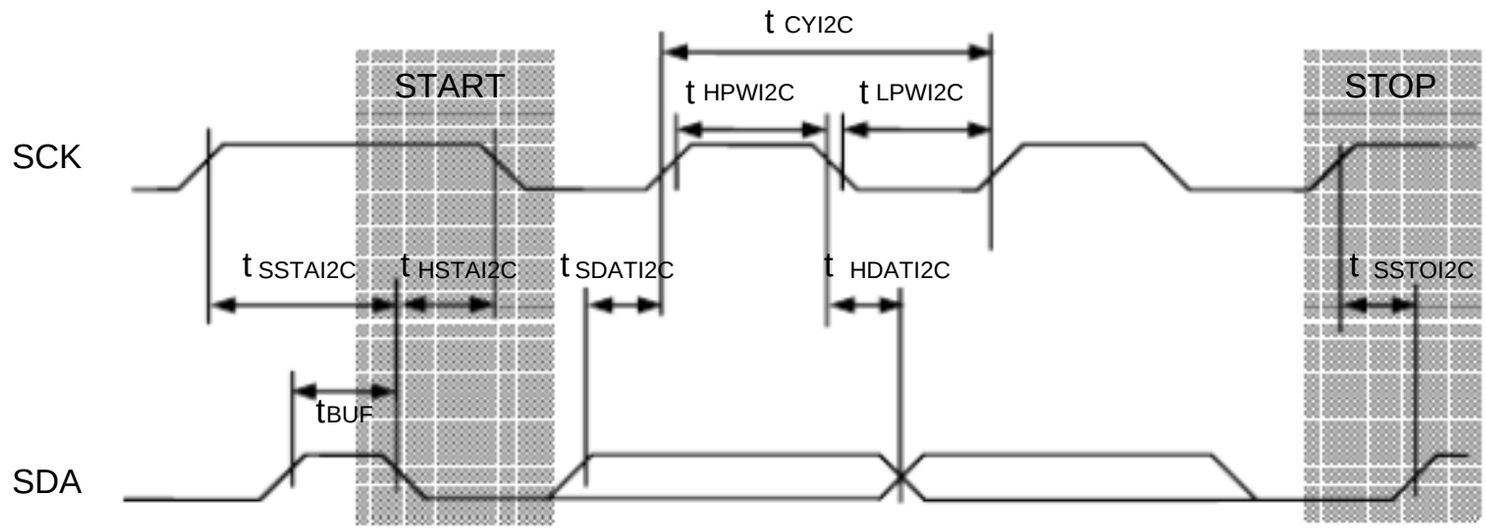


FIGURE 19: Serial bus timing characteristics (for I2C)

(2.5V ≤ VDD < 3.3V, Ta= – 30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ VDD < 3.3V, Ta= – 30 to +85°C)				(Read / Write)		
tCYI2C	SCK	SCK cycle time		580 / 275	–	nS
tHPWI2C		High pulse width		290 / 110		
tLPWI2C		Low pulse width		290 / 165		
tSSTAI2C	SCK SDA	Setup time – START		28	– nS	
tHSTAI2C		Hold time – START		55		
tSDAI2C		Setup time – Data		28		
tHDAI2C		Hold time – Data		11		
tSSTOI2C		Setup time – STOP		28		
tBUF	SDA	Bus Free time between STOP and START		165	–	nS
(1.65V ≤ VDD < 2.5V, Ta= – 30 to +85°C)				(Read / Write)		
tCYI2C	SCK	SCK cycle time		750 / 330	–	nS
tHPWI2C		High pulse width		375 / 130		
tLPWI2C		Low pulse width		375 / 200		
tSSTAI2C	SCK SDA	Setup time – START		28	– nS	
tHSTAI2C		Hold time – START		65		
tSDAI2C		Setup time – Data		55		
tHDAI2C		Hold time – Data		11		
tSSTOI2C		Setup time – STOP		28		
tBUF	SDA	Bus Free Time between STOP and START		220	–	nS

Note: tr (Rising time), tf (falling time) : 15nS

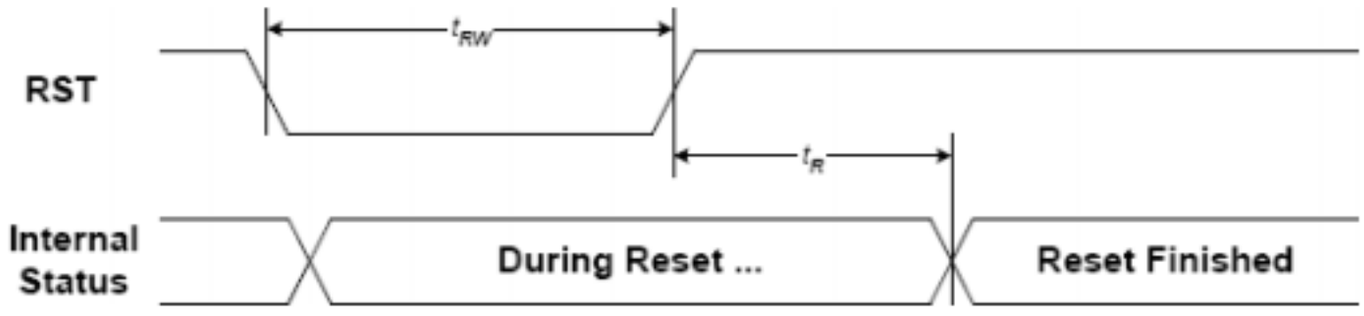


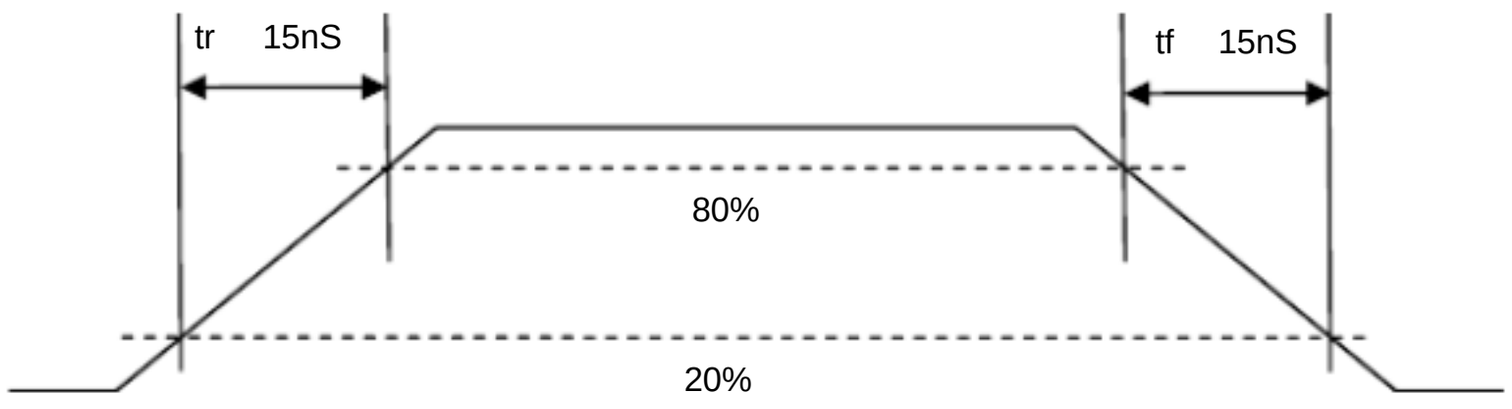
FIGURE 20: Reset Characteristics

(1.65V V_{DD} < 3.3V, Ta= – 30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
t_{RW}	RST	Reset low pulse width		3	–	μS
t_R	RST, Internal Status	Reset to Internal Status pulse delay		6	–	mS

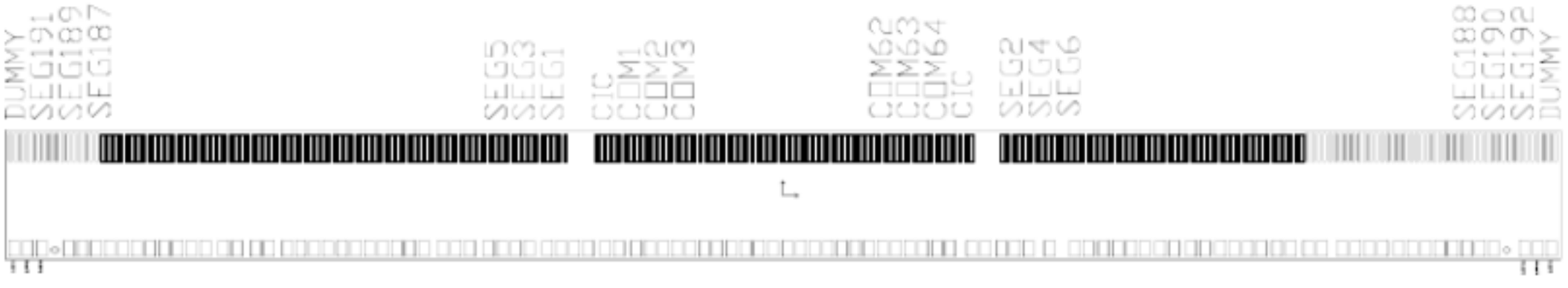
Note:

For each mode, the signal ’s rising and falling times (tr, tf) are stipulated to be equal to or less than 15nS each.



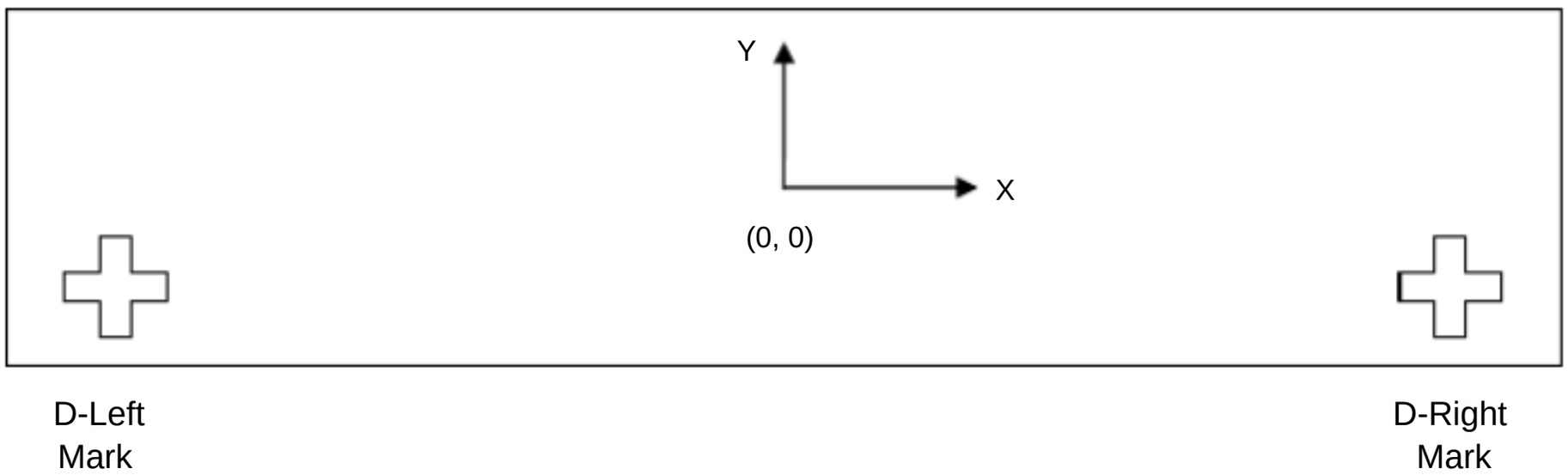
PHYSICAL DIMENSIONS

Circuit / Bump View:

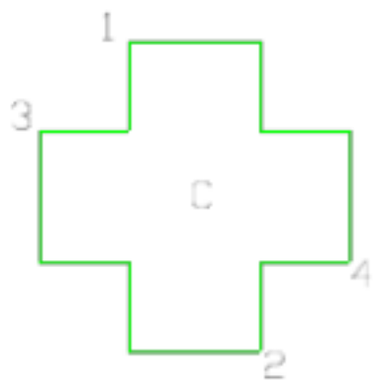


Die Size:	7480 μM x 652 μM ± 40 μM	Bump Size:	15.6 μM x 130 μM
Die Thickness:	400 μM ± 20 μM	Bump Pitch:	27.6 μM
Die TTV:	$(D_{MAX} - D_{MIN})$ within die 2 μM	Bump Area:	2028 μM^2
Hardness:	90 Hv ± 25 Hv	Coordinate origin:	Chip center
Bump Height:	15 μM ± 3 μM	Pad reference:	Pad center
	$(H_{MAX} - H_{MIN})$ within die 2 μM		

ALIGNMENT MARK INFORMATION



Shape of the alignment mark:

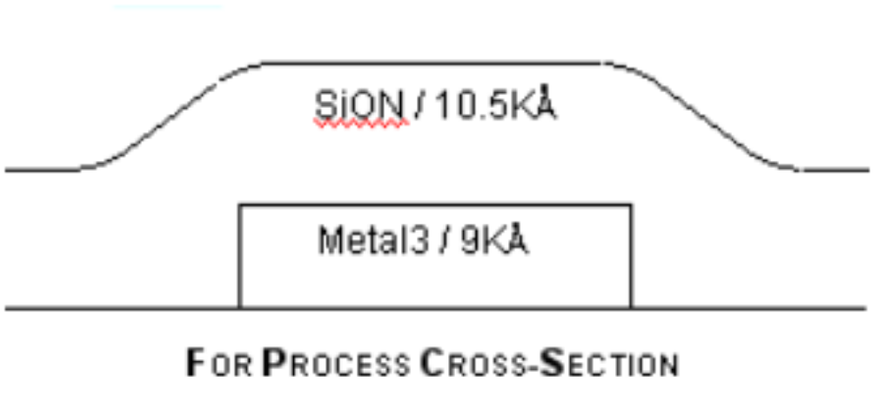


Remark:
The cross mark itself is symmetric both horizontally and vertically.

Coordinates:

Point	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1 -3489.5		-245.5 3454.5	-245.5	
2 -3474.5		-280.5 3469.5	-280.5	
3 -3499.5		-255.5 3444.5	-255.5	
4 -3464.5		-270.5 3479.5	-270.5	
C -3482		-263	3462	-263

Top Metal and Passivation:



FOR PROCESS CROSS-SECTION

Remark:
Alignment marks are on Metal3 under Passivation

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY	-3676	-255	50	73
2	DUMMY	-3611	-255	50	73
3	DUMMY	-3546	-255	50	73
4	DUMMY	-3414.75	-255	50	73
5	DUMMY	-3349.75	-255	50	73
6	CS0	-3284.75	-255	50	73
7	CS1	-3219.75	-255	50	73
8	VDDX	-3154.75	-255	50	73
9	RSTB	-3089.75	-255	50	73
10	CD	-3024.75	-255	50	73
11	WR0	-2959.75	-255	50	73
12	VDDX	-2894.75	-255	50	73
13	WR1	-2829.75	-255	50	73
14	D0	-2761.35	-255	50	73
15	D1	-2674.65	-255	50	73
16	D2	-2609.65	-255	50	73
17	D3	-2522.95	-255	50	73
18	D4	-2457.95	-255	50	73
19	D5	-2371.25	-255	50	73
20	D6	-2306.25	-255	50	73
21	VDDX	-2241.25	-255	50	73
22	D7	-2176.25	-255	50	73
23	BM0	-2107.85	-255	50	73
24	VDDX	-2042.85	-255	50	73
25	BM1	-1977.85	-255	50	73
26	ID	-1912.85	-255	50	73
27	VDDX	-1847.85	-255	50	73
28	POR	-1782.85	-255	50	73
29	vdd	-1717	-255	50	73
30	DUMMY -1627.5		-255	50	73
31	DUMMY -1562.5		-255	50	73
32	DUMMY -1497.5		-255	50	73
33	vdd	-1408	-255	50	73
34	vdd	-1343	-255	50	73
35	vdd	-1278	-255	50	73
36	vdd	-1213	-255	50	73
37	vdd2 -1126.3		-255	50	73
38	vdd2 -1061.3		-255	50	73
39	vdd2	-996.3	-255	50	73
40	vdd2	-931.3	-255	50	73
41	DUMMY	-849.3	-255	50	73
42	DUMMY	-784.3	-255	50	73
43	vdd2	-702.3	-255	50	73
44	vdd2	-637.3	-255	50	73
45	vdd2	-572.3	-255	50	73
46	vdd3	-507.3	-255	50	73
47	vdd3	-442.3	-255	50	73
48	vdd3	-377.3	-255	50	73
49	vdd3	-312.3	-255	50	73
50	vdd3	-247.3	-255	50	73
51	DUMMY -178.15		-255	50	73
52	DUMMY -113.15		-255	50	73
53	DUMMY	-48.15	-255	50	73

#	Pad	X	Y	W	H
54	vss 21		-255	50	73
55	vss 86		-255	50	73
56	vss 151		-255	50	73
57	vss 216		-255	50	73
58	vss 281		-255	50	73
59	vss 346		-255	50	73
60	vss2 411		-255	50	73
61	vss2 476		-255	50	73
62	vss2 541		-255	50	73
63	vss2 606		-255	50	73
64	vss2 671		-255	50	73
65	vss2 736		-255	50	73
66	DUMMY 801		-255	50	73
67	TST4 903		-255	50	73
68	TST4 968		-255	50	73
69	TST4 1044		-255	50	73
70	TST4 1109		-255	50	73
71	TST2 1174		-255	50	73
72	TST2 1275.45		-255	50	73
73	VB0- 1395.35		-255	50	73
74	VB0- 1460.35		-255	50	73
75	VB0- 1535.5		-255	50	73
76	VB0- 1600.5		-255	50	73
77	VB0+ 1665.5		-255	50	73
78	VB0+ 1730.5		-255	50	73
79	VB0+ 1805.65		-255	50	73
80	VB0+ 1870.65		-255	50	73
81	VB1- 1952.65		-255	50	73
82	VB1- 2017.65		-255	50	73
83	VB1- 2092.8		-255	50	73
84	VB1- 2157.8		-255	50	73
85	VB1+ 2222.8		-255	50	73
86	VB1+ 2287.8		-255	50	73
87	VB1+ 2362.95		-255	50	73
88	VB1+ 2427.95		-255	50	73
89	VLCDIN 2511.95		-255	50	73
90	VLCDIN 2576.95		-255	50	73
91	VLCDIN 2673.95		-255	50	73
92	VLCDIN 2738.95		-255	50	73
93	VLCDOUT 2803.95		-255	50	73
94	VLCDOUT 2868.95		-255	50	73
95	VLCDOUT 2944.95		-255	50	73
96	VLCDOUT 3009.95		-255	50	73
97	DUMMY 3074.95		-255	50	73
98	DUMMY 3139.95		-255	50	73
99	DUMMY 3204.95		-255	50	73
100	DUMMY 3269.95		-255	50	73
101	DUMMY 3334.95		-255	50	73
102	DUMMY 3399.95		-255	50	73
103	DUMMY 3546		-255	50	73
104	DUMMY 3611		-255	50	73
105	DUMMY 3676		-255	50	73
106	DUMMY 3694.2	225.5	15.6	130	

#	Pad	X	Y	W	H
107	SEG192	3666.6	225.5	15.6	130
108	SEG190	3639	225.5	15.6	130
109	SEG188	3611.4	225.5	15.6	130
110	SEG186	3583.8	225.5	15.6	130
111	SEG184	3556.2	225.5	15.6	130
112	SEG182	3528.6	225.5	15.6	130
113	SEG180	3501	225.5	15.6	130
114	SEG178	3473.4	225.5	15.6	130
115	SEG176	3445.8	225.5	15.6	130
116	SEG174	3418.2	225.5	15.6	130
117	SEG172	3390.6	225.5	15.6	130
118	SEG170	3363	225.5	15.6	130
119	SEG168	3335.4	225.5	15.6	130
120	SEG166	3307.8	225.5	15.6	130
121	SEG164	3280.2	225.5	15.6	130
122	SEG162	3252.6	225.5	15.6	130
123	SEG160	3225	225.5	15.6	130
124	SEG158	3197.4	225.5	15.6	130
125	SEG156	3169.8	225.5	15.6	130
126	SEG154	3142.2	225.5	15.6	130
127	SEG152	3114.6	225.5	15.6	130
128	SEG150	3087	225.5	15.6	130
129	SEG148	3059.4	225.5	15.6	130
130	SEG146	3031.8	225.5	15.6	130
131	SEG144	3004.2	225.5	15.6	130
132	SEG142	2976.6	225.5	15.6	130
133	SEG140	2949	225.5	15.6	130
134	SEG138	2921.4	225.5	15.6	130
135	SEG136	2893.8	225.5	15.6	130
136	SEG134	2866.2	225.5	15.6	130
137	SEG132	2838.6	225.5	15.6	130
138	SEG130	2811	225.5	15.6	130
139	SEG128	2783.4	225.5	15.6	130
140	SEG126	2755.8	225.5	15.6	130
141	SEG124	2728.2	225.5	15.6	130
142	SEG122	2700.6	225.5	15.6	130
143	SEG120	2673	225.5	15.6	130
144	SEG118	2645.4	225.5	15.6	130
145	SEG116	2617.8	225.5	15.6	130
146	SEG114	2590.2	225.5	15.6	130
147	SEG112	2562.6	225.5	15.6	130
148	SEG110	2535	225.5	15.6	130
149	SEG108	2507.4	225.5	15.6	130
150	SEG106	2479.8	225.5	15.6	130
151	SEG104	2452.2	225.5	15.6	130
152	SEG102	2424.6	225.5	15.6	130
153	SEG100	2397	225.5	15.6	130
154	SEG98	2369.4	225.5	15.6	130
155	SEG96	2341.8	225.5	15.6	130
156	SEG94	2314.2	225.5	15.6	130
157	SEG92	2286.6	225.5	15.6	130
158	SEG90	2259	225.5	15.6	130
159	SEG88	2231.4	225.5	15.6	130
160	SEG86	2203.8	225.5	15.6	130

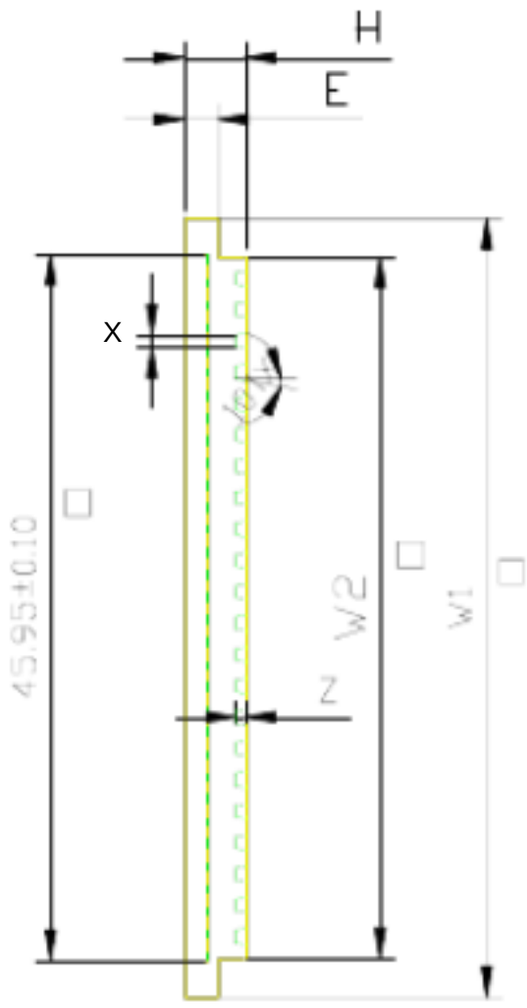
#	Pad	X	Y	W	H
161	SEG84	2176.2	225.5	15.6	130
162	SEG82	2148.6	225.5	15.6	130
163	SEG80	2121	225.5	15.6	130
164	SEG78	2093.4	225.5	15.6	130
165	SEG76	2065.8	225.5	15.6	130
166	SEG74	2038.2	225.5	15.6	130
167	SEG72	2010.6	225.5	15.6	130
168	SEG70	1983	225.5	15.6	130
169	SEG68	1955.4	225.5	15.6	130
170	SEG66	1927.8	225.5	15.6	130
171	SEG64	1900.2	225.5	15.6	130
172	SEG62	1872.6	225.5	15.6	130
173	SEG60	1845	225.5	15.6	130
174	SEG58	1817.4	225.5	15.6	130
175	SEG56	1789.8	225.5	15.6	130
176	SEG54	1762.2	225.5	15.6	130
177	SEG52	1734.6	225.5	15.6	130
178	SEG50	1707	225.5	15.6	130
179	SEG48	1679.4	225.5	15.6	130
180	SEG46	1651.8	225.5	15.6	130
181	SEG44	1624.2	225.5	15.6	130
182	SEG42	1596.6	225.5	15.6	130
183	SEG40	1569	225.5	15.6	130
184	SEG38	1541.4	225.5	15.6	130
185	SEG36	1513.8	225.5	15.6	130
186	SEG34	1486.2	225.5	15.6	130
187	SEG32	1458.6	225.5	15.6	130
188	SEG30	1431	225.5	15.6	130
189	SEG28	1403.4	225.5	15.6	130
190	SEG26	1375.8	225.5	15.6	130
191	SEG24	1348.2	225.5	15.6	130
192	SEG22	1320.6	225.5	15.6	130
193	SEG20	1293	225.5	15.6	130
194	SEG18	1265.4	225.5	15.6	130
195	SEG16	1237.8	225.5	15.6	130
196	SEG14	1210.2	225.5	15.6	130
197	SEG12	1182.6	225.5	15.6	130
198	SEG10	1155	225.5	15.6	130
199	SEG8	1127.4	225.5	15.6	130
200	SEG6	1099.8	225.5	15.6	130
201	SEG4	1072.2	225.5	15.6	130
202	SEG2	1044.6	225.5	15.6	130
203	COMS	898.5	225.5	15.6	130
204	COM64	870.9	225.5	15.6	130
205	COM63	843.3	225.5	15.6	130
206	COM62	815.7	225.5	15.6	130
207	COM61	788.1	225.5	15.6	130
208	COM60	760.5	225.5	15.6	130
209	COM59	732.9	225.5	15.6	130
210	COM58	705.3	225.5	15.6	130
211	COM57	677.7	225.5	15.6	130
212	COM56	650.1	225.5	15.6	130
213	COM55	622.5	225.5	15.6	130
214	COM54	594.9	225.5	15.6	130

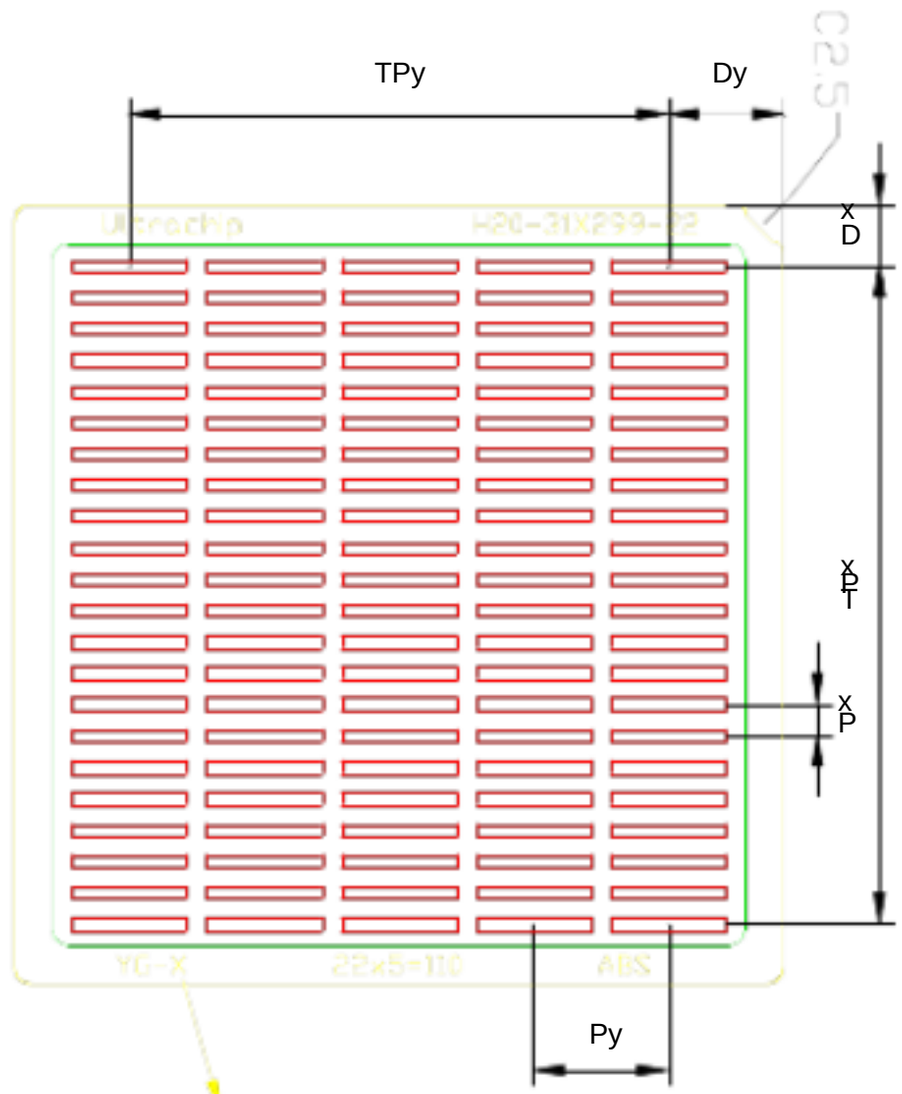
#	Pad	X	Y	W	H
215	COM53	567.3	225.5	15.6	130
216	COM52	539.7	225.5	15.6	130
217	COM51	512.1	225.5	15.6	130
218	COM50	484.5	225.5	15.6	130
219	COM49	456.9	225.5	15.6	130
220	COM48	429.3	225.5	15.6	130
221	COM47	401.7	225.5	15.6	130
222	COM46	374.1	225.5	15.6	130
223	COM45	346.5	225.5	15.6	130
224	COM44	318.9	225.5	15.6	130
225	COM43	291.3	225.5	15.6	130
226	COM42	263.7	225.5	15.6	130
227	COM41	236.1	225.5	15.6	130
228	COM40	208.5	225.5	15.6	130
229	COM39	180.9	225.5	15.6	130
230	COM38	153.3	225.5	15.6	130
231	COM37	125.7	225.5	15.6	130
232	COM36	98.1	225.5	15.6	130
233	COM35	70.5	225.5	15.6	130
234	COM34	42.9	225.5	15.6	130
235	COM33	15.3	225.5	15.6	130
236	COM32	-12.3	225.5	15.6	130
237	COM31	-39.9	225.5	15.6	130
238	COM30	-67.5	225.5	15.6	130
239	COM29	-95.1	225.5	15.6	130
240	COM28	-122.7	225.5	15.6	130
241	COM27	-150.3	225.5	15.6	130
242	COM26	-177.9	225.5	15.6	130
243	COM25	-205.5	225.5	15.6	130
244	COM24	-233.1	225.5	15.6	130
245	COM23	-260.7	225.5	15.6	130
246	COM22	-288.3	225.5	15.6	130
247	COM21	-315.9	225.5	15.6	130
248	COM20	-343.5	225.5	15.6	130
249	COM19	-371.1	225.5	15.6	130
250	COM18	-398.7	225.5	15.6	130
251	COM17	-426.3	225.5	15.6	130
252	COM16	-453.9	225.5	15.6	130
253	COM15	-481.5	225.5	15.6	130
254	COM14	-509.1	225.5	15.6	130
255	COM13	-536.7	225.5	15.6	130
256	COM12	-564.3	225.5	15.6	130
257	COM11	-591.9	225.5	15.6	130
258	COM10	-619.5	225.5	15.6	130
259	COM9	-647.1	225.5	15.6	130
260	COM8	-674.7	225.5	15.6	130
261	COM7	-702.3	225.5	15.6	130
262	COM6	-729.9	225.5	15.6	130
263	COM5	-757.5	225.5	15.6	130
264	COM4	-785.1	225.5	15.6	130
265	COM3	-812.7	225.5	15.6	130
266	COM2	-840.3	225.5	15.6	130
267	COM1	-867.9	225.5	15.6	130
268	COMS	-895.5	225.5	15.6	130

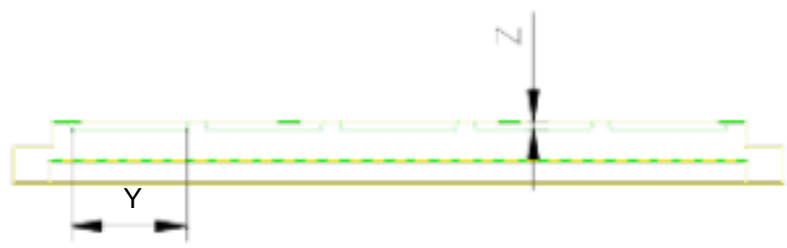
#	Pad	X	Y	W	H
269	SEG1	-1045.1	225.5	15.6	130
270	SEG3	-1072.7	225.5	15.6	130
271	SEG5	-1100.3	225.5	15.6	130
272	SEG7	-1127.9	225.5	15.6	130
273	SEG9	-1155.5	225.5	15.6	130
274	SEG11	-1183.1	225.5	15.6	130
275	SEG13	-1210.7	225.5	15.6	130
276	SEG15	-1238.3	225.5	15.6	130
277	SEG17	-1265.9	225.5	15.6	130
278	SEG19	-1293.5	225.5	15.6	130
279	SEG21	-1321.1	225.5	15.6	130
280	SEG23	-1348.7	225.5	15.6	130
281	SEG25	-1376.3	225.5	15.6	130
282	SEG27	-1403.9	225.5	15.6	130
283	SEG29	-1431.5	225.5	15.6	130
284	SEG31	-1459.1	225.5	15.6	130
285	SEG33	-1486.7	225.5	15.6	130
286	SEG35	-1514.3	225.5	15.6	130
287	SEG37	-1541.9	225.5	15.6	130
288	SEG39	-1569.5	225.5	15.6	130
289	SEG41	-1597.1	225.5	15.6	130
290	SEG43	-1624.7	225.5	15.6	130
291	SEG45	-1652.3	225.5	15.6	130
292	SEG47	-1679.9	225.5	15.6	130
293	SEG49	-1707.5	225.5	15.6	130
294	SEG51	-1735.1	225.5	15.6	130
295	SEG53	-1762.7	225.5	15.6	130
296	SEG55	-1790.3	225.5	15.6	130
297	SEG57	-1817.9	225.5	15.6	130
298	SEG59	-1845.5	225.5	15.6	130
299	SEG61	-1873.1	225.5	15.6	130
300	SEG63	-1900.7	225.5	15.6	130
301	SEG65	-1928.3	225.5	15.6	130
302	SEG67	-1955.9	225.5	15.6	130
303	SEG69	-1983.5	225.5	15.6	130
304	SEG71	-2011.1	225.5	15.6	130
305	SEG73	-2038.7	225.5	15.6	130
306	SEG75	-2066.3	225.5	15.6	130
307	SEG77	-2093.9	225.5	15.6	130
308	SEG79	-2121.5	225.5	15.6	130
309	SEG81	-2149.1	225.5	15.6	130
310	SEG83	-2176.7	225.5	15.6	130
311	SEG85	-2204.3	225.5	15.6	130
312	SEG87	-2231.9	225.5	15.6	130
313	SEG89	-2259.5	225.5	15.6	130
314	SEG91	-2287.1	225.5	15.6	130
315	SEG93	-2314.7	225.5	15.6	130
316	SEG95	-2342.3	225.5	15.6	130
317	SEG97	-2369.9	225.5	15.6	130
318	SEG99	-2397.5	225.5	15.6	130
319	SEG101	-2425.1	225.5	15.6	130
320	SEG103	-2452.7	225.5	15.6	130
321	SEG105	-2480.3	225.5	15.6	130
322	SEG107	-2507.9	225.5	15.6	130

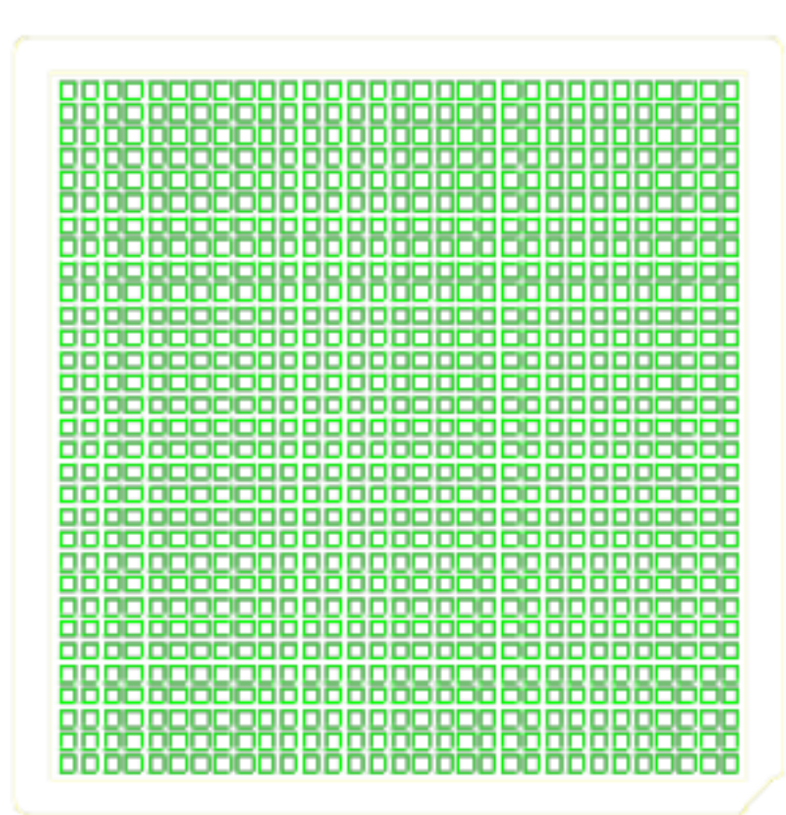
#	Pad	X	Y	W	H
323	SEG109	-2535.5	225.5	15.6	130
324	SEG111	-2563.1	225.5	15.6	130
325	SEG113	-2590.7	225.5	15.6	130
326	SEG115	-2618.3	225.5	15.6	130
327	SEG117	-2645.9	225.5	15.6	130
328	SEG119	-2673.5	225.5	15.6	130
329	SEG121	-2701.1	225.5	15.6	130
330	SEG123	-2728.7	225.5	15.6	130
331	SEG125	-2756.3	225.5	15.6	130
332	SEG127	-2783.9	225.5	15.6	130
333	SEG129	-2811.5	225.5	15.6	130
334	SEG131	-2839.1	225.5	15.6	130
335	SEG133	-2866.7	225.5	15.6	130
336	SEG135	-2894.3	225.5	15.6	130
337	SEG137	-2921.9	225.5	15.6	130
338	SEG139	-2949.5	225.5	15.6	130
339	SEG141	-2977.1	225.5	15.6	130
340	SEG143	-3004.7	225.5	15.6	130
341	SEG145	-3032.3	225.5	15.6	130
342	SEG147	-3059.9	225.5	15.6	130
343	SEG149	-3087.5	225.5	15.6	130
344	SEG151	-3115.1	225.5	15.6	130
345	SEG153	-3142.7	225.5	15.6	130
346	SEG155	-3170.3	225.5	15.6	130
347	SEG157	-3197.9	225.5	15.6	130
348	SEG159	-3225.5	225.5	15.6	130
349	SEG161	-3253.1	225.5	15.6	130
350	SEG163	-3280.7	225.5	15.6	130
351	SEG165	-3308.3	225.5	15.6	130
352	SEG167	-3335.9	225.5	15.6	130
353	SEG169	-3363.5	225.5	15.6	130
354	SEG171	-3391.1	225.5	15.6	130
355	SEG173	-3418.7	225.5	15.6	130
356	SEG175	-3446.3	225.5	15.6	130
357	SEG177	-3473.9	225.5	15.6	130
358	SEG179	-3501.5	225.5	15.6	130
359	SEG181	-3529.1	225.5	15.6	130
360	SEG183	-3556.7	225.5	15.6	130
361	SEG185	-3584.3	225.5	15.6	130
362	SEG187	-3611.9	225.5	15.6	130
363	SEG189	-3639.5	225.5	15.6	130
364	SEG191	-3667.1	225.5	15.6	130
365	DUMMY	-3694.7	225.5	15.6	130

TRAY INFORMATION









	Spec
W1	50.70±0.10 (1996)
W2	45.70±0.10 (1799)
H	3.95±0.10 (156)
E	2.20±0.05 (87)
Dx	3.93±0.05 (155)
TPx	42.84±0.10(1687)
Dy	7.55±0.05 (297)
TPy	35.60±0.10(1402)
Px	2.04±0.05 (80)
Py	8.90±0.05 (350)
X	0.78±0.05 (31)
Y	7.60±0.05 (299)
Z	0.55±0.05 (22)

<NOTE>
1. SURFACE RESISTANCE: 10 e 7~10 e 11 ohm/sq
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: BLACK
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: MAX. 0.1mm
6. THE BOTTOM OF POCKET: ROUGH SURFACE

REVISION HISTORY

Revision	Contents	Date
0.1	N / A	Sep. 3, 2009
0.6	(1) V_{DD} 2/3 (Typical) range is adjusted: 2.5V~3.3V ? 2.7V~3.3V V_{DD} 2/3 (Minimum) is adjusted: 2.4V ? 2.6V	Jul. 22, 2010
	(2) The drawing of COG Layout presents.	
	(3) The sample codes for Power Up are updated.	
	(4) Data of ESD consideration present.	
	(5) V_{IH} (Min.) is adjusted: 0.8V $_{DD}$? 0.9V $_{DD}$ V_{IL} (Max) is adjusted: 0.2V $_{DD}$? 0.1V $_{DD}$	
	(6) The Power Consumption data present.	
	(7) The tray drawing presents.	