XN297LBW Datasheet

Single Chip 2.4GHz Transceiver

FEATURES

- Low Power
  - ➢ 16mA TX at 0dBm output power
  - ➢ 15mA RX at 2Mbps air data rate
  - ➢ 2uA in power down
- Low Cost BOM
  - ➢ Few external components
    Four Capacitors, One crystal oscillator
- High Performance
  - ➢ Excellent Receiver sensitivity
    -85dBm@2Mbps
    -88dBm@1Mbps
    -93dBm@250Kbps
  - ➢ Programmable Output Power Up to 13dBm
  - ➢ Stable RF performance over a wide operating voltage range
  - ➢ Built-in LDO 1.8V

APPLICATIONS

- TV and STB remote controls
- Wireless Mouse and keyboard
- Toys and wireless audio
- Wireless gamepads
- Active RFID
- Smart home automation

GENERAL DESCRIPTION

The XN297LBW is a single chip 2.4GHz transceiver , designed for operation in the world wide ISM frequency band at 2.400~2.483GHz. The XN297LBW integrates radio frequency (RF) transmitter and receiver, frequency synthesizer, crystal oscillator, baseband GFSK modem, and so on. The XN297LBW supports one to multiple network and communication with ACK. TX power, frequency channel, and data rate can be set by SPI. Multiple external components are integrated into the chip.

2Mbps, 1Mbps 250kbps optional data rate	Up to 4Mbps SPI interface rate
Support 32 and 64 byte payload length	Compact 8-pin SOP8 package
Support ±20ppm 16MHz crystal	Operating voltage 2.2V~3.3V

GFSK Modulation	Support automatic reply and automatic retransmission
Support RSSI detector	Support Data whitening and CRC

1 Electrical characteristics

Table1 XN297L Electrical characteristics

Symbol	Condition	Parameter			Unit
	at VCC = 3V±5%, T=25℃	Min	Typ	Max	
ICC	Sleep		2		uA
	Standby I		30		uA
	Standby III		650		uA
	Standby II		780		uA
	TX at -35dBm output power		9		mA
	TX at -20dBm output power		9.5		mA
	TX at 0dBm output power		16		mA
	TX at 2dBm output power		19		mA
	TX at 8dBm output power		30		mA
	TX at 13dBm output power		66		mA
	RX at 2Mbps		16.5		mA
	RX at 1Mbps		15.5		mA
	RX at 250kbps		15		mA
General RF					
f_{OP}	Operating frequency	2400		2483	MHz
PLL_{res}	PLL Programming resolution		1		MHz
f_{XTAL}	Crystal frequency		16		MHz
DR	Data rate	1		2	Mbps
Δf_{250K}	Frequency deviation at 250kbps		125		KHz
Δf_{1M}	Frequency deviation at 1Mbps		160	250	KHz
Δf_{2M}	Frequency deviation at 2Mbps		320	500	KHz
FCH_{250K}	Channel spacing at 250Kbps		1		MHz
FCH_{1M}	Channel spacing at 1Mbps		1		MHz
FCH_{2M}	Channel spacing at 2Mbps		2		MHz
Transmitter					
PRF	Typical output power	2	8	13	dBm
$PRFC$	Output Power Range	-35		13	dBm
$PBW1$	20dB Bandwidth for		2		MHz

	Modulated Carrier at 2Mbps				
$PBW2$	20dB Bandwidth for Modulated Carrier at 1Mbps		1		MHz
$PBW3$	20dB Bandwidth for Modulated Carrier at 250Kbps		500		KHz
Receiver					
RX_{max}	Maximum received signal at <0.1% BER		0		dBm
$RXSENS1$	Sensitivity (0.1%BER) @2Mbps		-83		dBm
$RXSENS2$	Sensitivity (0.1%BER) @1Mbps		-87		dBm
$RXSENS3$	Sensitivity (0.1%BER) @250Kbps		-93		dBm
C/I_{CO}	C/I Co-channel (@2Mbps)		10		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I		-6		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I		-10		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I		-22		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I		-34		dBc
C/I_{CO}	C/I Co-channel (@1Mbps)		10		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I		1		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I		-18		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I		-23		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I		-32		dBc

C/I_{6TH}	6th Adjacent Channel Selectivity C/I		-35		dBc
C/I_{CO}	C/I Co-channel (@250Kbps)		2		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I		-8		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I		-18		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I		-24		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I		-32		dBc
C/I_{6TH}	6th Adjacent Channel Selectivity C/I		-35		dBc
Operating conditions					
VDD	Supply voltage	2.2	3	3.3	V
VSS	Ground		0		V
V_{OH}	Output high level voltage	VDD-0.3		VDD	V
V_{OL}	Output low level voltage	VSS		VSS+0.3	V
V_{IH}	Input high level voltage	2.0	3	3.6	V
V_{IL}	Input low level voltage	VSS		VSS+0.3	V

* Note: In the channels, such as 2416 and 2432 MHz, integer times of 16MHz crystal, receiver sensitivity degrades about 2dB; and modulation quality of the emission signal (EVM) falls by 10%.

* Note: In 250KBps mode, it should not be more than 16 bytes of payload length, because of frequency drift in open-loop transmition.

2 Absolute maximum ratings

Table 2 XN297LBW absolute maximum ratings

Symbol	Condition	Parameter			Unit
		Min	Typ	Max	
maximum ratings					
V_{DD}	Supply voltage	-0.3		3.6	V
V_I	Input voltage	-0.3		5	V
V_O	Output voltage	VSS		VDD	
Pd	Total Power Dissipation (TA=-40℃~85℃)			300	mW
T_{OP}	Operating Temperature	-40		85	℃
T_{STG}	Storage Temperature	-40		125	℃

* Note: Exceeding one or more of the limiting values may cause permanent damage to XN297LBW.

* Caution: Electrostatic sensitive device, comply with protection rules when operating.
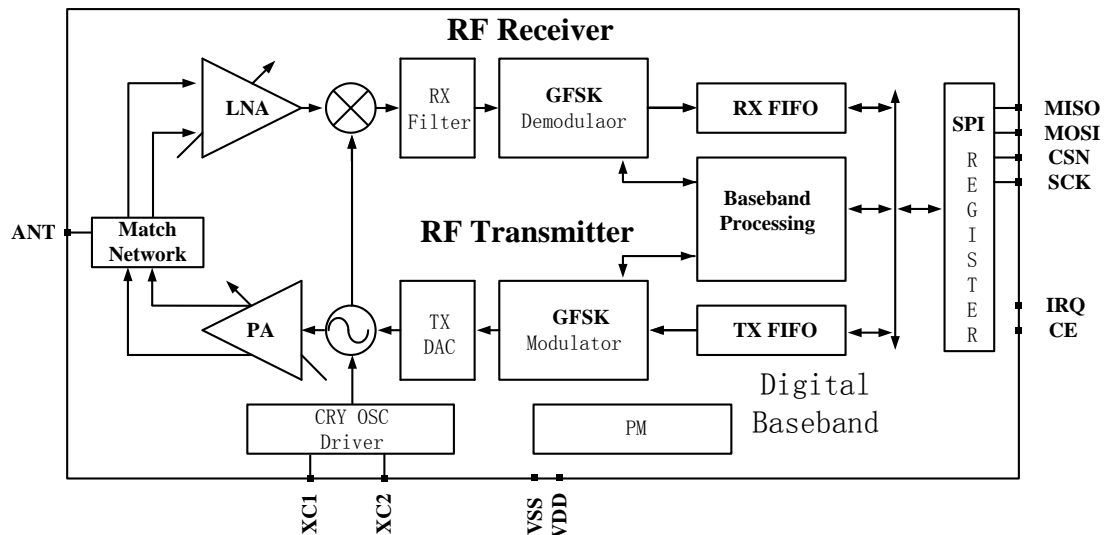
3 Block diagram
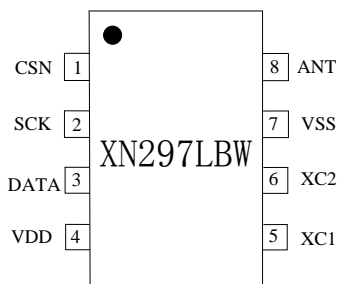

Figure 1 XN297LBW block diagram

4 Pin definition

Figure2 XN297LBW pin definition

Table 3 Pin function

PIN	Name	Function	PIN	Name	Function
1	CSN	SPI Chip Select	5	XC1	Crystal Pin 1
2	SCK	SPI Clock	6	XC2	Crystal Pin 2
3	DATA	SPI Data Input/Output	7	VSS	Ground
4	VDD	Power Supply	8	ANT	Antenna interface

5 Operational Modes

This chapter describes XN297LBW all kinds of working mode, and is used to control the chip into the working mode of method. XN297LBW own state machine is controlled by chip internal registers configuration values and external signal pin.
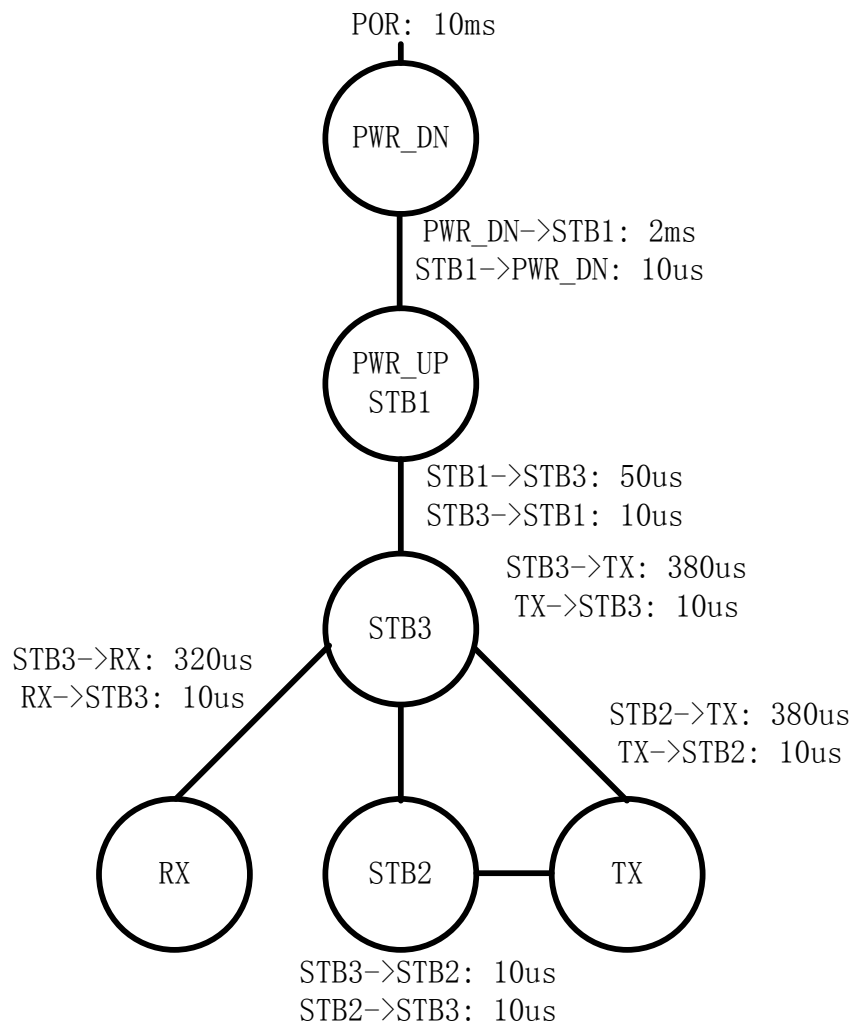
5.1 State diagram

Six kinds of working mode in table 4 gives the corresponding mode of control register and FIFO registers.

Table 4 Control BIT and function description

MODE	PWR_DN	STB1	STB3	STB2	RX	TX
CONTROL BIT						
PWR_UP	0	1	1	1	1	1
EN_PM	0	0	1	1	1	1
CE	0	0	0	1	1	1
PRIM_RX	X	X	X	0	1	0
FUNCTION DESCRIPTION						
SPI operation	√	√	√	√	√	√
Keep register value	√	√	√	√	√	√
Crystal oscillator work	X	√	√	√	√	√
Crystal oscillator output	X	X	X	√	√	√
Main power management work	X	X	√	√	√	√
TX work	X	X	X	X	X	√
RX work	X	X	X	X	√	X

5.2 State diagram

Figure 3 is XN297LBW working state diagram, said six working mode between jump XN297LBW in VDD is greater than 2.2 V to begin to work properly into sleep mode, the MCU can be sent via SPI configuration commands and CE pin into the other five state.

POR: 10ms

PWR_DN

PWR_DN->STB1: 2ms
STB1->PWR_DN: 10us

PWR_UP
STB1

STB1->STB3: 50us
STB3->STB1: 10us

STB3->TX: 380us
TX->STB3: 10us

STB3

STB3->RX: 320us
RX->STB3: 10us

STB2->TX: 380us
TX->STB2: 10us

RX

STB2

TX

STB3->STB2: 10us
STB2->STB3: 10us

Figure3 state diagram

5.3 IRQ PIN

In the status register TX_DS RX_DR or MAX_RT is 1, report and the corresponding interrupt enable bit is 0, IRQ pins interrupt trigger. The MCU writes 1 to the corresponding interrupt source, clear the interrupt. IRQ pins interrupt trigger can be blocked or enabled, report by setting the interrupt enable bit is 1, ban IRQ pins interrupt triggered.
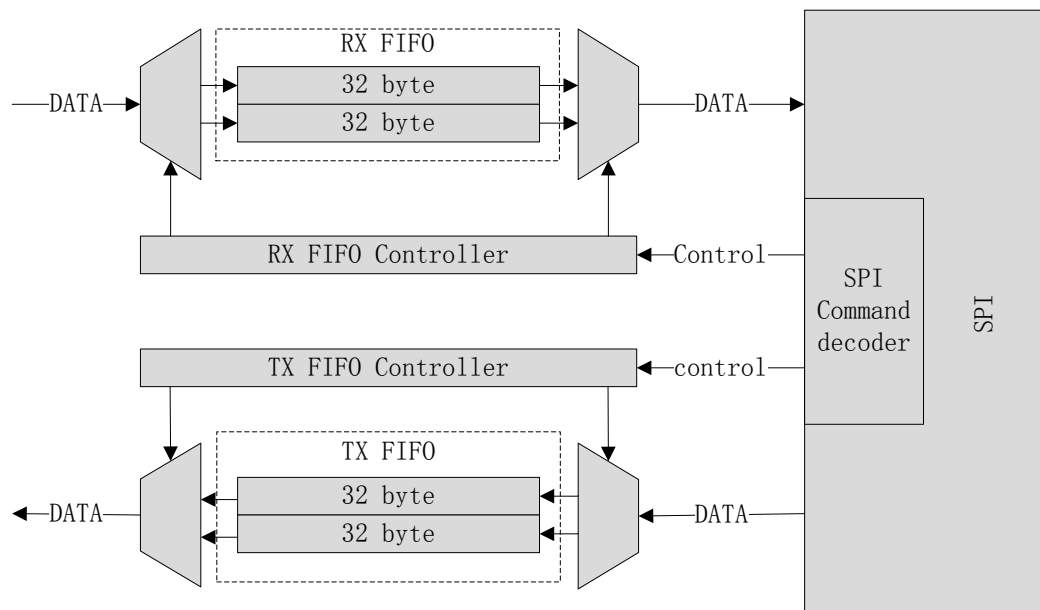
6 DATA FIFO

Figure 4 FIFO block diagram

The XN297LBW contains TX FIFO, RX FIFO. It is sent via SPI read/write command. It writes TX FIFO in TX mode by W_TX_PAYLOAD and W_TX_NO_ACK instructions. If MAX_RT interruption, data will be cleared in the TX FIFO. It reads PAYLOAD in RX FIFO in receiving mode by R_RX_PAYLOAD, and it reads the length of the PAYLOAD by R_RX_PL_WID instruction. FIFO_STATUS register indicates FIFO states.

7 SPI CONTROL

The XN297L is controlled by SPI port for read and write register, and command. The XN297L is a slave terminal, SPI transfer rate depends on the MCU interface speed, and the maximum data transfer rate is 4 MBps.

SPI interface is a standard SPI interface are shown in table 5, you can use the general I/O for MCU simulation SPI interface. CSN pin to 0, SPI interface instructions to be performed. From 1 to 0 a CSN pin changes execute one instruction. After the change from 1 to 0 CSN pin can be read by MISO status register contents.

Table 5 SPI port

PIN	I/O DIRECTION	FUNCTION DESCRIPTION
CSN	Input	SPI Chip Select
SCK	Input	Clock
DATA	Input/Output	Serial Data Input/Output

*Note1: CSN Pin to 0, Data pin input the addr from MCU. After 8 clock, Data Pin transformed from input status to output status, and MCU read data.
*Note2: CE status is controlled by SPI.
*Note3: IRQ status is obtained by inquiring register
*Note4: During emitting signal, SPI writing/reading is forbidden.

7.1 SPI Commands

Table 6 SPI command format

<Command word: MSBit to LSBit (one byte)>

<Data bytes: LSByte to MSByte, MSBit in each byte first>

COMMAND	COMMAND WORD	DATA BYTES	OPERATION

	(BINARY)		
R_REGISTER	000A AAAA	1 to 5	Read registers. AAAAA =5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5	Write registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32/64	Read RX-payload. A read operation starts at byte 0. Payload is deleted from RX FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32/64	Write TX-payload. A write operation starts at byte 0. Used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode
REUSE_TX_PL	1110 0011	0	Used for a PTX device, reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH_TX is executed.
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_TX_PAYLOAD_NOACK • W_ACK_PAYLOAD This is executable in power down or standby modes only.

DEACTIVE			This write command followed by data 0x8C deactivates the following features:
R_RX_PL_WID	0110 0000	0	Read RX-payload width for the top, R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD	1010 1PPP	1 to 32/64	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum two ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle.
W_TX_PAYLOAD_NO ACK	1011 0000	1 to 32/64	Write Payload to be transmitted, used in TX mode. Disable auto ACK on this packet.
CE_FSPI_ON	1111 1101	1	SPI command CE internal logic 1, use the command followed by the data 0x00
CE_FSPI_OFF	1111 1100	1	SPI command CE internal logic 0, use the command followed by the data 0x00
RST_FSPI_HOLD	0101 0011	1	With the command followed by data 0x5A, makes the XN297L into reset and maintain
RST_FSPI_RELS			With the command followed by data 0xA5, release the XN297 reset and start to work normally

NOP	1111 1111	0	No Operation.

The R_REGISTER and W_REGISTER commands can operate on single or multi-byte registers. When accessing multi-byte registers, first read or write the MSBit of LSByte. Terminate the writing before all bytes in a multi-byte register are written, then it leaves the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register.
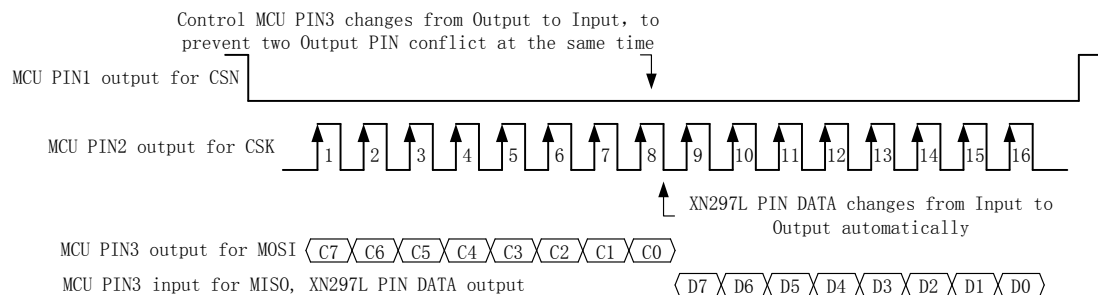
7.2 SPI Timing

Figure 5 SPI read operation

8 Packet format description

8.1 Packet format for normal Burst

Table 7 Packet format for normal burst

Preamble (3 byte)	Address (3~5 byte)	Payload (1~32/64 byte)	CRC (0/2 byte)

It can choose Address and Payload part to scramble, according to scrambler

configuration bits.

8.2 Packet format for Enhanced Burst

Table 8 Packet format for enhanced burst

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			Payload (1~32/64 byte)	CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)		

It can choose Address, Package control field and Payload part to scramble, according to scrambler configuration bits.

8.3 Packet format for Enhanced Burst ACK

Table 9 Packet format for enhanced burst ack

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)	

It can choose Address, Package control field to scramble, according to scrambler configuration bits.
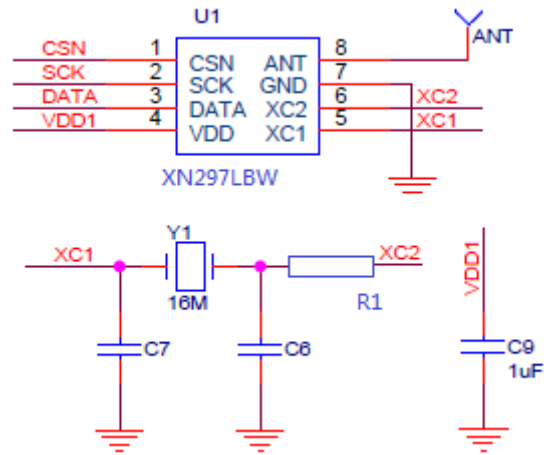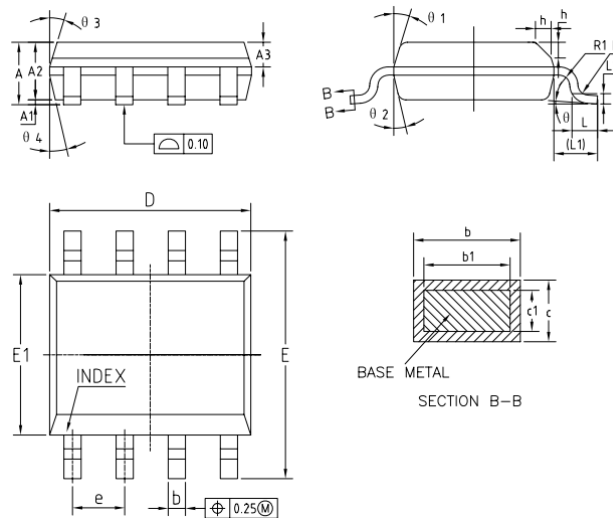
9 Application example

Figure6 XN297L application

10 Package size

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°
θ3	15°	17°	19°
θ4	11°	13°	15°

Figure 7 SOP8L package size