OV5620 Color CMOS QSXGA (5.17 MPixel) CAMERACHIP™ with OmniPixel2™ Technology

General Description

The OV5620 (color) CAMERACHIP™ is a high performance 5.17 mega-pixel image sensor for digital still image and video camera products.

This device incorporates a 2592 x 1944 image array and an on-chip 10-bit A/D converter capable of operating at up to 7.5 frames per second (fps) in full resolution. The OV5620 can also output 864 x 600 resolution at 60 fps enabling enhanced video viewing on TV. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming, dark current and lens shading. The control registers allow for flexible control of timing, polarity, and CAMERACHIP operation, which, in turn, allows the engineer a great deal of freedom in product design.

Note: The OV5620 is available in a lead-free package.

Features

- Optical black level calibration
- Video or snapshot operations
- Programmable/Auto Exposure and Gain Control
- Programmable/Auto White Balance Control
- Horizontal and vertical sub-sampling for high frame rate with excellent image quality
- High frame rate output mode
- Programmable image windowing
- Variable frame rate control
- On-chip Luminance Average Counter
- VarioPixel® (binning) 1:2, 1:3, 1:4
- Subsampling (skip) 1:2, 1:3, 1:4, 1:8
- Flash control output (strobe pin)
- 50/60 Hz light auto detection
- Image vertical flip / horizontal mirror
- Defect pixel correction
- Internal/External frame synchronization
- Serial bus interface
- Power-on reset and power-down modes

Ordering Information

Product	Package
OV05620-C03A (Color)	CLCC-48

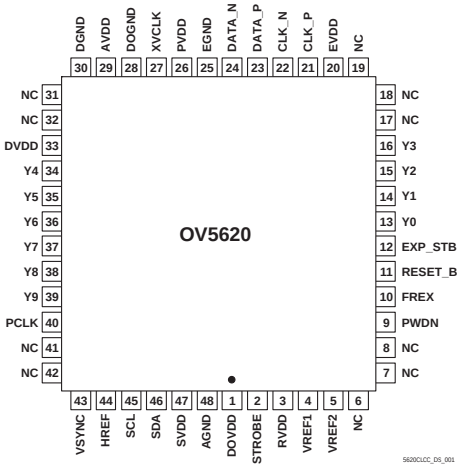
Applications

- Digital still cameras
- Digital video cameras
- PC camera/dual mode
- Video conference equipment

Key Specifications

Array Size		2592 x 1944
Power Supply	**Analog**	2.6 ~ 3.0V
	Digital	1.3V ± 5%
	I/O	1.7 ~ 3.3V
Power Requirements	**Active**	TBD
	Standby	250 µA
Electronics Exposure		1 T_{LINE} to 1/F where F = frame rate
Shutter		Electronic rolling shutter, snapshot
Output Format		10-bit digital RGB Raw data
Lens Size		1/2.5"
Lens Chief Ray Angle		12.5°
Input Clock		6 - 27 MHz
Maximum System Clock		48 MHz
Maximum Data Rate		48 MHz
Max Image Transfer Rate	**Full**	7.5 fps
	1.3Mpixel	30 fps
	D1MD	60 fps
	VGA	60 fps
	QVGA	120 fps
Sensitivity		TBD
S/N Ratio		TBD
Dynamic Range		TBD
Scan Mode		Progressive
Pixel Size		2.2 µm x 2.2 µm
Dark Current		TBD
Fixed Pattern Noise		TBD
Image Area		5.808 mm x 4.294 mm
Package Dimensions		14.22 mm x 14.22 mm

Figure 1 OV5620 Pin Diagram (Top View)



Version 1.1, May 9, 2006

Functional Description

Figure 2 shows the functional block diagram of the OV5620 image sensor. The OV5620 includes:

- Image Sensor Array (2592+16) x (1944+4) resolution)
- Analog Amplifier
- Gain Control
- Balance Control
- 10-Bit A/D Converter
- Test Pattern Generator
- Digital Signal Processor (DSP)
- Snapshot (Frame Exposure) Mode Timing
- Frame Rate Adjust
- SCCB Interface
- Channel Average Calculator

Figure 2 Functional Block Diagram

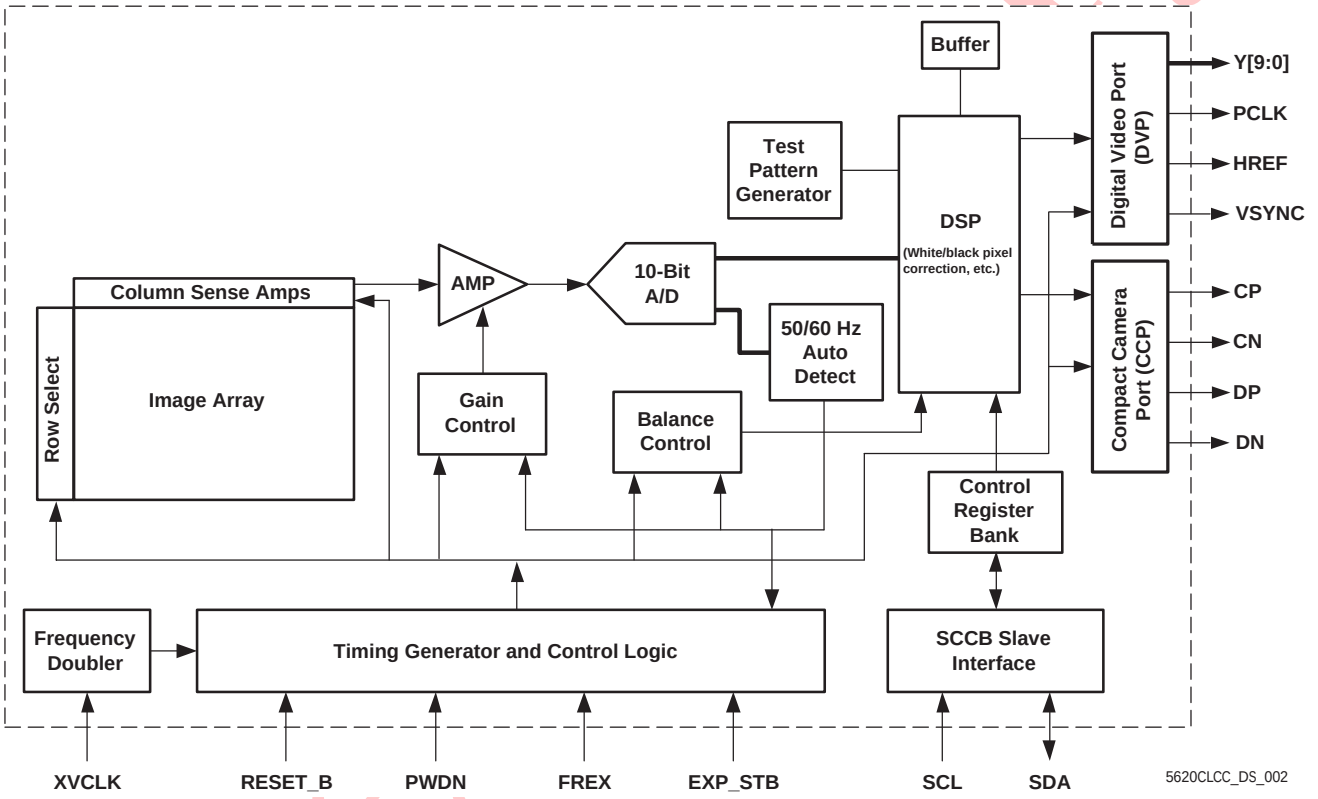


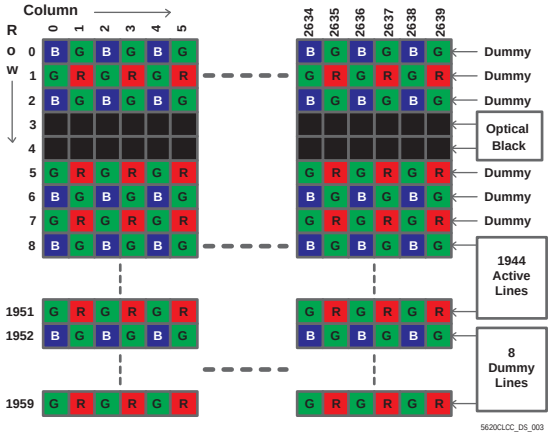
Image Sensor Array

The OV5620 sensor is a 1/2.5-inch CMOS imaging device. The sensor contains 5,174,400 pixels. Figure 3 shows the color filter layout.

The color filters are in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 5,174,400 pixels, 5,080,384 are active. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

Figure 3 Sensor Array Region Color Filter Layout



Analog Amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain Control

The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC). The gain adjustment range is 0-24 dB.

Balance Control

Channel balance can be done manually by the user or by the internal automatic white balance (AWB) controller.

10-Bit A/D Converter

The balanced signal is then digitized by the on-chip 10-bit ADC. It can operate at up to 27 MHz and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

Test Pattern Generator

The Test Pattern Generator features the following:

- 8-bar color bar pattern
- Fade-to-gray color bar pattern
- Shift "1" in output pin

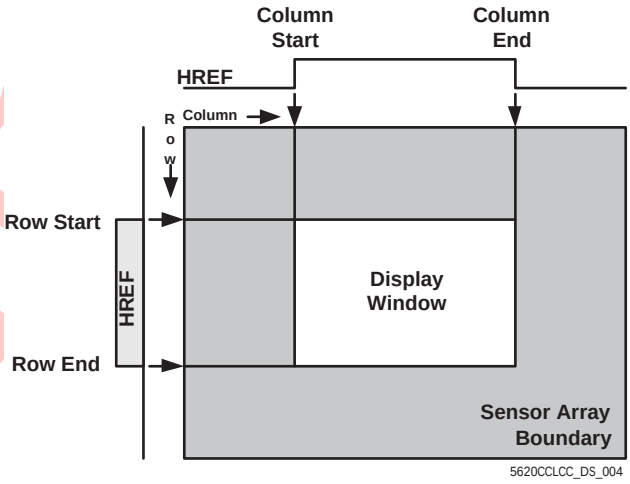
Digital Signal Processor (DSP)

- White/black pixel correction
- Lens shading correction

Windowing

The OV5620 allows the user to define window size or region of interest (ROI), as required by the application. Window size setting (in pixels) ranges from 2 x 4 to 2592 x 1944 (QSXGA) or 2 x 2 to 1280 x 960 (1.3 Mpixel) and 640 x 480 (VGA), and can be anywhere inside the 2592 x 1944 boundary. The windowing control merely alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical ROI.

Figure 4 Windowing



VarioPixel (Binning) 1:2, 1:3, 1:4

Figure 5 Horizontal/Vertical 1:2 Average (Binning)

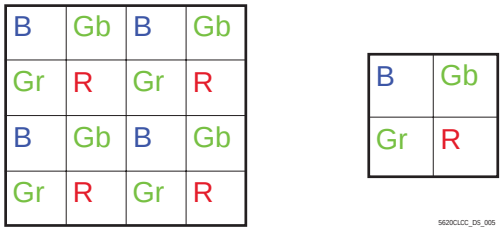


Figure 6 Horizontal 1:3 Average (Binning)

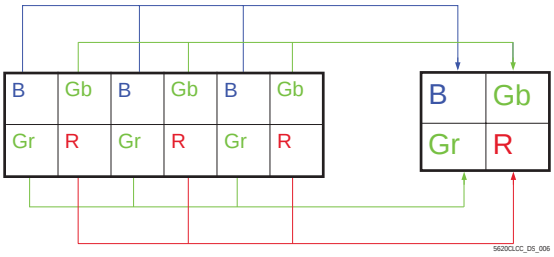


Figure 7 Vertical 1:3 Average (Binning)

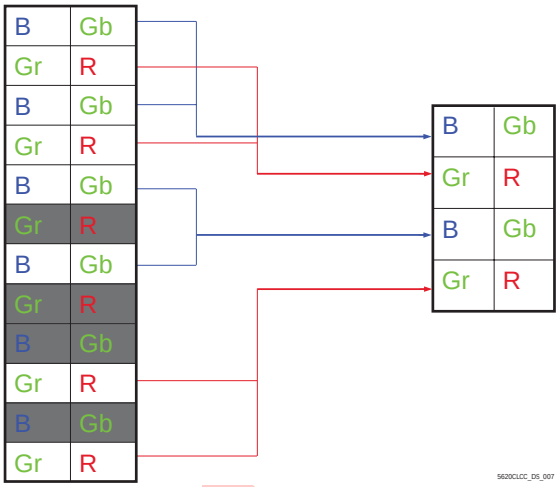


Figure 8 Horizontal 1:4 Average (Binning)

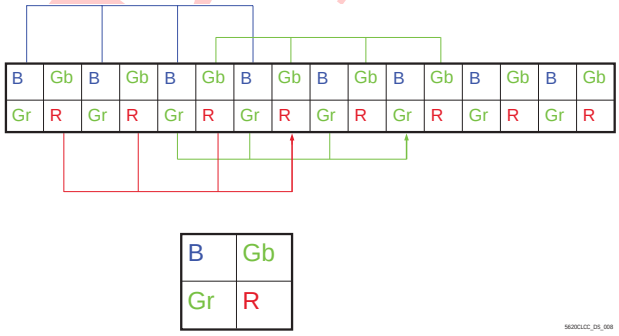
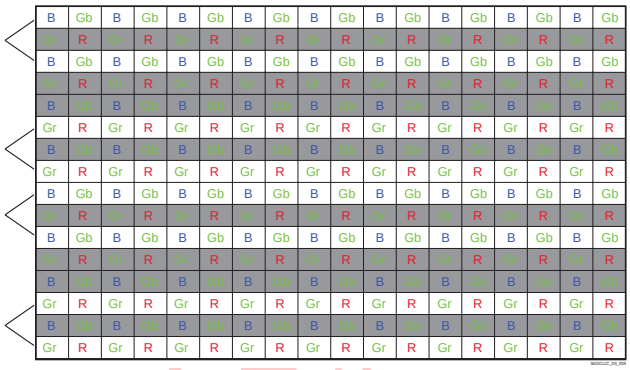


Figure 9 Vertical 1:4 Average (Binning)



Flash Control Output (Strobe Pin)

The OV5620 has a Strobe mode that allows it to work with an external flash and LED.

Snapshot (Frame Exposure) Mode Timing

The OV5620 supports snapshot (frame exposure) mode. Typically, the snapshot mode must work with the aid of an external shutter.

The frame exposure pin, FREX (pin 10), is the snapshot mode enable pin and the EXP_STB pin (pin 12) serves as the sensor's exposure start trigger. When the external master device asserts the FREX pin high, the sensor array is quickly pre-charged and stays in reset mode until the EXP_STB pin is pulled low (sensor exposure time can be defined as the period between EXP_STB low to shutter close). After the FREX pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data output, the OV5620 will output continuous live video data unless in single frame transfer mode. Figure 17 shows detailed timing of the Frame Exposure mode and Table 10 shows the timing specifications for this mode.

When the OV5620 is working in snapshot mode, every line is sampled at different times causing different dark current levels line-by-line. To eliminate the dark current difference, the OV5620 provides line optical black pixel output. The difference in dark current can be calibrated line-by-line.

Frame Rate Adjust

The OV5620 offers four methods for frame rate adjustment:

- Clock prescaler: (see "CLKRC" on page 17)
  By changing the system clock divide ratio, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 … 1/64 of the PLL output clock.
- Horizontal blanking: (see "REG2A" on page 20 and see "EXHCL" on page 20)
  By changing the horizontal blank timing in each line after active pixel output, the frame rate can be changed while leaving the pixel rate as is.
- Vertical blanking:
  By adding dummy line periods to the vertical sync period (see "ADDVSL" on page 20 and "ADDVSH" on page 20) or after the active lines (see "DMLNL" on page 21 and "DMLNH" on page 21), the frame rate can be altered while the pixel rate remains the same.
- PLL control: Supports more flexible clock control

SCCB Interface

The OV5620 provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of OV5620 operation.

Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Slave Operation Mode

The OV5620 can be programmed to operate in slave mode (default is master mode).

When used as a slave device, the OV5620 re-uses input pins, RESET_B and PWDN, for use as horizontal and vertical synchronization input triggers supplied by a master device. The master device must provide the following signals:

1. System clock MCLK to XVCLK pin
2. Horizontal sync MHSYNC to RESET_B pin
3. Vertical frame sync MVSYNC to PWDN pin

See Figure 10 for slave mode connections and Figure 11 for detailed timing considerations.

Figure 10 Slave Mode Connection

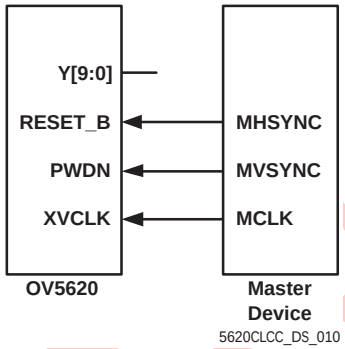
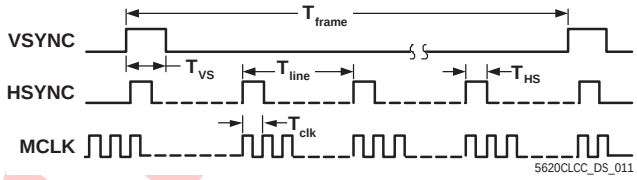


Figure 11 Slave Mode Timing



NOTE:
1) $T_{HS} > 6\ T_{clk}$, Tvs > T_{line}
2) $T_{line} = 3252 \times T_{clk}$ (QSXGA); $T_{line} = 1640 \times T_{clk}$ (1.3 Mpixel)
3) $T_{frame} = 1968 \times T_{line}$ (QSXGA); $T_{frame} = 976 \times T_{line}$ (1.3 Mpixel)

Channel Average Calculator

The OV5620 provides average output level data for frame-averaged luminance level. Access to the data is provided via the SCCB interface.

Reset_B

The OV5620 includes a RESET_B pin (pin 11) that forces a complete hardware reset when it is pulled low (ground). The OV5620 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface.

Power Down Mode

Two methods are available to place the OV5620 into power-down mode.

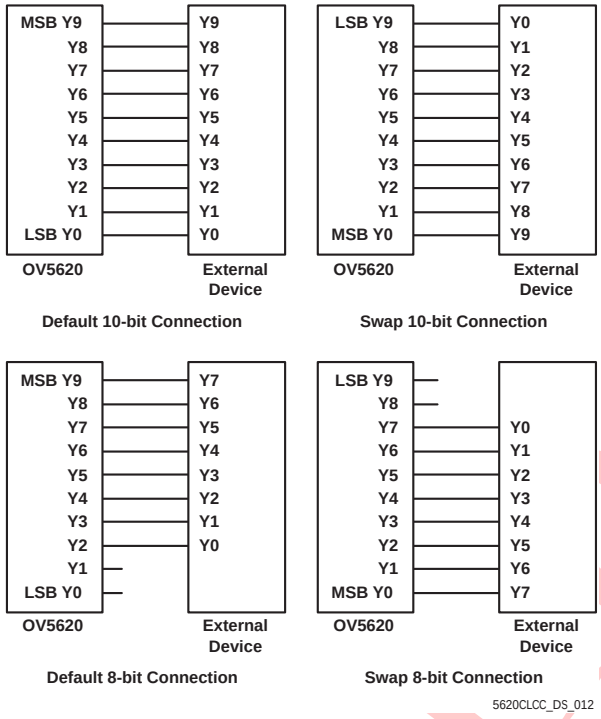
- Hardware power-down may be selected by pulling the PWDN pin (pin 9) high (DOVDD). When this occurs, the OV5620 internal device clock is halted and all internal counters are reset. The current draw is less than 250 µA in this standby mode.
- Software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. The current requirements drop to less than 1 mA in this mode. All register content is maintained in standby mode.

Digital Video Port

MSB/LSB Swap

The OV5620 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 12 shows some examples of connections with external devices.

Figure 12 Connection Examples



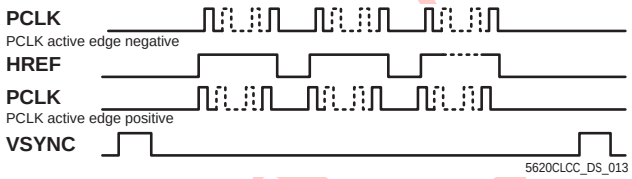
Line/Pixel Timing

The OV5620 digital video port can be programmed to work in either master or slave mode.

In both master and slave modes, pixel data output is synchronous with PCLK (or MCLK if port is a slave), HREF, and VSYNC. The default PCLK edge for valid data is the negative edge but may be programmed using register COM10[4] for the positive edge. Basic line/pixel output timing and pixel timing specifications are shown in Figure 15 and Table 8.

Also, PCLK output can be programmed using register COM10[5] to be gated by the active video period defined by the HREF signal. See Figure 13 for details.

Figure 13 PCLK Output Only at Valid Pixels



The specifications shown in Table 8 apply for DVDD = +1.3 V, DOVDD = +3.3 V, T_A = 25°C, sensor working at 10 fps, external loading = 30 pF.

Pixel Output Pattern

Table 1 shows the output data order from the OV5620. The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$... $B_{0,2590}$ $G_{0,2591}$. After the second HREF the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$... $G_{1,2590}$ $R_{1,2591}$..., etc.

Table 1 Data Pattern

R/C	0	1	2	3	. . .	2590	2591
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,2590}$	$G_{0,2591}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,2590}$	$R_{1,2591}$
2	$B_{2,0}$	G_2	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,2590}$	$G_{2,2591}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,2590}$	$R_{3,2591}$
. . .					. . .		
1942	$B_{1942,0}$	$G_{1942,1}$	$B_{1942,2}$	$G_{1942,3}$		$B_{1942,2590}$	$G_{1942,2591}$
1943	$G_{1943,0}$	$R_{1943,1}$	$G_{1943,2}$	$R_{1943,3}$		$G_{1943,2590}$	$R_{1943,2591}$

Pin Description

Table 2 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	DOVDD	Power	Power for I/O circuit (1.7V to 3.3V)
02	STROBE	Output	LED control output
03	RVDD	Power	Regulator power (2.8V)
04	VREF1	Analog	Internal reference - connect to ground using a 0.1 µF capacitor
05	VREF2	Analog	Internal reference - connect to ground using a 0.1 µF capacitor
06	NC	–	No connection
07	NC	–	No connection
08	NC	–	No connection
09	PWDN	Input (0)	Power down control, active high (hardware standby)
10	FREX	Input (0)	Frame exposure control 1
11	RESET_B	Input (1)	Hardware reset, active low
12	EXP_STB	Input (0)	Frame exposure control 2
13	Y0	Output	Bit[0] of video output port
14	Y1	Output	Bit[1] of video output port
15	Y2	Output	Bit[2] of video output port
16	Y3	Output	Bit[3] of video output port
17	NC	–	No connection
18	NC	–	No connection
19	NC	–	No connection
20	EVDD	Power	CCP2 power (2.8V)
21	CLK_P	Output	CCP2 positive clock output
22	CLK_N	Output	CCP2 negative clock output
23	DATA_P	Output	CCP2 interface positive data output
24	DATA_N	Output	CCP2 interface negative data output
25	EGND	Power	CCP2 ground
26	PVDD	Power	PLL power (2.8V)
27	XVCLK	Input	System clock input
28	DOGND	Power	Ground for I/O circuit
29	AVDD	Power	Analog power (2.8V)
30	DGND	Power	Digital ground
31	NC	–	No connection

Table 2 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
32	NC	–	No connection
33	DVDD	Power	Internal reference - connect to ground using a 0.1 µF capacitor or digital power (1.3V)
34	Y4	Output	Bit[4] of video output port
35	Y5	Output	Bit[5] of video output port
36	Y6	Output	Bit[6] of video output port
37	Y7	Output	Bit[7] of video output port
38	Y8	Output	Bit[8] of video output port
39	Y9	Output	Bit[9] of video output port
40	PCLK	Output	Pixel clock output
41	NC	–	No connection
42	NC	–	No connection
43	VSYNC	Output	Vertical synchronization output
44	HREF	Output	Horizontal reference (data valid) output
45	SCL	Input	I2C clock
46	SDA	I/O	I2C data
47	SVDD	Power	Analog power (2.8V)
48	AGND	Power	Analog ground

Electrical Characteristics

Table 3 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	-20	+70	°C
Storage temperature[a]	-40	+125	°C

a. Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.

Table 4 DC Characteristics (-20°C < T_A < 70°C, Voltages referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD1}	Supply voltage (RVDD, EVDD, PVDD, AVDD, SVDD)	2.6	2.8	3.0	V
V_{DD2}	Supply voltage (DOVDD)	1.7	2.8	3.3	V
V_{DD3}	Supply voltage (DVDD)	1.24	1.3	1.37	V
$I_{DD-VDD1}$	Supply current (QSXGA at 7.5 fps)		TBD		mA
$I_{DD-VDD2}$	Supply current (QSXGA at 7.5 fps)		TBD		mA
$I_{DD-VDD3}$	Supply current (QSXGA at 7.5 fps)		TBD		mA
Digital Inputs					
V_{IL}	Input voltage LOW			0.3 x V_{DD2}	V
V_{IH}	Input voltage HIGH	0.7 x V_{DD2}			V
C_{IN}	Input capacitor			10	pF
Digital Outputs					
V_{OH}	Output voltage HIGH	0.9 x V_{DD2}			V
V_{OL}	Output voltage LOW			0.1 x V_{DD2}	V
SCCB Inputs					
V_{IL}	SCL and SDA			0.3 x V_{DD2}	V
V_{IH}	SCL and SDA	0.7 x V_{DD2}			V

Table 5 AC Characteristics (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		24	27	MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for 1.3 Mpixel/QSXGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 6 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XVCLK)	6	24	27	MHz
t_r, t_f	Clock input rise/fall time			2	ns
	Clock input duty cycle	45	50	55	%

Timing Specifications

Figure 14 Serial Bus Timing Diagram

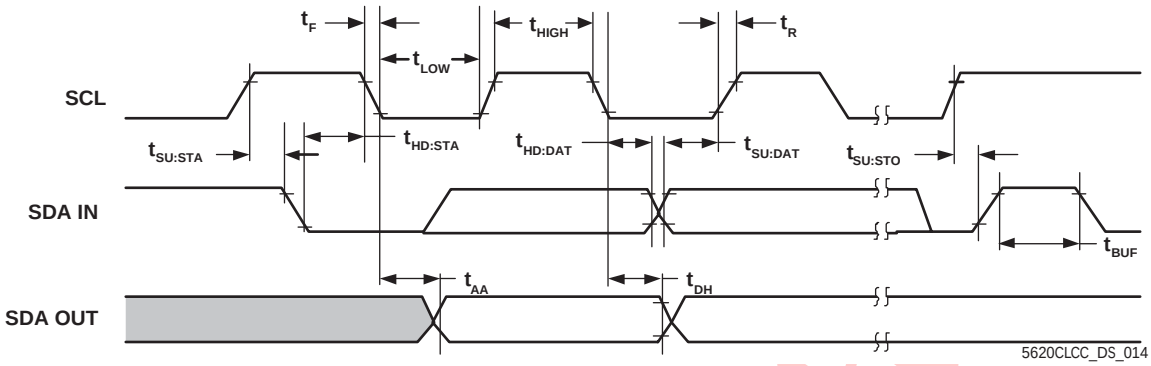


Table 7 Serial Bus Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SCL low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	Serial Bus Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 15 QSXGA, 1.3 Mpixel, VGA and HF Mode Line/Pixel Output Timing

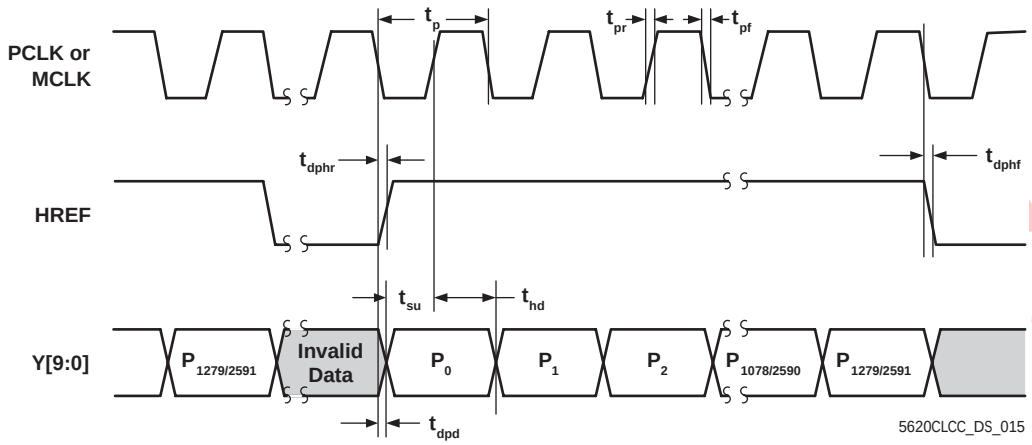
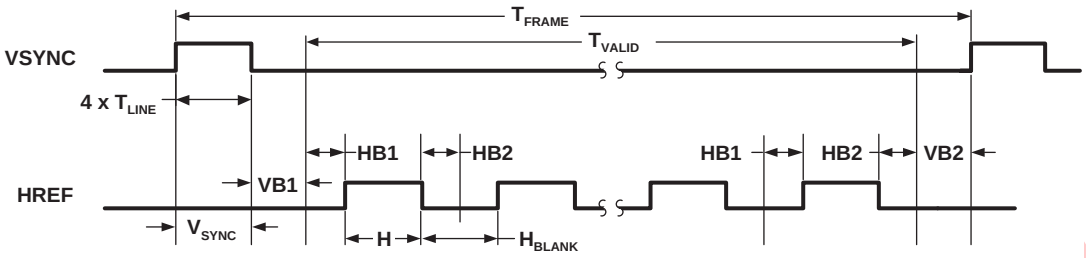


Table 8 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		20.83		ns
t_{pr}	PCLK rising time		4		ns
t_{pf}	PCLK falling time		1		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 16 Frame Timing



NOTES:

1. $T_{FRAME} = T_{VALID} + V_{BLANK}$
2. $H_{BLANK} = HB1 + HB2$
3. $T_{LINE} = H + H_{BLANK}$
4. $V_{BLANK} = VB1 + VB2 + V_{SYNC}$

5620CLCC_DS_016

Table 9 Control Parameters for Standard Resolution Output

Format	H_Size (pixels)	V_Size (pixels)	H_Bin	V_Bin	VB2	V_{SYNC}	VB1	HB1	HB2[a]	H_{BLANK}(pixels)	V_{BLANK} (T_{LINES})	Frame Rate[b] (fps)
5 Mpixel	2592	1944	1:1	1:1	0	4	20	192	468	660	24	7.5
1.3 Mpixel	1280	960	1:2	1:2	0	4	13	192	168	360	17	30
D1MD	864	600	1:3	1:3	0	4	13	192	244	436	17	60
QFMD[c]	1280	480	1:2	1:4	0	4	13	192	140	332	17	60
HF[d]	1280	240	1:2	1:8	0	4	13	192	88	280	17	120

a. $HB2 = H_{BLANK} - HB1$

b. Frame Rate listed is based on 48MHz internal system clock

c. VGA (640x480) is derived from QFMD with 2:1 times skip/average in horizontal direction to get 60fps based on 24MHz PCLK (48MHz/2)

d. QVGA (320x240) is derived from HF with 4:1 times skip/average in horizontal direction to get at 120fps based on 12MHz PCLK (48MHz/4)

Figure 17 Snapshot Mode Timing with EXP_STB Asserted

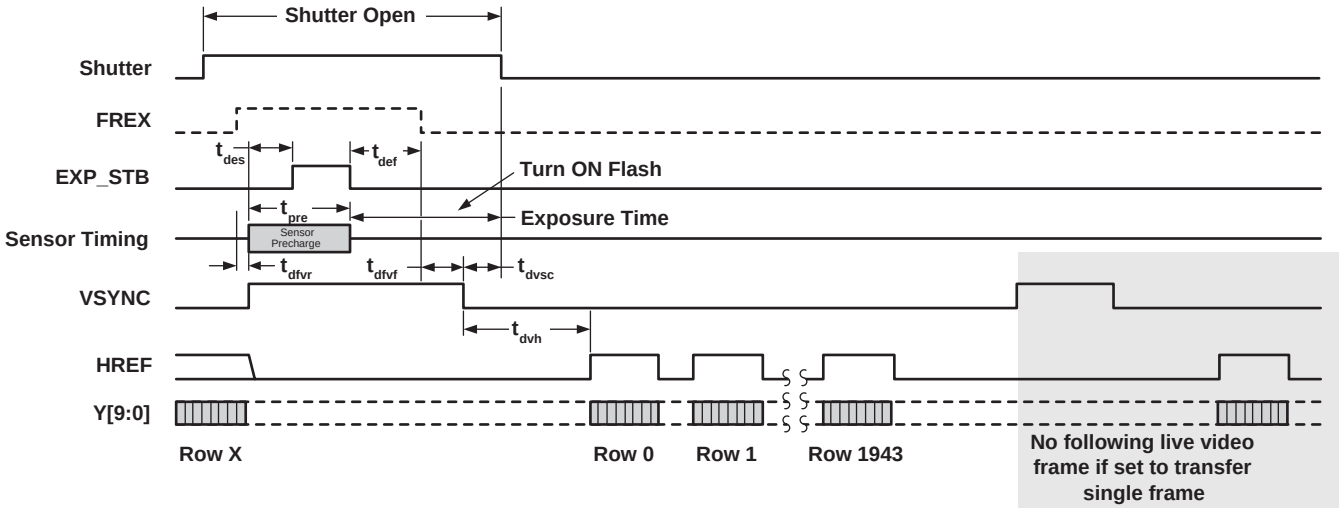


Table 10 Snapshot Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		3252 (QSXGA)		tp
tdfvr	8		9	tp
tdfvf		8		tline
tdvsc			2	tline
tdvh		17 (QSXGA)		tline
tdhso	0			ns
tdef	20			tp
tdes			230 (QSXGA)	tp

NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
2) Shutter must be closed no later then 6000 tp after VSYNC falling edge.

Register Set

Table 11 provides a list and description of the Device Control registers contained in the OV5620. The device slave addresses for the OV5620 are 60 for write and 61 for read.

Table 11 Device Control Register List (Sheet 1 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7]: Reserved - must be set to "0" Bit[6:0]: Gain setting • Range: 1x to 16x Gain = (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) ***Note:*** *Set COM8[2] = 0 to disable AGC.*
01	BLUE	80	RW	Digital AWB Blue Gain Control • Range: 0 to 4x ([00] to [FF])
02	RED	80	RW	Digital AWB Red Gain Control • Range: 0 to 4x ([00] to [FF])
03	COM1	4A	RW	Common Control 1 Bit[7:6]: Dummy frame control 00: Not used 01: Allow 1 dummy frame 10: Allow 3 dummy frames 11: Allow 7 dummy frames Bit[5:4]: Reserved Bit[3:2]: Vertical window end line control 2 LSBs Bit[1:0]: Vertical window start line control 2 LSBs
04	REG04	00	RW	Register 04 Bit[7]: Horizontal mirror Bit[6]: Vertical flip Bit[5:3]: Reserved Bit[2:0]: AEC lower 3 bits – AEC[2:0]
05-08	RSVD	XX	–	Reserved
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Sleep mode enable 0: Normal mode 1: Sleep mode Bit[3]: Reserved Bit[2]: Pins PWDN and RESET_B used as SLVS and SLHS, respectively Bit[1:0]: Output drive current select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PIDH	56	R	Product ID Number MSB (Read only)
0B	PIDL	20	R	Product ID Number LSB (Read only)

Table 11 Device Control Register List (Sheet 2 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	COM3	08	RW	Common Control 3 Bit[7]: Array horizontal output size select 0: 1280, if COM4[7] = 1; 864, if COM4[0] = 1; otherwise, 2592 1: 1280, if in 1.3 Mpixel, QFMD, or HF mode; 864, if in D1MD mode; otherwise, 2592 Bit[6]: Array vertical skip mode select 0: Skip 2, if COM4[6] = 1; skip 3, if COM4[5] = 1; skip 4, if COM4[4] = 1; skip 8, if COM4[3] = 1; otherwise, no skip or full mode 1: Skip 2, if in 1.3 Mpixel mode; skip 3, if in D1MD mode; skip 4, if in QFMD mode; skip 8, if in HF mode; otherwise, no skip or full mode Bit[5:4]: Reserved Bit[3]: Number of vertical blanking line select 0: 24 lines, if in full mode; 16, if in 1.3 Mpixel, D1MD, QFMD, or HF mode 1: Full mode: DMLN > 24: determined by DMLN DMLN ≤ 24: 24 lines 1.3 Mpixel/D1MD/QFMD/HF: DMLN > 16: determined by DMLN DMLN ≤ 16: 16 lines ***Note:*** *DMLN is set by registers {DMLNH[7:0] (0x47), DMLNL[7:0] (0x46)}* Bit[2]: Array vertical output size select 0: Full mode: 1944 1.3 Mpixel: 960 D1MD: 600 QFMD: 480 HF: 240 1: Output size determined by registers COM32[7:0] and COM30[5:4] Output size = 2 x {COM32[7:0], COM30[5:4]} Bit[1]: Number of horizontal blanking line select 0: Full mode: 660 1.3 Mpixel: 360 D1MD: 436 QFMD: 332 HF: 280 1: Determined by register EXHC[11:0] ***Note:*** *EXCH[11:0] is set by registers {REG2A[7:4] (0x2A), EXHCL[7:0] (0x2B)}* Bit[0]: Array horizontal output size select 0: Full mode: 1944 1.3 Mpixel: 960 D1MD: 600 QFMD: 480 HF: 240 1: Output size is determined by COM31[7:0] and COM30[2:0] Output size = 2 x {COM31[7:0], COM30[2:0]}

Table 11 Device Control Register List (Sheet 3 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0D	COM4	06	RW	Common Control 4 Bit[7:3]: Reserved Bit[2]: Clock output power-down pin status 0: Tri-state data output pin at power-down 1: Data output pin hold at last status before power-down Bit[1]: Data output pin status selection at power-down 0: Tri-state data VSYNC, PCLK, HREF, and CHSYNC pins upon power-down 1: VSYNC, PCLK, HREF, and CHSYNC pins hold on last state before power-down Bit[0]: Reserved
0E	COM5	01	RW	Common Control 5 Bit[7:0]: Reserved
0F	COM6	43	RW	Common Control 6 Bit[7:2]: Reserved Bit[1]: Reset enable/disable when sensor working mode changes 0: Sensor timing does not reset when mode changes 1: Sensor timing resets when mode changes Bit[0]: Reserved
10	AEC	63	RW	Automatic Exposure Control - AEC[10:3] 6 MSBs (AEC[16:11]) are in register REG45[5:0] and 3 LSBs (AEC[2:0]) are in register REG04[2:0]). AEC[16:0] - Exposure time $T_{EX} = t_{LINE}$ x AEC[16:0] ***Note:*** *The maximum exposure time is 1 frame period even if T_{EX} is longer than 1 frame period*
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Reserved Bit[6]: System clock divider enable 0: Clock from PLL output 1: Enable system clock divider Bit[5:0]: Clock divider If CLKRC[5:0] = 0, then CLK = PLL CLK / 2 If CLKRC[5:0] ≠ 0, then CLK = PLL CLK / [(decimal value of CLKRC[5:0] + 1) x 2]

Table 11 Device Control Register List (Sheet 4 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COM7	00	RW	Common Control 7 Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6:3]: Resolution selection 0000: 5 Mpixel (full size) mode - no binning 0001: HF mode - 1:8 binning 0010: QFMD mode - 1:4 binning 0100: D1MD mode - 1:3 binning 1000: 1.3 Mpixel mode - 1:2 binning Bit[2:0]: Reserved
13	COM8	C7	RW	Common Control 8 Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6:3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14	COM9	40	RW	Common Control 9 Bit[7:5]: AGC gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: Reserved 101: Reserved 110: Reserved 111: Reserved Bit[4:3]: Reserved Bit[2]: VSYNC drop option 0: VSYNC is always output 1: VSYNC is dropped if frame data is dropped Bit[1]: Frame data drop 0: Disable data drop 1: Drop frame data if exposure is not within tolerance. In AEC mode, data is normally dropped when data is out of range. Bit[0]: Reserved

Table 11 Device Control Register List (Sheet 5 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COM10	00	RW	Common Control 10 Bit[7:6]: Reserved Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK edge selection 0: Data is updated at the failing edge of PCLK (user can latch data at the next rising edge of PCLK) 1: Data is updated at the rising edge of PCLK (user can latch data at the next falling edge of PCLK) Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for valid data Bit2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
16	GREEN	80	RW	Digital AWB Green Gain Control • Range: 0 to 4x ([00] to [FF])
17	HREFST	12	RW	Horizontal Window Start 8 MSBs (3 LSBs in REG32[2:0]) Bit[10:0]: Select beginning of horizontal window, each LSB represents two pixels
18	HREFEND	B4 in 1.3 Mp	RW	Horizontal Window End 8 MSBs (3 LSBs in REG32[5:3] Bit[10:0]: Select end of horizontal window, each LSB represents two pixels
19	VSTRT	01 in 1.3 Mp	RW	Vertical Window Line Start 8 MSBs (2 LSBs in register COM1[1:0]) Bit[9:0]: Selects the start of the vertical window, each LSB represents two scan lines.
1A	VEND	F4 in 1.3 Mp	RW	Vertical Window Line End 8 MSBs (2 LSBs in register COM1[3:2]) Bit[9:0]: Selects the end of the vertical window, each LSB represents two scan lines.
1B	PSHFT	00	RW	Pixel Shift Bit[7:0]: Pixel delay count - provides a method to fine tune the output timing of the pixel data relative to the HREF pulse. It physically shifts the video data output time in units of pixel clock counts. The largest delay count is [FF] and is equal to 255 x PCLK.
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-23	RSVD	XX	–	Reserved

Table 11 Device Control Register List (Sheet 6 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC operation AEC/AGC value decreases in auto mode when average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC operation AEC/AGC value increases in auto mode when average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]
27-29	RSVD	XX	–	Reserved
2A	REG2A	00	RW	Register 2A Bit[7:4]: 4 MSBs of EXHC (8 LSBs in register EXHCL[7:0]) Bit[3:2]: HSYNC timing end point adjustment 2 MSBs Bit[1:0]: HSYNC timing start point adjustment 2 MSBs
2B	EXHCL	00	RW	8 LSBs of EXHC - pixel count in horizontal blank (valid only when COM3[1] = 1)
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width 8 LSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse Width 8 MSBs Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average - this register will auto update
30	HSDY	08	RW	HSYNC Position and Width Start 8 LSBs This register and register REG2A[1:0] define the HSYNC start position. Each LSB will shift HSYNC starting point by a 2 pixel period.
31	HEDY	30	RW	HSYNC Position and Width End 8 LSBs This register and register REG2A[3:2] define the HSYNC end position. Each LSB will shift HSYNC end point by a 2 pixel period.
32	REG32	00 in 1.3 Mp	RW	Register 32 Bit[7:6]: Pixel clock divide option 00: No effect on PCLK 01: No effect on PCLK 10: PCLK frequency divide by 2 11: PCLK frequency divide by 4 Bit[5:3]: Horizontal window end position 3 LSBs Bit[2:0]: Horizontal window start position 3 LSBs

Table 11 Device Control Register List (Sheet 7 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
33-44	RSVD	XX	–	Reserved
45	REG45	00	RW	Register 45 Bit[7:6]: AGC[9:8], AGC 2 MSBs Bit[5:0]: AEC[15:10], AEC 6 MSBs
46	DMLNL	00	RW	Number of Vertical Blanking Lines LSBs
47	DMLNH	00	RW	Number of Vertical Blanking Lines MSBs
48	ZOOMSL	00	RW	Common Control 19 Bit[7:2]: Reserved Bit[1:0]: Zoom mode vertical start window 2 LSBs (see register ZOOMSH[7:0] (0x49) for 8 MSBs)
49	ZOOMSH	00	RW	Zoom Mode Vertical Window Start Point 8 MSBs
4A-5E	RSVD	XX	–	Reserved
5F	COM30	00	RW	Common Control 30 Bit[7:6]: Reserved Bit[5:4]: Array vertical output size (valid only when COM3[2] = 1) Bit[3]: Reserved Bit[2:0]: Array hoizontal output size (valid only when COM3[0] = 1)
60	COM31	00	RW	Common Control 31 Bit[7:0]: Array horizontal output size (valid only when COM3[0] = 1)
61	COM32	00	RW	Common Control 32 Bit[7:0]: Array vertical output size (valid only when COM3[2] = 1)
62	RSVD	XX	–	Reserved
63	COM34	00	RW	Common Control 34 Bit[7]: Reserved Bit[6]: De-noise enable 0: Disable 1: Enable Bit[5]: Strength of de-noise select 0: DNSTH x 1 1: DNSTH x 4 Bit[4:0]: De-noise threshold setting
64-7F	RSVD	XX	–	Reserved

Table 11 Device Control Register List (Sheet 8 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
80	DSPEN	01	RW	DSP Function Enable Control Bit[7:5]: Reserved Bit[4]: Color bar enable 0: Disable 1: Enable Bit[3:2]: Reserved Bit[1]: Raw data output select 0: Raw data after CIP 1: Raw data before CIP Bit[0]: New CIP enable 0: Disable 1: Enable
81	DSP01	00	RW	DSP01 Bit[7:4]: Reserved .Bit[3]: WBC delay option when DSP01[1] and DSP01[2] are disabled 0: Do not delay 1: Delay output Bit[2]: Black pixel canceling enable 0: Disable 1: Enable Bit[1]: White pixel canceling enable 0: Disable 1: Enable Bit[0]: White and black pixel canceling enable 0: Disable 1: Enable
82	RSVD	XX	–	Reserved
83	DGCTRL	80	RW	Digital Gain Control Bit[7:2]: Reserved Bit[1:0]: Digital gain select 00: 1x 01: 2x 10: 4x 11: 4x
84	AWBBIAS	00	RW	AWB Gain Bias Setting
85	DSPCTRL	00	RW	DSP Control Bit[7:0]: Reserved
86-88	RSVD	XX	–	Reserved
89	DSP09	29	RW	DSP09 Bit[7:6]: Reserved Bit[5]: AWB gain enable 0: Disable 1: Enable Bit[4:0]: Reserved

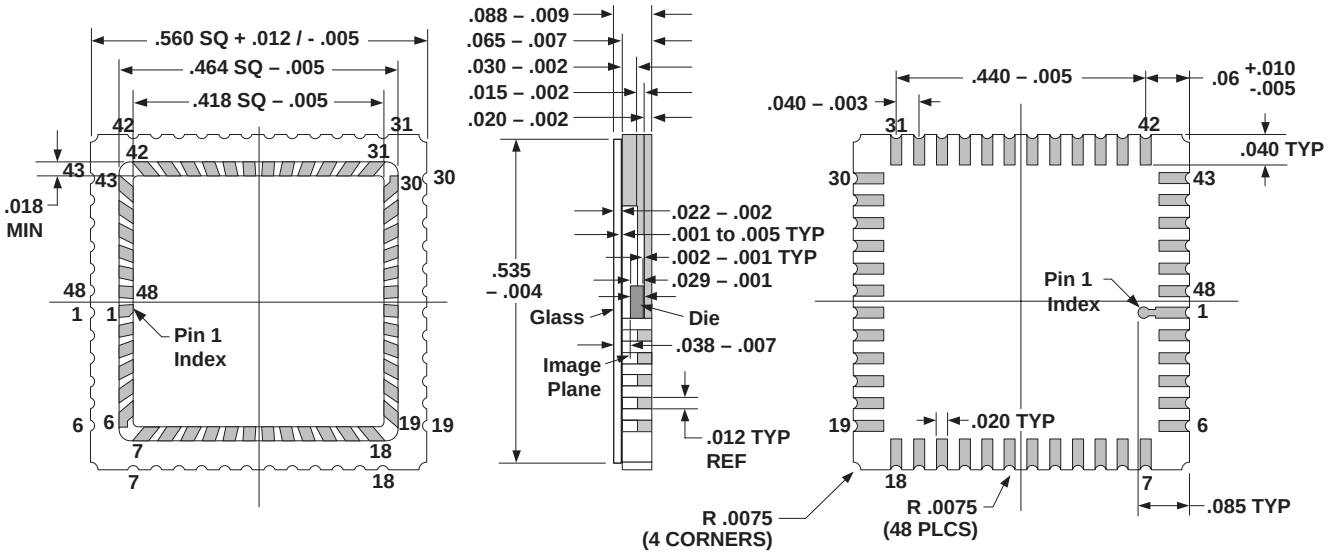
Table 11 Device Control Register List (Sheet 9 of 9)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
8A	RSVD	XX	–	Reserved
8B	DSP0B	1F	RW	DSP0B Bit[7:6]: Reserved Bit[5]: Gamma enable 0: Disable 1: Enable Bit[4:0]: Reserved
8C-A7	RSVD	XX	–	Reserved
A8	BOTLMT	10	RW	Pixel Value Lower Limit
A9	TOPLMT	F0	RW	Pixel Value Upper Limit
AA-B7	RSVD	XX	–	Reserved
B8	REDLMT	F0	RW	Red Gain Limit Bit[7:4]: Red gain upper limit Value = bit[7:4] x 16 + 15 Bit[3:0]: Red gain lower limit Value = bit[3:0] x 16
B9	GREENLMT	F0	RW	Green Gain Limit Bit[7:4]: Green gain upper limit Value = bit[7:4] x 16 + 15 Bit[3:0]: Green gain lower limit Value = bit[3:0] x 16
BA	BLUELMT	F0	RW	Blue Gain Limit Bit[7:4]: Blue gain upper limit Value = bit[7:4] x 16 + 15 Bit[3:0]: Blue gain lower limit Value = bit[3:0] x 16
BB-F6	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV5620 uses a 48-pin ceramic package. Refer to Figure 18 for package information and Figure 19 for the array center on the chip.

Figure 18 OV5620 Package Specifications



NOTES:

1. ALL EXPOSED METALLIZED AREAS SHALL BE GOLD-PLATED 0.50 m MIN. THK. OVER NICKEL PLATE UNLESS OTHERWISE SPECIFIED IN PURCHASE ORDER.
2. SEAL AREA AND DIE ATTACH AREA SHALL BE WITHOUT METALLIZATION.

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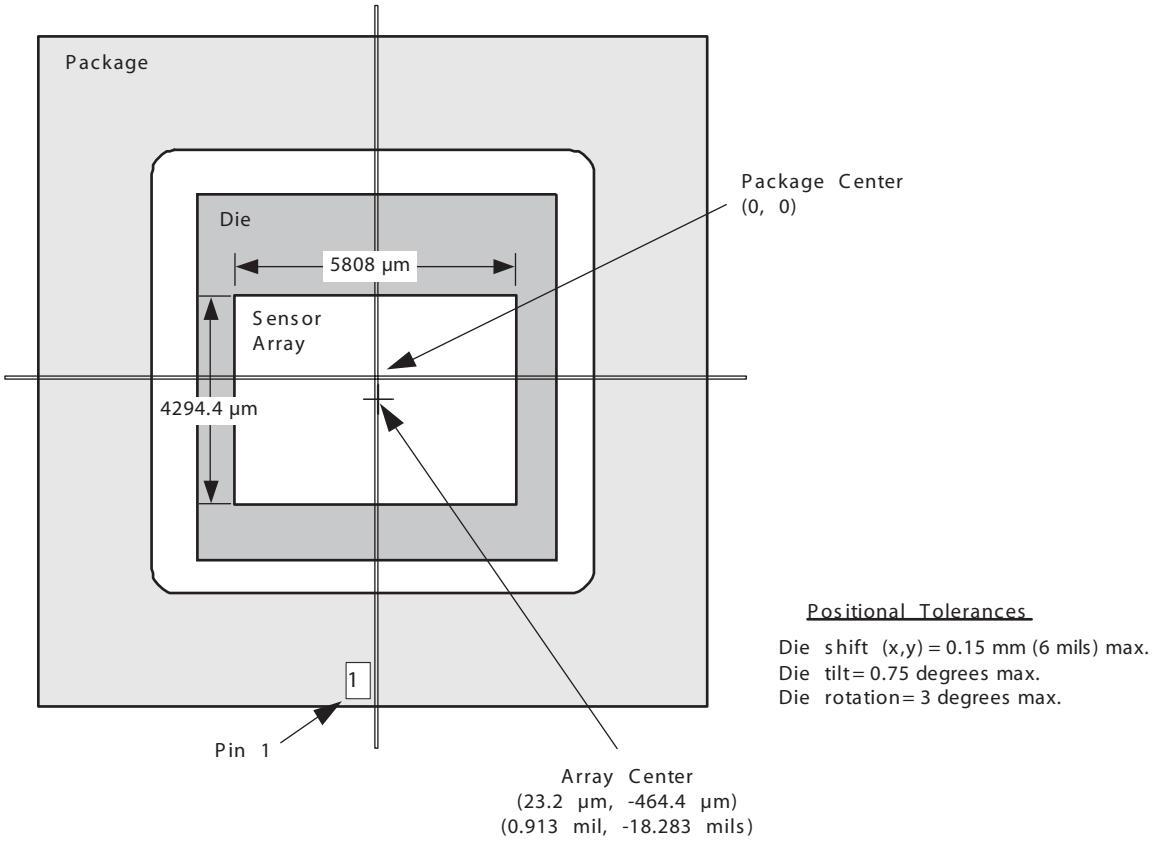
Table 12 OV5620 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 +0.30 / -0.13 SQ	.560 +.012 / -.005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Base Height	0.51 ± 0.05	.020 ± .002
Cavity Size	10.62 ± 0.13 SQ	.418 ± .005 SQ
Castellation Height	1.14 ± 0.14	.045 ± .006
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.18	.040 ± .003
Package Edge to First Lead Center	1.52 +0.26 / -0.13	.06 +.010 / -.005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	13.6 ± 0.1 SQ	.535 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002
Die Thickness	0.733 ± 0.015	.029 ± .001
Top of Glass to Image Plane	0.95 ± 0.18	.037 ± .007
Substrate Height	1.65 ± 0.18	.065 ± .007

Sensor Array Center

Figure 19 OV5620 Sensor Array Center



Important: Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 (DOVDD) down as shown.

NOTE: Picture is for reference only, not to scale.

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The recommended lens chief ray angle for the OV5620 is 12.5° degrees.

IR Reflow Ramp Rate Requirements

OV5620 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 20 IR Reflow Ramp Rate Requirements

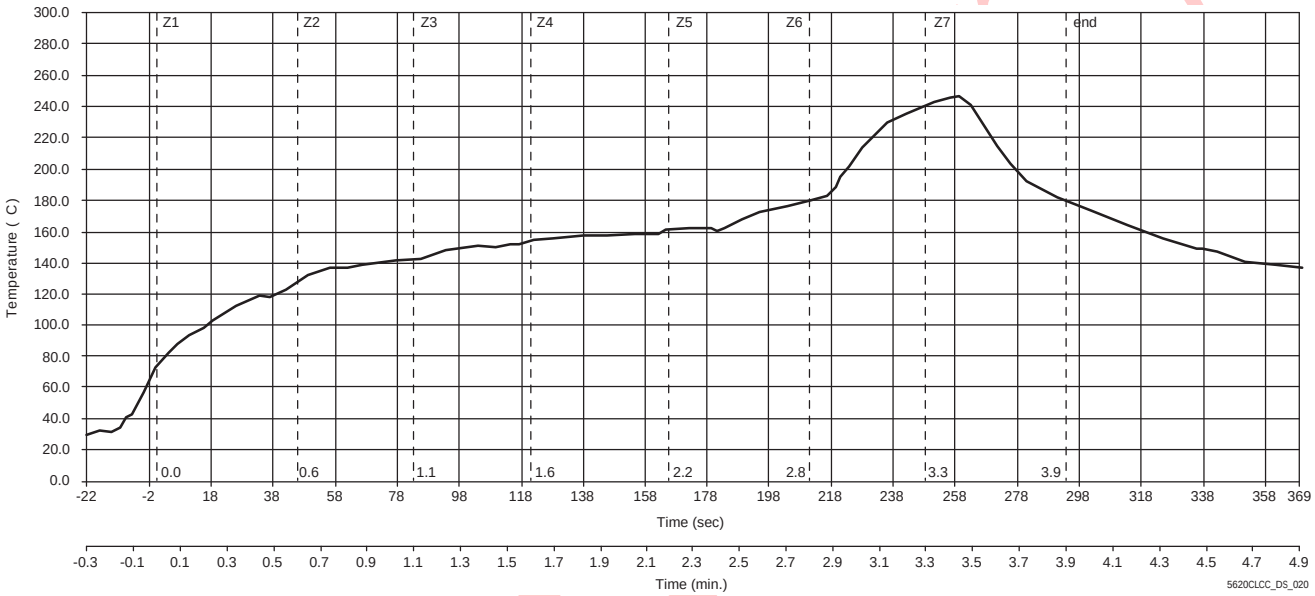

Table 13 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV5620 (CLCC) Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

- Initial Release

REVISION CHANGE LIST

Document Title: OV5620 (CLCC) Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.0:

- Under Features on page 1, deleted (previously 11th) bulleted item “Vertical VarioPixel® (binning) 1:2, 1:3
- Under Featuress on page 1, changed 10th bulleted item from “Horizontal VarioPixel® (binning) 1:2, 1:3, 1:4, 1:8” to “VarioPixel® (binning) 1:2, 1:3, 1:4”
- Under Features on page 1, changed 11th bulleted item from “Vertical skip 1:2, 1:3, 1:4, 1:8” to “Subsampling (skip) 1:2, 1:3, 1:4, 1:8”
- Moved section title “Horizontal VarioPixel/Binning 1:2, 1:3” to page 4 and changed it to “VarioPixel (Binning) 1:2, 1:3, 1:4”
- On page 4, deleted section title “Vertical VarioPixel/Binning 1:2, 1:3”
- On page 4, deleted “Horizontal 1:2 Skip” figure (previously Figure 8)
- Under General Description on page 1, changed the second line in the second paragraph from “...can also output 864 x 648 ...” to “...can also output 864 x 600 ...”
- Under Key Specifications on page 1, changed Digital Power Supply specification from “1.2V $\pm$ 5%” to “1.3V $\pm$ 5%”
- Under Key Specifications on page 1, changed Standby Power Requirements from “<10 µA” to “250 µA”
- Under Key Specifications on page 1, corrected Shutter specification from “Electronic rolling shutter, snapshort” to “Electronic rolling shutter, snapshot”
- Under Key Specifications on page 1, changed specification for Lens Chief Ray Angle from “TBD” to “12.5°”
- Under Key Specifications on page 1, changed Max Image Transfer Rate parameter from “SXGA” to “1.3 Mpixel”, from “D1” to “D1MD”, and from “HF” to “QVGA”
- In Figure 1 on page 1, changed OV5620 chip so that pin 1 is down
- Under Gain Control subsection on page 3, changed the last line from “The gain adjustment range 0-42 dB” to “The gain adjustment range is 0-24 dB”
- On page 4, deleted section title “Vertical Skip 1:2, 1:3, 1:4, 1:8”
- On page 4, deleted “Vertical 1:2 Skip” figure (previously Figure 9), “Vertical 1:3 Skip” figure (previously Figure 10), “Vertical 1:4 Skip” figure (previously Figure 11), and “Vertical 1:8 Skip” figure (previously Figure 12)
- On page 4, added Figure 8 “Horizontal 1:4 Average (Binning)” and Figure 9 “Vertical 1:4 Average (Binning)”
- Under Frame Rate Adjust on page 5, changed first line from “The OV5620 offers three methods ...” to “The OV5620 offers four methods ...”

DESCRIPTION OF CHANGES (CONTINUED)

- Under Frame Rate Adjust on page 5, changed the last line of the first bulleted item from "... of the input clock rate" to "... of the PLL output clock"
- Under Frame Rate Adjust on page 5, changed first line of the second bulleted item from "By adding a dummy pixel timing in ..." to "By changing horizontal blank timing in ..."
- Under Frame Rate Adjust on page 5, added "... or after the active lines (see "DMLNL" on page 21 and "DMLNH" on page 21")" to first line of third bulleted item
- Under Frame Rate Adjust on page 5, added a fourth bulleted item of "PLL control: Supports more flexible clock control"
- In the Notes for Figure 10 on page 5, changed note 2 from " T_{line} = 3000 x T_{clk} (QSXGA); T_{line} = 1632 x T_{clk} (SXGA)" to "T_{line} = 3252 x T_{clk} (QSXGA); T_{line} = 1640 x T_{clk} (1.3 Mpixel)"
- In the Notes for Figure 10 on page 5, changed note 3 from "T_{frame} = 2000 x T_{line} (QSXGA); T_{frame} = 980 x T_{line} (SXGA)" to "T_{frame} = 1968 x T_{line} (QSXGA); T_{frame} = 976 x T_{line} (1.3 Mpixel)"
- Under Power Down Mode on page 5, changed first line of the first bulleted item from "... high (+3.3VDC)..." to "... high (DOVDD)..."
- Under Power Down Mode on page 5, changed last line of the second bulleted item from "The current draw is less than 10 µA in this standby mode" to "The current draw is less than 250 µA in this standby mode"
- In Line/Pixel Timing section on page 6, changed the last paragraph from "The specification shown in Table 8 apply for DVDD = +1.2 V, ..." to "The specification shown in Table 8 apply for DVDD = +1.3 V, ..."
- In Table 2 on page 7, changed description of pin 1 from "Power for I/O circuit (1.8V to 3.3V)" to "Power for I/O circuit (1.7V to 3.3V)"
- In Table 2 on page 7, deleted "(1.8V to 3.3V)" from the description of pin 28
- In Table 2 on page 8, changed description of pin 33 from "... or digital power (1.2V)" to "... or digital power (1.3V)"
- In Table 4 on page 9, changed Min, Typ, and Max for Supply voltage (DVDD) (V_{DD3}) from "1.14", "1.2", and "1.26" to "1.24", "1.3", and "1.37", respectively
- In Figure 16 on page 13, added callout for V_{SYNC} and changed Note 4
- In Table 9 on page 13, added columns for VB2, V_{SYNC}, VB1, HB1, and HB2
- In Table 9 on page 13, changed Formats "XGA" and "AFMD" to "1.3Mpixel" and "HF", respectively
- In Table 9 on page 13, changed Frame Rate of HF (previously AFMD) from "60" to "120"
- In Figure 17 on page 14, deleted "t_{dhv}"
- In Table 10 on page 14, deleted rows for "tvs" and "tdhv"
- In Table 10 on page 14, changed Typ for tline from "3000 (QSXGA)" to "3252 (QSXGA)"
- In Table 10 on page 14, deleted Max for tdfvf and added Typ spec of "8"

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 10 on page 14, changed Typ for tdvh from “18268 (QSXGA)” to “17 (QSXGA)” and changed Unit from “tp” to “tline”
- In Table 10 on page 14, changed Max for tdes from “2500 (QSXGA)” to “230 (QSXGA)”
- In Table 11 on page 15. changed description of register GAIN (0x00) from:

  AGC Gain Control

  Bit[7:0]: Gain setting
  - Range: 1x to 32x

  Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16)

  Note: *Set COM8[2] = 0 to disable AGC.*

  to:

  AGC Gain Control

  Bit[7]: Reserved - must be set to “0”

  Bit[6:0]: Gain setting
  - Range: 1x to 16x

  Gain = (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16)

  Note: *Set COM8[2] = 0 to disable AGC.*
- In Table 11 on page 15, changed description of register BLUE (0x01) from “Range: 0 to 4x ([00] to [44])” to “Range: 0 to 4x ([00] to [FF])”
- In Table 11 on page 15, changed description of register RED (0x02) from “Range: 0 to 4x ([00] to [44])” to “Range: 0 to 4x ([00] to [FF])”
- In Table 11 on page 16, changed description for register bit COM3[7] from:

  Bit[7]: Array horizontal output size select (excluding crop mode)

  to:

  Bit[7]: Array horizontal output size select
- In Table 11 on page 16, changed description for register bit COM3[6] from:

  Bit[6]: Array vertical skip mode select (excluding crop mode)

  0: Skip 2 (output size = 960), if COM4[6] = 1;
  skip 3 (output size = 600), if COM4[5] = 1;
  skip 4 (output size = 480), if COM4[4] = 1;
  skip 8 (output size = 240), if COM4[3] = 1;
  otherwise, no skip or full mode (output size = 1944)

  1: Skip 2 (output size = 960), if in XGA mode;
  skip 3 (output size = 600), if in D1MD mode;
  skip 4 (output size = 480), if in QFMD mode;
  skip 8 (output size = 240), if in AFMD mode;
  otherwise, no skip or full mode (output size = 1944)

  to:

  Bit[6]: Array vertical skip mode select

  0: Skip 2, if COM4[6] = 1;
  skip 3, if COM4[5] = 1;
  skip 4, if COM4[4] = 1;
  skip 8, if COM4[3] = 1;
  otherwise, no skip or full mode

  1: Skip 2, if in 1.3 Mpixel mode;
  skip 3, if in D1MD mode;
  skip 4, if in QFMD mode;
  skip 8, if in HF mode;
  otherwise, no skip or full mode

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 11 on page 16, changed description for register bit COM3[3] from:

  Bit[3]: Number of vertical blanking line select (excluding crop mode)
  - 0: 24 lines, if in full mode;
    16, if in XGA, D1MD, QFMD, or AFMD mode
  - 1: 24 lines, if in full mode; less than 24lines, if register DMLN is less than 24; otherwise, number of blanking lines is determined by register DMLN

  16 lines, if in XGA, D1MD, QFMD, or AFMD mode;
  less than 16 lines, if register DMLN is less than 16; otherwise, number of blanking lines is determined by DMLN

  to:

  Bit[3]: Number of vertical blanking line select
  - 0: 24 lines, if in full mode;
    16, if in 1.3 Mpixel, D1MD, QFMD, or HF mode
  - 1: Full mode:

    DMLN > 24: determined by DMLN

    DMLN ≤ 24: 24 lines

    1.3Mpixel/D1MD/QFMD/HF:

    DMLN > 16: determined by DMLN

    DMLN ≤ 16: 16 lines

- In Table 11 on page 16, changed description for register bit COM3[2] from:

  Bit[2]: Array vertical output size select (excluding crop mode)
  - 0: 1944, if in full mode; 960, if in XGA mode; 600, if in D1MD mode; 480, if in QFMD mode; 240, if in AFMD mode
  - 1: Output size determined by registers COM32[7:0] and COM30[5:4]
    Output size = 2 x {COM32[7:0], COM30[5:4]}

  to:

  Bit[2]: Array vertical output size select
  - 0: Full mode: 1944
    1.3 Mpixel: 960
    D1MD: 600
    QFMD: 480
    HF: 240
  - 1: Output size determined by registers COM32[7:0] and COM30[5:4]
    Output size = 2 x {COM32[7:0], COM30[5:4]}

- In Table 11 on page 16, changed description for register bit COM3[1] from:

  Bit[1]: Number of horizontal blanking line select (excluding crop mode)
  - 0: 660, if in full mode; 360, if in XGA mode; 436, if in D1MD mode; 280, if in AFMD mode
  - 1: Determined by register EXHC[11:0]

  to:

  Bit[1]: Number of horizontal blanking line select
  - 0: Full mode: 660
    1.3 Mpixel: 360
    D1MD: 436
    QFMD: 332
    HF: 280
  - 1: Determined by register EXHC[11:0]

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 11 on page 16, changed description for register bit COM3[0] from:

  Bit[0]: Array horizontal output size select (excluding crop mode)
  - 0: 1944, if in full mode; 960, if in XGA mode; 600, if in D1MD mode; 480, if in QFMD mode; 240, if in AFMD mode
  - 1: Output size is determined by COM31[7:0] and COM30[2:0]
    Output size = 2 x {COM31[7:0], COM30[2:0]}

  to:

  Bit[0]: Array horizontal output size select
  - 0: Full mode: 1944
    1.3 Mpixel: 960
    D1MD: 600
    QFMD: 480
    HF: 240
  - 1: Output size is determined by COM31[7:0] and COM30[2:0]
    Output size = 2 x {COM31[7:0], COM30[2:0]}

- In Table 11 on page 18, changed description of register bits COM9[7:5] (0x14) from:

  Bit[7:5]: AGC gain ceiling
  - 000: 2x
  - 001: 4x
  - 010: 8x
  - 011: 16x
  - 100: 32x
  - 101: Reserved
  - 110: Reserved
  - 111: Reserved

  to:

  Bit[7:5]: AGC gain ceiling
  - 000: 2x
  - 001: 4x
  - 010: 8x
  - 011: 16x
  - 100: Reserved
  - 101: Reserved
  - 110: Reserved
  - 111: Reserved

- In Table 11 on page 20, added "- pixel count in horizontal blank valid only when Reg0C[1] = 1" to description of register EXHCL (0x2B)
- In Table 11 on page 20, changed description for register ADDVSL[7:0] from:

  VSYNC Pulse Width 8 LSBs

  Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 2 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.

  to:

  VSYNC Pulse Width 8 LSBs

  Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.

- In Table 11 on page 21, deleted row for register ZOOMW (0x34)
- In Table 11 on page 21, changed addresses for RSVD from "35-44" to "34-44"
- In Table 11 on page 22, changed description of register bit DSPEN[7] (0x80) to "Reserved"
- In Table 11 on page 23, changed address for RSVD row from "BB-DF" to "BB-F6"
- In Table 11 on page 23, deleted rows for registers E0 to F6
- In Figure 19 on page 25, changed orientation of OV5620 chip so pin 1 is down