Qualcomm Technologies, Inc.

SMB1350/SMB1351

Device Specification

80-NL405-1 Rev. F

October 26, 2015

For additional information or to submit technical questions go to https://createpoint.qti.qualcomm.com/

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Revision history

Revision	Date	Description
A	May 2014	Initial release

B	August 2014	▪ Section 1.1 Document overview: Added section and Table 1-1 Primary SMB1350/SMB1351 documentation
		▪ Table 3-1 Pin description:
		  ▫ Updated pin description for pin 37
		  ▫ Updated pin name and description for pin 31
		▪ Table 4-3 DC operating characteristics:
		  ▫ Added R_{DSON} under battery charger
		  ▫ Changed min and max for I_{FCHG}
		  ▫ Added APSD to FlexCharge
		▪ Table 4-4: Added watchdog and charger hold off specification
		▪ Table 5-1 Split into three tables; Table 5-1, Table 5-2, and Table 5-3
		▪ Table 5-1 Configuration registers 00h–14h: Updated
		  ▫ Address 01h precharge current, termination current, and USB5/1 command polarity
		  ▫ Address 02h suspend mode control, not used, AICL, 5.0 V AICL detect threshold, and battery OV
		  ▫ Address 04h current termination, not used, and TurboCharge+
		  ▫ Address 06h USB fail low
		  ▫ Address 07h load battery with 10 mA during float voltage compensation and thermistor monitor
		  ▫ Address 08h not used
		  ▫ Address 0Ah OTG current limit at DCIN
		  ▫ Address 0Ch and 0Dh all sections
		  ▫ Address 10h charger configuration
		  ▫ Address 11h timeout select for APSD, SDP suspend, not used, and DCD
		  ▫ Address 13h VBATT low disabled or reset state and not used
		  ▫ Address 14h all sections
		▪ Table 5-2 Nonvolatile registers 15h–16h (read only): Modified nonvolatile register access
		  ▫ Address 15h SYSOK pin configuration
		  ▫ Address 16h volatile writes permission
		▪ Table 5-3 Command and status registers 30h–46h: Updated table
		▪ Section 7.1.14 EN input: Updated description
		▪ Section 7.1.15 Status and interrupt:
		  ▫ Removed second status/IRQ list
		  ▫ Added SMB1350/SMB1351 includes a register bank that will indicate various conditions and activate an interrupt (IRQ) output and/or status bit. The IRQ signal is a latched condition and is initiating pulses for 0.6 ms every 350 ms at the STAT output pin. All IRQ signals are cleared by reading the corresponding status register. Interrupt signals generated because of a charge error or the collapse of the input voltage are cleared by disabling charging.
		  ▫ Table 5-3 Status and IRQ register
		▪ Table 7-10 Adapter input current limit mapping: Added table
		▪ Section 8.2 Inductor: Added link to comment for layout guidelines

Revision	Date	Description

C	December 2014	▪ Table 1-1 Primary SMB1350/SMB1351 documentation: Added *SMB1350/SMB1351 Device Revision Guide* (80-NL405-4) and removed TBD
		▪ Figure 2-2 USB adapter charging algorithm with TurboCharge: Updated figure
		▪ Table 4-2 Recommended operating conditions: Added note on about 3 MHz operation is not supported above the 9 V operating range.
		▪ Table 5-1 Configuration registers 00h – 14h:
		  ▫ Changed “AICL done” to “AICL failed”
		  ▫ Changed “active low” to “normal output” and “active high” to “invert output”
		  ▫ Table 5-3 Command and status registers 30h–46h:
		  ▫ Changed “fast charge status” to “unused” and “hard limit status” to “unused”
		  ▫ Changed “AICL done” to “AICL failed”
		  ▫ Table 7-2 Charge configuration: Added table
		▪ Added more details to the descriptions for the following sections:
		  ▫ 7.1.3 Prequalification mode
		  ▫ 7.1.5 Precharge mode
		  ▫ 7.1.6 Fast charge mode
		  ▫ 7.1.7 Constant voltage mode
		  ▫ 7.1.8 Charge completion
		  ▫ 7.1.9 Automatic battery recharge
		  ▫ 7.1.10 Charger inhibit
		  ▫ 7.1.12 Watchdog timer
		  ▫ 7.1.13 STAT output
		  ▫ 7.1.14 EN input
		  ▫ 7.1.16 USB OTG mode
		  ▫ 7.1.17 Hard thermal monitor
		  ▫ 7.1.20 Automatic power source detection
		  ▫ 7.1.23 Power source detection
		  ▫ 7.1.24 USB dead battery charging
		  ▫ 7.1.26 Programmable battery charging
		  ▫ 7.1.30 OptiCharge (AICL) mode
		  ▫ 7.1.31 INOK/SYSOK/CHG_DET_N output
		  ▫ 7.1.40 BMS integration
		▪ Table 7-2 Charge configuration: Changed “AICL done” to “AICL fail” and updated definition
		▪ Table 7-5 USB charging specification: Added table
		▪ Table 7-6 PGOOD polarity: Added table

Revision	Date	Description

D	April 2015	▪ Updated Figure 2-1
		▪ Modified max peak current on Table 4-1 in terms of DC current and added note regarding DC current and peak current limit
		▪ Updated Table 4-3 based on characterization data
		▪ Updated Table 5-2
		▪ Updated Table 5-3
		▪ Added Section 6.4
		▪ Added Section 7.1.40
		▪ Updated Section 8.1 with new descriptions and recommendations
		▪ Added Section 8.2 for PMUX support
		▪ Added Figure 8-1 to board layout section
		▪ Updated Chapter 9
		▪ Added Chapter 11
		▪ Global changes:
		  ▫ Replaced the 900 mA setting with 685 mA
		  ▫ Added a description for PGOOD programmability for INOK and SYSOK options
		  ▫ Updated the SYSON operation description
		  ▫ Improved SUSP/SHDN function and the pin description
		  ▫ Updated the VDP_UP min and max specification
		  ▫ Updated the Qualcomm Quick Charge 3.0 description for rev 2.0 implementation
		  ▫ Updated AICL glitch filter times
		  ▫ Increased the max voltage rating to 22 V
		  ▫ Removed the 2.6 s battery missing poller
		  ▫ Defeatured termination and precharge currents < 300 mA
		  ▫ Added description for system short circuit protection
		  ▫ Updated description for shutdown/suspend mode

E	June 2015	▪ Cover: Added Qualcomm Quick Charge 2.0 logo
F	October 2015	▪ Updated the Qualcomm Quick Charge 3.0 description for rev 2.1 implementation ▪ Corrected the top output current level to reflect the actual register value of 4.6 A throughout the document ▪ Exposed registers and features relevant to Qualcomm Quick Charge 3.0 throughout the document ▪ Removed SYSON/VBAT capacitor from Figure 2-1 ▪ Added SW pin transient voltage tolerance specifications to Table 4-1 ▪ Updated OVLO C value to capture rev 2.1; added Vsys regulation data for room temperature to Table 4-3 ▪ Added 50 mV option for Vsys tracking in factory programmable registers in Table 5-2 ▪ Improved description of Table 7-11 ▪ Updated system short circuit protection for rev 2.1 in Section 7.1.40 ▪ Added stipulation for SYSON to VBAT capacitor in Section 8.1.3 ▪ Corrected description for Figure 9-1 ▪ Added ball shear information in Section 11.1

Contents

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Tables

1 Introduction

1.1 Document overview

This device specification defines the SMB1350/SMB1351 device. The Qualcomm Technologies, Inc. (QTI) SMB1350/SMB1351 solution is a programmable, 2.6/4.6 A switching Li+ battery charger with Qualcomm® Quick Charge™ 3.0 technology, TurboCharge™ mode, CurrentPath, AICL, AFVC, USB OTG, and JISC8714/JEITA support.

Additional technical information for this device is primarily covered by the documents listed in Table 1-1. All documents should be studied for a thorough understanding of the device and its applications. Released SMB1350/SMB1351 documents are available from the CDMATech Support website at https://createpoint.qti.qualcomm.com/.

Table 1-1 Primary SMB1350/SMB1351 documentation

Document number	Title/description
80-NL405-5	*SMB1350/SMB1351 Layout Guidelines* This document outlines how to lay out the SMB1350/SMB1351 device in detail on a single-sided PCB.
80-NL405-4	*SMB1350/SMB1351 Device Revision Guide* This document reviews the technical limitations of each revision of silicon.
80-NL405-3	*SMB1350/SMB1351 Evaluation User Guide* This document provides instructions for evaluating various features of the SMB1350/SMB1351 device.

This SMB1350/SMB1351 device specification is organized as follows:

Chapter 1 Provides an overview of the SMB1350/SMB1351 documentation, gives a high-level functional description of the device, lists the device features, and applications.

Chapter 2 Provides a detailed description of the SMB1350/SMB1351 and includes multiple flowcharts and diagrams.

Chapter 3 Defines the device pin assignments.

Chapter 4 Defines the device electrical performance specifications, including absolute maximum ratings and operating conditions.

Chapter 5 Provides the SMB1350/SMB1351 device configuration register.

Chapter 6 Discusses the I^2C programming information.

Chapter 7 Provides detailed information on the device operation.

Chapter 8	Discusses the external components, board layout recommendations, and power dissipation.
Chapter 9	Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.
Chapter 10	Discusses the shipping, storage, and handling of the SMB1350/SMB1351 device.
Chapter 11	Describes device reliability testing.

1.2 SMB1350/SMB1351 introduction

The SMB1350/SMB1351 device is a programmable single-cell lithium-ion (Li-Ion)/lithium-polymer (Li-Polymer) battery charger designed for a variety of portable applications. The device provides a simple and efficient way to charge high-capacity Li-Ion batteries and power the system via a universal serial bus (USB) or AC adapter input. Unlike conventional charging devices, the SMB1350/SMB1351 high efficiency switch mode operation eliminates the low charge current and thermal problems of conventional solutions. The switching architecture in conjunction with programmability enables faster charging from current limited inputs such as USB.

Charge current can be set up to 2.6 A for the SMB1350 device and 4. 6 A for the SMB1351 device. An input current limit of up to 3 A is supported for both the products. The SMB1350/SMB1351 device manages two outputs independently: battery charging and system power. This allows immediate system operation under missing or deeply discharged battery conditions. The SMB1350/SMB1351 device supports USB on-the-go (OTG) devices by providing the required USB OTG (+5.0 V and up to 1.8 A power supply) using the Li-Ion battery as a source. The USB battery charging specification 1.2 and ACA standard are supported.

Charge control includes input current limit (supporting USB 2.0 and USB 3.0), trickle charge, precharge, constant current/constant voltage, float voltage, and termination/safety settings. These are fully programmable via a serial I^2C/SMBus and stored in nonvolatile memory, making the device a flexible solution. Fast charge current level is set via I^2C (limited by the input current settings). Input signal pins are provided to suspend charging or turning off the input FETs for the USB suspend mode. Built-in reverse current blocking prevents inadvertent cell discharge.

The SMB1350/SMB1351 device offers a wide variety of features that protect the battery pack, the charger, and the input circuitry: overcurrent, under or over voltage (OV), safety timers, float voltage, charge current, float voltage compensation, and thermal protection. Status is monitored via the serial port for charge state and fault conditions. The STAT output is used to signal the charge status. The operating voltage is specified between 3.6–14 V with +22 V nonoperating input tolerance. The SMB1350/SMB1351 device is available in small WLNSP package and is rated over a -30 to +85 °C temperature range.

1.3 Features

- Efficient battery charging eliminates heat issues
  - Higher than 90% conversion efficiency
- Charge current up to 4.6 A for the SMB1351 and 2.6 A for the SMB1350
- Autonomous Quick Charge 3.0 support for fast charging

- OptiCharge (AICL) for USB/AC/DC adapter compatibility
- TurboCharge+, improving charge time by safely adjusting float voltage based on charge status
- FlexCharge per latest USB charging specification 1.2
- Programmable input current limiting (USB 2.0/3.0 compliant)
- Up to 750 mA charging output from a 500 mA USB port or 4.5 A from an AC adapter using TurboCharge
- No startup delay
  - 50 mA SYSON auxiliary output allows system operation with discharged or missing battery
  - Output CurrentPath control allows system operation with discharged or missing battery
- USB OTG power support (up to 1.8 A at +5.0 V)
- USB OTG short circuit protection
- Hardware based, programmable JEITA and JISC 8714 support
- Switching frequency of 750 kHz, 1 MHz, 1.5 MHz, and 3 MHz
- 3.6–14 V operating input voltage range
- +22 V input rating (nonoperating) with over-voltage protection
- Digital programming of all major parameters via I^2C interface
- ±0.5% V_{FLT} accuracy
- Comprehensive protection features
  - Status/fault indicators
  - Battery/IC thermal protection
  - OC/UV/OV protection
  - Charge termination safety timers
- Small WLNSP packages

1.4 Applications

- Tablet computers
- Smartphones
- MID devices
- Mobile routers
- Digital camcorders
- Battery banks

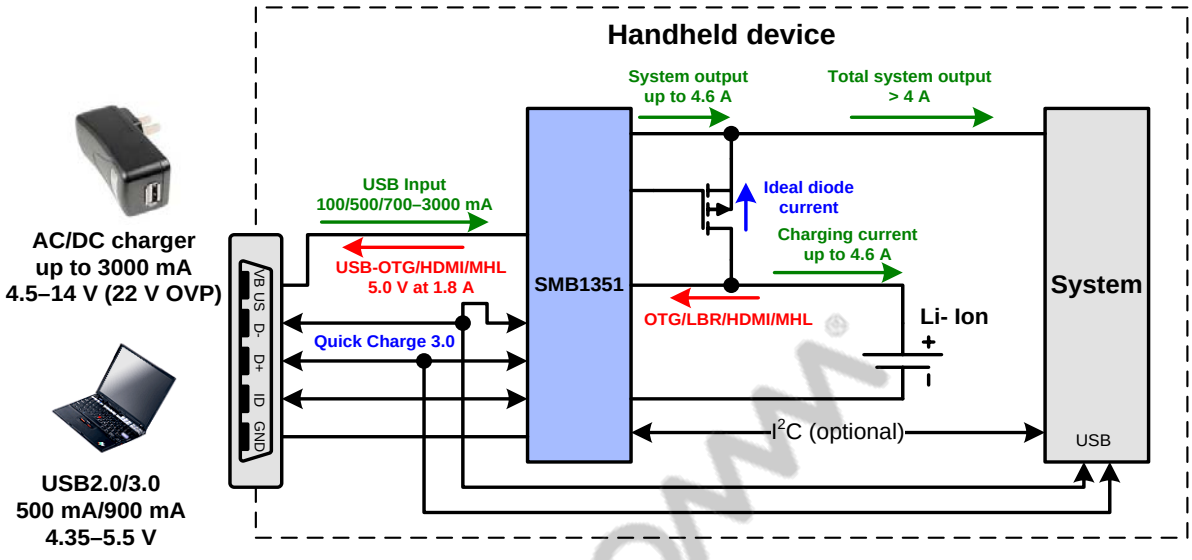

Figure 1-1 SMB1350/SMB1351 simplified application

2 General description

The SMB1350/SMB1351 device is a fully programmable switch-mode Li-Ion battery charger and output power controller for portable devices. The device is designed to be used in conjunction with systems using high capacity, single cell Li-Ion and Li-Polymer battery packs. The SMB1350/SMB1351 device provides two major functions to the end system: input selection and arbitration, and battery charging. The device is fully programmable via the I^2C interface and configuration registers are nonvolatile. This allows the device to be configured into different powerup states and be reprogrammed during operation.

The SMB1350/SMB1351 high efficiency switch mode operation allows low power dissipation and short charging times. TurboCharge+ allows additional savings in charging time, while ensuring safe operation, by adjusting the float voltage based on charging status.

The SMB1350/SMB1351 device incorporates an optional feature that makes the device capable of automatically detecting power source type per the latest USB battery charging specification 1.2. This allows the system to draw currents in excess of the USB 2.0 or USB 3.0 specification for charging or powering up from a dedicated, USB AC/DC charger. The SMB1350/SMB1351 device uses the D+ and D- USB lines to determine the type of charger connected to the handheld device and the input current automatically adjusts based on the power source type. A logic signal applied on the USB5/1/AC pin (configurable as a USBCS pin) is used as an indication from the transceiver that a dedicated USB charger is connected, thereby directing the device to adjust current levels accordingly.

The device automatically maximizes the charge current for a given power source level by detecting the maximum stable output current of the AC/DC adapter and allowing optimization of the current level between the power adapter and the portable device.

The SMB1350/SMB1351 device is powered from a variety of power sources and offers programmable input current limiting to protect upstream charging sources (such as USB). The device features CurrentPath that allows instant system on operation.

The SMB1350/SMB1351 device provides four main charging phases: trickle-charge, preconditioning (precharge), constant current (fast charge), and constant voltage (taper charge). All phases, except trickle charge, are fully programmable allowing various battery charging algorithms supporting multiple system designs and new battery technologies. The following parameters are programmable:

- Precharge current
- Fast charge current
- Termination current
- Float voltage
- Precharge voltage threshold
- Input current limit

- Safety timer duration
- Battery thermal limits

An additional feature, which adds flexibility, is the USB OTG mode. The SMB1350/SMB1351 device uses the battery as the input source and provides power to peripherals compliant with the USB OTG specification. This unique function is enabled by reversing the internal path and using the DCIN input as an output, providing 5.0 V and more than 1.8 A.

A wide range of IC protection features are also included in the SMB1350/SMB1351 device. These include input and output over-voltage/overcurrent protection, thermal shutdown, charger current or float voltage compensation (JEITA support), and battery missing detection (BMD). An open-drain STAT output indicates a variety of status and fault conditions, which are selected via the STAT output configuration register. A second open-drain or push-pull output (PGOOD) is available to indicate a valid input power presence.

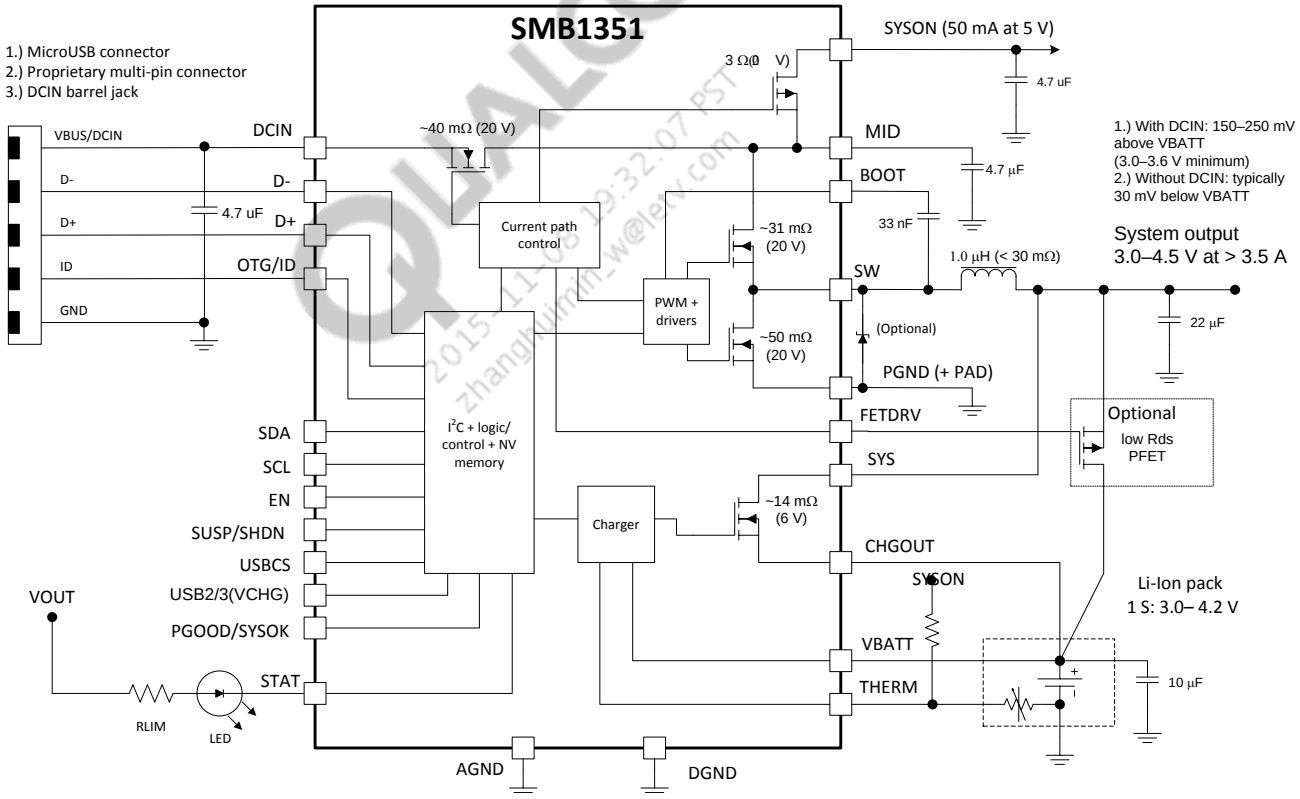

Figure 2-1 Typical charging application

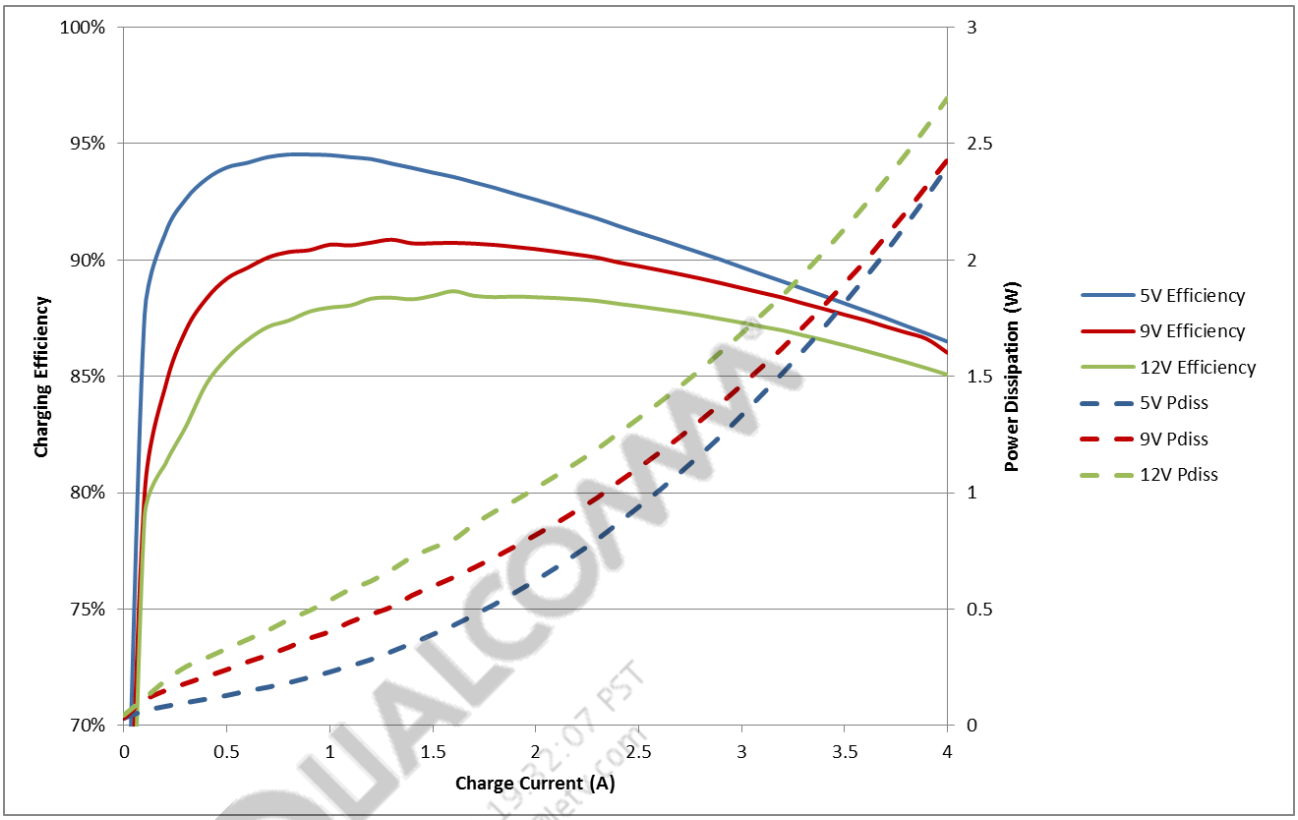

Figure 2-2 SMB1350/SMB1351 charging efficiency and power dissipation

NOTE: Efficiency and power dissipation data was taken at 3.8 V battery with a Toko DFE252012F inductor at 750 kHz and includes CHGFET power dissipation. See Chapter 8 for detailed recommendations on accurate efficiency measurements.

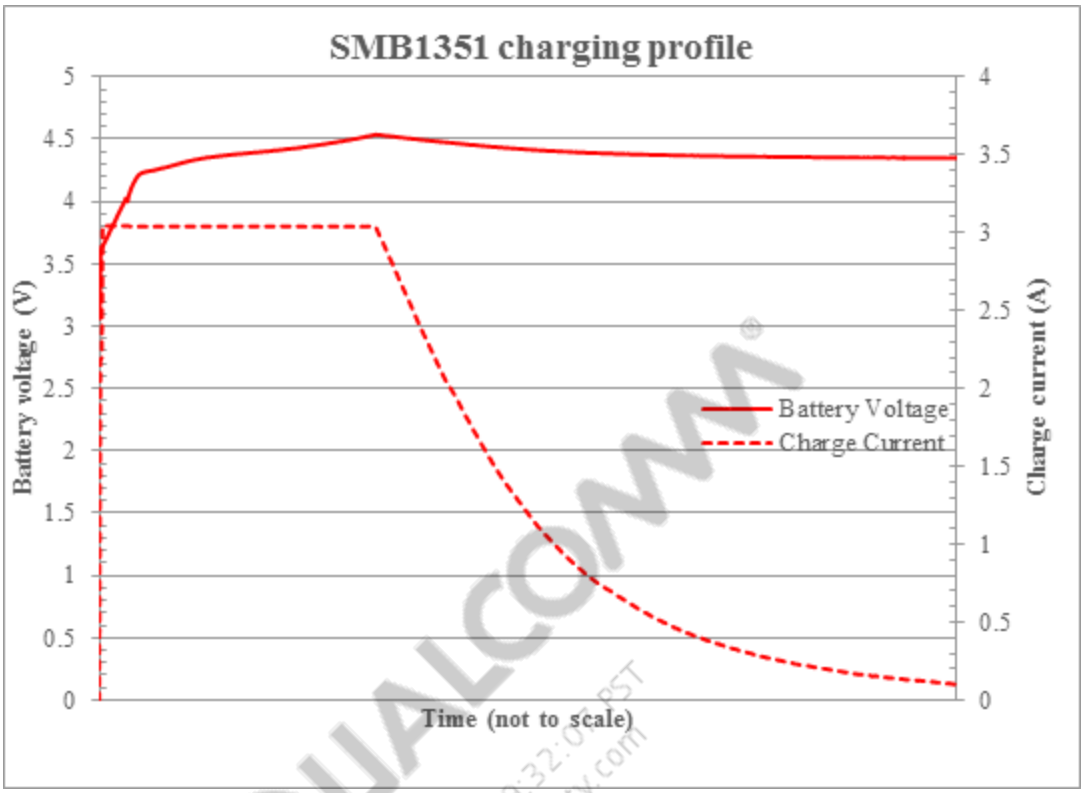

Figure 2-3 USB adapter charging algorithm with TurboCharge

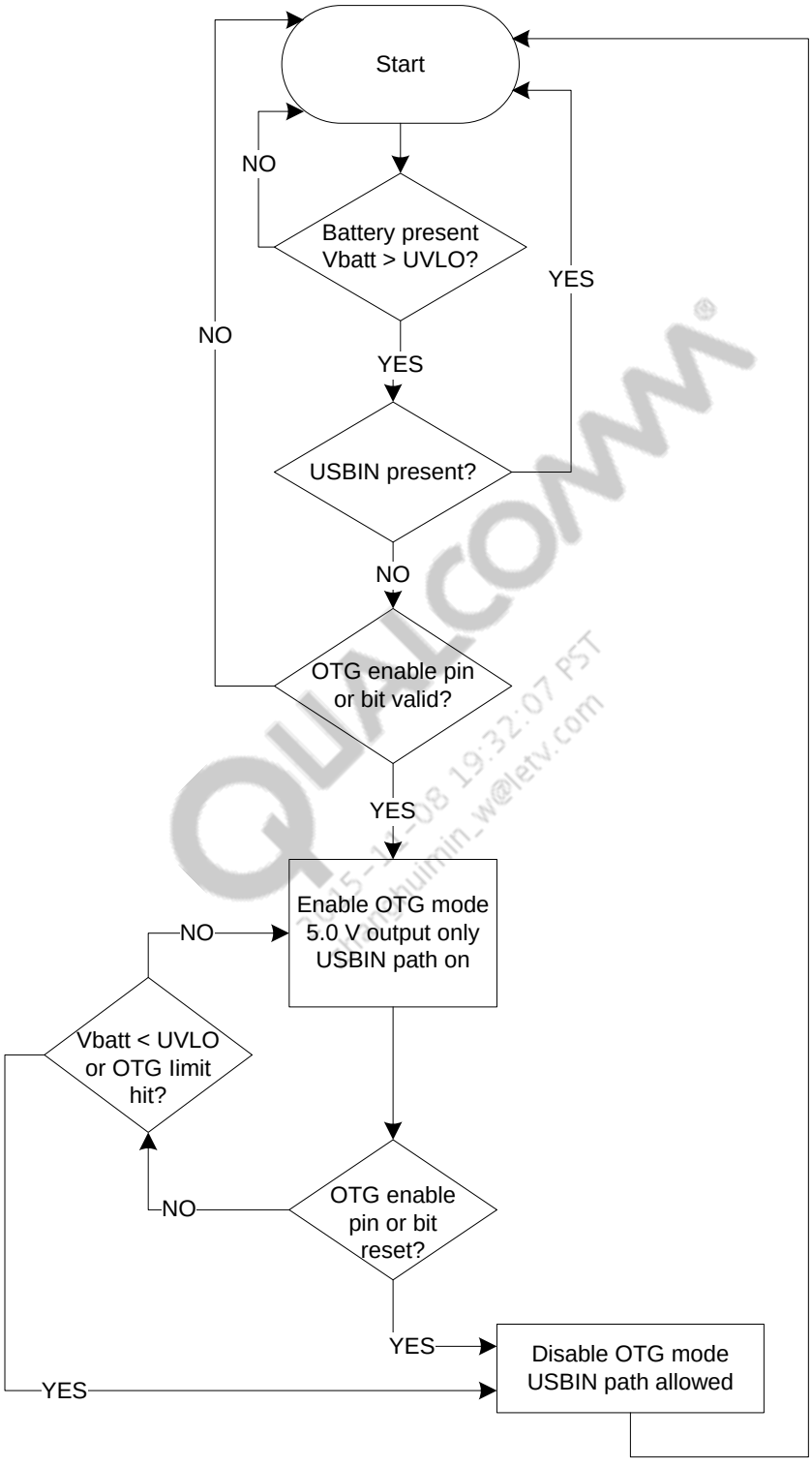

Figure 2-4 OTG functional flowchart

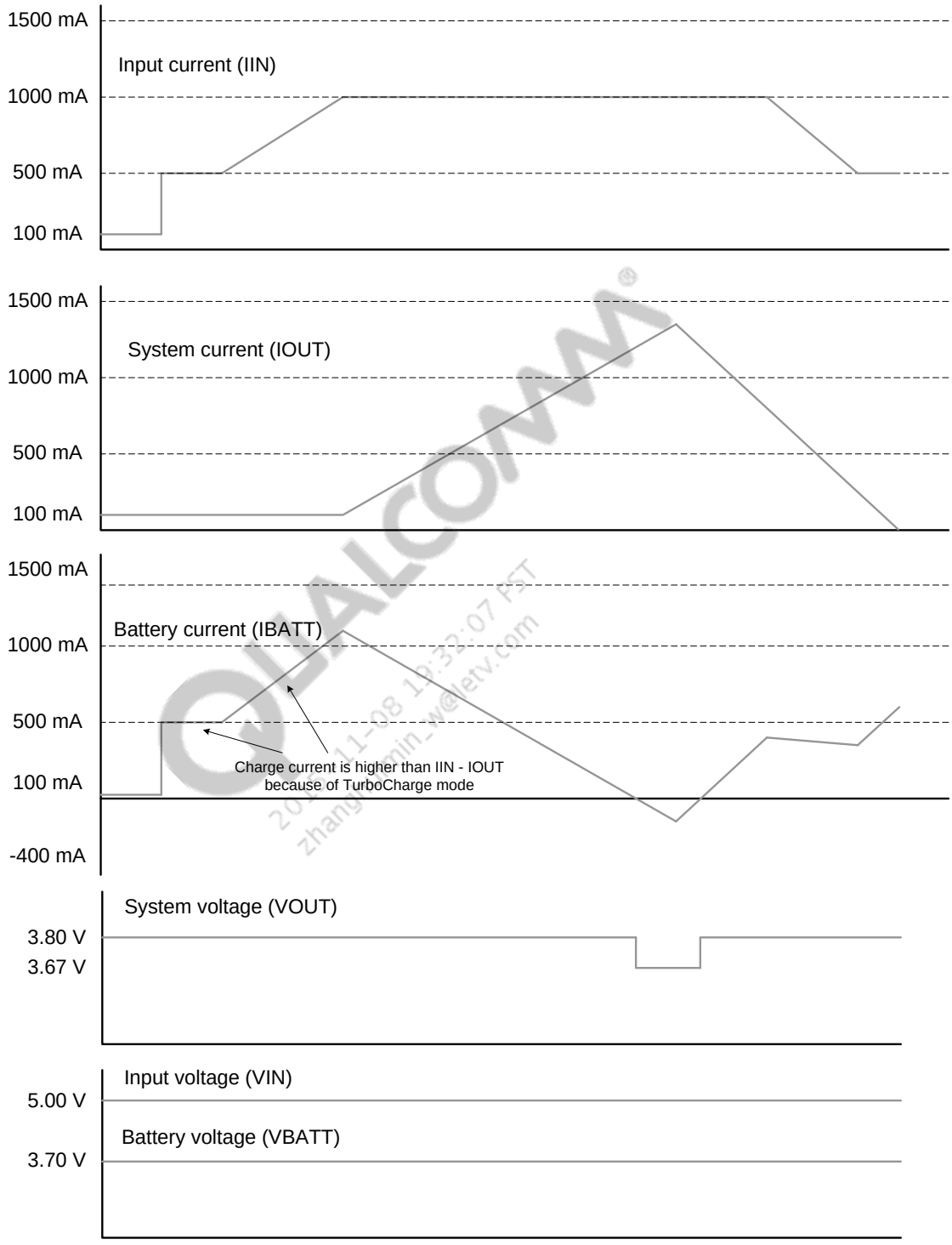

Figure 2-5 Input/output voltage/current diagrams

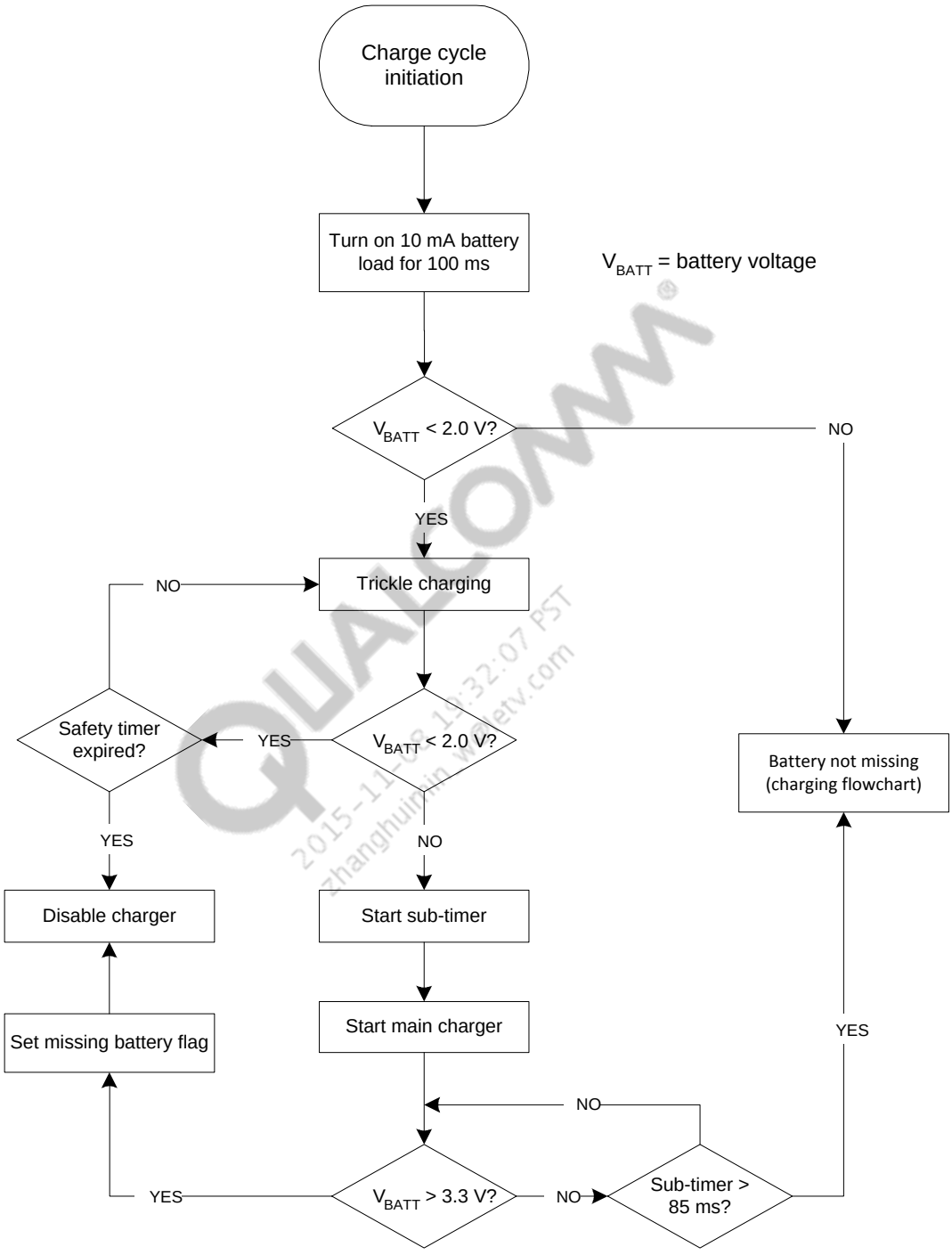

Figure 2-6 Missing battery detection

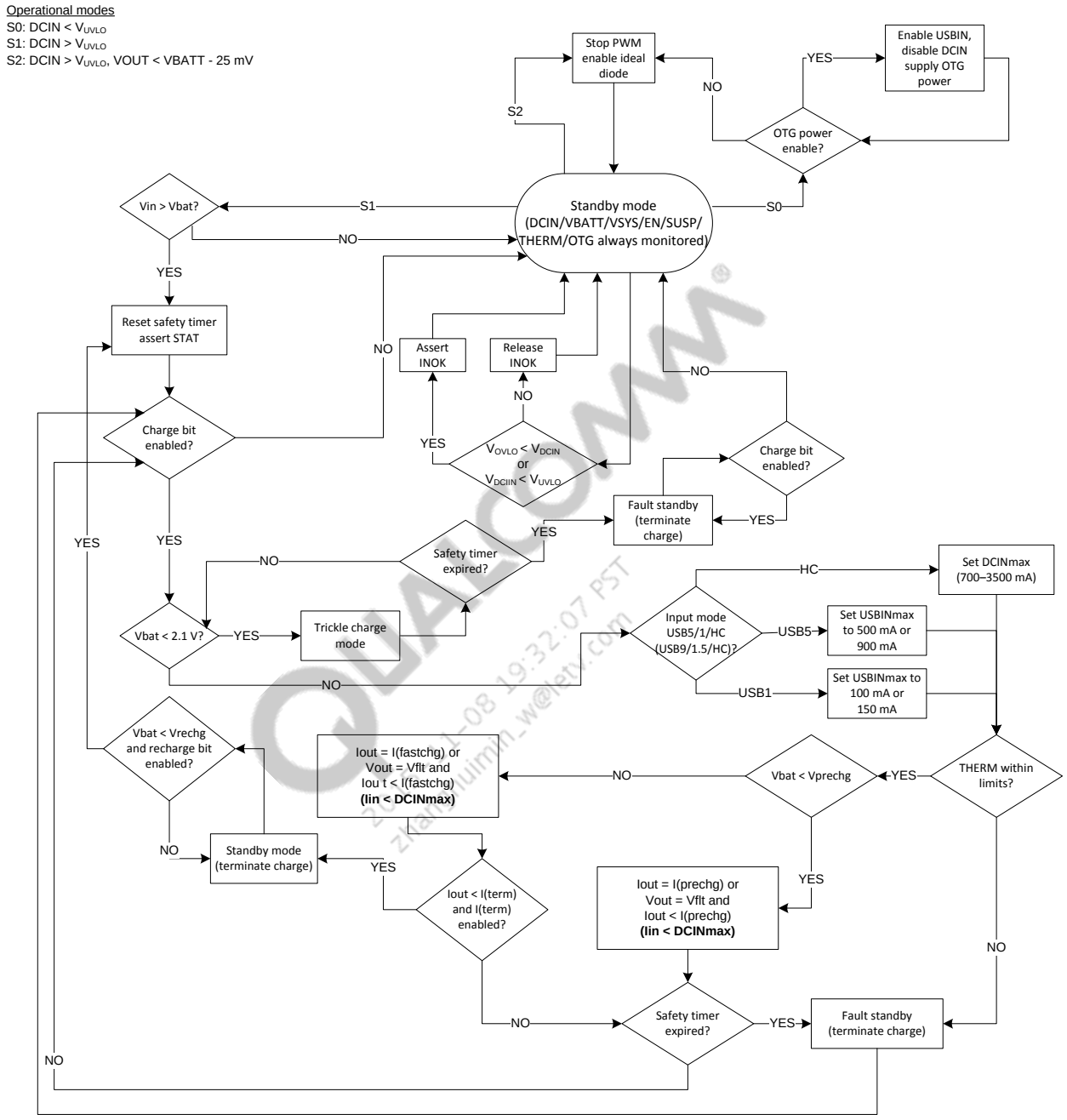

Figure 2-7 Functional flowchart

3 Pin descriptions

Table 3-1 Pin descriptions

Ball number	Pin name	Ball type	Pin description
40, 41, 42, 47, 48, 49	DCIN	Power	DCIN input – Connect to the USB VBUS (3.6–5.5 V) or the DC input (3.6–14 V) and bypass with a 4.7 µF or greater MLCC. This input is current limited to 100 mA/500 mA (or 150 mA/900 mA programmable option) or 500–3000 mA depending on the power source type.
33, 34, 35	MID	Output	FET midpoint – Connect a 4.7 µF capacitor to the ground. The MID pin sees either the input voltage minus a diode drop (input present) or the battery voltage minus a diode drop (no input present). If a load is connected to this pin it has to take into account that input over-voltage events appear at this pin.
11	BOOT	Output	Boot capacitor node – Connect 33 nF minimum MLCC capacitor for the buck regulator high-side drive bootstrap voltage generation.
18, 19, 20, 21, 25, 26, 27, 28	SW	Output	Switch node – Connect to the output inductor of the switching regulator.
4, 5, 6, 7, 12, 13, 14	PGND	Ground	Power ground – Connect to the PCB ground.
30	FETDRV	Output	External FET drive –Optional, low Rds-on battery discharge path (or battery to system disconnect FET). Connect to the gate of the external PFET. Leave floating when not in use.
3, 10, 17, 24	SYS	Output	System output/charger input – Connect to the system loads and bypass with a 22 µF or greater MLCC.
2, 9, 16, 23	CHGOUT	Output	Battery charger output – Connect to the positive terminal of the battery. Bypass with a 10 µF MLCC.
8	VBATT	Input	Auxiliary power/kelvin sense – Input power path from the battery. Connect to the positive terminal of the battery. Use a separate trace to route this pin.
15	THERM	Input	Battery thermistor sense – Connect to the T terminal of the battery pack. This pin expects an NTC thermistor inside the battery pack. Add a bias resistor from this pin to SYSON.
36	GND	Ground	Ground – Connect to the PCB ground.
43	STAT	Output	Status/fault/interrupt indicator – Open drain output that indicates charging or fault status. This is multiplexed static (fault) or pulsed output (IRQ) and has programmable polarity.
22	PGOOD	Output	Power good or SYSOK indicator – Open drain or push pull output that indicates either a valid input power presence ($V_{UVLO} < V_{IN} < V_{OVLO}$) or a battery level for system operation.

Ball number	Pin name	Ball type	Pin description
37	USBCS	Input	USB9/5/1.5/1/HC selector – Three state input pin that limits input current depending on the mode. High selects USB 500 (or USB 900) and low selects USB 100 (or USB 150). Leave floating for the HC mode (500–3000 mA). Can also be programmed to dual state mode. Add a 100 pF cap if this pin needs to be floated. High selects HC mode and low selects USB 500 (or USB 900). This can be controlled by the USBCS register bit.
1	SUSP/ SHDN	Input	USB suspend /shutdown input – Can be used as an active high logic input pin to enter USB suspend mode when an input is present. If no input is present, shutdown mode will be enabled if the pin is biased low.
29	EN	Input	Enable input – Logic high or low (programmable) to enable or resume charging. This is activated by a register bit.
45	SDA	Input/output	I^2C bus data
46	SCL	Input	I^2C bus clock
32	OTG/ID	Input	OTG mode enable or OTG ID monitor – Multiplexed input that is used to either enable OTG mode (this function is controlled by the OTG enable bit) or to detect an OTG ID resistor value. Programmable polarity for an OTG input.
44	D+	Input/output	Power source detection – Connect to USB D+ signal line.
38	D-	Input/output	Power source detection – Connect to USB D- signal line.
39	SYSON	Output	Auxiliary output – 50 mA (minimum) output supply bypassing the charger ($V_{UVLO} < V_{SYSON} < V_{OVLO}$) for instant on system operation. This output is active during the OTG mode. Connect a 4.7 µF capacitor to the ground.
31	USB2/3 (VCHG)	Input	Two factory program options are available: ▪ USB 2.0/USB 3.0: Input current limit selector ▪ VCHG: Analog output (0–2.5 V) – Voltage corresponds to charge (VCHG = ICHG × 0.5) or input current (VCHG = IIN × 0.55).

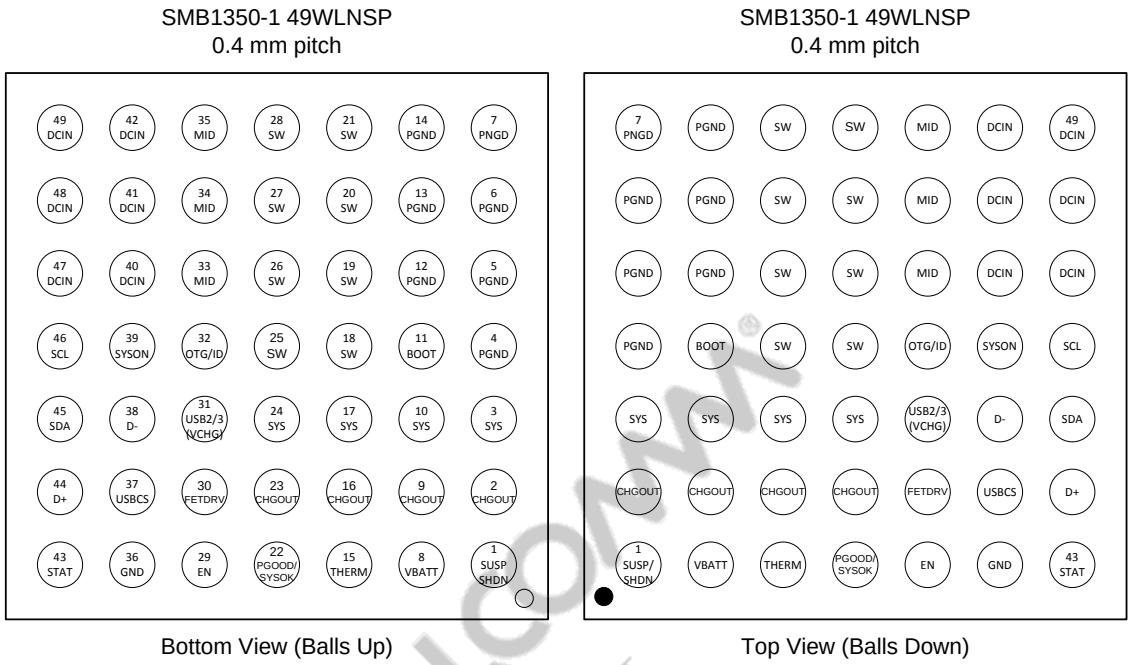

Figure 3-1 49WLNSP package and ball configuration

4 Operating characteristics

Table 4-1 Absolute maximum ratings

Parameter	Value
Terminal voltage with respect to GND:	
DCIN and MID	-0.3 V to +22 V
BOOT and SW (DC)	-0.3 V to +20 V
SW (transient)	-2 V (for 20 ns) to 16 V (for 10 ns)
All others	-0.3 V to +6 V
All others	< DCIN or VBATT +0.5 V
Maximum DC current	4.6 A
Lead solder temperature (10 s)	300 °C
Junction temperature	150 °C
ESD rating per JEDEC	2000 V
Latch-up testing per JEDEC	±100 mA

NOTE: The device must be powered/biased via DCIN with VBATT at a typical battery voltage greater than 3 V before applying power on any of the other I/Os. Maximum DC current specified at a minimum of 0.68 µH of inductance and at an operating voltage of 13.2 V to account for increased current ripple. See Section 8.1.2 for more detailed information on inductor selection.

Table 4-2 Recommended operating conditions

Parameter	Value
Temperature range	-30 °C to +85 °C
DCIN	3.6 V to 14 V
SW	-0.3 V to 14 V
Package thermal resistance (θ_{JA}):	
49WLNSP	26 °C/W
Moisture classification per J-STD – 020:	
49WLNSP	Level 1 (MSL1)
Reliability characteristics	
Data retention	20 years

NOTE: The device is not guaranteed to function outside its operating rating. Stresses listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification are not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. It is recommended to take precautions during handling of the device. Operation at 3 MHz is not supported above the 9 V operating range.

Table 4-3 DC operating characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A= -30 to +85°C, V_{DCIN} = 5 V, V_{FLT} = 4.2 V, V_{BATT} = 3.7 V unless otherwise noted. All voltages are relative to GND (note 3).						
General						
V_{DCIN}	USB or AC input voltage	V_{FLT} = 4.2 V	4.35	–	V_{OVLO}	V
V_{UVLO}	Input under-voltage lockout (UVLO) (note 1)	V_{DCIN} falling, option A	3.4	3.6	3.8	V
		V_{DCIN} falling, option B	7.6	7.8	8.0	
		V_{DCIN} falling, option C	8.9	9.2	9.5	
		Hysteresis	–	2.5	–	%
V_{OVLO}	Input over-voltage lockout (OVLO) (note 1)	V_{DCIN} rising, option A	6.2	6.4	6.6	V
		V_{DCIN} rising, option B	10.0	10.3	10.6	
		V_{DCIN} rising, option C	13.2	14.7	15.2	
		Hysteresis	–	2.5	–	%
V_{USB-OK}	USB_OK low threshold	V_{DCIN} falling (note 1)	3.70	3.85	4.00	V
		Hysteresis	–	0.1	–	V
V_{CL}	Current limit threshold (HC mode)	V_{DCIN} falling, V_{CL} = 4.25 V	-3.5	–	+3.5	%
$I_{DD-ACTIVE}$	Active supply current		–	12	–	mA
$I_{DD-STBY-BATT}$	Battery standby supply current	V_{BATT} > 2.4 V, DCIN = 0	–	80	100	μA
$I_{DD-SHDN-BATT}$	Battery shutdown current	V_{BATT} > 2.4 V, DCIN = 0 V, SUSP = 0 V	–	10	–	μA
$I_{DD-SUSP-DCIN}$	DCIN suspend current	DCIN = 5 V, SUSP = HIGH	–	0.6	1	mA
$I_{IN-BIAS}$	Input prebias current	DCIN input present, enabled	50	–	–	mA
I_{IN-PD}	DCIN OV pull down current	DCIN OV	-	10	-	mA
I_{DD-OTG}	OTG supply current	OTG mode, no load	–	1	–	mA
T_{REG}	Thermal regulation temperature (note 8)	I_{CHG} reduction, option A	–	100	–	°C
		I_{CHG} reduction, option B	–	120	–	
T_{SHDN}	IC thermal shutdown temp	Note 8	–	140	–	°C
T_{HYST}	IC thermal shutdown hysteresis	Note 8	–	20	–	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PWM buck regulator						
R_{RDSON}	FET on resistance	High side	25	31	37	mΩ
		Low side	24	29	35	mΩ
		Front porch	50	60	72	
I_{LIMIT}	Peak switch current limit	V_{DCIN} = 5.0 V (note 8)	–	5.0	–	A
		V_{DCIN} = 9.0 V (note 8)	–	6.0	–	
D.C.	Duty cycle	Maximum (note 8)	–	98	–	%
		Minimum (note 8)	–	0	–	%
Logic inputs/outputs						
V_{IL}	Input low level		–	–	0.55	V
V_{IH}	Input high level		1.4	–	–	V
V_{OL}	SDA/STAT/PGOOD output low level	I_{SINK} = 3 mA	–	–	0.3	V
RPULL	INOK/SYSOK/PGOOD output	Configured as push-pull, V_{DD} = 2.5 V	–	50	–	kΩ
Battery charger						
R_{DSON}	BATT-to-SYS FET on resistance	Note 8	12	15	19	mΩ
V_{BOV}	Battery over-voltage lockout	V_{BATT} rising (note 11)	–	V_{FLT} + 0.1	–	V
V_{ASHDN}	Automatic charger shutdown threshold voltage	V_{DCIN} - V_{BATT}, falling	–	40	–	mV
$V_{ASHDNHYS}$	Automatic charger shutdown threshold voltage hysteresis	V_{DCIN} - V_{BATT}, falling	–	130	–	mV
$V_{TRICKLECHG}$	Trickle charge to precharge voltage threshold		2.0	2.1	2.2	V
$I_{TRICKLECHG}$	Nominal trickle charge current	V_{BATT} = 1.7 V	–	30	–	mA
V_{PRECHG}	Precharge to fast charge voltage threshold	Programmable 2.4–3.0 V, V_{BATT} rising, (four steps)	-4	–	+4	%
I_{PRECHG}	Precharge current	Programmable 300–700 mA, five steps, T = 0–70 °C, I_{PRECHG} = 300 mA–700 mA	-25	–	+25	%
		T = 0–70 °C, I_{PRECHG} = 200 mA	-40	–	+40	%
I_{FCHG}	Fast charge current	Programmable 1000–2600 mA/4640 mA, I_{FCHG} = 1000 mA, T = 0–70 °C	-7.5	–	+7.5	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{FLT}	Float voltage	Programmable 3.46–4.72 V in 20 mV steps, V_{FLT} = 4.2 V or V_{FLT} = 4.35 V, T= 0–70 °C	-1	–	+1	%
I_{TERM}	Charge termination current	Programmable 300–700 mA, five steps, T = 0–70 °C, I_{TERM} = 300 mA–700 mA	-20	–	+20	%
		T = 0–70 °C, I_{TERM} = 200 mA	-40	–	+40	%
V_{RECH}	Recharge threshold voltage	Two programmable options, V_{FLT} - V_{BATT} falling	–	50	–	mV
			–	100	–	
Missing battery detection						
I_{BMDDIS}	Missing battery detection discharge current	For the first 100 ms	–	10	–	mA
V_{BMDDIS}	Missing battery detection voltage threshold	Internal algorithm	–	3.3	–	V
		THERM	–	0.96 × V_{SYSON}	–	
USB OTG mode						
V_{OTG}	OTG output voltage	Note 9	4.75	5	5.25	V
$V_{OTG-P-P}$	OTG output ripple	C_{IN} = 4.7 µF, C_{OUT} = 10 µF	–	400	–	mV
$V_{BATUVLO}$	Battery UVLO	Programmable 2.7–3.4 V	-4	–	+4	%
$V_{BATUVLOHY}$	UVLO hysteresis	OTG operation	–	0.2	–	V
$I_{OTG-LIM}$	Output current limit (at output DCIN) – steady state	V_{BATT} = 3.7 V, programmable 500–1800 mA (four steps), $I_{OTG-LIM}$ = 500 mA, T = 0–70 °C	400	500	600	mA
SYSON output						
V_{SYSON}	SYSON output voltage	I_{OUT} = 50 mA (note 6 and 8) V_{DCIN} > 5 V	4.75	5.0	5.25	V
$V_{SYSONUVLO}$	SYSON UVLO	V_{DCIN} falling	3.5	3.6	3.7	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CurrentPath controller						
$I_{LIM-DCIN}$	DCIN absolute input current limit (note 2)	USB 500 mode, T = 0–70 °C	450	475	500	mA
		USB 100 mode, SYS > 2.0 V, T = 0–70 °C	80	90	100	mA
		USB 900 mode, T = 0–70 °C	810	855	900	mA
		USB 150 mode, SYS > 2.0 V, T = 0–70 °C (note 5)	120	135	150	mA
		USB AC mode 500–3000 mA, $I_{LIM-DCIN}$ = 900 mA, T = 0–70 °C	810	855	900	mA
V_{SYS}	Regulated output voltage	Input present option A (factory programmable option for 1.5x)	3.15, 3.3, 3.45, 3.6	V_{BATT} + 0.10	–	V
		Input present option B (factory programmable option for 1.5x)	3.15, 3.3, 3.45, 3.6	V_{BATT} + 0.25	–	
ΔV_{SYS}	Regulated output voltage accuracy	V_{SYS} = 3.56 V, I_{SYS} = 1 A, T = 0–70 °C	-3.5	±1	+3.5	%
		V_{SYS} = 4.35 V, I_{SYS} = 1 A, T = 0–70 °C	-2	±1	+2	
		V_{SYS} = 4.35 V, I_{SYS} = 1 A, T = 25 °C	-0.5	±0.25	+0.5	
$\Delta V_{SYS\ LOAD}$	Output voltage load regulation accuracy	I_{OUT} = 0 A to 1 A in 15 µs	V_{BATT} - 0.2	V_{BATT} - 0.1	–	V
V_{REVFET}	Ideal diode regulation voltage	SYS falling, V_{BATT} > SYS, I_{OUT} = 1000 mA	–	V_{BATT} - 50	–	mV
R_{DS-ON}	DCIN path	DCIN = 5.0 V, DCIN-to-SW path	–	90	–	mΩ
Battery thermal monitor						
V_{CHARD}	Hard cold temperature trip point, programmable: 0.665–0.805 V_{IN}, four steps	V_{THERM} rising, V_{COLD} = 0.76 V_{SYSON}	0.74	0.76	0.78	V_{COLD}/V_{SYSON}
V_{CSOFT}	Soft cold temperature trip point, programmable: 0.61–0.76 V_{IN}, four steps	V_{THERM} rising, V_{COLD} = 0.715 V_{SYSON}	0.695	0.715	0.735	V_{COLD}/V_{SYSON}
V_{CHYST}	Cold temperature trip point hysteresis	Rising from V_{CHARD} or V_{CSOFT}	–	80	–	mV
V_{HHARD}	Hard hot temperature trip point, programmable: 0.185–0.276 V_{IN}, four steps	V_{THERM} falling, V_{HOT} = 0.212 V_{SYSON}	0.197	0.212	0.227	V_{HOT}/V_{SYSON}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSOFT}	Soft hot temperature trip point programmable: 0.242–0.356 V_{IN}, four steps	V_{THERM} falling, V_{HOT} = 0.315 V_{SYSON}	0.300	0.315	0.330	V_{HOT}/V_{SYSON}
V_{HHYST}	Hot temperature trip point hysteresis	Rising from V_{HHARD} or V_{HSOFT}	–	70	–	mV
VCHG output						
V_{CHG}	Output voltage proportional to charge/input current	Programmable option A	–	V_{CHG} = I_{CHG} × 0.5 Ω	–	V
		Programmable option B	–	V_{CHG} = I_{IN} × 0.55 Ω	–	
V_{CHGACC}	Charge output voltage accuracy	I_{CHG} = 200mA, T = 0–70 °C	-40	–	+40	mV
		I_{CHG} = 1000 mA, T = 0–70 °C	-150	–	+150	
$V_{CHGDRIVE}$	Charge output drive capability		–	–	50	pF
FlexCharge/automatic power source detection (APSD) – (note 10)						
V_{DP_SRC}	D+ source voltage	I_{DP_SRC} > 250 µA	0.5	0.6	0.7	V
V_{DAT_REF}	Data detect voltage		0.25	0.325	0.4	V
I_{DM_SINK}	D- sink current		50	–	150	µA
I_{DP_SRC}	Data contact detect current source		7	–	13	µA
Low-battery/SYSOK voltage detector						
$V_{LOWBATT}$	Low battery voltage/SYSOK detection threshold range	15 steps, battery voltage falling	2.5	–	3.58	V
$V_{LOWBATTACC}$	Low battery voltage/SYSOK detection threshold accuracy	$V_{LOWBATT}$ = 2.8 V	2.7	2.8	2.9	V
$V_{LOWBATTHYS}$	Low battery voltage/SYSOK detection threshold hysteresis	Rising	–	100	–	mV

Notes for Table 3-3 can be found after Table 3-4.

Table 4-4 AC operating characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
T_A= -30 to +85°C, V_{IN} = 5 V, V_{FLT} = 4.2 V, V_{BATT} = 3.7 V unless otherwise noted. All voltages are relative to GND (note 3).						
Oscillator						
f_{OSC}	Oscillator frequency (note 9)	Programmable, option A	0.60	0.75	0.90	MHz
		Programmable, option B	0.85	1.0	1.15	
		Programmable, option C	1.3	1.5	1.70	
		Programmable, option D	2.5	3.0	3.5	
Battery charger						
t_{CTOPC}	Precharge timeout	Duration: 60 min	-20	–	+20	%
t_{CTOFC}	Complete charge timeout	Programmable 6 hr, 12 hr, 18 hr	-20	–	+20	%
t_{GLITCH}	Battery voltage glitch filter		–	175	–	ms
t_{WD}	Watchdog timer	Option A	–	18	–	s
		Option B	–	36	–	s
		Option C	–	72	–	s
T_{CHGHO}	Charger startup holdoff	Enabled	250	–	–	ms
		Disabled	–	700	–	µs
SYSON output						
t_{SYSON}	SYSON response time	From SYSON enable to 5 V regulated voltage on SYSON (note 6)	–	40	–	µs
FlexCharge (D+/D-) (note 10)						
$t_{SVLD\_CON\_WKB}$	Dead battery charging timer		–	30	45	min
$t_{CHGR\_DET\_DBNC}$	Charger detect debounce		10	–	–	ms
$t_{DCD\_TIMEOUT}$	DCD timeout	Note 10	300	–	900	ms

Notes for Table 3-3 and Table 3-4:

1. When the DCIN voltage rises/falls above/below this threshold, the corresponding status register indicates a UVLO/OVLO/USB-OK condition. If the user selects the appropriate bit, the STAT output asserts an IRQ signal indicating this condition.
2. I_{CHG} is overridden by the input current limit (I_{LIM}).
3. Voltage and current accuracies are only guaranteed for factory programmed settings. Changing the output voltage from that reflected in the customer-specific CSIR code results in inaccuracies exceeding those specified above.
4. During shutdown mode, the internal BATT-to-SYS FET is off.
5. When V_{BATT} falls below V_{SYS} the corresponding status register indicates a low battery condition.
6. This time does not include the debounce glitch filter time of approximately 50 ms for determining a valid input.
7. Subject to thermal derating.
8. Not 100% production tested. Guaranteed by design and/or characterization.

9. Dynamic switching frequency selection when the switcher is running is not allowed. It is recommended to use a 3 MHz operation only when a regulated or unregulated 5 V power source is used.
10. Refer to the USB battery charging specification 1.2 for additional information (http://www.usb.org/developers/devclass_docs).
11. During a true battery over-voltage event the switcher operation is disabled to prevent occurrence of boost-back operation.
12. Precharge and termination current settings below 300 mA are still present on Table 5-1 but are not guaranteed to comply with specifications listed and therefore de-featured.

Table 4-5 I²C 2-wire serial interface AC operating characteristics (400 kHz)

Symbol	Parameter	Conditions	400 kHz			
			Min	Type	Max	Units
f_{SCL}	SCL clock frequency		0	–	400	kHz
T_{LOW}	Clock low period		1.3	–	–	µs
T_{HIGH}	Clock high period		0.6	–		µs
t_{BUF}	Bus free time between a STOP and a START condition	Before new transmission	1.3	–	–	µs
$t_{SU:STA}$	Start condition setup time		0.6	–	–	µs
$t_{HD:STA}$	Start condition hold time		0.6	–	–	µs
$t_{SU:STO}$	Stop condition setup time		0.6	–	–	µs
t_R	SCL and SDA rise time[1]		20 + 0.1C_b	–	300	ns
t_F	SCL and SDA fall time[1]		20 + 0.1C_b	–	300	ns
$t_{SU:DAT}$	Data in setup time		100	–	–	ns
$t_{HD:DAT}$	Data in hold time		0	–	0.9	µs
TI	Noise filter SCL and SDA	Noise suppression	–	100	–	ns

1. Not 100% production tested. Guaranteed by design and/or characterization.

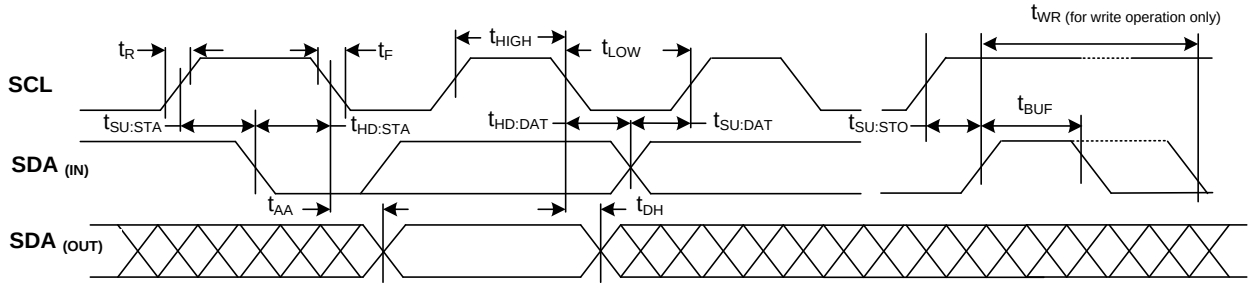

Figure 4-1 I²C timing diagram

5 Configuration register

Table 5-1 Configuration registers 00h – 14h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 00h – Fast charge and input current – nonvolatile and volatile (mirror)								
Fast charge current[1]								
1000 mA	0	0	0	0	X	X	X	X
1200 mA	0	0	0	1	X	X	X	X
1400 mA	0	0	1	0	X	X	X	X
1600 mA	0	0	1	1	X	X	X	X
1800 mA	0	1	0	0	X	X	X	X
2000 mA	0	1	0	1	X	X	X	X
2200 mA	0	1	1	0	X	X	X	X
2400 mA	0	1	1	1	X	X	X	X
2600 mA	1	0	0	0	X	X	X	X
2800 mA (2600 mA for SMB1350)	1	0	0	1	X	X	X	X
3000 mA (2600 mA for SMB1350)	1	0	1	0	X	X	X	X
3400 mA (2600 mA for SMB1350)	1	0	1	1	X	X	X	X
3600 mA (2600 mA for SMB1350)	1	1	0	0	X	X	X	X
3800 mA (2600 mA for SMB1350)	1	1	0	1	X	X	X	X
4000 mA (2600 mA for SMB1350)	1	1	1	0	X	X	X	X
4640 mA (2600 mA for SMB1350)	1	1	1	1	X	X	X	X
AC input current limit (maximum value)								
500 mA	X	X	X	X	0	0	0	0
685 mA	X	X	X	X	0	0	0	1
1000 mA	X	X	X	X	0	0	1	0
1100 mA	X	X	X	X	0	0	1	1
1200 mA	X	X	X	X	0	1	0	0
1300 mA	X	X	X	X	0	1	0	1
1500 mA	X	X	X	X	0	1	1	0
1600 mA	X	X	X	X	0	1	1	1
1700 mA	X	X	X	X	1	0	0	0
1800 mA	X	X	X	X	1	0	0	1
2000 mA	X	X	X	X	1	0	1	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2200 mA	X	X	X	X	1	0	1	1
2500 mA	X	X	X	X	1	1	0	0
3000 mA	X	X	X	X	1	1	0	1
Address: 01h – Other charge currents – nonvolatile and volatile (mirror)								
Precharge current[1]								
200 mA	0	0	0	X	X	X	X	X
300 mA	0	0	1	X	X	X	X	X
400 mA	0	1	0	X	X	X	X	X
500 mA	0	1	1	X	X	X	X	X
600 mA	1	0	0	X	X	X	X	X
700 mA	1	0	1	X	X	X	X	X
Termination current[1]								
200 mA	X	X	X	0	0	0	X	X
300 mA	X	X	X	0	0	1	X	X
400 mA	X	X	X	0	1	0	X	X
500 mA	X	X	X	0	1	1	X	X
600 mA	X	X	X	1	0	0	X	X
700 mA	X	X	X	1	0	1	X	X
USB 2.0/USB 3.0 selection								
Controlled by register	X	X	X	X	X	X	0	X
Controlled by USB2/3 pin	X	X	X	X	X	X	1	X
USB5/1 command polarity								
0 = USB1, 1 = USB5	X	X	X	X	X	X	X	0
0 = USB5, 1 = USB1 (from the command register h32 [1])	X	X	X	X	X	X	X	1
Address: 02h – Various functions – nonvolatile and volatile (mirror)								
Suspend mode control								
Controlled by SUSP pin	0	X	X	X	X	X	X	X
Controlled by register	1	X	X	X	X	X	X	X
Battery to system power control								
Normal operation	X	0	X	X	X	X	X	X
Turn off FET (user override)	X	1	X	X	X	X	X	X
Not used								
Not used	X	X	0	X	X	X	X	X
Automatic input current limit (AICL)								
Disabled	X	X	X	0	X	X	X	X
Enabled	X	X	X	1	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 V AICL detect threshold								
4.25 V	X	X	X	X	0	X	X	X
4.50 V	X	X	X	X	1	X	X	X
FlexCharge (APSD)								
Disabled	X	X	X	X	X	0	X	X
Enabled	X	X	X	X	X	1	X	X
Battery OV								
Battery OV does not shutdown charge cycle	X	X	X	X	X	X	0	X
Battery OV ends charge cycle	X	X	X	X	X	X	1	X
VCHG function								
Disabled	X	X	X	X	X	X	X	0
Enabled	X	X	X	X	X	X	X	1
Address: 03h – Float voltage – nonvolatile and volatile (mirror)								
Precharge to fast charge voltage threshold								
2.4 V	0	0	X	X	X	X	X	X
2.6 V	0	1	X	X	X	X	X	X
2.8 V	1	0	X	X	X	X	X	X
3.0 V	1	1	X	X	X	X	X	X
Float voltage (20 mV/step)								
3.50 V	X	X	0	0	0	0	0	0
3.52 V	X	X	0	0	0	0	0	1
….	X	X	….	….	….	….	….	….
4.34 V	X	X	1	0	1	0	1	0
4.35 V	X	X	1	0	1	0	1	1
4.38 V	X	X	1	0	1	1	0	0
4.48 V	X	X	1	1	0	0	0	1
4.50 V	X	X	1	1	0	0	1	0
….	X	X	….	….	….	….	….	….
4.50 V	X	X	1	1	1	1	1	1
Address: 04h – Charge control register – nonvolatile and volatile (mirror)								
Automatic recharge								
Enabled	0	X	X	X	X	X	X	X
Disabled	1	X	X	X	X	X	X	X
Current termination								
Enabled	X	0	X	X	X	X	X	X
Disabled	X	1	X	X	X	X	X	X
Max HC input current limit								
2500 mA	X	X	0	0	X	X	X	X
3000 mA	X	X	0	1	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Auto recharge threshold								
50 mV	X	X	X	X	0	X	X	X
100 mV	X	X	X	X	1	X	X	X
TurboCharge+ – automatic float voltage compensation (AFVC)								
Disabled	X	X	X	X	X	0	0	0
25 mV	X	X	X	X	X	0	0	1
50 mV	X	X	X	X	X	0	1	0
75 mV	X	X	X	X	X	0	1	1
100 mV	X	X	X	X	X	1	0	0
125 mV	X	X	X	X	X	1	0	1
150 mV	X	X	X	X	X	1	1	0
175 mV	X	X	X	X	X	1	1	1
Address: 05h – STAT and timers control register – nonvolatile and volatile (mirror)								
STAT output polarity								
Active low	0	X	X	X	X	X	X	X
Active high	1	X	X	X	X	X	X	X
STAT output mode								
Indicates charging state	X	0	X	X	X	X	X	X
Indicates USB fail	X	1	X	X	X	X	X	X
STAT output control								
STAT output enabled (still allows IRQs)	X	X	0	X	X	X	X	X
STAT output disabled (still allows IRQs)	X	X	1	X	X	X	X	X
Other charger input current limit								
500 mA	X	X	X	0	X	X	X	X
HC settings	X	X	X	1	X	X	X	X
Complete charge timeout[2]								
192 min	X	X	X	X	0	0	X	X
384 min	X	X	X	X	0	1	X	X
768 min	X	X	X	X	1	0	X	X
1536 min	X	X	X	X	1	1	X	X
Precharge timeout[2]								
24 min	X	X	X	X	X	X	0	0
48 min	X	X	X	X	X	X	0	1
96 min	X	X	X	X	X	X	1	0
192 min	X	X	X	X	X	X	1	1
Address: 06h – Pin and enable control – nonvolatile and volatile (mirror)								
LED blinking function								
Disabled	0	X	X	X	X	X	X	X
Enabled	1	X	X	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Enable (EN) pin control								
I^2C control – 0 in command register disables charger	X	0	0	X	X	X	X	X
I^2C control – 0 in command register enables charger	X	0	1	X	X	X	X	X
Pin controls – active high	X	1	0	X	X	X	X	X
Pin controls – active low	X	1	1	X	X	X	X	X
USBCS control								
Register control	X	X	X	0	X	X	X	X
Pin control	X	X	X	1	X	X	X	X
USBCS input state								
Tristate input	X	X	X	X	0	X	X	X
Dual state input	X	X	X	X	1	X	X	X
Charger error								
Does not trigger IRQ	X	X	X	X	X	0	X	X
Triggers IRQ	X	X	X	X	X	1	X	X
APSD done								
Does not trigger IRQ	X	X	X	X	X	X	0	X
Triggers IRQ	X	X	X	X	X	X	1	X
USB fail low								
Valid in LV range (3.85 V < USBIN < LV_OV)	X	X	X	X	X	X	X	0
Valid in any charger range (3.38 V < USBIN < LV_OV or HV_UV < USBIN < HV_OV)	X	X	X	X	X	X	X	1
Address: 07h – THERM control A – nonvolatile and volatile (mirror)								
Minimum system voltage								
3.15 V	0	0	X	X	X	X	X	X
3.30 V	0	1	X	X	X	X	X	X
3.45 V	1	0	X	X	X	X	X	X
3.60 V	1	1	X	X	X	X	X	X
Load battery with 10 mA during float voltage compensation								
Disabled	X	X	0	X	X	X	X	X
Enabled	X	X	1	X	X	X	X	X
Thermistor monitor[3]								
Enabled	X	X	X	0	X	X	X	X
Disabled	X	X	X	1	X	X	X	X
Soft cold temp limit behavior[4]								
No response	X	X	X	X	0	0	X	X
Charge current compensation	X	X	X	X	0	1	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Float voltage compensation	X	X	X	X	1	0	X	X
Charge current and float voltage compensation	X	X	X	X	1	1	X	X
Soft hot temp limit behavior[4]								
No response	X	X	X	X	X	X	0	0
Charge current compensation	X	X	X	X	X	X	0	1
Float voltage compensation	X	X	X	X	X	X	1	0
Charge current and float voltage compensation	X	X	X	X	X	X	1	1
Address: 08h – Watchdog and safety timer control – nonvolatile and volatile (mirror)								
AICL fail behavior option								
AICL fail forces suspend mode	0	X	X	X	X	X	X	X
AICL fail forces 150 mA input current limit	1	X	X	X	X	X	X	X
Watchdog timer								
18 s	X	0	0	X	X	X	X	X
36 s	X	0	1	X	X	X	X	X
72 s	X	1	X	X	X	X	X	X
Safety timer after watchdog IRQ								
12 min	X	X	X	0	0	X	X	X
24 min	X	X	X	0	1	X	X	X
48 min	X	X	X	1	0	X	X	X
96 min	X	X	X	1	1	X	X	X
Watchdog IRQ safety timer								
Disabled	X	X	X	X	X	0	X	X
Enabled	X	X	X	X	X	1	X	X
Watchdog option								
Run ACK after reload	X	X	X	X	X	X	0	X
Run ACK always	X	X	X	X	X	X	1	X
Watchdog timer								
Disabled	X	X	X	X	X	X	X	0
Enabled	X	X	X	X	X	X	X	1
Address: 09h – OTG and USBIN AICL control – nonvolatile and volatile (mirror)								
OTG/ID pin control								
RID disabled, OTG I^2C control	0	0	X	X	X	X	X	X
RID disabled, OTG pin control	0	1	X	X	X	X	X	X
RID enabled, OTG I^2C control	1	0	X	X	X	X	X	X
RID enabled, auto OTG	1	1	X	X	X	X	X	X
OTG pin polarity								
Active low	X	X	0	X	X	X	X	X
Active high	X	X	1	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AICL LV collapse rising edge glitch filter configuration								
5 ms glitch filter	X	X	X	X	X	0	X	X
15 µs glitch filter	X	X	X	X	X	1	X	X
AICL collapse with high voltage charger								
Input collapse disables charging	X	X	X	X	X	X	0	X
Input collapse disables charging and input FET	X	X	X	X	X	X	1	X
AICL collapse with low voltage or unregulated charger								
Input collapse disables charging	X	X	X	X	X	X	X	0
Input collapse disables charging and input FET	X	X	X	X	X	X	X	1
Address: 0Ah – OTG and TLIM control – nonvolatile and volatile (mirror)								
Switching frequency (3 MHz operation is only available for 5 V input voltage operation)								
750 kHz	0	0	X	X	X	X	X	X
1.0 MHz	0	1	X	X	X	X	X	X
1.5 MHz	1	0	X	X	X	X	X	X
3.0 MHz	1	1	X	X	X	X	X	X
Digital thermal regulation temperature threshold								
100 °C	X	X	0	0	X	X	X	X
110 °C	X	X	0	1	X	X	X	X
120 °C	X	X	1	0	X	X	X	X
130 °C	X	X	1	1	X	X	X	X
OTG current limit at DCIN								
1800 mA	X	X	X	X	0	0	X	X
500 mA	X	X	X	X	0	1	X	X
750 mA	X	X	X	X	1	0	X	X
1000 mA	X	X	X	X	1	1	X	X
OTG battery UVLO threshold								
2.7 V	X	X	X	X	X	X	0	0
2.9 V	X	X	X	X	X	X	0	1
3.1 V	X	X	X	X	X	X	1	0
3.3 V	X	X	X	X	X	X	1	1
Address: 0Bh – Hard/soft limit cell temperature monitor 8-bit – nonvolatile and volatile (mirror)								

		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hard limit cold temperature alarm trip point (β = 3750)									
Temperature	V_{THERM} % VSYSON								
+10 °C	0.665	0	0	X	X	X	X	X	X
+5 °C	0.715	0	1	X	X	X	X	X	X
0 °C	0.760	1	0	X	X	X	X	X	X
-5 °C	0.805	1	1	X	X	X	X	X	X

		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hard limit hot temperature alarm trip point (β = 3750)									
Temperature	V_{THERM} % VSYSON								
+50 °C	0.276	X	X	0	0	X	X	X	X
+55 °C	0.242	X	X	0	1	X	X	X	X
+60 °C	0.212	X	X	1	0	X	X	X	X
+65 °C	0.185	X	X	1	1	X	X	X	X
Soft limit cold temperature alarm trip point (β = 3750)									
Temperature	V_{THERM} % VSYSON								
+15 °C	0.610	X	X	X	X	0	0	X	X
+10 °C	0.665	X	X	X	X	0	1	X	X
+5 °C	0.715	X	X	X	X	1	0	X	X
0 °C	0.760	X	X	X	X	1	1	X	X
Soft limit hot temperature alarm trip point (β = 3750)									
Temperature	V_{THERM} % VSYSON								
+40 °C	0.356	X	X	X	X	X	X	0	0
+45 °C	0.315	X	X	X	X	X	X	0	1
+50 °C	0.276	X	X	X	X	X	X	1	0
+55 °C	0.242	X	X	X	X	X	X	1	1
Address: 0Ch – FAULT interrupt register – nonvolatile and volatile (mirror)									
Hot/cold hard limit									
Does not trigger IRQ		0	X	X	X	X	X	X	X
Triggers IRQ		1	X	X	X	X	X	X	X
Hot/cold soft limit									
Does not trigger IRQ		X	0	X	X	X	X	X	X
Triggers IRQ		X	1	X	X	X	X	X	X
Battery UVLO (OTG fail) in OTG mode									
Does not trigger IRQ		X	X	0	X	X	X	X	X
Triggers IRQ		X	X	1	X	X	X	X	X
OTG OC									
Does not trigger IRQ		X	X	X	0	X	X	X	X
Triggers IRQ		X	X	X	1	X	X	X	X
Input OVLO									
Does not trigger IRQ		X	X	X	X	0	X	X	X
Triggers IRQ		X	X	X	X	1	X	X	X
Input UVLO									
Does not trigger IRQ		X	X	X	X	X	0	X	X
Triggers IRQ		X	X	X	X	X	1	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AICL failed								
Does not trigger IRQ	X	X	X	X	X	X	0	X
Triggers IRQ	X	X	X	X	X	X	1	X
Internal over-temperature condition								
Does not trigger IRQ	X	X	X	X	X	X	X	0
Triggers IRQ	X	X	X	X	X	X	X	1
Address: 0Dh – STATUS interrupt register – nonvolatile and volatile (mirror)								
Charge timeout or precharge timeout								
Does not trigger IRQ	0	X	X	X	X	X	X	X
Triggers IRQ	1	X	X	X	X	X	X	X
RID charge								
Does not trigger IRQ	X	0	X	X	X	X	X	X
Triggers IRQ	X	1	X	X	X	X	X	X
Battery OVP								
Does not trigger IRQ	X	X	0	X	X	X	X	X
Triggers IRQ	X	X	1	X	X	X	X	X
Fast, term, taper, recharge, or inhibit								
Does not trigger IRQ	X	X	X	0	X	X	X	X
Triggers IRQ	X	X	X	1	X	X	X	X
Watchdog timer								
Does not trigger IRQ	X	X	X	X	0	X	X	X
Triggers IRQ	X	X	X	X	1	X	X	X
POK								
Does not trigger IRQ	X	X	X	X	X	0	X	X
Triggers IRQ	X	X	X	X	X	1	X	X
Missing battery								
Does not trigger IRQ	X	X	X	X	X	X	0	X
Triggers IRQ	X	X	X	X	X	X	1	X
Low battery								
Does not trigger IRQ	X	X	X	X	X	X	X	0
Triggers IRQ	X	X	X	X	X	X	X	1
Address: 0Eh – Various functions – nonvolatile and volatile (mirror)								
Charging hold-off timer after plugin								
700 µs	0	X	X	X	X	X	X	X
350 ms	1	X	X	X	X	X	X	X
Charger inhibit								
Disabled	X	0	X	X	X	X	X	X
Enabled	X	1	X	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Fast charge current compensation in battery pack soft limit mode								
500 mA	X	X	0	X	X	X	X	X
1000 mA	X	X	1	X	X	X	X	X
Float voltage compensation level in battery pack soft limit mode[4]								
VFLT - 60 mV	X	X	X	0	0	X	X	X
VFLT - 120 mV	X	X	X	0	1	X	X	X
VFLT - 180 mV	X	X	X	1	0	X	X	X
VFLT - 240 mV	X	X	X	1	1	X	X	X
Hard temperature limit behavior								
Charging is suspended when battery temperature is outside hard limits	X	X	X	X	X	0	X	X
Charging is not suspended when battery temperature is outside hard limits	X	X	X	X	X	1	X	X
Precharge to fast charge (based on command bit)								
Automatic	X	X	X	X	X	X	0	X
Requires command bit	X	X	X	X	X	X	1	X
STAT pin configuration								
Charging status and pulsed IRQ	X	X	X	X	X	X	X	0
Static IRQ output	X	X	X	X	X	X	X	1
Address: 10h – FlexCharge+ register – nonvolatile and volatile (mirror)								
AFVC IRQ								
Does not assert an IRQ signal	0	X	X	X	X	X	X	X
Asserts an IRQ signal	1	X	X	X	X	X	X	X
Charger configuration (use with register 15h [7:6])								
5 V with register 14h [7:6] = 00	X	0	0	0	X	X	X	X
9 V with register 14h [7:6] = 01	X	0	1	0	X	X	X	X
5 V and 9 V with register 14h [7:6] = 01	X	0	1	1	X	X	X	X
12 V with register 14h [7:6] = 01	X	1	0	0	X	X	X	X
5 V and 12 V with register 14h [7:6] = 01	X	1	0	1	X	X	X	X
9–12 V with register 14h [7:6] = 01	X	1	1	0	X	X	X	X
5 V and 9–12 V with register 14h [7:6] = 01	X	1	1	1	X	X	X	X
5 V or 5 V unregulated [5] with register 14h [7:6] = 01	X	0	0	X	X	X	X	X
5 V, 5 V unregulated, or 9 V with register 14h [7:6] = 01	X	0	1	X	X	X	X	X
5 V, 5 V unregulated, or 12 V with register 14h [7:6] = 01	X	1	0	X	X	X	X	X
5 V, 5 V unregulated, or 9–12 V with register 14h [7:6] = 01	X	1	1	X	X	X	X	X
5–9 V with register 14h [7] = 1	X	0	X	X	X	X	X	X
5–12 V with register 14h [7] = 1	X	1	X	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Low-battery/SYSOK voltage detection threshold								
Disabled	X	X	X	X	0	0	0	0
2.50 V	X	X	X	X	0	0	0	1
2.60 V	X	X	X	X	0	0	1	0
2.70 V	X	X	X	X	0	0	1	1
2.80 V	X	X	X	X	0	1	0	0
2.90 V	X	X	X	X	0	1	0	1
3.00 V	X	X	X	X	0	1	1	0
3.10 V	X	X	X	X	0	1	1	1
3.70 V	X	X	X	X	1	0	0	0
2.88 V	X	X	X	X	1	0	0	1
3.00 V	X	X	X	X	1	0	1	0
3.10 V	X	X	X	X	1	0	1	1
3.25 V	X	X	X	X	1	1	0	0
3.35 V	X	X	X	X	1	1	0	1
3.46 V	X	X	X	X	1	1	1	0
3.58 V	X	X	X	X	1	1	1	1
Address: 11h – Various functions – nonvolatile and volatile (mirror)								
Safety timer enable								
Precharge safety timer and total charge safety timer enabled	0	0	X	X	X	X	X	X
Precharge safety timer disabled, total charge safety timer enabled	0	1	X	X	X	X	X	X
Precharge safety timer and total charge safety timer disabled	1	X	X	X	X	X	X	X
Block suspend during VBATT LOW								
Disabled	X	X	0	X	X	X	X	X
Enabled	X	X	1	X	X	X	X	X
Timeout select for APSD								
660 ms	X	X	X	0	X	X	X	X
330 ms	X	X	X	1	X	X	X	X
SDP suspend								
Normal SPD operation	X	X	X	X	0	X	X	X
SDP enters suspend	X	X	X	X	1	X	X	X
Quick Charge 3.0 auto increment mode								
Disabled	X	X	X	X	X	0	X	X
Enabled	X	X	X	X	X	1	X	X
Quick Charge 3.0 authentication algorithm								
Disabled	X	X	X	X	X	X	0	X
Enabled	X	X	X	X	X	X	1	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DCD								
Enabled	X	X	X	X	X	X	X	0
Disabled	X	X	X	X	X	X	X	1
Address: 12h – HVDCP and battery missing control 8-bit – nonvolatile and volatile (mirror)								
HVDCP adapter select								
5 V	0	0	X	X	X	X	X	X
9 V	0	1	X	X	X	X	X	X
12 V	1	X	X	X	X	X	X	X
HVDCP								
Disabled	X	X	0	X	X	X	X	X
Enabled	X	X	1	X	X	X	X	X
Unused								
Unused	X	X	X	0	X	X	X	X
Battery missing on input plugin								
Disabled	X	X	X	X	0	X	X	X
Enabled	X	X	X	X	1	X	X	X
Battery missing algorithm								
Disabled	X	X	X	X	X	X	0	X
Enabled	X	X	X	X	X	X	1	X
Battery missing THERM pin source								
Disabled	X	X	X	X	X	X	X	0
Enabled	X	X	X	X	X	X	X	1
Address: 13h – PON options – nonvolatile and volatile (mirror)								
SYSOK/INOK polarity								
Normal output	0	X	X	X	X	X	X	X
Invert output	1	X	X	X	X	X	X	X
SYSOK options								
INOK option 1	X	0	0	0	X	X	X	X
INOK option 2	X	0	0	1	X	X	X	X
SYSOK option A, option 1	X	0	1	0	X	X	X	X
SYSOK option A, option 2	X	0	1	1	X	X	X	X
SYSOK option B, option 1	X	1	0	0	X	X	X	X
SYSOK option B, option 2	X	1	0	1	X	X	X	X
Charge detect option 1	X	1	1	0	X	X	X	X
Charge detect option 2	X	1	1	1	X	X	X	X
Input missing poller configuration								
Disabled	X	X	X	X	0	X	X	X
Enabled (default)	X	X	X	X	1	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VBATT LOW disabled or reset sate								
Assume VBATT is not low	X	X	X	X	X	0	X	X
Assume VBATT is low	X	X	X	X	X	1	X	X
Quick Charge 3.0 authentication IRQ								
Enabled	X	X	X	X	X	X	X	1
Disabled	X	X	X	X	X	X	X	0
Address: 14h – OTG mode power options – nonvolatile and volatile (mirror)								
Adapter configuration use with register 10h [6:4]								
Unregulated 5 V disabled	0	0	X	X	X	X	X	X
Unregulated 5 V enabled	0	1	X	X	X	X	X	X
Continuous mode (see register 10h [6:4])	1	X	X	X	X	X	X	X
Adapter identification use for HVDCP								
Disabled (default)	X	X	0	X	X	X	X	X
Enabled	X	X	1	X	X	X	X	X
SDP low battery forces USB5 over USB1								
Disabled (default)	X	X	X	0	X	X	X	X
Enabled	X	X	X	1	X	X	X	X
Unused								
Unused	X	X	X	X	0	X	X	X
Unused	X	X	X	X	1	X	X	X
OTG hiccup mode								
Disabled	X	X	X	X	X	0	X	X
Enabled	X	X	X	X	X	1	X	X
Adapter identification mode								
Normal mode	X	X	X	X	X	X	0	0
Mode 1	X	X	X	X	X	X	0	1
Mode 2	X	X	X	X	X	X	1	0
Mode 3	X	X	X	X	X	X	1	1

Notes:

1. May be derated by input current limit setting (see Figure 2-6, Chapter 4, and Section 7.1). Also see note 12 from Chapter 4.
2. All timer durations remain the same, independent of the frequency selection.
3. When the battery pack temperature is outside the hard limits and a thermal monitor is enabled, charging is automatically suspended until the battery pack temperature falls below the corresponding threshold.
4. When the battery pack temperature is outside the soft limits, the float voltage or the charge current (depending on selection) are automatically adjusted to the float voltage or the charge current compensation values.

Table 5-2 Nonvolatile registers (read only and programmable in OTP)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 15h – Factory settings								
Disable AFVC when entering taper								
AFVC enabled in taper [IRQ from termination]	X	X	X	X	0	X	X	X
AFVC disabled in taper [IRQ from taper]	X	X	X	X	1	X	X	X
VCHG IINV								
VCHG measures charge current	0	X	X	X	X	0	X	X
VCHG measures input current	1	X	X	X	X	1	X	X
AFVC override								
AFVC enabled	X	X	X	X	X	X	0	X
AFVC disabled	X	X	X	X	X	X	1	X
SYSOK pin configuration								
Open drain	X	X	X	X	X	X	X	0
Push-pull	X	X	X	X	X	X	X	1
Address: 16h – I^2C bus/slave address 8-bit								
I^2C slave address								
0000	0	0	0	0	X	X	X	X
0001	0	0	0	1	X	X	X	X
0010	0	0	1	0	X	X	X	X
0011	0	0	1	1	X	X	X	X
0100	0	1	0	0	X	X	X	X
0101	0	1	0	1	X	X	X	X
0110	0	1	1	0	X	X	X	X
0111	0	1	1	1	X	X	X	X
1000	1	0	0	0	X	X	X	X
1001	1	0	0	1	X	X	X	X
1010	1	0	1	0	X	X	X	X
1011	1	0	1	1	X	X	X	X
1100	1	1	0	0	X	X	X	X
1101	1	1	0	1	X	X	X	X
1110	1	1	1	0	X	X	X	X
1111	1	1	1	1	X	X	X	X
I^2C bus address								
000	X	X	X	X	0	0	0	X
001	X	X	X	X	0	0	1	X
010	X	X	X	X	0	1	0	X
011	X	X	X	X	0	1	1	X
100	X	X	X	X	1	0	0	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
101	X	X	X	X	1	0	1	X
110	X	X	X	X	1	1	0	X
111	X	X	X	X	1	1	1	X
Volatile write permission								
Allow volatile writes	X	X	X	X	X	X	X	0
Prevents volatile writes	X	X	X	X	X	X	X	1
Address: 1Ch – Factory settings								
Vsys tracking voltage								
+50 mV	X	X	X	X	X	0	1	1
+100 mV	X	X	X	X	X	1	1	0
Address: 25h – Factory settings								
INOK selection source								
Input FET on	X	0	X	X	X	X	X	X
Input valid	X	1	X	X	X	X	X	X
Address: 27h – Factory settings								
Quick Charge 3.0 optimization algorithm								
Advanced optimization algorithm	X	0	X	X	X	X	X	X
Conservative algorithm	X	1	X	X	X	X	X	X
System short circuit protection								
Enabled	X	X	X	0	X	X	X	X
Disabled	X	X	X	1	X	X	X	X
Address: 28h – Factory settings								
Dead battery timer								
Enabled	X	X	0	X	X	X	X	X
Disabled	X	X	1	X	X	X	X	X
Reload on unplug								
Enabled	X	X	X	0	X	X	X	X
Disabled	X	X	X	1	X	X	X	X
Address: 2Ch – Factory settings								
Re-run AICL								
Disabled	X	X	X	0	X	X	X	X
Enabled	X	X	X	1	X	X	X	X
Address: 2Dh – Factory settings								
SYSOK assertion timing								
SYSOK option B1 waits for BMA result	X	X	X	X	X	X	0	X
SYSOK option B1 does not wait for BMA result	X	X	X	X	X	X	1	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 2Eh – Factory settings								
HV OTG protection								
Disabled	0	X	X	X	X	X	X	X
Enabled	1	X	X	X	X	X	X	X

Table 5-3 Command and status registers 30h–46h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 30h – Command register I^2C								
Command reload	1	X	X	X	X	X	X	X
BQ configuration access	X	1	X	X	X	X	X	X
Not used	X	X	0	0	0	0	0	0
Address: 31h – Command register IL								
Command override								
Turn off battery FET (only if register 2h [6] = 1)	1	X	X	X	X	X	X	X
Suspend mode (this bit has no effect if register 02h [7] = 0)								
Normal	X	0	X	X	X	X	X	X
Suspend	X	1	X	X	X	X	X	X
Not used								
Not used	X	X	0	0	X	X	X	X
Input current mode								
Use APSD results for input current mode	X	X	X	X	0	X	X	X
Use command register for input current mode	X	X	X	X	1	X	X	X
USB 2/3 select (this bit has no effect if register 01h [1] = 1)								
USB2 (100 mA/500 mA current limits)	X	X	X	X	X	0	X	X
USB3 (150 mA/900 mA current limits)	X	X	X	X	X	1	X	X
USB1/5/AC control (only is register 06h [4] = 1)								
USB 100 mode with register 01h [0] = 0 USB 500 mode with register 01h [0] = 1	X	X	X	X	X	X	0	0
USB 500 mode with register 01h [0] = 0 USB 100 mode with register 01h [0] = 1	X	X	X	X	X	X	1	0
USB AC mode	X	X	X	X	X	X	X	1
Address: 32h – Command register CHG								
Not used	0	0	0	X	X	X	X	X
Thermistor monitor disable command	X	X	X	1	X	X	X	X
Turn off STAT pin (still allows pulsed IRQ's)	X	X	X	X	1	X	X	X
Pre to fast enable (only with register 0eh [1] = 1)	X	X	X	X	X	1	X	x

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Charge enabled (polarity from register 06h [5]) This bit has no effect if register 06h [6] = 1	X	X	X	X	X	X	1	X
OTG enabled This bit has no effect if register 09h [6] = 1	X	X	X	X	X	X	X	1
Address: 33h – Command register (write only)								
Stop dead battery timer								
Stop dead battery timer	X	X	X	X	X	X	X	X
Address: 34h – Command register HVDCP								
APSD rerun (self-clearing)								
Rerun APSD	1	X	X	X	X	X	X	X
Quick Charge 3.0 Commands								
Force Quick Charge 2.0 mode	X	X	1	X	X	X	X	X
Quick Charge 3.0 auto increment mode	X	X	X	1	X	X	X	X
Unused	X	X	X	X	1	X	X	X
Decrement 200 mV	X	X	X	X	X	1	X	X
Unused	X	X	X	X	X	X	1	X
Increment 200 mV	X	X	X	X	X	X	X	1
Address: 36h –Status register								
AICL status								
Not done	0	X	X	X	X	X	X	X
Done	1	X	X	X	X	X	X	X
Input current limit								
High current	X	0	0	X	X	X	X	X
USB100 mode	X	0	1	X	X	X	X	X
USB500 mode	X	1	0	X	X	X	X	X
Reserved	X	1	1	X	X	X	X	X
DCIN input current limit status								
Suspend	X	X	X	1	X	X	X	X
500 mA	X	X	X	0	0	0	0	0
685 mA	X	X	X	0	0	0	0	1
1000 mA	X	X	X	0	0	0	1	0
1100 mA	X	X	X	0	0	0	1	1
1200 mA	X	X	X	0	0	1	0	0
1300 mA	X	X	X	0	0	1	0	1
1500 mA	X	X	X	0	0	1	1	0
1600 mA	X	X	X	0	0	1	1	1
1700 mA	X	X	X	0	1	0	0	0
1800 mA	X	X	X	0	1	0	0	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2000 mA	X	X	X	0	1	0	1	0
2200 mA	X	X	X	0	1	0	1	1
2500 mA	X	X	X	0	1	1	0	0
3000 mA	X	X	X	0	1	1	0	1
Address: 37h – Status register 1								
Input range								
12 V	1	X	X	X	X	X	X	X
5–9 V	X	1	X	X	X	X	X	X
9 V	X	X	1	X	X	X	X	X
5 V	X	X	X	1	X	X	X	X
Address: 38h – Status register 2								
Unused	1	X	X	X	X	X	X	X
Unused	X	1	X	X	X	X	X	X
Float voltage (after compensation)								
3.5 V	X	X	0	0	0	0	0	0
3.52 V	X	X	0	0	0	0	0	1
….	….	….	….	….	….	….	….	….
4.48 V	X	X	1	1	0	0	0	1
4.50 V	X	X	1	1	0	0	1	0
….	….	….	….	….	….	….	….	….
4.50 V	X	X	1	1	1	1	1	1
Address: 39h – Status register 3								
Charging status								
Not fast charging	0	X	X	X	X	X	X	X
Fast charging	1	X	X	X	X	X	X	X
Precharge current (after compensation)								
200 mA	0	0	0	0	0	0	0	0
300 mA	X	0	0	1	X	X	X	X
400 mA	X	0	1	0	X	X	X	X
500 mA	X	0	1	1	X	X	X	X
600 mA	X	1	0	0	X	X	X	X
700 mA	X	1	0	1	X		XX	X
Fast charge current (after compensation)								
1000 mA	X	X	X	0	0	0	0	0
1200 mA	X	X	X	1	0	0	0	1
1400 mA	X	X	X	X	0	0	1	0
1600 mA	X	X	X	X	0	0	1	1
1800 mA	X	X	X	X	0	1	0	0
2000 mA	X	X	X	X	0	1	0	1
2200 mA	X	X	X	X	0	1	1	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2400 mA	X	X	X	X	0	1	1	1
2600 mA	X	X	X	X	1	0	0	0
2800 mA	X	X	X	X	1	0	0	1
3000 mA	X	X	X	X	1	0	1	0
3400 mA	X	X	X	X	1	0	1	1
3600 mA	X	X	X	X	1	1	0	0
3800 mA	X	X	X	X	1	1	0	1
4000 mA	X	X	X	X	1	1	1	0
4640 mA	X	X	X	X	1	1	1	1
Address: 3Ah – Status register 4								
OTG status								
OTG switcher disabled	0	X	X	X	X	X	X	X
OTG switcher enabled	1	X	X	X	X	X	X	X
Automatic float voltage compensation status								
Inactive	X	0	X	X	X	X	X	X
Active	X	1	X	X	X	X	X	X
Done status								
No charging cycles have terminated since charging first enabled	X	X	0	X	X	X	X	X
At least 1 charging cycle has terminated since charging first enabled	X	X	1	X	X	X	X	X
Battery voltage < 2 V status								
False	X	X	X	0	X	X	X	X
True	X	X	X	1	X	X	X	X
Hold-off status								
Inactive	X	X	X	X	0	X	X	X
Active	X	X	X	X	1	X	X	X
Charging status								
Not charging	X	X	X	X	X	0	0	X
Precharging	X	X	X	X	X	0	1	X
Fast charging	X	X	X	X	X	1	0	X
Taper charging	X	X	X	X	X	1	1	X
Charge enabled								
Not asserted	X	X	X	X	X	X	X	0
Asserted	X	X	X	X	X	X	X	1
Address: 3Bh – Status register 5								
Source detected								
Charging downstream port	1	X	X	X	X	X	X	X
Dedicated charging port	X	1	X	X	X	X	X	X
Other charging port	X	X	1	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Standard downstream port	X	X	X	1	X	X	X	X
ACA-A charging port	X	X	X	X	1	X	X	X
ACA-B charging port	X	X	X	X	X	1	X	X
ACA-C charging port	X	X	X	X	X	X	1	X
ACA dock	X	X	X	X	X	X	X	1
Address: 3Ch – Status register 6								
Data connect device timeout								
Not active	0	X	X	X	X	X	X	X
Active	1	X	X	X	X	X	X	X
RID_FLOAT state-machine								
Not detected	X	X	X	X	0	X	X	X
Detected	X	X	X	X	1	X	X	X
RID_A state-machine								
Not detected	X	X	X	X	X	0	X	X
Detected	X	X	X	X	X	1	X	X
RID_B state-machine								
Not detected	X	X	X	X	X	X	0	X
Detected	X	X	X	X	X	X	1	X
RID_C state-machine								
Not detected	X	X	X	X	X	X	X	0
Detected	X	X	X	X	X	X	X	1
Address: 3Dh – Status register 7								
HVDCP_STATUS								
12 V HVDCP	X	X	X	X	1	X	X	X
9 V HVDCP	X	X	X	X	X	1	X	X
5 V HVDCP	X	X	X	X	X	X	1	X
Address: 3Eh – Status register 8								
Not used								
Not used	0	0	X	X	X	X	X	X
USBIN_HV_INPUT								
Not selected	X	X	0	X	X	X	X	X
HV USBIN charger selected	X	X	1	X	X	X	X	X
USBIN_LV_UNREG_INPUT								
Not selected	X	X	X	0	X	X	X	X
Unregulated charger detected	X	X	X	1	X	X	X	X
USBIN_LV_INPUT								
Not selected	X	X	X	X	0	X	X	X
5 V or 5–9 V USBIN charger detected	X	X	X	X	1	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not used								
Not used	X	X	X	X	X	0	0	0
Address: 3Fh – Revision control								
GUI revision								
Rev. 0	0	0	0	0	X	X	X	X
Device revision								
Device rev. 1.0	X	X	X	X	X	X	0	0
Device rev. 2.0	X	X	X	X	X	X	0	1
Device rev. 2.1	X	X	X	X	X	X	1	1
Address: 40h – IRQ-A								
Hot hard limit								
Triggered IRQ	1	X	X	X	X	X	X	X
Status	X	1	X	X	X	X	X	X
Cold hard limit								
Triggered IRQ	X	X	1	X	X	X	X	X
Status	X	X	X	1	X	X	X	X
Hot soft limit								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X
Cold soft limit								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1
Address: 41h – IRQ_B								
Battery terminal removed								
Triggered IRQ	1	X	X	X	X	X	X	X
Status	X	1	X	X	X	X	X	X
Battery missing from pin								
Triggered IRQ	X	X	1	X	X	X	X	X
Status	X	X	X	1	X	X	X	X
Low battery voltage								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X
Internal temperature limit								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1
Address: 42h – IRQ_C								
Pre to fast voltage								
Triggered IRQ	1	X	X	X	X	X	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	X	1	X	X	X	X	X	X
Recharge								
Triggered IRQ	X	X	1	X	X	X	X	X
Status	X	X	X	1	X	X	X	X
Taper								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X
Termination								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1
Address: 43h – IRQ_D								
Battery OV								
Triggered IRQ	1	X	X	X	X	X	X	X
Status	X	1	X	X	X	X	X	X
Charger error								
Triggered IRQ	X	X	1	X	X	X	X	X
Status	X	X	X	1	X	X	X	X
Charge timeout								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X
Precharge timeout								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1
Address: 44h – IRQ_E								
USBIN OV								
Triggered IRQ	1	X	X	X	X	X	X	X
Status	X	1	X	X	X	X	X	X
USBIN UV								
Triggered IRQ	X	X	1	X	X	X	X	X
Status	X	X	X	1	X	X	X	X
Automatic float voltage compensation								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X
Power OK								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 45h – IRQ_F								
OTG over current (requires toggling to re-enable)								
Triggered IRQ	1	X	X	X	X	X	X	X
Status	X	1	X	X	X	X	X	X
OTG fail								
Triggered IRQ	X	X	1	X	X	X	X	X
Status	X	X	X	1	X	X	X	X
RID change								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X
OTG OC retry								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1
Address: 46h – IRQ_G								
Source detect status								
Triggered IRQ	1	X	X	X	X	X	X	X
Status	X	1	X	X	X	X	X	X
AICL done								
Triggered IRQ	X	X	1	X	X	X	X	X
Status	X	X	X	1	X	X	X	X
AICL failed								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X
Charge inhibit								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1
Address: 47h – IRQ_G								
Unused								
Triggered IRQ	1	X	X	X	X	X	X	X
Status	X	1	X	X	X	X	X	X
Input current limiting								
Status	X	X	1	X	X	X	X	X
Quick Charge 3.0 detected								
Status	X	X	X	1	X	X	X	X
Quick Charge 3.0 authentication done								
Triggered IRQ	X	X	X	X	1	X	X	X
Status	X	X	X	X	X	1	X	X

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Watchdog timeout								
Triggered IRQ	X	X	X	X	X	X	1	X
Status	X	X	X	X	X	X	X	1

6 I²C programming information

6.1 Serial interface

Access to the configuration registers, general purpose memory, and command and status registers is carried out over an industry standard two-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers, SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used to generate a start and stop condition that precede and end most transactions on the serial bus. A high to low transition of SDA when SCL is high is considered a start condition while a low to high transition of SDA when SCL is high is considered a stop condition.

The interface protocol allows the operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 7-bit device type identifier (slave address). The remaining bit indicates either a read or a write operation. See the Table 2-1, Table 2-2, and Table 2-3 for a description of the address bytes used by the SMB1350/SMB1351 device.

The device type identifier for the memory array, the configuration registers, and the command and status registers, are accessible with the same slave address. The slave address is programmed to any seven bit number 0000000_{BIN} through 1111111_{BIN}.

6.2 Write

Writing to the memory or a configuration register is illustrated in Figure 4-1 and Figure 4-2. A start condition followed by the slave address byte is provided by the host; the SMB1350/SMB1351 device responds with an acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMB1350/SMB1351 device responds with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data are clocked in by the host to write to the consecutive addresses within the same page. After the last byte is clocked in and the host receives an acknowledge, a stop condition must be issued to initiate the nonvolatile write operation.

6.3 Read

The address pointer for the nonvolatile configuration registers, memory registers, the volatile command, and the status registers, must be set before data is read from the SMB1350/SMB1351 device. This is set by issuing a dummy write command, which is a write command that is not followed by a stop condition. A dummy write command sets the address from which data is read. After the dummy write command is issued, a start command followed by the address byte is sent

from the host. The host waits for an acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes are clocked out of the consecutive addresses with the host providing an acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the acknowledge clock cycle and then issuing a stop condition. See Figure 4-3 for an illustration of the read sequence.

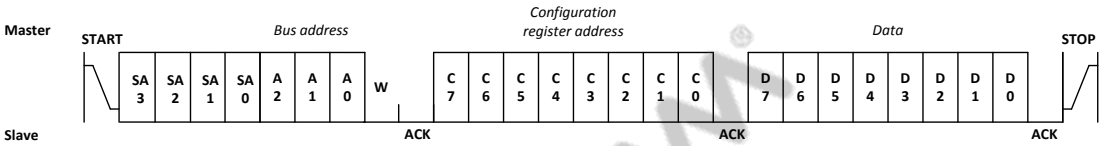

Figure 6-1 Register byte write

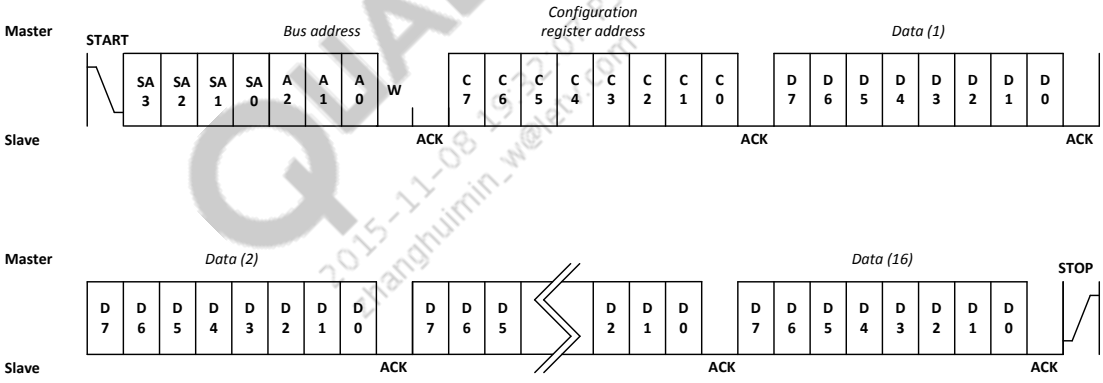

Figure 6-2 Register page write

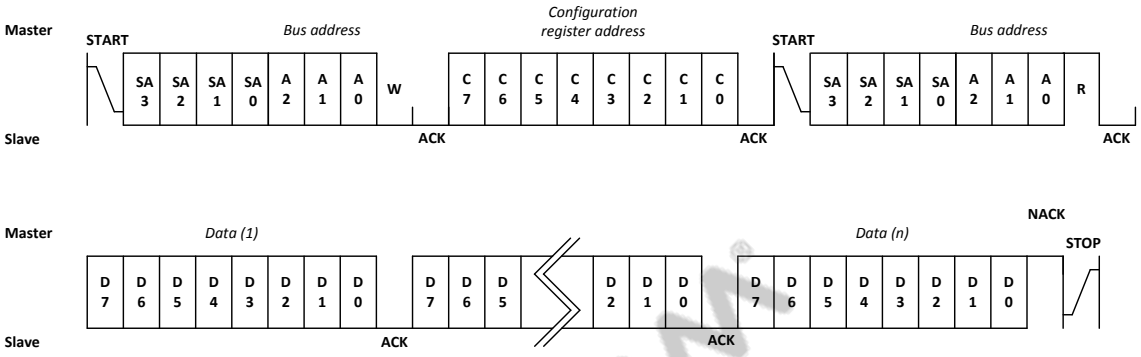

Figure 6-3 Register read

6.4 Device memory structure

The memory structure for the SMB1350/SMB1351 is composed of four sections; configuration, trim, command, and status registers. The configuration registers are further divided into volatile and nonvolatile, or factory-programmable, register banks.

The volatile registers can be written to and read from using standard I^2C commands and are used to change charging and system parameters on the fly. These can include charge currents, float voltage, and many other parameters. The register contents will remain in the volatile memory as long as there is power on the input or the battery output. However, when an input is removed, the settings will revert back to their default OTP configuration. The nonvolatile register bank cannot be modified or written to but can be selected when defining default OTP configurations. Refer to the *SMB1350/SMB1351 Evaluation User Guide* for instructions on how to select default OTP configurations.

The trim registers are programmed by QTI and unavailable to external parties.

The command registers control immediate actions of the part, such as enabling or disabling charging. These registers can be written to and read from and are reset to all zeros when the input is removed.

Status registers give real time information as to what is happening in the system. Various status and fault registers include charge state (pre-charge, fast-charge, or taper), various errors, and input power source information.

7 Detailed device operation

7.1 Device operation

The SMB1350/SMB1351 device is a fully programmable battery charger and system power manager for designs utilizing single cell Li-Ion and Li-Polymer battery packs. The device high efficiency, switch mode operation reduces heat dissipation and allows higher current capability for a given package size – up to 4.5 A to the battery and/or the system. The SMB1350/SMB1351 device provides four main charging phases: trickle charge, preconditioning (precharge), constant (fast charge) current, and constant voltage. The device is used with a USB or an AC/DC input power source. The main battery charging and system power parameters are programmable, allowing high design flexibility and sophisticated battery and system management.

High input voltage tolerance (22 V) and multiple safety features increase the system and the battery reliability. A programmable battery pack thermal monitor allows charge suspension, system notification, and charge current or float voltage compensation, during extreme temperature conditions. Additional safety functions include safety timers, input and battery over-voltage protection, IC thermal monitoring, and status/fault interrupts.

The SMB1350/SMB1351 device manages two outputs independently: battery charging and system power. This allows immediate system operation even under missing or deeply discharged battery conditions. The SMB1350/SMB1351 device supports load peaks by supplementing current from the battery when the input source is overloaded. The device supports USB OTG devices by providing the necessary power (+5.0 V at up to 1800 mA) without any additional external components. The SMB1350/SMB1351 device supports USB-IF-defined ACA by eliminating the need for additional hardware and software for the system.

7.1.1 Power supply

The SMB1350/SMB1351 device is powered from an input voltage between 3.6–14 V, applied between the DCIN pin and ground. The voltage on the DCIN pin is monitored by UVLO and OVLO circuits, preventing the charger from turning on when the voltage at this node is less than the UVLO threshold or greater than the OVLO threshold. A third and optional threshold (USB OK) exists for the input voltage to detect the USB input source collapse because of the high load current. In this case, the SMB1350/SMB1351 device indicates the condition via the STAT output. When the input supply is removed, the SMB1350/SMB1351 device enters a low power mode, exhibiting a very low discharge leakage current and extending the battery life. During this mode, charging is automatically disabled.

The minimum battery voltage to keep the volatile memory alive, without any input power source connected to DCIN, is approximately 2.5 V (falling) with a hysteresis of approximately 200 mV.

NOTE: The input OV, UV, and the battery OV fault bits, are not active when the charger is disabled.

7.1.2 Automatic input prebias

The SMB1350/SMB1351 device incorporates a 60 mA automatic prebias that allows the voltage of loosely regulated adapters to be nominal and suitable for battery charging. Such power sources (e.g., wall adapters, wireless pads, etc.) may not be preloaded in the adapter itself for reducing quiescent current when the adapter is plugged into a wall, but is unloaded. The 60 mA load is enabled when the input voltage at the DCIN pin is higher than 6.3 V, and is disabled when the input voltage at the DCIN pin crosses approximately 7 V (minimum). Table 5-1 shows the conditions that drive prebias status.

Table 7-1 Prebias status

Condition	Input prebias status
DCIN voltage is inserted between 6.3–7 V, no charging	On
DCIN – VBATT < VASHDN	Off
Charging in trickle charge mode	On
Charging in precharge mode	Off
Charging in fast charge mode	Off
Charging in taper charge mode	On
Charge termination	On

NOTE: When the DCIN voltage is higher than 7.7 V during the input prebias mode, the input power source is considered to be 9 V or 12 V.

7.1.3 Prequalification mode

When an external wall adaptor or a USB cable is connected to the corresponding input, the SMB1350/SMB1351 device performs a series of prequalification tests before initiating the first charge cycle. The input voltage level must be higher than the UVLO threshold, lower than the OVLO threshold, and 100 mV greater than the battery voltage; the appropriate ENABLE register I^2C command, or an EN input must be asserted. The prequalification parameters are continuously monitored and the charge cycle is suspended when one of them is outside the limits. The UVLO and OVLO thresholds are determined by a combination of reg10[6:4] and reg14[7:6] and are mapped in Table 5-2.

Table 7-2 Charge configuration

Charger configuration	Reg10[6:4]	Reg14[7:6]	Charger configuration	Reg10[6:4]	Reg14[7:6]
5 V	000	00	5 V, 9 V–12 V	111	00
9 V	010	00	5 V, Unreg 5 V	000	01
5 V, 9 V	011	00	5 V, Unreg 5 V, 9 V	010	01
12 V	100	00	5 V, Unreg 5 V, 12 V	100	01
5 V, 12 V	101	00	5 V, Unreg 5 V, 9 V–12 V	110	01
9 V–12 V	110	00	5 V–9 V	000	10
–	–	–	5 V–12 V	100	10

NOTE: 3 MHz operation is not supported above the 9 V operating range.

7.1.4 Trickle charge mode

Once all prequalification conditions are met, the device checks the battery voltage to decide if trickle charging is required. If the battery voltage is below approximately 2.1 V, a charging current of 30 mA (typical) is applied on the battery cell. This allows a reset of the protection circuit in the battery pack and brings the battery voltage to a higher level without compromising safety.

7.1.5 Precharge mode

Once the battery voltage crosses the 2.1 V level, the SMB1350/SMB1351 device precharges the battery to safely charge deeply discharged cells. The precharge current is programmable in reg01[7:5]. The SMB1350/SMB1351 device remains in this mode until the battery voltage reaches the pre-to-fast charge voltage threshold set by reg03[7:6]. If the pre-to-fast charge voltage threshold is not exceeded before the precharge timer expires, the charge cycle terminates and a corresponding timeout fault signal is asserted.

7.1.6 Fast charge mode

When the battery voltage exceeds the pre-to-fast charge voltage threshold, the device enters the constant current or fast charge mode. During this mode, the fast charge current level is set by the corresponding reg00[7:4]. The fast charge current can be programmed as high as 2.6 A for SMB1350 and 4.5 A for SMB1351. The fast charge current output is always limited by the input current limit setting.

7.1.7 Constant voltage mode

When the battery voltage reaches the predefined float voltage, the fast charge current starts to taper down. The float voltage is programmable from 3.46–4.72 V in 20 mV steps via reg03[5:0]. The higher float voltage settings of the SMB1350/SMB1351 device enables the charging of modern battery packs with a required float voltage of 3.6 V, 4.3 V, 4.4 V, and 4.5 V. The ability to dynamically adjust the float voltage allows the implementation of sophisticated battery charging and control algorithms.

NOTE: The 4.36 V setting is removed and replaced with a 4.35 V setting.

7.1.8 Charge completion

The charge cycle is considered complete when the charge current reaches the programmed termination current threshold, assuming current termination is enabled in reg04[6]. The termination current is programmable in six thresholds in reg01[4:2]. If the termination current threshold is not met before the charge timer expires, the charge cycle is terminated and a corresponding timeout fault signal is asserted (charge timeout).

7.1.9 Automatic battery recharge

The SMB1350/SMB1351 device allows the battery to be automatically recharged when the battery voltage falls by a value of V_{RECH} set in reg04[3] below the programmed float voltage. Setting reg04[7] enables this feature. Provided that the input power supply is still present, charging remains enabled, and all the prequalification parameters are still met, a new charging cycle is initiated. This ensures that the battery state of charge remains high, without the need to manually restart a charging cycle.

7.1.10 Charger inhibit

An option exists via reg0E[6] for preventing charging initiation upon power cycling or charge enabling/disabling unless the battery voltage is below the programmed automatic recharge threshold voltage. This prevents over-stressing of the battery via continuous charging cycles in systems with short run times and frequent power cycling. Since this function is only active during power cycling and manual charge enabling, if the device enters and then exists suspend mode, charging will continue even if the battery is above the charge inhibit voltage threshold.

7.1.11 Safety timers

The integrated safety timers provide protection in case of a defective battery pack. Both the precharge and the complete charge timer are programmable to start after the prequalification check is completed (and trickle charging has started). The precharge timer resets when the transition to the constant current mode occurs. The charge timer expires and the charging mode is terminated if the termination current level is not reached within the predetermined duration. Both timers are disabled by the appropriate bit selection. The safety timers do not operate during the USB OTG mode.

NOTE: During the supplemental mode and during a thermal shutdown event, the timers are paused.

7.1.12 Watchdog timer

A watchdog timer is available for charging, standby, and OTG modes and is enabled in reg08[0]. This timer is started after the first I^2C read/write takes place after charging is enabled or disabled, OTG is enabled or disabled, or via a reload command. The timer is reset with every I^2C ACK (acknowledge) signal addressed to the SMB1350/SMB1351 device.

When enabled, the watchdog timer has a duration of 72, 36, or 18 seconds set in reg08[6:5]. An IRQ signal generated via the STAT pin indicates watchdog timer expiration. Every time the watchdog timer expires, the default OTP settings are re-loaded to the device. If the additional watchdog IRQ safety timer is disabled in reg08[2], charging (or OTG power) is also terminated. If the additional fifteen minute timer is enabled in reg08[2], the WD timer expiration only loads the default NV values and initiates after the fifteen minute timer begins. If the fifteen minute timer expires, the command registers are reset and charging (or OTG power) is terminated. If an I^2C transaction happened during the fifteen minute timer, the short WD timer will be restarted.

NOTE: When the default values are reloaded due to the power-on-reset command register, this timer will also be initiated (if enabled). After the fifteen minute timer has expired, charging (or OTG power) may be reinitiated if the device is configured that way via the default settings.

7.1.13 STAT output

The STAT is an open drain output that indicates the battery charge status or a USB fail ($V_{USB-OK} > V_{DCIN}$ or $V_{DCIN} > V_{OVLO}$) condition when enabled in reg05[5]. The type of indication is selected via the corresponding bit in reg05[6] with programmable polarity set by reg05[7]. A STAT is asserted low whenever the battery is charging (including during trickle charge), or the voltage at DCIN is higher than OVLO, or lower than UVLO thresholds, and de-asserted at all other times. A volatile command allows the system to disable the STAT output in reg32[3]. This selection does not have an effect on the interrupt signaling pulses (Section 2.4.15). These interrupts can be programmed as pulsed IRQs or a static level based on the configuration of reg0E[0]. A pull-up resistor is connected to this pin for interfacing to a microcontroller or other logic IC.

An option also exists for the STAT output to provide blinking functionality during a charging error condition. This feature is used in conjunction with an LED to visually notify the user of a charge fault condition. There are two modes of the blinking STAT operation:

- Charger error: The blinking starts when a charging error (safety timer expiration, battery over-voltage condition, or missing battery via internal algorithm) occurs and stops when charging is disabled, suspend mode is entered, or when the input has a fault, or is unplugged. In this case, the period for the blinking is approximately 350 ms and the duty cycle for the blinking is 50%.
- Temperature fault: The blinking occurs whenever there is an internal (IC) over temperature condition, or a battery temperature hard limit fault, and an input is present. In this case, the period for the blinking is approximately 1.4 s and the duty cycle for the blinking is 50%.

NOTE: Blinking is enabled when the internal temperature remains hot but not when it is reduced per the device normal operation. In addition, when missing battery detection via THERM I/O is selected, a missing battery event causes slow LED blinking.

7.1.14 Charger enable input

EN is a logic input for enabling, or disabling the battery charging, or restarting a charge cycle. The logic can be programmed to control via the EN pin or register control in reg06[6:5] and both of these settings are also programmed to enable charging as active low or high to enable charging. If charging is enabled when an adapter is connected, the start of charging can be delayed by 700 µs or 350 ms set by reg0E[7] after the system voltage enters regulation.

7.1.15 Status and interrupt registers

SMB1350/SMB1351 includes a register bank that will indicate various conditions and activate an interrupt (IRQ) output and/or status bit. The IRQ signal is a latched condition and is initiating pulses for 0.6 ms every 350 ms at the STAT output pin. All IRQ signals are cleared by reading the corresponding status register. Interrupt signals generated because of a charge error or the collapse of the input voltage are cleared by disabling charging.

Table 7-3 Status and IRQ register map

IRQ/Status	Status register	IRQ register	Description
Complete charge timeout	h43 [2]	h43 [3]	Charging does not terminate within the programmed amount of time.
AFVC active	h44 [2]	h44 [3]	Automatic float voltage compensation is activated.
Precharge timeout	h43 [0]	h43 [1]	The battery does not charge above the pre to fast voltage threshold within the programmed amount of time.
Input OV	h44 [6]	h44 [7]	The input voltage crosses the OVLO level for the deglitch timer duration.
Input UV	h44 [4]	h44 [5]	The input voltage crosses the UVLO level for the deglitch timer duration. The UVLO IRQ is a useful way to determine when an input is inserted or removed.
Battery OV	h43 [6]	h43 [7]	During charging, the battery rises above the OVLO level (Vfloat + 100 mV) for the deglitched timer duration.
Charge error	h43[4]	h43[5]	A charger error (battery over-temperature, battery missing, and safety timer expiration) occurs.
OTG fail	h45 [4]	h45 [5]	During OTG operation, if the battery discharges below the programmed UVLO threshold for the deglitched timer duration, OTG is disabled and this IRQ is triggered.
OTG OC	h45 [6]	h45 [7]	During OTG operation, if the output current at USBIN exceeds the preprogrammed value for the deglitched timer duration, OTG is disabled and this IRQ is triggered. The OTG short circuit protection circuit triggers this IRQ if tripped and a retry is unsuccessful.
Battery terminal removed	h41 [6]	h41[7]	The battery is determined to be missing by the battery missing algorithm.
Battery THERM pin missing	h41 [4]	h41[5]	The battery is determined to be missing by the THERM pin.
Battery pre to fast threshold	h42 [6]	h42 [7]	During charging, the battery voltage rises above the programmed pre to fast threshold.
Taper charging	h43 [2]	h43 [3]	The charger enters the constant voltage mode.
Charging complete	h43 [0]	h43 [1]	The battery charge current tapers below the programmed termination level.
Battery hard hot temperature condition	h40 [6]	h40 [7]	The battery temperature exceeds the preprogrammed hard hot thermal limits.
Battery soft hot temperature condition	h40 [2]	h40 [3]	The battery temperature exceeds the preprogrammed hard hot thermal limits.
Battery hard cold temperature condition	h40 [4]	h40 [5]	The battery temperature exceeds the preprogrammed hard hot thermal limits.
Battery soft cold temperature condition	h40 [0]	h40 [1]	The battery temperature exceeds the preprogrammed hard hot thermal limits.

IRQ/Status	Status register	IRQ register	Description
APSD complete	h46 [6]	h46 [7]	Power source detection on the USBIN input in accordance with the BC1.2 specification is complete.
RID change	h45 [2]	h45 [3]	The resistance on the USB ID pin is changed.
Automatic recharge	h42 [4]	h42 [5]	Charging is enabled, at least one charge cycle is complete (input is still present) and the battery voltage discharges to Vfloat (Vautorecharge).
Low battery	h41 [2]	h41 [3]	The battery voltage crosses the preprogrammed low battery threshold.
AICL done	h43 [4]	h43 [5]	An AICL collapse has occurred
AICL failed	h46 [2]	h46 [3]	If an AICL run results in less than 500 mA.
Charger inhibit	h46 [1]	h46 [0]	Charger inhibit threshold has been tripped
OTG OC retry	h45 [0]	h45 [1]	The OTG short circuit protection is tripped and OTG attempts a retry.
Power OK	h44 [0]	h44 [1]	The input voltage is within the programmed UV and OV thresholds.
Internal temperature limit reached	h41 [0]	h41 [1]	The IC internal over-temperature limit is reached.
AICL status	h36 [7]		Indicates that AICL is done.
Input current limit	h36 [6:5]		Provides information on USBC1.2 State: 500/100/HC.
DCIN input current limit status	h36 [5:0]		Indicates the input current limit, including AICL results.
Input voltage range	h37 [7:4]		Determines which input range the DCIN voltage falls in.
Fast charge status	h38 [7]		If 1, indicates that the device is in fast charge.
Hard limit status	h38 [6]		If 1, indicates that the device is in hard temperature limit.
Float voltage status	h38 [5:0]		Indicates current float voltage, including JEITA compensation.
Charging status	h39 [7]		If 1, indicates fast charging.
Precharge current status	h39 [6:4]		Indicates the current precharge current, including JEITA compensation.
Fast charge status	h39 [3:0]		Indicates the current fast charge current, including JEITA compensation.
OTG active status	h3A [7]		Indicates when the OTG mode is enabled.
AFVC status	h3A [6]		Indicates when the automatic float voltage compensation is active.
Complete charge cycle status	h3A [5]		Indicates that at least once charging cycle has terminated since charging was first enabled.
Low battery voltage status	h3A [4]		Active when VBATT is less than 2 V.
Hold off status	h3A [3]		Active when the charger is in hold-off.
Charging status	h3A [2:1]		Indicates if the charger is in precharging, fast charging, or taper charging mode.
Charger enable status	h3A [0]		Active if charging is enabled via command write or pin logic.
APSD detection result status	h3B [7:0]		Indicates the result of APSD.
DCD timeout status	h3C [7]		Indicates that the data contact detect timed out.

IRQ/Status	Status register	IRQ register	Description
RID float status	h3C [3]		RID state-machine detects RID float.
RID A status	h3C [2]		RID state-machine detects RID A.
RID B status	h3C [1]		RID state-machine detects RID B.
RID C status	h3C [0]		RID state-machine detects RID C.
HVDCP status	h3D [7:0]		Indicates HVDCP detection result.
Charger type status	h3E [5:3]		Indicates whether an HV, LV, or unregulated charger is detected.
Quick Charge 3.0 detected	h47[4]		Indicates that a Quick Charge 3.0 adapter has been detected via the Quick Charge 3.0 authentication algorithm
Input current limiting status	h47[5]		Indicates when the input current loop is active
Quick Charge 3.0 authentication algorithm done	h47[3]	h47[2]	The Quick Charge 3.0 authentication algorithm has completed
Watchdog timeout	h47[1]	h47[0]	The charger, OTG, or standby watchdog timers expires.
Revision control status	h3F [3:0]		Indicates device revision number.

Prior to enabling charging, the IRQ signal for the over or under temperature conditions is active even when the battery thermal monitor is enabled (configurable device option).

NOTE: When an IRQ is observed, the status registers are read first. Depending on the source of the IRQ, the charger, or OTG mode, are disabled. Finally, the IRQ is cleared.

7.1.16 USB OTG mode

The SMB1350/SMB1351 device is capable of supplying a regulated 5 V output at the DCIN (VBUS) pin for powering peripherals compliant with the USB OTG specification. During this mode, the SMB1350/SMB1351 device is powered by the battery. This boost converter in OTG mode is synchronous and uses the same power train and external components with the buck converter in charging mode. The SMB1350/SMB1351 can enter OTG mode in one of three ways set by reg09h[7:6]. RID detection is BC1.2 compliant detection of the ID line in the USB interface. When AUTO OTG is configured, OTG will automatically enable per the BC1.2 specification. If OTG pin control is set, OTG will enable based on the logic set in reg09h[5]. Alternatively, when OTG I^2C control is selected, sending a command to reg32[0] will enable OTG mode. The OTG boost converter has four current limit levels set in reg0A[3:2].

The device does not enter the OTG mode if the battery is below the programmable battery UVLO threshold in reg0A[1:0] to ensure that the battery is not drained. In this case, reinitiating the OTG power delivery requires toggling the OTG pin or the register. In order to enable the OTG mode, the DCIN pin must be below 1.0 V. If this condition is not met, the OTG mode does not begin until this condition is valid.

The SMB1350/SMB1351 includes a short circuit protection feature to protect the device from stressful conditions such as the application of large capacitive loads. The current sensing element measures voltage across the inductor at the SYS and SW nodes to measure the inductor current from the battery to VBUS. Therefore, the maximum inductor current in OTG mode is dependent on the DCR of the selected inductor. The OTG inductor current limit is determined and set by the factory.

SMB1350/SMB1351 includes an OTG retry feature that ensures robust device operation in OTG mode. If an OTG retry is triggered, SMB1350/SMB1351 will autonomously disable OTG mode and re-enable 30 ms later. A number of conditions can trigger an OTG retry including:

- Upon enabling OTG if the DCIN pin does not go above 1 V level within approximately 100 µs
- When OTG mode is enabled and the DCIN pin falls below VASHDN
- When OTG mode is enabled and the short circuit protection feature is tripped
- When the battery voltage dips below 2.7 V

When an OTG retry is triggered, the OTG Retry IRQ reg45[1] will be issued. The SMB1350/SMB1351 will either retry once, or enter hiccup mode if reg14[2] is set. In hiccup mode the SMB1350/SMB1351 will continue to retry OTG for 300 ms. After the hiccup mode timer expires, or the first retry if hiccup mode is disabled, the OTG OC IRQ will be tripped. Once the OTG OC IRQ is tripped, reinitiating OTG mode requires toggling the corresponding OTG off and on commands.

When the battery voltage is initially above the OTG UVLO threshold then falls below it because of the OTG power consumption, the OTG is suspended and OTG fail IRQ reg45[5] is issued. In this case, reinitiating OTG power delivery requires toggling the corresponding OTG off and on commands.

7.1.17 Hard thermal monitor

A temperature sensing I/O (THERM) is provided to prevent excessive battery temperatures during charging. If the temperature limits are exceeded, battery charging is suspended and safety timers maintain their values but are paused. During this mode, the FET between the battery and the system is turned on for the system to be powered by the battery. Charging is automatically re-enabled, the corresponding fault bit is reset, and safety timers continue counting once the temperature level returns to the safe operating range (with some hysteresis). However, the corresponding status bit is not latched and changes in real time (with some hysteresis) as the temperature moves in or out of the temperature limits. In cases where the battery temperature is outside the specified temperature limits as soon as charging is enabled (i.e., before the hold off timer expires), charging does not start at all. A device option exists for notifying the system of a battery thermal condition, without suspending battery charging.

Figure 5-1 demonstrates the battery pack temperature monitor architecture of the SMB1350/SMB1351 device for detecting cold and hot battery pack temperature events. The internal and the external resistor strings are powered by the same power supply and the THERM monitor trip points depend on the ratio of resistors rather than the absolute value of the current sources. Therefore, the accuracy of the THERM monitor is greatly improved versus traditional implementations with current sources. The external bias resistor R1 is selected with the help of the graphic user interface to program the soft and hard temperature limits (cold and hot). A second, optional resistor R2 is used to further adjust the battery pack temperature limits, if necessary. R2 can be shorted if not in use.

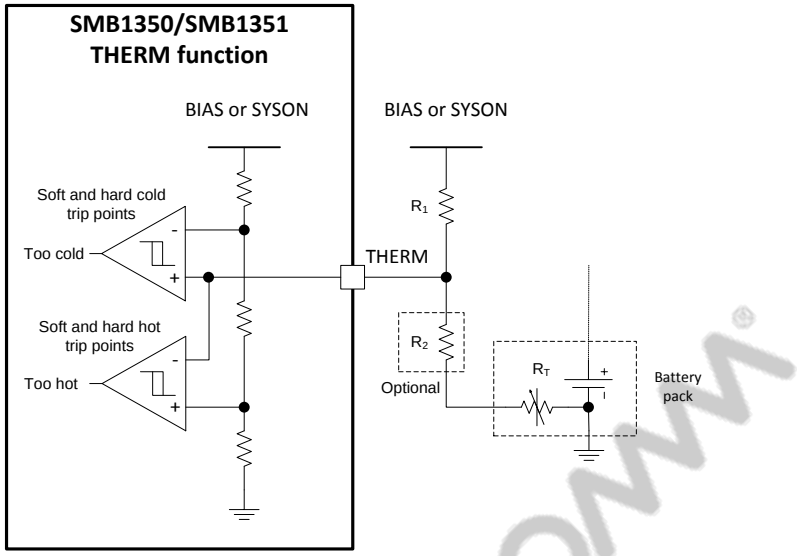

Figure 7-1 THERM monitor architecture

The hard hot temperature limit is factory adjustable from 0.185 V × V_{SYSON} to 0.276 × V_{SYSON} in reg0B[5:4].These voltage trip points correspond to a temperature range of 50–65 °C, in 5 °C steps, when an NTC with a beta of 3750 and a bias resistor equal to the NTC resistance are used. The hard cold temperature limit is factory adjustable from 0.665 V × V_{IN} to 0.805 × V_{IN} in reg0B [7:6]. These voltage trip points correspond to a temperature range of -5 to +10 °C in 5 °C steps, when an NTC with a beta of 3750 and a bias resistor equal to the NTC resistance are used. Other temperature limits are possible when using NTCs with a different beta coefficient or by adjusting the bias resistor value. See Table 5-4 for more information. Disabling the thermal monitor is also possible via reg07[4]. THERM monitoring response behavior is set in reg07[3:0] and hard limit behavior is enabled in reg0E[2].

NOTE: The SMB1350/SMB1351 GUI allows the user to calculate temperature limits based on various conditions.

Table 7-4 Temperature thresholds for different NTC beta values

VTHERM (% VIN)	β = 3375	β = 3500	β = 3750	β = 4000
0.805	-8	-7	-5	-3
0.760	-2.5	-1.5	0	+1.5
0.715	+3	+3.5	+5	+6
0.665	+8	+9	+10	+11
0.610	+14	+14.5	+15	+15.5
0.356	+41.5	+41	+40	+39
0.315	+47	+46.5	+45	+43.5
0.276	+53	+52	+50	+48.5
0.242	+58.5	+57.5	+55	+53
0.212	+64.5	+63	+60	+57.5
0.185	+70	+68.5	+65	+62.5

7.1.18 Soft thermal monitor

The temperature sensing I/O (THERM) is used for adaptive charge current or float voltage control. This allows the SMB1350/SMB1351 device to still charge the battery when the battery pack temperature is between the soft and hard over/under temperature limits, making the device compatible with the latest JIS8714 and JEITA standards. The soft hot temperature limit is programmable from 40–55 °C, and the soft under-temperature limit is programmable from 0–15 °C, each in 5 °C increments using register 0Bh (assuming a beta of 3750). The corresponding soft charge current and soft float voltage settings are also programmable (see register 0Eh). See Figure 5-2 and Figure 5-3 for more details.

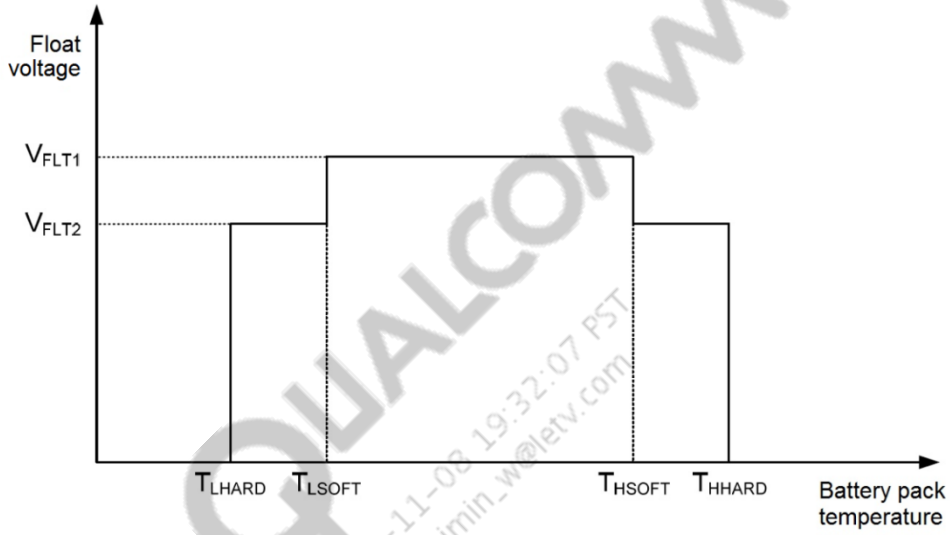

Figure 7-2 Float voltage compensation based on battery temperature conditions

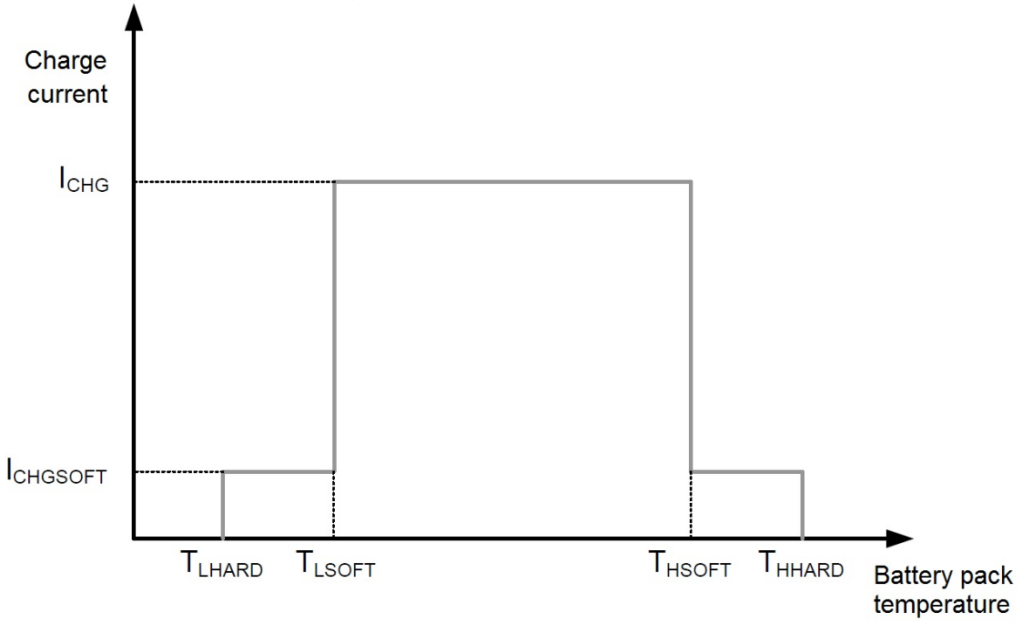

Figure 7-3 Charge current compensation based on battery temperature conditions

7.1.19 Analog thermal foldback

The SMB1350/SMB1351 device is optimized to maximize power delivery while limiting the junction temperature during operation, thereby increasing system reliability and enabling slim industrial designs. The device limits charge current based on die temperature. Once junction temperature reaches approximately 100 °C, 110 °C, 120 °C, or 130 °C (user programmable) charge current is reduced to prevent high power dissipation.

If the system current keeps increasing and junction temperature reaches approximately 140 °C, then the input power FET is turned off (to avoid more current flowing into the part) and the output power FET is turned on to allow system operation from the battery. When the junction temperature falls below the thermal shutdown threshold plus a temperature hysteresis, the input FET is turned on again and thermal regulation is reinitiated. This allows charging and system power optimization while ensuring IC and system reliability.

7.1.20 Automatic power source detection

The SMB1350/SMB1351 fully supports the USB Battery Charging Specification 1.2 and provides a method for determining what input a device is connected to using automatic power source detection, or APSD, which is enabled in reg02[2]. The SMB1350/SMB1351 includes the option to force a DCD timeout in reg11[0] and offers a flexible timeout option in reg11[4].

The power source detection algorithm runs as soon as the VBUS (DCIN) voltage is detected and is independent of the charge enable status. An IRQ is issued when APSD completes in reg46[7:6] and the results of APSD can be read from status reg3B[7:0]. When the APSD algorithm is completed, the D+ and D- signal lines enter a high-Z state with approximately 4 pF of capacitive load.

APSD can be rerun after the completion by sending a command to self-clearing reg34[7]. Sending a command to rerun APSD immediately disables the switcher and sets D+ and D- in a high-Z state. The battery is charged adequately before rerunning APSD to ensure that the system voltage does not brown out when the switcher disables. Therefore, APSD does not rerun unless Vbatt > Vlowbatt or Vlowbatt detection is disabled. APSD reruns after the charge detect debounce time and use the D+/D- lines until completion. When an HVDCP adapter is detected, a 5 V request followed by a 500 ms delay must be made before the rerun APSD command is sent.

The six power source types that are detected are:

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)
- High-voltage dedicated charging port (HVDCP)
- ACA charger
- Other charging port (not covered by USB Charging Specification 1.2)

When APSD results in an SDP charger, the SMB1350/SMB1351 can be configured to use pin control or register control to determine the current limit in reg06h[4]. If configured to pin control, the USB5/1/HC pin logic is used in dual-state or tri-state in reg06h[3] to set the current. See Table 5-5 for USBCS pin logic. If configured to I^2C control, a combination of reg01h[0] and command reg31h[1:0] set the input current limit. USB500 or USB100 can also be configured for USB 3.0 charging modes by configuring reg01[1] as pin control or command reg31[2].

Table 7-5 USB charging specification

	Pin control dual state	Pin control tristate
High	USBHC	USB500
Low	USB500	USB100
Float	N/A	USBHC

The current limit can be changed by sending a command to reg31h[3]. Once this command is sent, the input current limit will be set using pin or I^2C logic as described above.

Additionally, OTG and ACAs are supported with the use of the ID pin and monitoring for what is attached to the ID, whether it is GND, RID_A, RID_B, RID_C, or floating, which can be read in reg3C[3:0]. An IRQ can be enabled to indicate when RID value has changed in reg45[3:2].

NOTE: Writing to the command register after the power source detection is complete resets the corresponding APSD status bit; however, the APSD complete bit remains set.

7.1.21 BMD

The SMB1350/SMB1351 device offers two different options for detecting a missing battery condition.

The first option incorporates the use of the battery pack thermal monitor I/O (THERM). The device checks if there is a resistor to ground on the third terminal of the battery (T). When no battery is detected, a corresponding bit is asserted and charging is suspended. Once the battery is reconnected, charging is automatically initiated, assuming that input power is present, all qualification parameters are met, and charging is enabled. When not used, THERM is to be connected to the GND for normal operation.

The second option provides a 10 mA discharge current for a short period of time (approximately 100 ms), then checks if the BATT pin is below 2.1 V at the initiation of a charge cycle. Next, it checks the pin to see if the charger brings the load capacitance above the missing battery threshold. The state of the BATT pin is latched at the onset of charging. If the BATT pin is below 2.1 V, the trickle charger (if enabled) begins to charge the BATT pin through the OUT pin. Once the BATT pin reaches 2.1 V, the OUT pin begins charging the BATT pin with the programmed precharge current and the battery missing timer begins. If the BATT pin is charged up above the missing battery voltage level before the expiration of the battery missing timer, the SMB1350/SMB1351 device asserts the missing battery status flag and the IRQ (if enabled).

NOTE: The BMD is only active when charging is enabled.

7.1.22 Internal thermal shutdown

When the die temperature of the SMB1350/SMB1351 device reaches approximately 140 °C, the PWM switcher is shut down (no input drawn from DCIN) to prevent further die heating. In this case, the system output voltage is regulated to the battery voltage (25 mV). This internal thermal protection circuit helps to improve the device (and consequently, the system) reliability. The device must be re-enabled for charging to be reinitiated.

7.1.23 USB dead battery charging

The SMB1350/SMB1351 device allows the portable device to automatically start the charging process when the battery voltage is below the programmable low battery threshold and the system is off. This is accomplished by setting the charge enable in the I^2C active low mode. When the system wakes up, charging is controlled by the system.

The SMB1351 includes an option to force USB500 mode rather than USB100 mode via reg14h[4] to allow the system to boot. Once the battery voltage rises above the programmed low battery threshold, the device will re-enter USB100 mode.

The SMB1350/SMB1351 device supports the USB dead battery provision. An integrated 30 minute timer enabled in reg28[5] ensures that the portable device with a dead battery does not draw 100 mA indefinitely. The timer is active when input power is present at the input and a USB host is detected. The timer ends under the following conditions:

- Suspend mode is entered
- I^2C write command to register 33h
- USB5/9 mode is selected
- Power source is not an SDP

During dead battery charging the SMB1350/SMB1351 device brings D+ high to +0.6 V to notify the host of its condition.

7.1.24 Nonvolatile reloads

The nonvolatile values are loaded from the embedded nonvolatile memory on initial power on. Certain conditions result to the reloading of the default, nonvolatile values to the configurations registers:

- Issuing a POR command via the command register
- Unplugging of the input power source as long as the part acknowledges an I^2C transaction since the last reload with Reload on Unplug enabled in reg28[4]

No reloads occur if the device is not written to since the last reload. During OptiCharge ($V_{IN} < V_{CL}$), the device does not reload default values. Since reloading of the nonvolatile data via reg30[7] can take up to 20 ms, it is recommended that the user wait 20 ms after initiating this command before communication is attempted.

7.1.25 Soft start

The SMB1350/SMB1351 device provides soft start control to allow a smooth input voltage ramp up and to prevent input current and voltage transients. Soft start is active anytime the input power transitions to a new state, such as initial input power, input current limit change (USB1 to USB5), and others.

7.1.26 Glitch filter

The SMB1350/SMB1351 device features a glitch filter to ensure that short violations in the VBATT OV or THERM settings are not the result of a fault-triggered action. The glitch filter duration is 175 ms.

NOTE: The glitch filter delays automatic recharge and current termination by 175 ms.

7.1.27 TurboCharge mode

The SMB1350/SMB1351 device performs battery charging using the benefits of TurboCharge. TurboCharge is derived from the intrinsic ability of the buck architecture to multiply the input current when stepping down the output voltage. This property is expressed mathematically in the following comparison and provides the ability to maximize battery charging from current limited devices, decrease power dissipation, and any heat related dissipation.

Linear charging:

Equation 1 (linear charge current relationship): $$I_{OUT} \approx I_{IN}$$

NOTE: Equation 1 does not take into account thermal foldback.

Equation 2 (efficiency of linear charger): $$\eta = \frac{V_{BATTERY}}{V_{INPUT}}$$

Equation 3 (TurboCharge current relationship): $$I_{BAT} = \frac{\eta V_{IN} I_{IN}}{V_{BATT}}$$

$\eta \approx 90\%$.

7.1.28 OptiCharge (AICL) mode

The SMB1350/SMB1351 device incorporates OptiCharge, and allows the SMB1350/SMB1351 device to automatically and safely maximize the current drawn from an AC/DC adapter or USB input. This algorithm is initiated only when the device enters the HC mode (not in USB1 or USB5). A corresponding reg02[4] allows the user to disable this functionality if it is not required.

When HC charging mode is enabled, the SMB1350/SMB1351 device initially sets AC input current limit to its lowest setting. Approximately 175 ms later, the device starts incrementing the AC input current limit level until either the programmed input current limit level is reached, or the adapter output voltage falls below the current limit threshold. In the case of collapse adapter voltage, charger current is cut off. Two thresholds are available to accommodate a wide variety of

AD/DC adapters: 4.25 V and 4.50 V. The AICL voltage thresholds for 5–12 V continuous range are 4.25 V and 4.5 V. For high voltage operation, the AICL threshold is 7.8V with a 5 ms glitch filter and a second 6.3 V threshold has a 15 µs glitch filter and will force the switcher to disable.

A 50 mV hysteresis prevents chattering. When AICL is done, status reg46[4] is activated. A read register in reg36[5:0] is also provided for the system to know at what level the input current is limited. If the adapter output voltage falls below the current limit threshold with lowest input current setting, the AICL fail IRQ will be issued in reg46[3:2] and the SMB1350/SMB1351 will either enter suspend mode or force 150 mA input current limit based on how reg08[7] is programmed.

Assuming that OptiCharge is enabled, the following events trigger the OptiCharge algorithm run:

- The OptiCharge operation is not yet completed.
- The OptiCharge operation is completed, but the adapter voltage collapses.
- The input current setting in the volatile register is updated with a value lower than the automatic input current setting.
- Every 45 seconds if AICL re-runs are enabled via the factory programmable setting reg2C[4]. When AICL re-runs are enabled, AICL is never allowed to fail or enter suspend mode.

7.1.29 INOK/SYSOK/CHG_DET_N output

The SMB1350/SMB1351 device provides an open drain output that is used as an input or a system OK indicator. There are six different modes of operation. The polarity of this output is programmable. When no input is present and SUSP/SHDN is active LOW, the SYSOK/INOK output signal is also active LOW. The option bit in reg13h[7] modifies the output logic of this bit in as seen in Table 5-6. The factory-programmable nonvolatile bit reg15[0] sets PGOOD as push-pull or open-drain configuration.

Table 7-6 PGOOD polarity

Reg13h[7]	PGOOD programming	
	INOK/CHG_DET_N	SYSOK
0	Active low output	Normal SYSOK table
1	Active high output	Invert SYSOK output

1. In the first mode (INOK – see register TBDh), the INOK output is asserted to indicate a valid input adapter presence (VIN > VUVLO, VIN < VOVLO). The polarity of INOK is programmable and goes active when a valid input voltage is present. During the active high state, this I/O is high impedance. In a shutdown mode, INOK goes LOW independent of the selected polarity. There are two factory-programmable options set in reg26[5] for the INOK operation:
   a. The INOK is asserted only per the input voltage level and as soon as the glitch filter timer expires.
   b. The INOK is asserted only when the input FET is off (i.e., also during suspend mode) and only after the APSD algorithm is complete (if enabled).

2. In the second mode (Option A1 – see registers TBD), the SYSOK goes active LOW when no valid input power is present and the battery voltage is lower than the programmable low battery/SYSOK voltage threshold (VLOWBATT) or the battery is missing. See Table 5-7.

Table 7-7 Option A1 SYSOK state

Input source	Battery voltage	SYSOK state
Present	< $V_{LOWBATT}$ (or missing battery)	High-Z
Present	> $V_{LOWBATT}$	High-Z
Missing	< $V_{LOWBATT}$ (or missing battery)	Low
Missing	> $V_{LOWBATT}$	High-Z

3. In the third mode (Option A2 – see registers TBD), the SYSOK goes active LOW when the battery voltage is lower than the programmable low battery/SYSOK voltage threshold (VLOWBATT) or the battery is missing. See Table 5-8.

Table 7-8 Option A2 SYSOK state

Input source	Battery voltage	SYSOK state
Present	< $V_{LOWBATT}$ (or missing battery)	Low
Present	> $V_{LOWBATT}$	High-Z
Missing	< $V_{LOWBATT}$ (or missing battery)	Low
Missing	> $V_{LOWBATT}$	High-Z

4. Table 5-9 lists the state of SYSOK under the various system conditions for the fourth mode (Option B1 – see register TBD).

Table 7-9 Option B1 SYSOK state

Battery voltage	Power source detection result	SYSOK state
< $V_{LOWBATT}$	Missing	Low
> $V_{LOWBATT}$	Missing	High-Z
No care	DCP/CDP/OCP/SDP500	High-Z
< $V_{LOWBATT}$	SDP100/Disabled/AICL< 500 mA	Low
> $V_{LOWBATT}$	SDP100/Disabled/AICL< 500 mA	High-Z

5. Table 5-10 lists the state of SYSOK under the various system conditions for the fifth mode (Option B2 – see register TBD).

Table 7-10 Option B2 SYSOK state

Battery voltage	Power source detection result	SYSOK state
< $V_{LOWBATT}$	Missing	Low
> $V_{LOWBATT}$	Missing	Low
No care	DCP/CDP/OCP/SDP500	High-Z
< $V_{LOWBATT}$	SDP100/Disabled/AICL< 500 mA	Low
> $V_{LOWBATT}$	SDP100/Disabled/AICL< 500 mA	High-Z

NOTE: When the BMD function is enabled, the battery voltage default state can be programmed in reg13[2], which will be assumed true until the battery voltage glitch filter of 175 ms expires. SYSOK options can also be programmed to wait for the BMA to complete or assert high without the BMA completion in the factory-programmable reg2D[1].

6. In accordance with USB Battery Charging Specification 1.2, this output can also be used as a CHG_DET_N output. In the first mode (CHG_DETN1) the SMB1350/SMB1351 can notify the system or a PMIC regarding the APSD results. The CHG_DET_N is asserted (active low) every time the device's algorithm detects a DCP, an HVDCP, a CDP, another charging port, and an ACA. The presence of a DCIN (primary priority) will also assert this signal. Furthermore, the charger detect signal is not clamped when the device is not powered. This option can also be used to indicate valid input voltage presence (VUVLO < VIN < VOVLO) to the system when the APSD function is disabled. A second option (CHG_DET_N2) is also provided to assert this output LOW unless and SDP, CDP, or ACA are detected.

7.1.30 VCHG output

The VCHG I/O provides an analog voltage (V_{CHG}) that is proportional to battery charge current (I_{CHG}) or to input current (I_{IN}) via factory-programmable reg15[2]. The relationship between these two parameters is: $V_{CHG} = I_{CHG}$ x 0.5 Ω or $V_{CHG} = I_{CHG}$ x 0.55 Ω.

7.1.31 SYSON output

The SYSON output is a current limited output that provides a minimum current of 55 mA and a voltage regulated to 5 V. The SYSON output becomes active for as long as the buck is enabled. Once the switcher is disabled, the SYSON voltage is pulled down to 0 V.

NOTE: During shutdown and suspend modes, SYSON is shut down and power consumption for THERM remains low.

7.1.32 SUSP/SHDN input

When a DCIN power source is present, SUSP/SHDN can be programmed in reg02[7] as a logic input pin for enabling or disabling USB suspend mode. The other logic option is for the SMB1350/SMB1351 device to enter suspend mode via the command reg31[6]. In suspend mode DCIN input current is less than 1 mA and both charging and system outputs are turned off.

When only a battery is present, the SUSP/SHDN pin is used to enter or exit shutdown mode. If SUSP/SHDN is high when no input is valid, I^2C communication is possible and the BATFET is on. If the SUSP/SHDN is low when no input is valid, the device is in SHDN mode meaning no I^2C communication is possible and the BATFET is off. The detailed SUSP/SHDN functionality is also shown in Table 7-11.

Table 7-11 SUSP functionality

Valid DCIN input present	SUSP/SHDN pin	Power mode	I^2C operation	BATFET state
No	Low	Shutdown	No	Off
No	High	Standby	Yes	On
Yes	High	Suspend*	Yes	On

Valid DCIN input present	SUSP/SHDN pin	Power mode	I²C operation	BATFET state
Yes	Low	Active	Yes	On

NOTE: * This assumes suspend mode is set to pin control in reg02[7].

NOTE: With the internal BATFET off, VSYS can be below VBAT by a forward voltage drop of the BATFET, which is approximately 0.5 V. This needs to be taken into account when powering on a system via a keypad power press or equivalent power on trigger with no DCIN present. Once SUSP/SHDN is biased high, it takes approximately 8 ms for the internal BATFET to fully turn on. A simple means of addressing this is by leveraging the FETDRV signal, which is used to drive an external PFET to keep VBAT and VSYS shorted with no bias on SUSP/SHDN.

7.1.33 CurrentPath control

The SMB1350/SMB1351 device features CurrentPath technology that allows separate control of the system and the battery outputs. The SMB1350/SMB1351 device gives the system output on VSYS priority on input power, allowing the system to power up even with a defective, deeply discharged, or missing battery. As system current requirements increase, input current is steered towards the system by reducing charging current to the battery. This is accomplished by keeping the input current constant. When the input current is not adequate to satisfy the system requirements, and the system voltage falls below the VREVFET threshold, the integrated ideal diode becomes forward biased and the battery starts supplementing the input current to the system load. During this supplemental mode only the internal ideal diode FET turns on. In all these cases, input current remains limited per the device configuration for meeting USB and other similar electrical specifications.

NOTE: During shutdown mode, the internal CHGFET remains off.

CurrentPath allows accurate charge termination, by allowing the system to know precisely when the charging current hits the current termination threshold versus implementations in which the battery and the system are connected to the same node. Four conditions need to be met for the SMB1350/SMB1351 device to terminate charge:

- The device enters the constant voltage charging phase.
- The input current does not reach the input current limit.
- The battery is not supplementing the input power for the system.
- The device does not enter the thermal regulation mode.

When the battery voltage is below 3.15 V, 3.3 V, 3.45 V, or 3.6 V as set by reg07[7:6], the system and battery are not connected together and the system voltage is regulated to Vsys_min. When the battery voltage is above Vsysmin, the CHGFET is turned fully on to ensure that power dissipation is kept to a minimum. When battery charging is completed, the system output is regulated to VFLT + 100 mV or +50 mV based on factory-programmable reg1C[2:0].

7.1.34 FlexCharge+

The SMB1350/SMB1351 device allows the user to select the allowable input voltage range via register 10h[6:4]. Depending on the selection, the input under-voltage and over-voltage thresholds are set accordingly to only allow the input voltage operation as specified. For example, for a 5 V input voltage selection, an input voltage of 9 V is considered an input over-voltage event. For a 9 V input voltage selection, a 5 V input voltage is considered an input under-voltage event and a 12 V input voltage is considered an input over-voltage event. When a 9–12 V input voltage range is selected, a 5 V input voltage is considered an under-voltage event and the input over-voltage threshold is set to its maximum value (that is, 6.2 V).

Anytime the unregulated input voltage is selected, the automatic prebias current is initiated when the input voltage is less than approximately 7 V. See Section 2.4.2 for additional information.

7.1.35 Quick Charge 2.0

The SMB1350/SMB1351 device incorporates the Quick Charge 2.0 algorithm, allowing the portable device to use wall adapters and negotiate for higher input voltage levels via the standard USB cables and connectors. This proprietary feature enables faster battery charging while maintaining USB battery charging 1.2 compatibility and allowing compatibility with other specifications that use the USB ID pin or communicate on USB VBUS. The SMB1350/SMB1351 device fully supports all of the class A voltage levels: 5 V, 9 V, and 12 V.

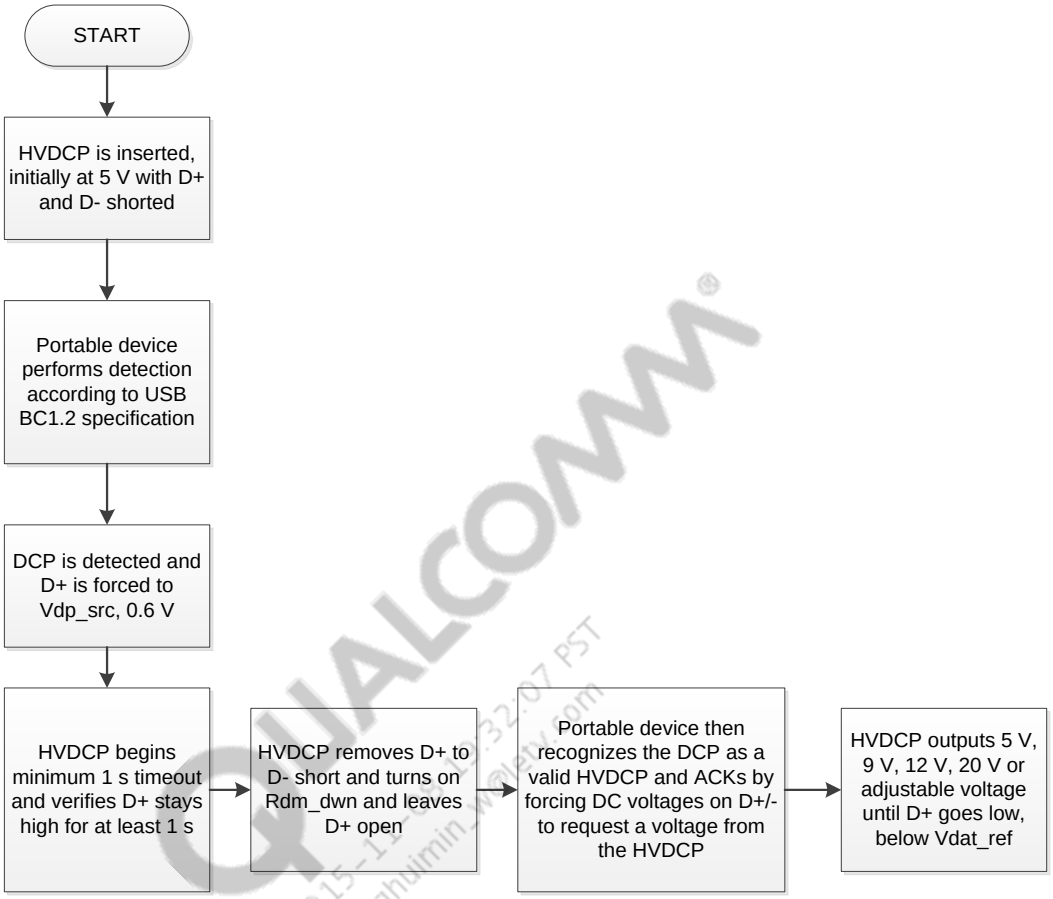

Figure 7-4 High-level Quick Charge 2.0 flowchart

7.1.36 Quick Charge 3.0

The SMB1350/SMB1351 includes hardware support of the latest fast charging specification, Quick Charge 3.0. Quick Charge 3.0 adds a request option from a 3.0 HVDCP that enables continuous voltage mode. In this mode, the SMB1350/SMB1351 can make requests to a Quick Charge 3.0 enabled HVDCP for voltages in 200 mV steps from 3.6 V to 12 V.

Upon detecting an HVDCP adapter, the SMB1351/SMB1350 runs an authentication algorithm (if enabled in reg11[1]) to determine if a Quick Charge 2.0 or a Quick Charge 3.0 HVDCP is connected.

If Quick Charge 3.0-authentication fails, a Quick Charge 2.0 adapter is determined to be connected and the voltage in reg12[7:6] is requested automatically. An IRQ in reg47[3] indicating that the algorithm has completed can be enabled in reg13[0]. A Quick Charge 3.0 adapter will be indicated with reg47[4]=1 after the authentication algorithm has completed. If the authentication algorithm is disabled, then the HVDCP is assumed to be Quick Charge 3.0 compliant upon detection of an HVDCP. The command reg34 can be used to force Quick Charge 2.0 behavior from Quick Charge 3.0 mode. In order to re-enter Quick Charge 3.0 mode, the APSD re-run function must be used.

Upon detection of a Quick Charge 3.0 adapter, the SMB1350/SMB1351 may enable one of two completely hardware autonomous algorithms that are designed to optimize the input voltage for a given operating point. The two algorithms, classified as conservative (27[6]=0) or advanced (27[6]=1), are factory-programmable bits. The algorithms can be disabled or enabled in reg11[2]. The SMB1350/SMB1351 also allows individual increment or decrement requests from the adapter by sending commands in reg34.

The advanced algorithm will automatically increment the voltage on VBUS to the minimum voltage for that operating point. This processing is only designed to request an increase in power and will not autonomously decrement when the output power needs are reduced.

The conservative algorithm is intended to optimize for a charge current of approximately 3 A without taking system loads or significant cable resistances into account.

Regardless of which optimization algorithm is enabled, if at any point the voltage on USBIN is detected to be above the 9 V OVLO level of 10.2 V, all further increments are barred. Furthermore, an automatic decrement function will continue to reduce the voltage output of the adapter until the voltage on VUSB is below the 9 V OVLO level.

7.1.37 Anti-boost back algorithm

All high-side NFET switching architectures have the inherent requirement to maintain charge on a boot capacitor in order to drive the gate of the high-side FET. This prevents the device from entering 100% duty cycle and forces a minimum on time for the low-side FET to switch. This creates a condition after the input adapter is removed, as the input voltage collapses, where the device enters maximum duty cycle but continues to switch. Under these conditions, the minimum on-time for low-side FET potentially transfer enough energy through the switcher such that the input voltage does not collapse below the UVLO threshold and the system is unable to detect the removal of the adapter. This is known as boost-back and is inherent to all high-side NFET topologies. In order to address boost-back, a proprietary algorithm is developed in the SMB1350/SMB1351 device that prevents boost-back from occurring. The SMB1350/SMB1351 device autonomously detects the conditions under which boost-back occurs and disables switching, allowing the system to detect the input adapter removal.

7.1.38 BMS integration

The SMB1350/SMB1351 device includes a configurable option in reg0E[7] to delay enabling the charge FET by 300 ms to allow a BMS to record an open circuit battery voltage measurement. This delay starts from the time when VSYS is powered and the SYSON LDO is enabled.

7.1.39 Adapter identification

A configurable feature in the SMB1350/SMB1351 device allows the restriction of allowed input current limits tested in AICL in order to identify specific adapter current limits. The SMB1350/SMB1351 device provides three options for preselected adapter current ratings to be tested by AICL. Any intermediate input current limit results are reduced to a lower, allowed input current limit. These options are mapped and tabulated in Table 5-12. If modes 1 through 3 are selected, the maximum AICL value is programmed in reg04[5:4]. These modes are applicable when high current mode is enabled and one of the following:

- DCP adapter attached
- HVDCP adapter attached, programmable in reg14[5]

- Other adapter attached, programmable in reg05[4]

Table 7-12 Adapter input current limit mapping

Setting	Disabled	Mode 1	Mode 2	Mode 3
0.5 A	Same	0.5 A	0.5 A	0.5 A
0.9 A	Same	0.685 A	0.685 A	0.685 A
1 A	Same	1 A	1 A	1 A
1.1 A	Same	1 A	1 A	1 A
1.2 A	Same	1 A	1.2 A	1 A
1.3 A	Same	1 A	1.2 A	1 A
1.5 A	Same	1 A	1.5 A	1.5 A
1.6 A	Same	1 A	1.5 A	1.5 A
1.7 A	Same	1 A	1.5 A	1.7 A
1.8 A	Same	1.8 A	1.5 A	1.7 A
2 A	Same	2 A	2 A	2 A
2.2 A	Same	2 A	2.2A	2 A
2.4 A	Same	2 A	2.2A	2 A
2.5 A	Same	2.5 A	2.5 A	2.5 A
3 A	Same	3 A	3 A	3 A
3.5 A	Same	3.5 A	3.5 A	3.5 A

7.1.40 System short circuit protection

The SMB1350/SMB1351 offers system short circuit protection behavior, which disables the buck completely when the following conditions are both true:

- Buck voltage soft-start is complete with a glitch filter of 5 ms for rev 2.1 silicon
- Vsys voltage is below 2.1 V

Once these conditions are met, the device will enter suspend mode and the associated status reg26[5] will be asserted. The only way to exit this state is to send a re-run APSD command reg31[2] or if the input is removed and re-applied. This protection applies to battery short circuit conditions as well because if charging is enabled, the battery voltage short will drag down the system voltage. If charging is disabled, the BATFET is off and the short is disconnected from the buck. This protection scheme is enabled in a factory-programmable reg27[5]. The glitch filter on soft-start complete is intended to allow the SMB1350/SMB1351 to power into a minimum of 500 µF of capacitance on the system node without triggering the short circuit protection.

NOTE: SMB1350/SMB1351 rev 2.0 silicon does not glitch filter the soft-start complete signal and can typically power into a maximum of 120 µF without triggering the system short circuit protection.

Short circuit phenomena create harmful conditions for integrated circuits regardless of the protection scheme employed. Therefore, it is not recommended, nor guaranteed, that the device can be subjected to repeated short circuit conditions and remain operational.

8 Application information

8.1 External components

The SMB1350/SMB1351 device programmable frequency synchronous operation with the built-in USB-OTG mode simplifies the solution schematic and the board space. Its 0.75 MHz, 1 MHz, 1.5 MHz, or 3 MHz switching frequency minimizes the size of external energy storing devices. The synchronous dead-time is optimized, and eliminates the need for an external Schottky diode although including one is highly recommended for efficiency improvement. The SMB1350/SMB1351 device uses the same external components to realize the USB-OTG mode as the normal battery charging mode. The battery voltage is boosted and provided on the DCIN (VBUS) by the SMB1350/SMB1351 device.

Designs in which the charging connector is away from the SMB1350/SMB1351 device charging IC, it is recommended that a 47 nF capacitor be placed close to the connector input power pin. This design practice mitigates potential EMI issues.

If any of the logic input or output I/Os (USB5CS, EN, USB2/3, THERM, D+, D-, and FETDRV) are not used, it is recommended to connect to the GND (do no leave floating). If APSD is used, D+ and D- are routed to the same distance from the USB connector to the USB PHY or transceiver. The D+ and D- lines are routed as a T to the SMB1350/SMB1351 devices such that reflections are the same (or nonexistent). To ease layout considerations, it is recommended to use series resistors that are 200 Ω or 300 Ω and not greater than 499 Ω from the T to D+ and D- of the SMB1350/SMB1351 device. Proper layout techniques still need to be used to ensure that USB signal integrity remains intact. Furthermore, routing a thick top layer of copper significantly improves thermal behavior.

8.1.1 Input and output capacitors

The input capacitors need to absorb all reflected input switching ripple current generated by the SMB1350/SMB1351 device during charging or system powering, to ensure that no ripple current is seen on the input supply. A 4.7 μF ceramic capacitor, X5R or X7R rated with low ESR on MID and DCIN sufficiently accommodates the above RMS current. These capacitors see the maximum input voltage; therefore the appropriate voltage is selected for a given application.

The output capacitor on Vsys is needed to ensure the stability of the charger and low output ripple voltage. A 22 μF ceramic capacitor, X5R or X7R rated with low ESR makes the SMB1350/SMB1351 device stable and absorbs all AC portion of the inductor switching ripple current, since the RMS value of the output ripple current is much larger than that of the input ripple current. This capacitor sees approximately 5 V maximum.

The SYSON LDO output powers the 33 nF BOOT capacitor which in turn powers the high side FET gate drive circuitry, as well as several other internal circuits. A 4.7 μF ceramic capacitor, X5R or X7R rated with low ESR should be populated at the SYSON pin in order to provide a stable voltage to these circuits. This capacitor sees approximately 6 V maximum.

A 10 µF capacitor on CHGOUT stabilizes the battery voltage and current measurements. This capacitor should be X5R or X7R rated with low ESR. This capacitor sees approximately 5 V maximum.

NOTE: DC bias capacitance reduction must be considered and it is therefore recommended that 0603 sized capacitors are chosen to ensure that the appropriate amount of capacitance is available at the DC operating point.

8.1.2 Inductor

The inductor in a buck type charger is selected to ensure that the form-factor, cost, switching ripple, and efficiency conform to the system requirement or constitute the best compromise.

Within a given package size, higher inductance value usually suggests a higher DCR value, which generates higher conduction losses. Therefore, it is typically beneficial to select lower inductance values in the same package to benefit from lower DCR values; however, the increase in peak current ripple must be taken into account based on the following equation:

$$\Delta I_L = \frac{Vin_{max} - Vbat}{L} \cdot \frac{Vbat}{Vin_{max} \cdot fs}$$

The larger peak current ripple produces a higher AC loss in the magnetic core and the windings and the inductor selected need to support the peak currents without saturating. The minimum inductance supported by the SMB1350/SMB1351 is 0.68 µH to guarantee safe peak current limit levels across operating input voltage, battery voltage, and switching frequency. See Figure 8-1 and Figure 8-2 for a comparison of SMB1351 efficiency with various inductor selections and switching frequencies.

A larger switching ripple will also produce a larger voltage ripple at the output of the buck converter on the Vsys node. This larger voltage ripple is viewed as acceptable since there is typically a very large capacitance on the Vsys node and downstream regulators can tolerate an increase in voltage ripple.

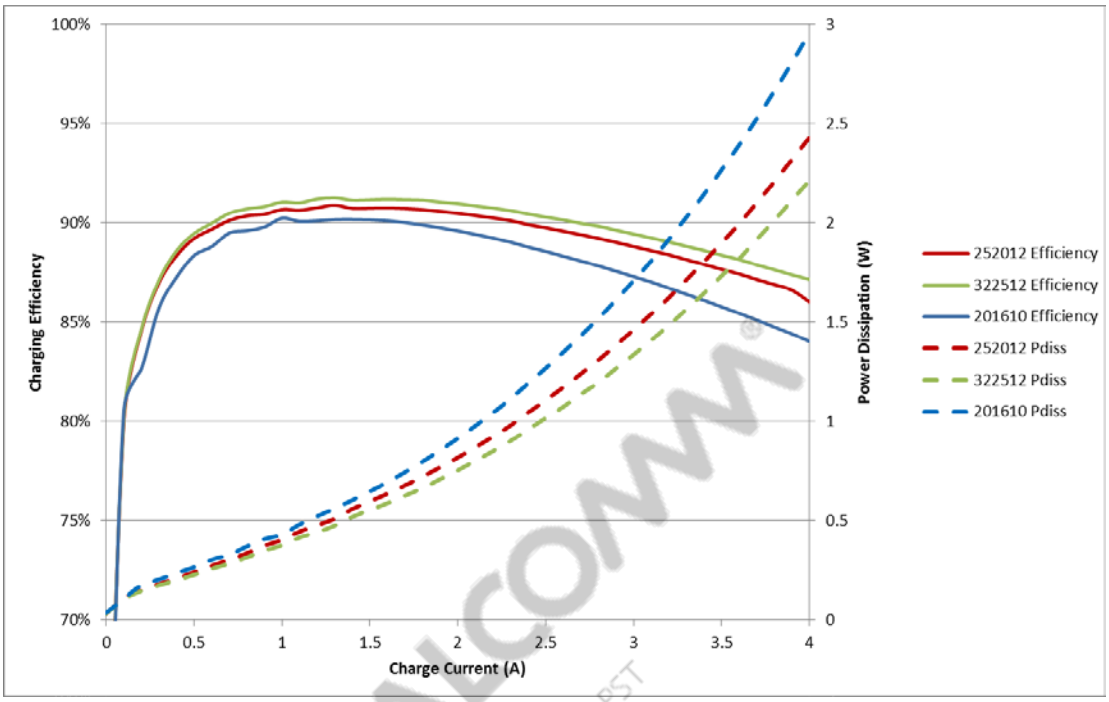

Figure 8-1 Efficiency and power dissipation for various inductor package sizes

NOTE: Data was taken at the 3.8 V battery with a 9 V input voltage. All inductors belong to the Toko DFE-F family.

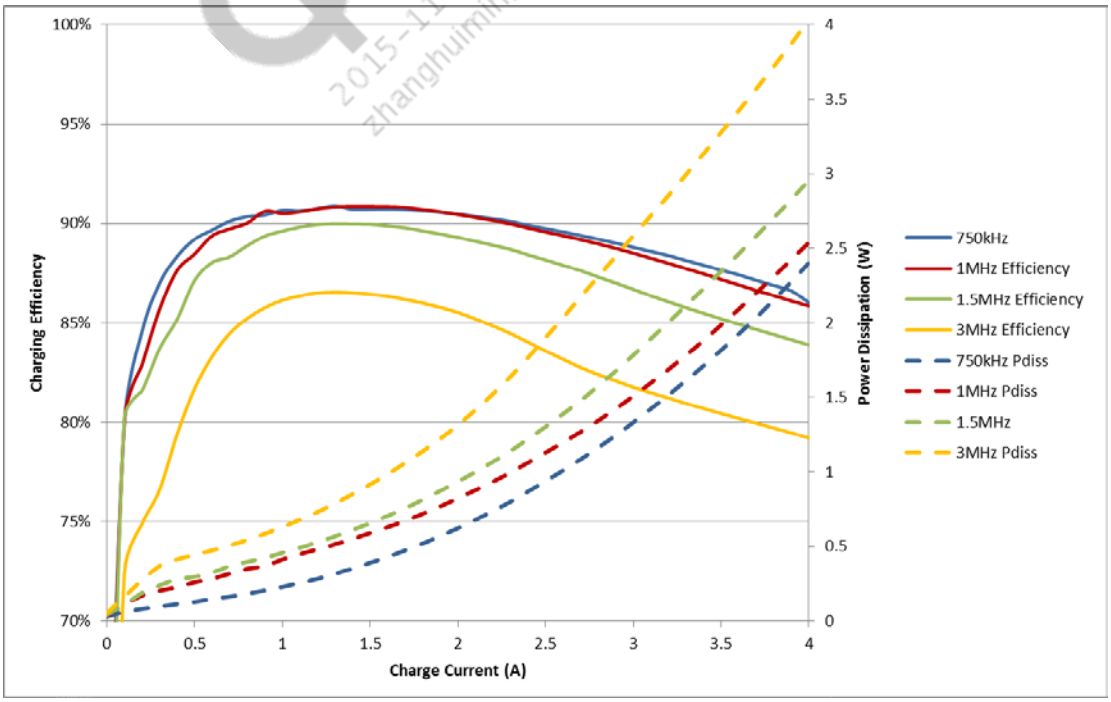

Figure 8-2 Efficiency and Pdiss for various switching frequency

NOTE: Data was taken at the 3.8 V battery with a Toko DFE250212F inductor with a 9 V input voltage.

8.1.3 SYSON to VBAT capacitor

A 4.7 µF capacitor from SYSON to the VBAT pin is required for low battery voltage recovery. This capacitor is used to bias a protection circuit to allow consistent buck startup behavior. This capacitor is not needed for applications based on rev 2.1 silicon, but required for rev 2.0 silicon.

8.1.4 Schottky diode

An external Schottky diode between SW and GND can be optionally added as a measure to increase operating efficiency. The Schottky diode increases efficiency by reducing power dissipation associated with reverse recovery losses and conduction losses of the low side FET body diode during fixed dead times. The improvement in efficiency is more pronounced at higher switching frequency when the fixed dead times become a larger percentage of the switching period. When selecting a Schottky diode, a higher forward current rating and lower forward voltage rating will lead to improved efficiency. The Schottky diode will only conduct during dead times and will see the peak current ripple values for short periods of time. The reverse current rating of the Schottky should also be taken into account for battery current leakage. See Figure 8-3 for a comparison of SMB1351 with and without a Schottky diode present.

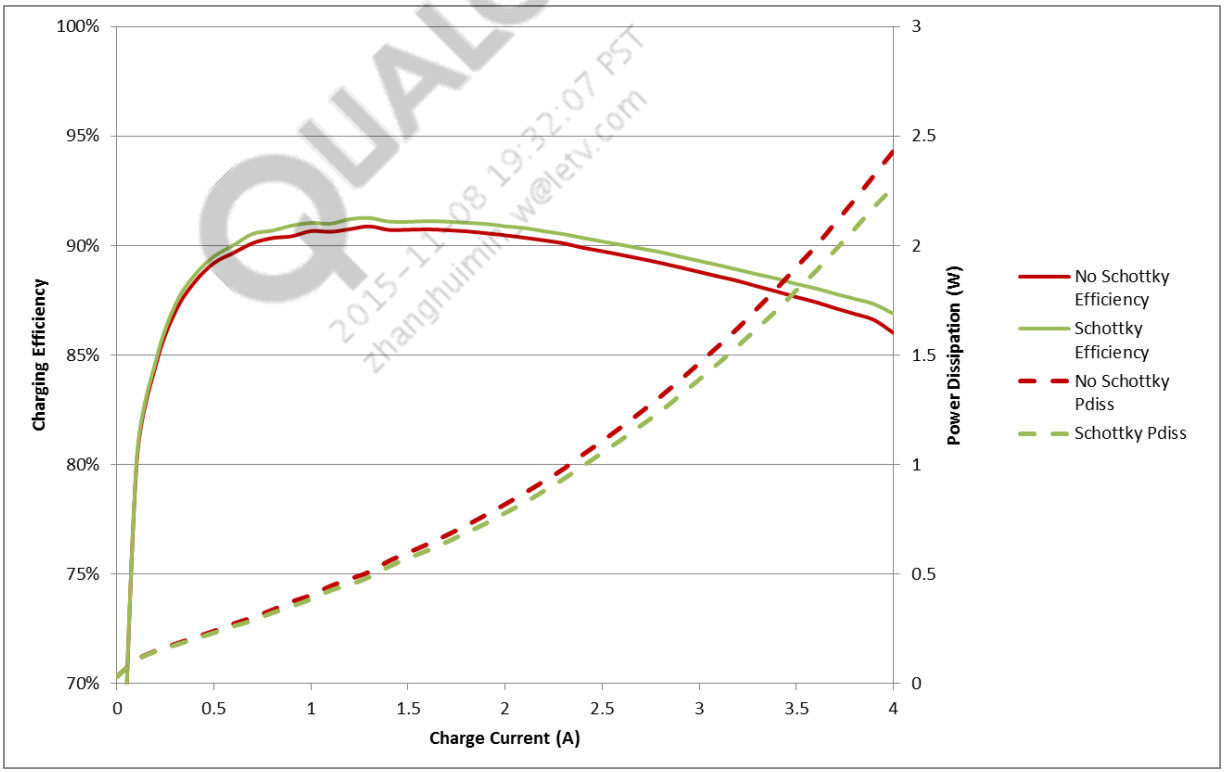

Figure 8-3 Efficiency and Pdiss data with a Schottky diode

NOTE: Data was taken at the 3.8 V battery with a Toko DFE250212F inductor with a 9 V input voltage.

8.2 Board layout recommendations

The SMB1350/SMB1351 device requires an inductor, input capacitors, output capacitors, midpoint capacitors, and small miscellaneous components because the top FET and the bottom

FET are internal. Place the input capacitors close to and on the same side as the IC. Place an inductor and an output capacitor close to each other. Pour sufficient copper on the DCIN, VBATT, SYS, SW, CHGOUT, and AGND nodes. If it is necessary to route from these nodes to the other side of the board, place a sufficient number of vias. Thermal vias, internal ground planes, and power planes quickly sink heat generated by the SMB1350/SMB1351 device and the inductor. Internal ground planes and power planes provide shielding and protect the SMB1350/SMB1351 device from noise. Figure 3-1 shows a simplified diagram for ideal component placement. Refer to the *SMB1350/SMB1351 Layout Guidelines* (80-NL405-5) for a detailed recommendation.

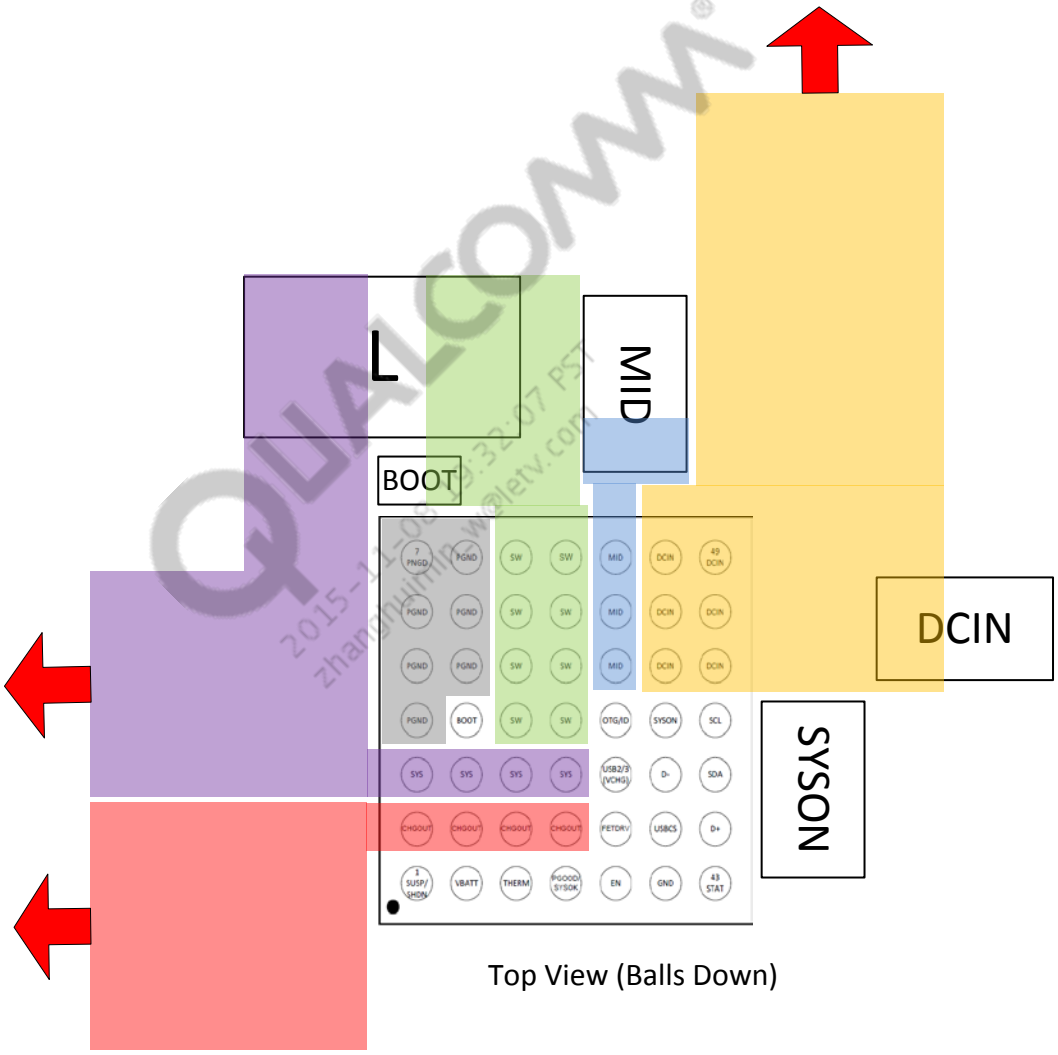

Figure 8-4 Ideal component placement

8.3 Typical BoM

Table 8-1 Bill of material

Item	Description	Vendor/part number	Quantity
1	10 kΩ, 0402, 1/8 W	Any	1

Item	Description	Vendor/part number	Quantity
2	4.7 µF, 0805, X5R, 16 V	Any	4
3	10 µF, 0603, X5R, 6.3 V	Any	1
4	33 nF, 0402, NPO, 25 V	Any	1
5	22 µF, 0603, X5R, 6.3 V	Any	1
6	Switching Li+ battery charger	SMB1350/SMB1351	1
7	1.0 µH, low DCR, I_{SAT} > 5 A	CIGT252010EH1R0MNE	1
8	Low R_{DSON} PFET (optional)	Analog power AM7321P	1
9	Schottky diode 3 A (optional)	DB2W31900L	1
10	PMUX (optional)	OnSemi NCP3901	1

8.4 Dual input support with external PMUX

A dual input, single output power source multiplexer (PMUX) has been built by a partner organization to support dual inputs with the SMB1350/SMB1351. The PMUX supports two modes of operation to fill two types of applications, autonomous mode and slave mode. The modes of operation are differentiated by biasing a MODE pin in different ways. For most SMB1350/SMB1351 applications, the PMUX should be used in autonomous mode. In autonomous mode, the CTRL pin serves as a functional enable pin, and the two enable logic pins are repurposed to provide interfacing functions with the PMIC system.

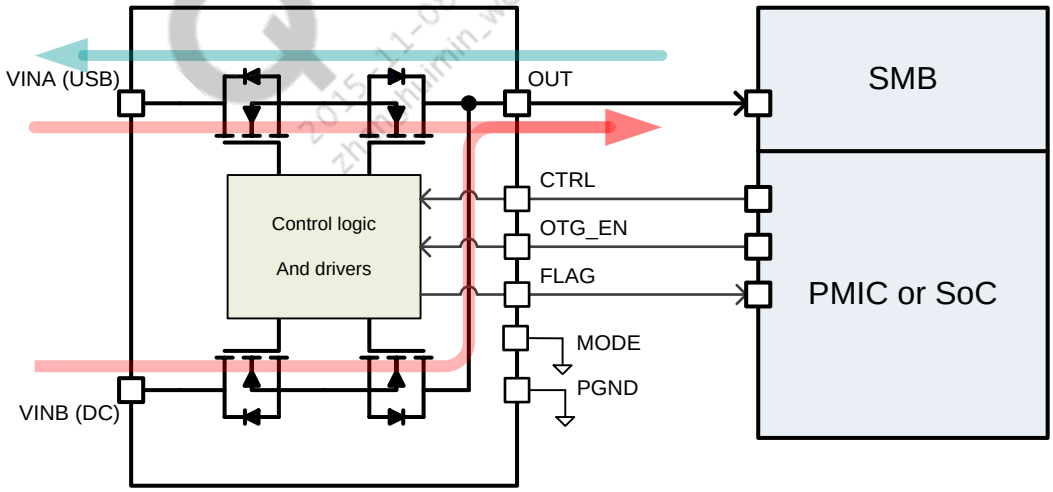

Figure 8-5 PMUX in autonomous mode

8.4.1 PMUX device operation

In autonomous mode, the PMUX uses its own logic to determine which input path should conduct and provide information to the system. Pulling MODE low puts the PMUX in autonomous mode that uses OTG enable and flag signals to interact with the system. In

autonomous mode, the CTRL pin can be asserted high to serve a LOCK function. Table 3-2 defines this logic.

Table 8-2 PMUX autonomous mode pin logic

Pin name	Pin description (autonomous mode)	Technical details
VINA	Priority input path when both inputs are present, passes through power when OTG Enable is high	28 V rating
VINB	Secondary input path	20 V rating
VINA_SNS	Provides protected sensed voltage of VINA	28 V rating
OUT	Output path of VINA/B and can also be treated as an input power path to supply VINA in OTG mode	20 V rating
OTG_EN	I/O to enable VINA current path to enter OTG mode	Uses 1.8 V logic to assert high
FLAG	I/O to indicate to the system when VINB is active. The system can pull this pin low to enable both VINA and VINB.	Push-pull capable of driving 1.8 V logic high and detecting when pulled low externally
CTRL	Pulled low to disable the LOCK function or high to enable the LOCK function and prevent an input switchover from VINB to VINA	Uses 1.8 V logic to assert high
MODE	Pulled to GND to enable autonomous mode	Pulled to GND with 2 kΩ maximum externally

8.4.1.1 OVP and surge protection

The PMUX can hold off 28 V DC on VINA and 20 V DC on VINB. The PMUX includes an OVP threshold that disables both VINA and VINB when the voltage applied to VINA or VINB exceeds 15 V. The response time of the overvoltage lock out is fast enough to prevent a voltage greater than 20 V at VOUT, including during IEC 61000-4-5 surge testing on VINA. In compliance with IEC 61000-4-5, both 1.2/50 µs and 10/700 µs surge waveforms up to 100 V, the PMUX clamps input voltage surges on VINA to 28 V and hold off the voltage. During these surges, the voltage at VOUT does not exceed 20 V.

8.4.1.2 Autonomous input control

In autonomous mode, VINA always assumes priority if both VINA and VINB are present. In the event of an input switch over, a 30 ms break-before-make timeout is set before allowing the second input to conduct. This allows the SMB1350/SMB1351 to detect the input has been swapped and re-detect the new input.

In order to prevent a system brown out during this 30ms break-before-make timeout, a LOCK function is available on the PMUX to prevent an input swap. This LOCK function is achieved by pulling the CTRL pin high with a GPIO. If VINB power is applied first followed by VINA, the PMUX does not allow an input switchover from VINB to VINA when CTRL is high. As soon as CTRL is pulled low, the break-before-make timer is applied. Alternatively, CTRL can be tied low if the LOCK function is not needed for an application. If VINA is removed with VINB power still applied, the PMUX will ignore the CTRL logic and initiate an input switchover after the break-before-make timer.

8.4.1.3 OTG enable

The 5 V is applied on the output of the PMUX during OTG mode. This 5 V is passed through the VINA path when the OTG_EN pin is driven high on the PMUX, regardless of the state of the LOCK function of the CTRL pin. When enabling OTG mode, VINA output powered from VOUT is soft-started for 1 ms.

- If the VINB source is conducting when OTG_EN is asserted, the PMUX will force the VINB source path off and enter the reverse OTG mode after 30 ms. If the VINB source is asserted after OTG_EN is asserted, the PMUX will ignore the VINB source until OTG_EN is removed. When OTG_EN is removed, the standard debounce times for VIN A/B are applied before the current path is enabled.
- If the VINA source is conducting when OTG_EN is asserted, the PMUX will ignore the OTG_EN logic since the VINA source power path is already active.
- If the VINA or VINB source is OV and not conducting, the PMUX will ignore the OTG_EN logic.

8.4.1.4 FLAG functionality

The FLAG pin on the PMUX serves two purposes: an indication to the system that the VINB path is active and a control input from the system that enables both VINA and VINB paths. This bidirectional functionality can be achieved using a single pin interface. The PMUX asserts FLAG by pulling it up above a 1.8 V logic high level immediately when VINB becomes active, simultaneous with soft-start beginning. The system should have this GPIO set as high-Z, with a maximum of 10 µA pull-down, initially to determine that VINB is conducting. The system can then pull this line low when requesting that the VINA path is enabled in addition to the VINB path. The PMUX will first check that VINA is below the UVLO threshold before enabling both paths; otherwise, it ignores the FLAG command.

9 Mechanical information

9.1 Device physical dimensions

The SMB1350/SMB1351 device is available in the 49WLNSP that includes ground pins for improved grounding, mechanical strength, and thermal continuity. The 49WLNSP has a 2.96 × 3.31 mm body with a maximum height of 0.55 mm. Pad 1 is located by an indicator mark on the top of the package. A preliminary version of the 49WLNSP outline drawing is shown in Figure 9-1. This figure will be updated in future revisions of this document.

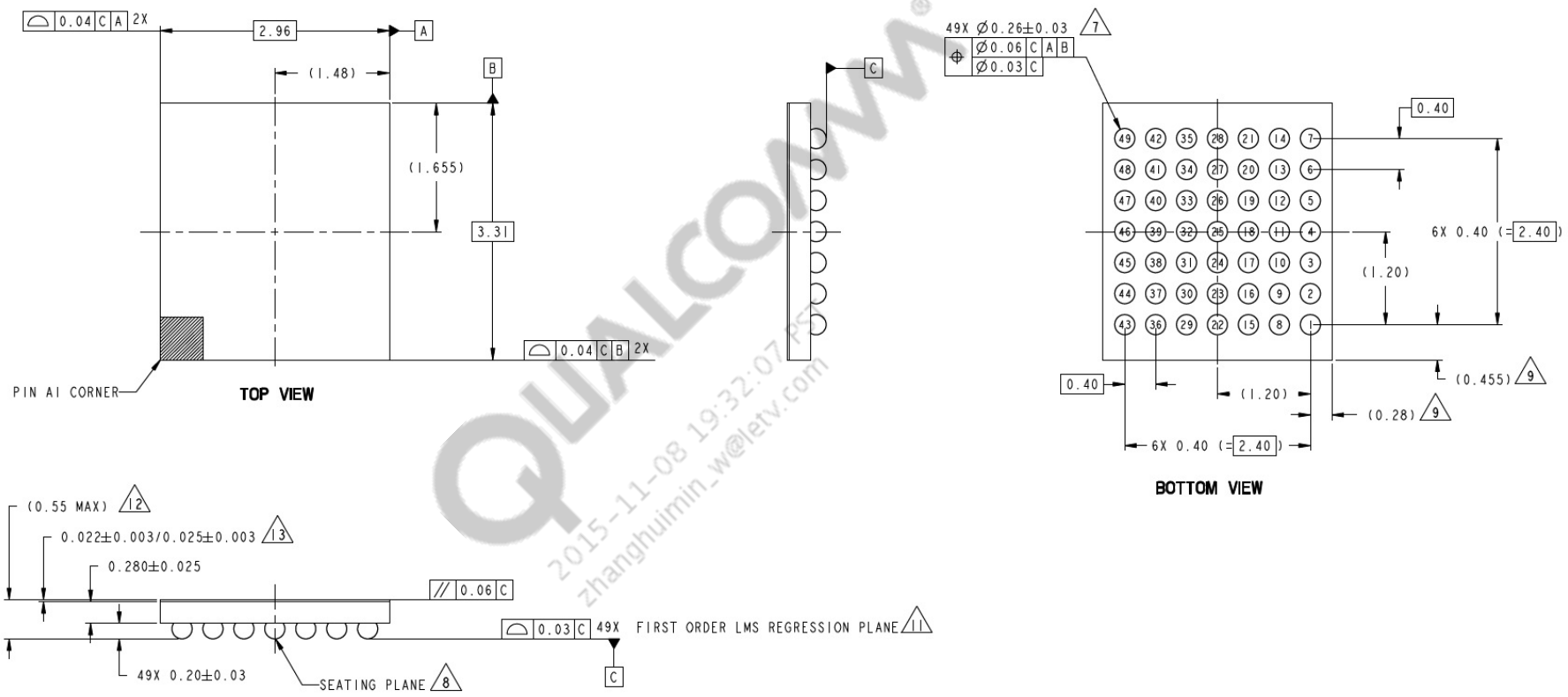

Figure 9-1 49WLNSP 2.96 × 3.31 × 0.55 mm package outline drawing

9.2 Part marking

Section 9.2 provides the preliminary information on the device marking for the 49WLNSP.

9.2.1 SMB1350/SMB1351 49WLNSP part marking

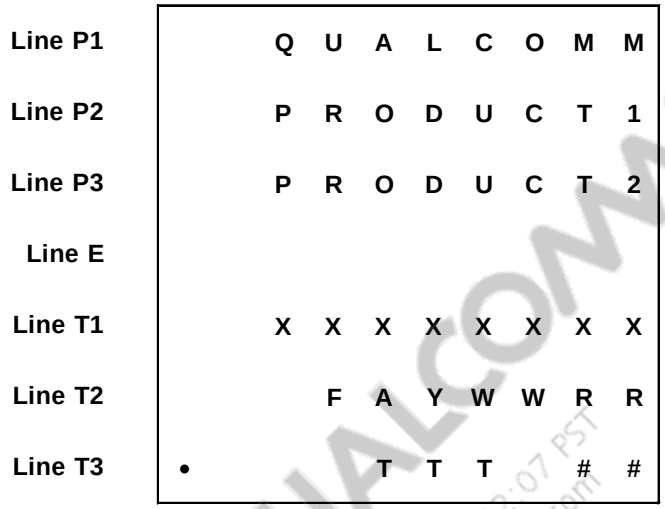

Figure 9-2 49WLNSP part marking (top view, not to scale)

Table 9-1 49WLNSP part marking line definitions

Line	Marking	Description
P1	Qualcomm	QTI name or logo
P2	PRODUCT1	Product name: SMB1350 SMB1351
P3	PRODUCT2	Config code + programmed ID
E	Blank or random	Additional content as necessary
T1	XXXXXXXX	Wafer lot trace ID
T2	FAYWWRR	F = wafer fab location source code ▪ M = Vanguard A = assembly code ▪ E = ASE Y = single/last digit of year WW = work week based on calendar year RR = revision code
T3	• TTT # #	• = dot identifying pin 1 TTT = engineering trace number # # = two-digit wafer number

9.3 Device ordering information

9.3.1 Specification-compliant devices

This device can be ordered using the item description shown in Figure 9-3.

Device ID code	AAA-AAAA-A	P	CCC	DDDDD	EE	RR	S	PI
Symbol definition	**Product name**	**Config code**	**Number of pins**	Package type	Shipping package	Product revision	Source code	Program ID
Example	**SMB-1350**	0	49	CWLNSP	TR	01	0	00
Example	**SMB-1351**	0	49	CWLNSP	TR	01	0	00
		P: always 0			HR = 100/reel SR = 500/reel TR = 4000/reel		S: always 0	PI: CSIR*

*The program ID (PI: CSIR) is sequential numeric (example 01, 02, …) and traced back to the CSIR with a part number. Multiple CSIRs will exist for a part number reflecting different device configurations. A sample item description/part number is: SMB-1351-0-40CWLNSP-TR-00-0-00.

Figure 9-3 Device ordering information

10 Carrier, storage, and handling information

Information about shipping, storing, and handling the SMB1350/SMB1351 device is presented in this chapter.

10.1 Carrier tape system

10.1.1 Tape and reel configurations

NOTE: Refer to *Approved Packing Materials for QTI IC Devices* (80-32511-5) for approved reels and protective bands.

Table 10-1 Units per reel

Products	MCN suffix	Units per reel	Reel Ø	Hub Ø
All	HR	100	178 mm	55 mm
	SR	500		
	TR	2000		

10.1.2 Carrier and cover tape

Table 10-2 Carrier tape attributes

Type	Feed	Width	Pitch	A0	B0	K0	K1
Flat	Single	12	8	3.14	3.49	0.73	–

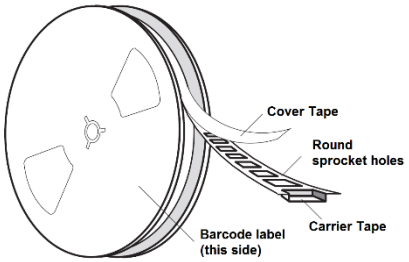

Figure 10-1 Tape orientation on reel

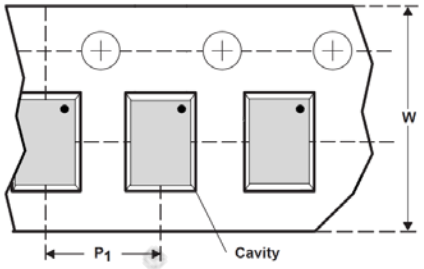

Figure 10-2 Part orientation in tape

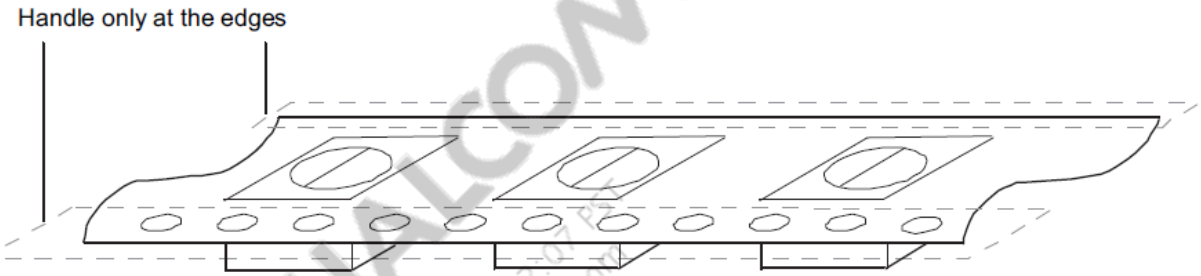

Figure 10-3 Carrier tape drawing (A)

10.2 Storage

10.2.1 Bagged storage conditions

SMB1350/SMB1351 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for the expected shelf life.

10.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Table 4-2.

10.3 Handling

Tape handling was described in Section 10.1.1. Other (IC-specific) handling guidelines are presented in the following sections.

10.3.1 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result. ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

See Table 4-1 for the SMB1350/SMB1351 ESD ratings.

10.4 Barcode label and packing for shipment

Refer to the *IC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

11 Part reliability

11.1 Reliability qualifications summary

Table 11-1 SMB1350/SMB1351 reliability qualification report for WLP-49 lead-free device from VIS

Tests, standards, and conditions	ASEKH sample	SCS sample	Result
AFR HTOL JESD22-A108 Stress temperature: 125 °C, duration: 240 hrs; 5 V DC supply from 3.6 V to 5.5 V, or DCIN from 3.6 V to 14 V bypassing with 4.7 µF MLCC, Tuse = 55 °C, Ea = 0.7, Gamma = 7, HTOL duration 240 hrs	240	N/A	λ = 35 FIT, pass
Mean time to failure (MTTF) t = 1/λ (million hrs)	240	N/A	~ 12 yrs
ESD – human-body model (HBM) rating; JESD22-A114-B	3	N/A	1500 V, all pins
ESD – charge device model (CDM) rating; JESD22-C101-D	3	N/A	500 V, all pins
Latch-up (I-test): EIA/JESD78 Trigger current: ±100 mA; temperature: 85 °C	3	N/A	Pass
Latch-up (V-supply overvoltage): EIA/JESD78 Trigger voltage: 1.5x Vdd; temperature: 85 °C	3	N/A	Pass
Moisture resistance test (MRT): MSL1; J-STD-020 3x reflow cycles @ 255 °C +5/-0 °C 100% CSAM delamination inspection	478	478	Pass
Temperature cycle: JESD22-A104 Temperature: -55 °C to +125 °C; number of cycles: 1000 Soak time at min/max temperature: 20 min Cycle rate: 2 cycles per hour (cph) **Preconditioning: MSL1;** JESD22-A113 Reflow temperature: 255 °C +5/-0 °C	240	240	Pass
Unbiased highly accelerated stress test (UHAST) JESD22-A118: 130 °C/85% RH **Preconditioning: MSL1;** JESD22-A113 Reflow temperature: 255C +5/-0 °C,	240	240	Pass
High temperature storage life (HTS): JESD22-A103 Temperature = 150 °C, 1000 hrs	240	240	Pass

11.2 Ball shear mechanical rating

Table 11-2 Ball shear rating

Quality characteristic	Criteria	Result		
		0X	5X	10X
Ball shear max	>2.5 g/mil2	4.43	4.51	5.11
Ball shear min	>2.5 g/mil2	3.64	3.66	3.16
Ball shear AVG	>2.5 g/mil2	3.9	4.13	4.25
Ball shear STDEV	N/A	0.21	0.24	0.37
Ball shear CPK	> 1.67	6.18	5.81	3.85