VERSION HISTORY

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Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Release version	2015-04-22			
Ver 1.3	Added USB port power option	2016-01-13			

Pine A64

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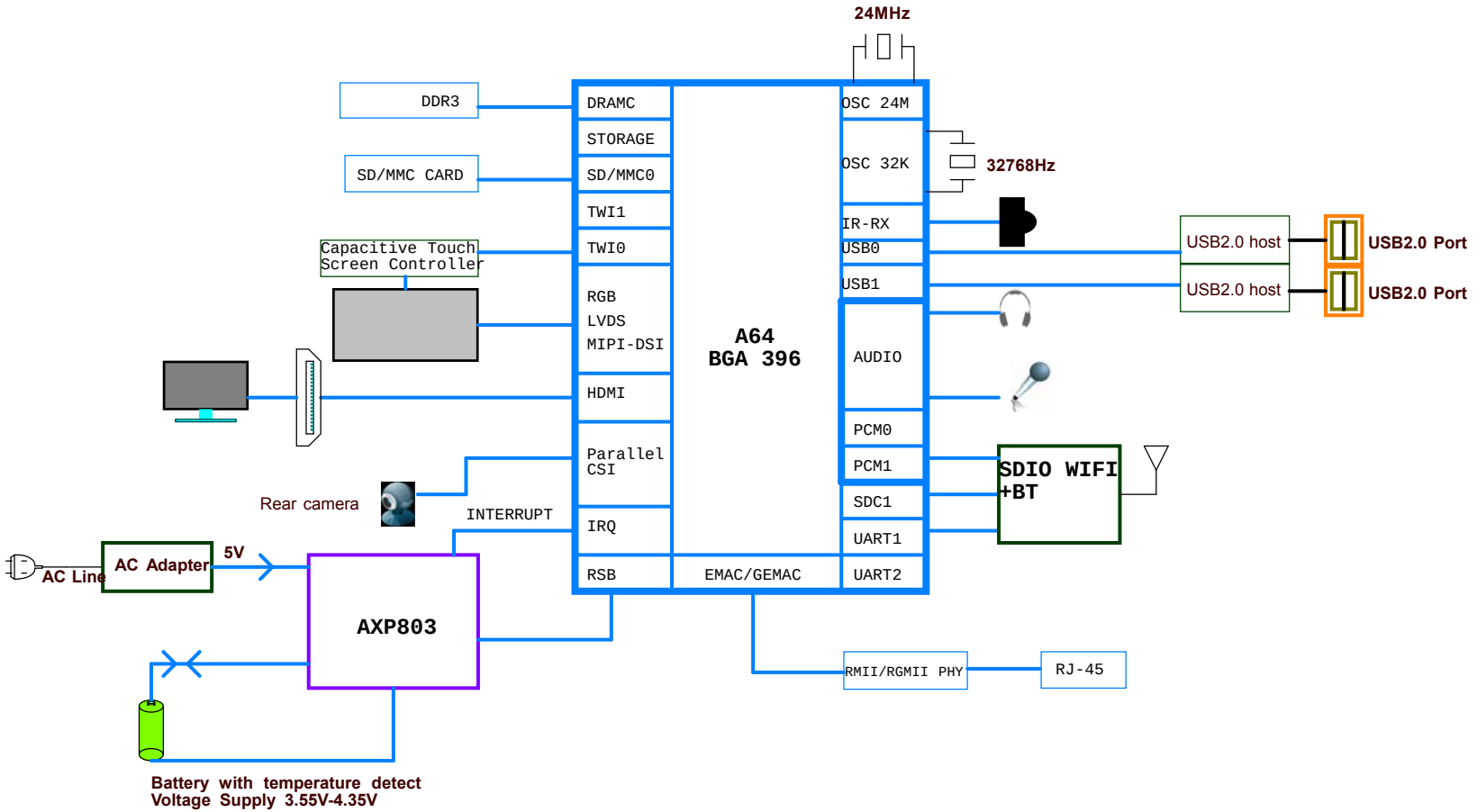
BLOCK DIAGRAM



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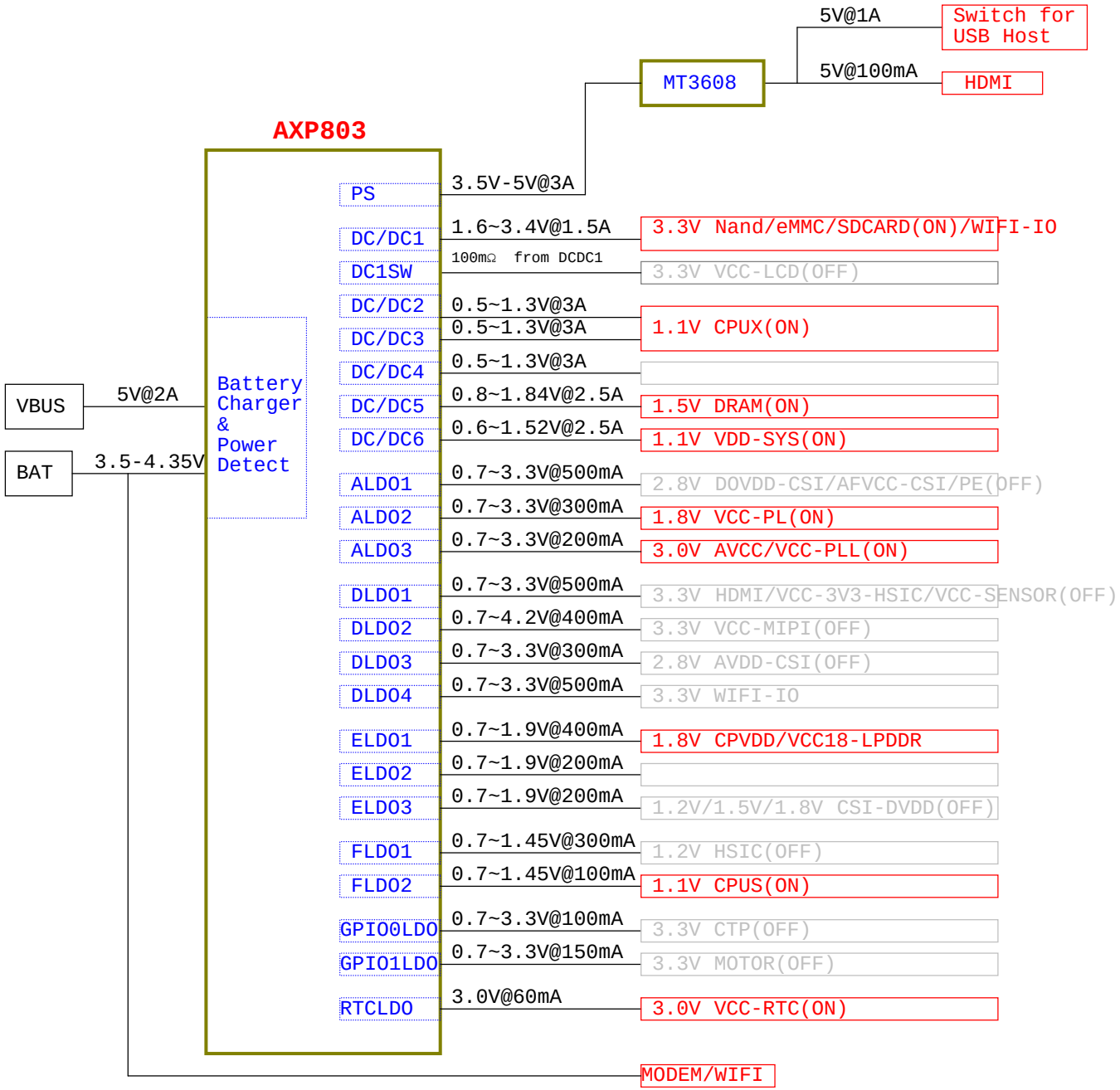
POWER TREE



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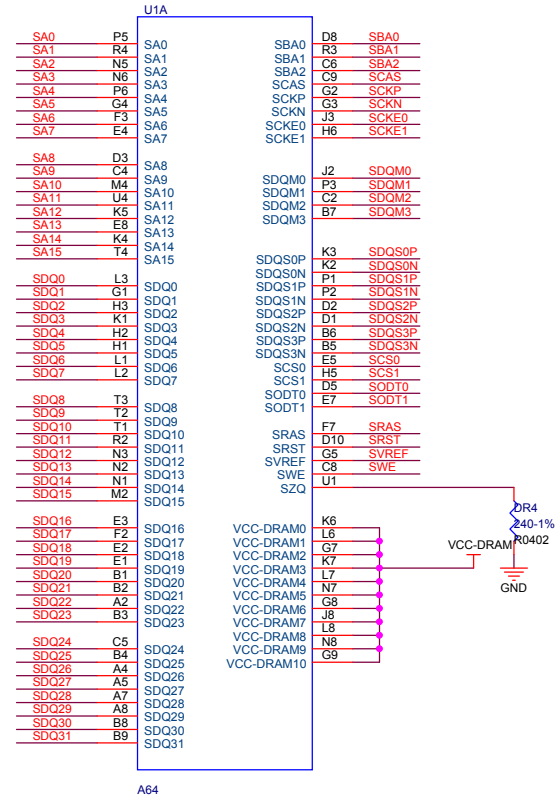
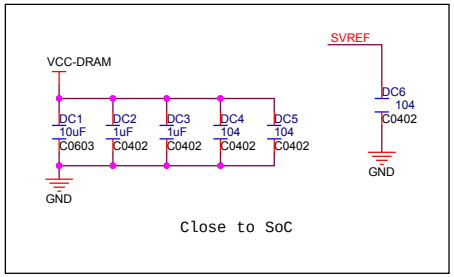
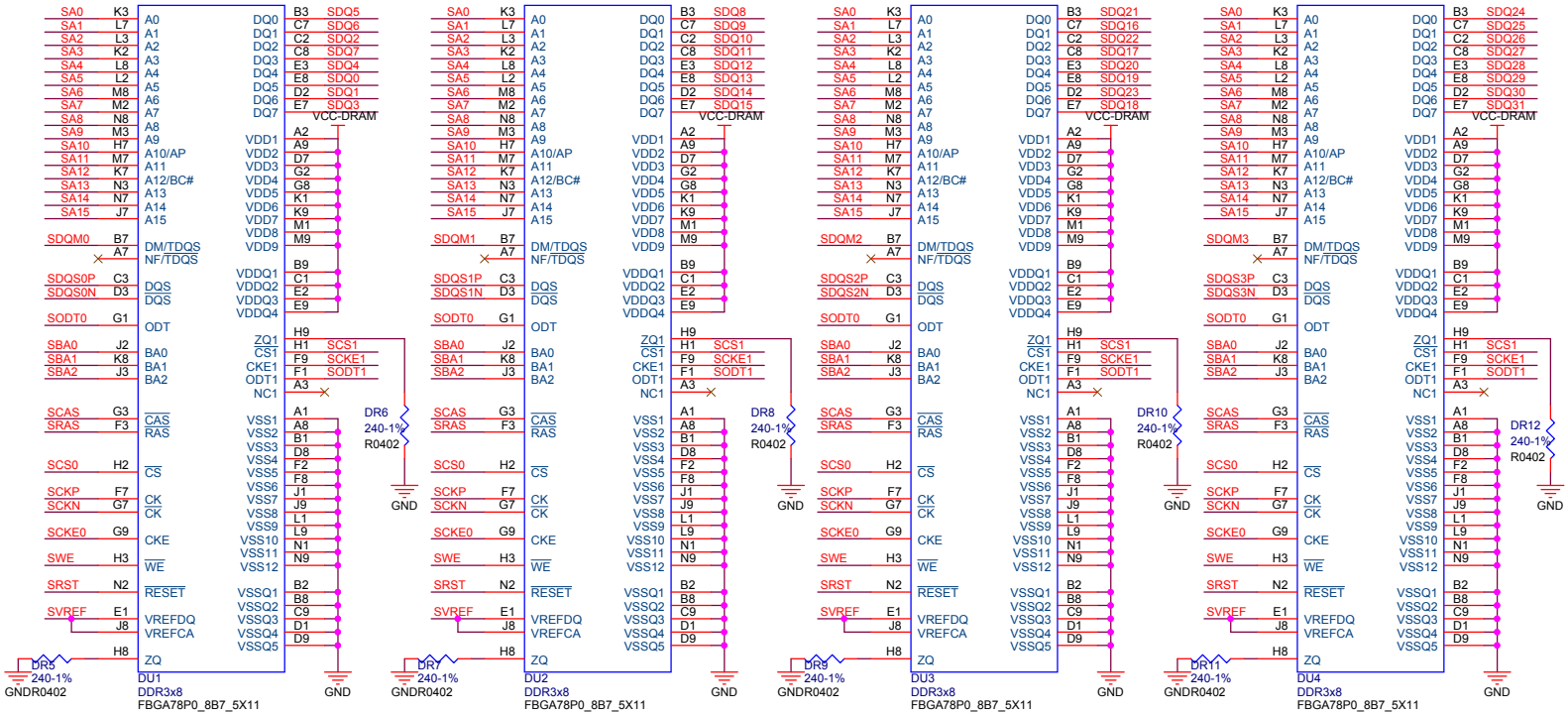
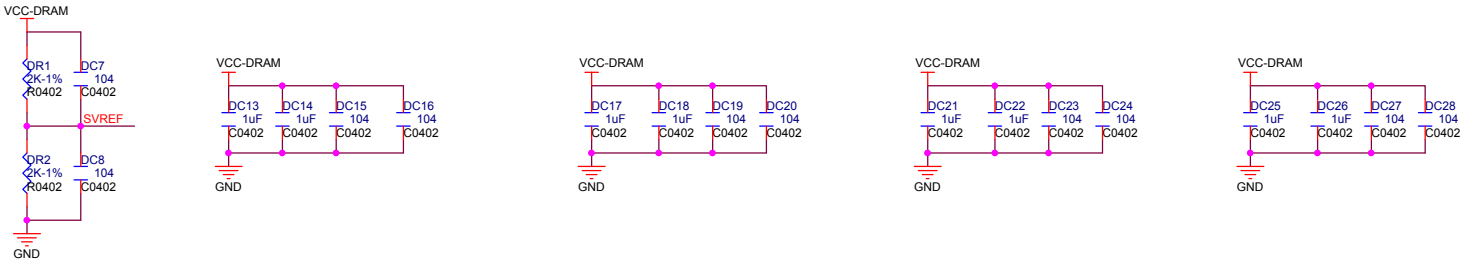
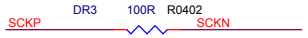
DDR3 8bx4











Pine A64

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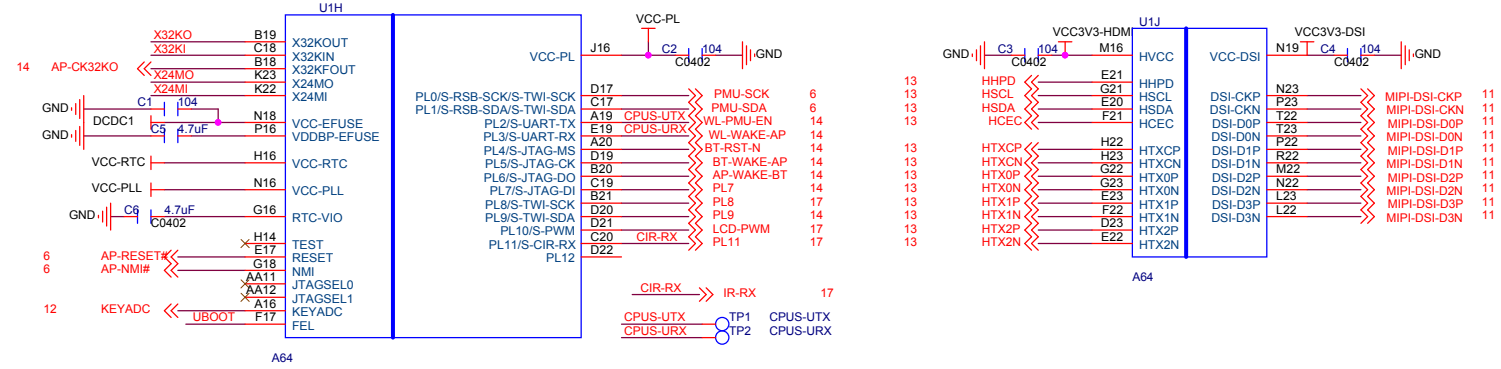
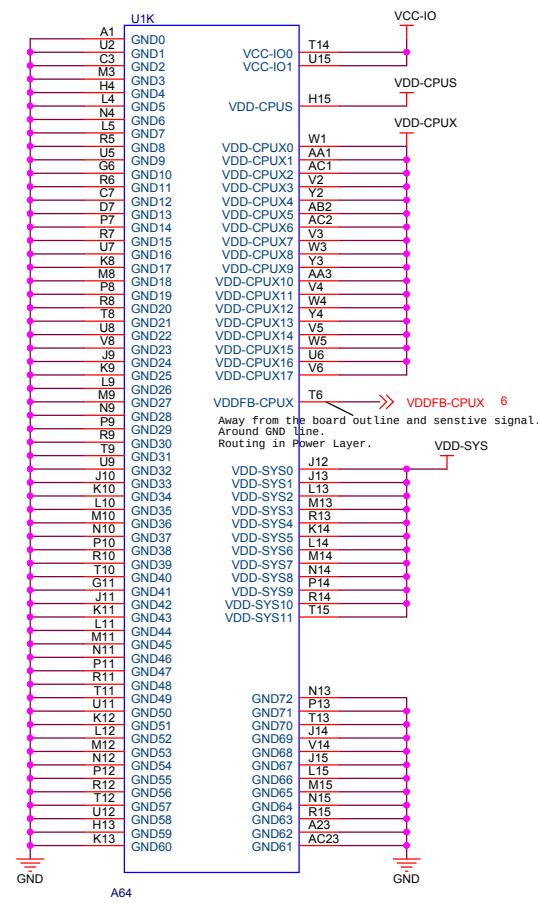
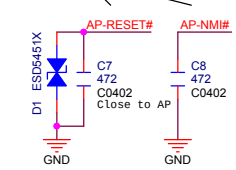
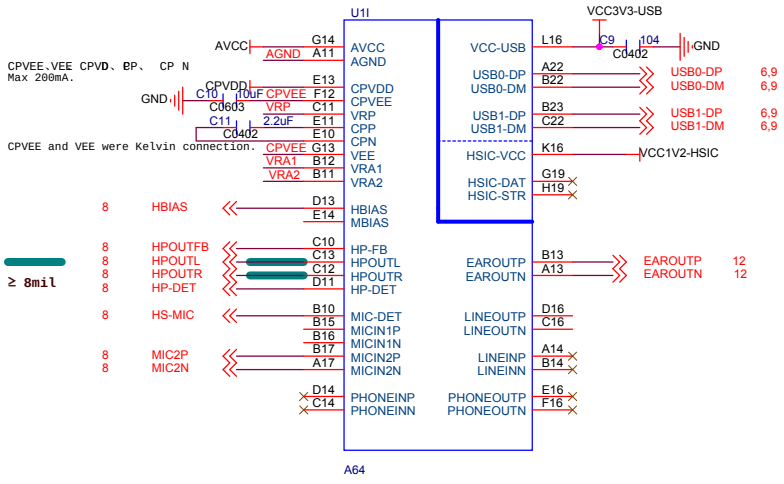
CPU

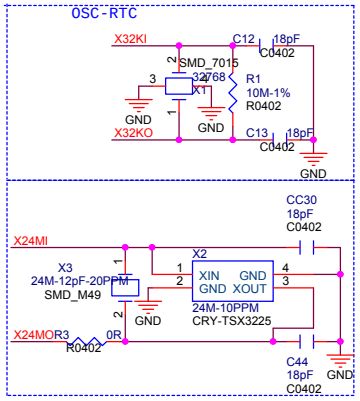


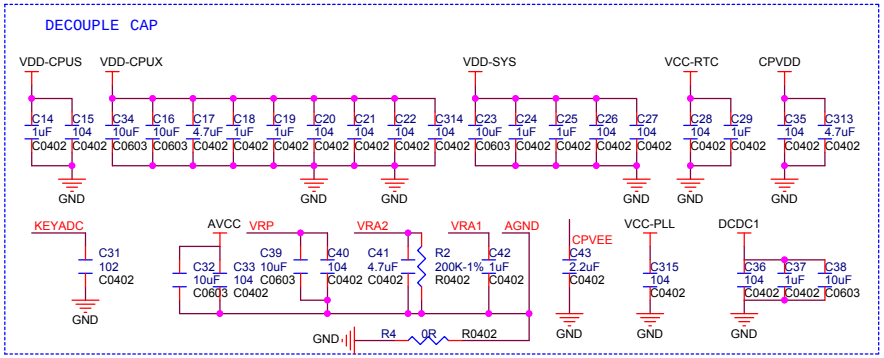


Away from the board outline and senstive signal.
Around GND line.









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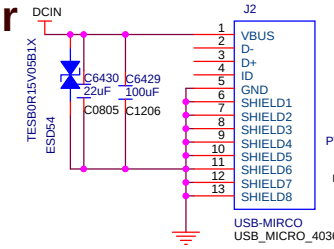
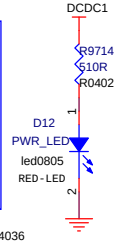
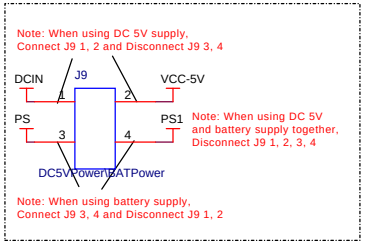
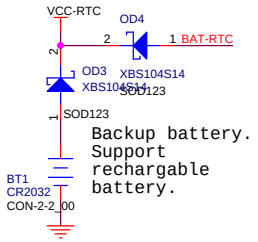
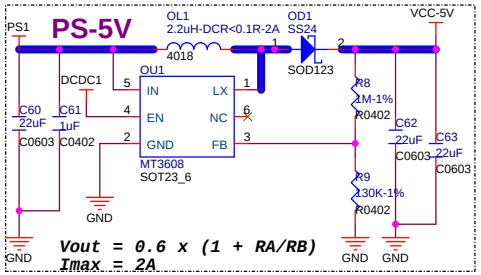
Power

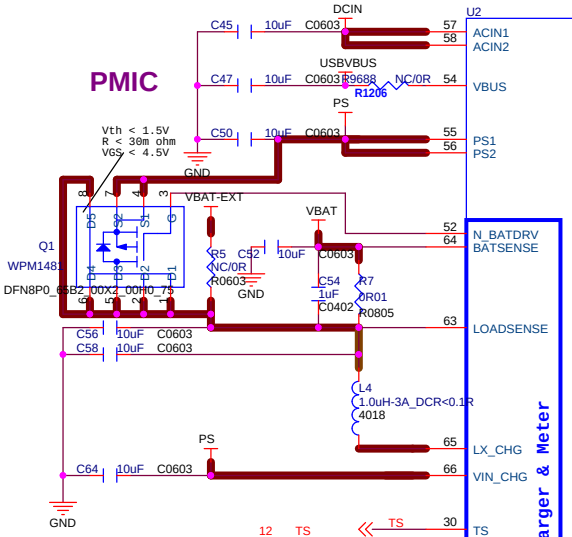


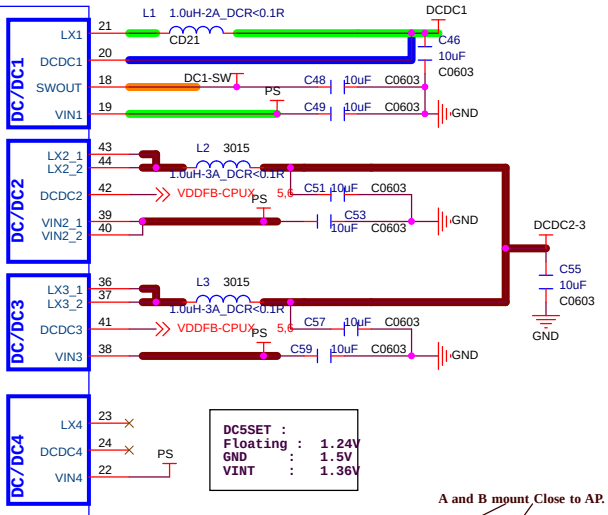


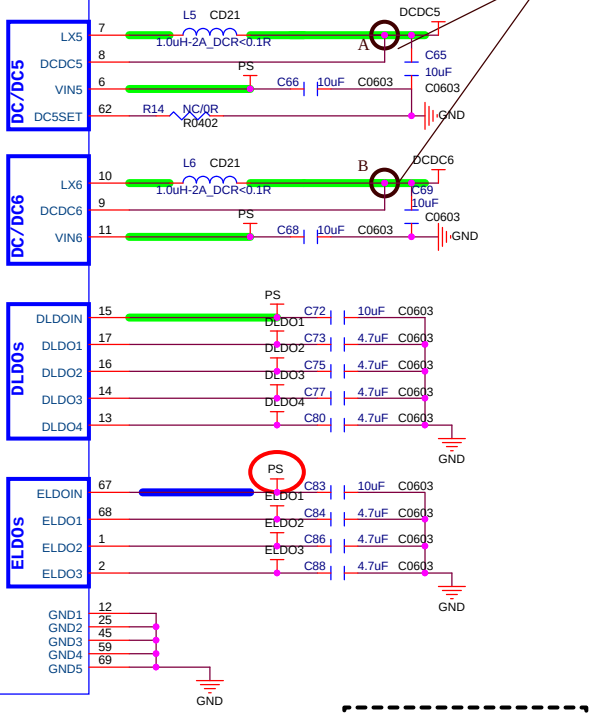


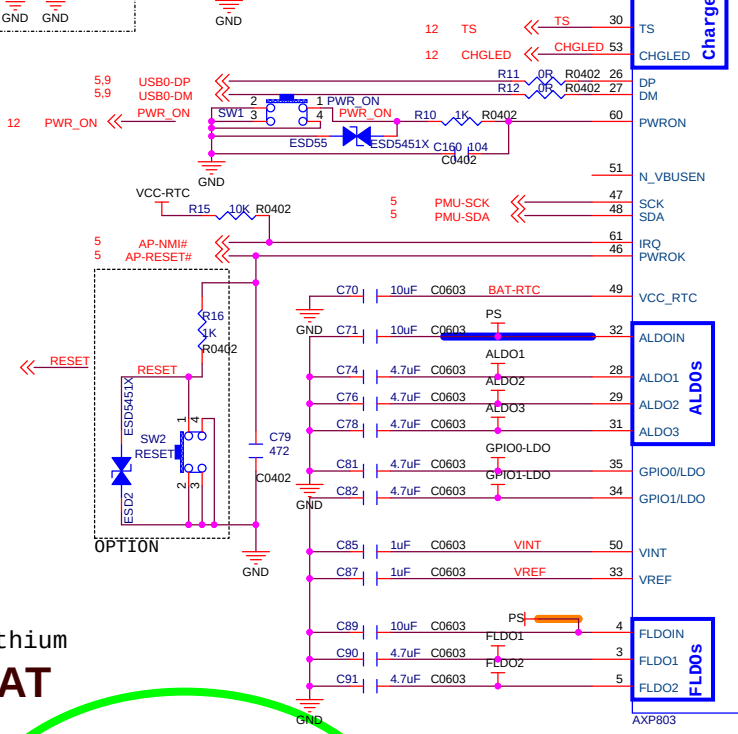


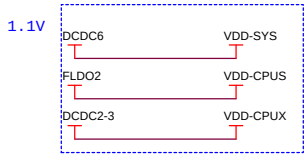


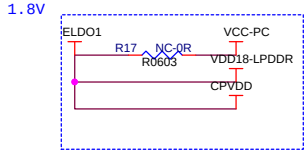


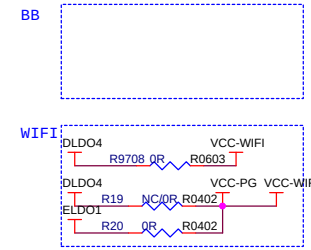


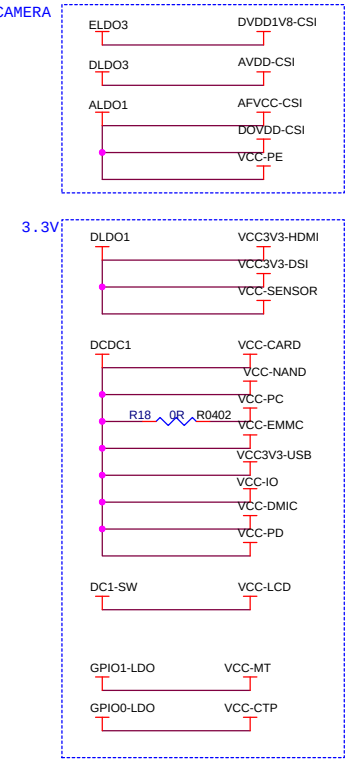


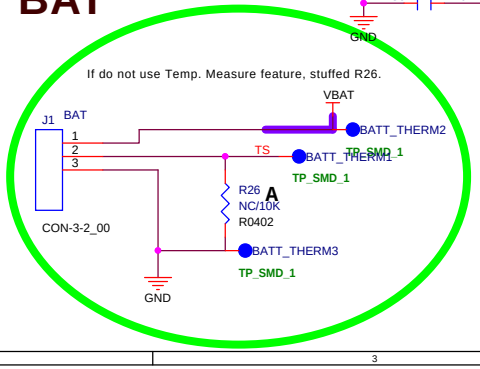


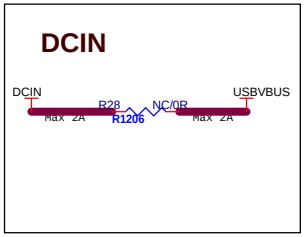


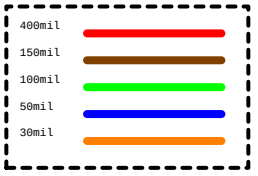












Pine A64

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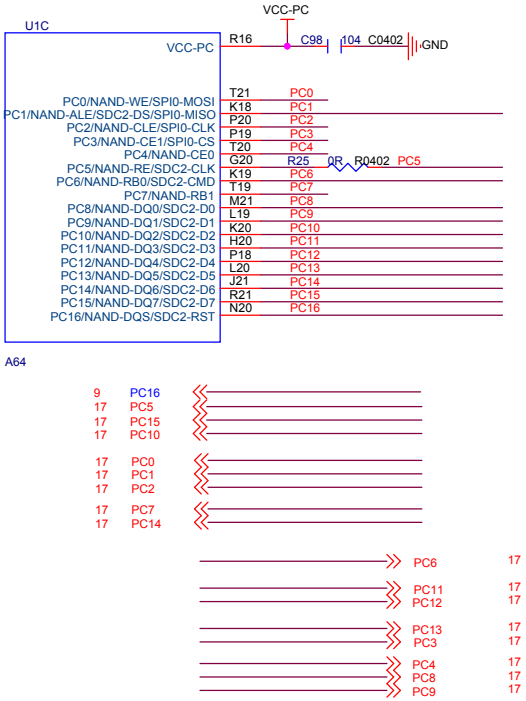
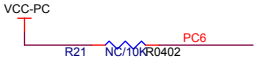
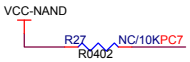
NAND/eMMC







Pine A64			
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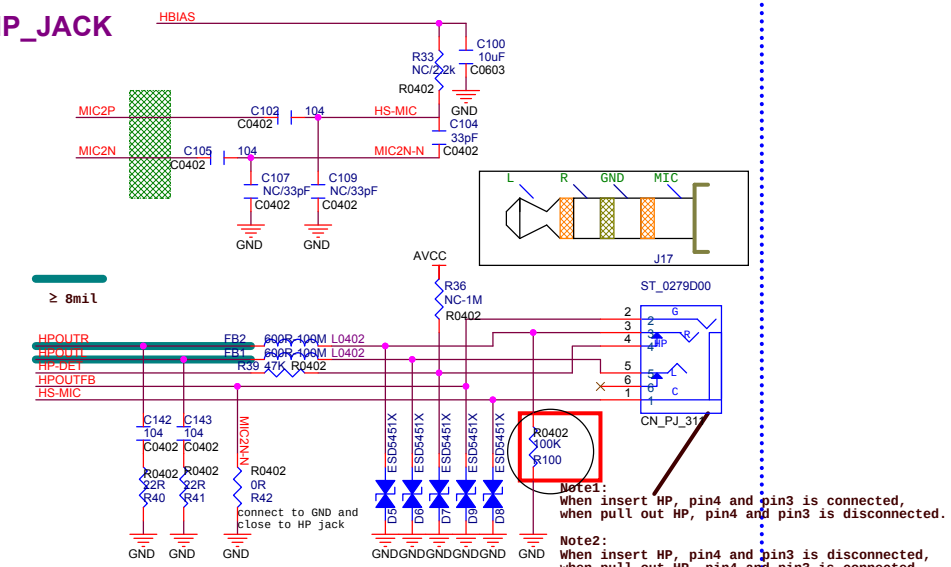
AUDIO

HP_JACK



Note1:
When insert HP, pin4 and pin3 is connected,
when pull out HP, pin4 and pin3 is disconnected.

Note2:
When insert HP, pin4 and pin3 is disconnected,
when pull out HP, pin4 and pin3 is connected.
Mount R100 3.3K.

5 HBIAS

5 HP-DET
5 HPOUTFB
5 HPOUTL
5 HPOUTR

5 MIC2N
5 MIC2P

5 HS-MIC

5 EAROUTP
5 EAROUTN

AVCC

VCC-5V

Pine A64			
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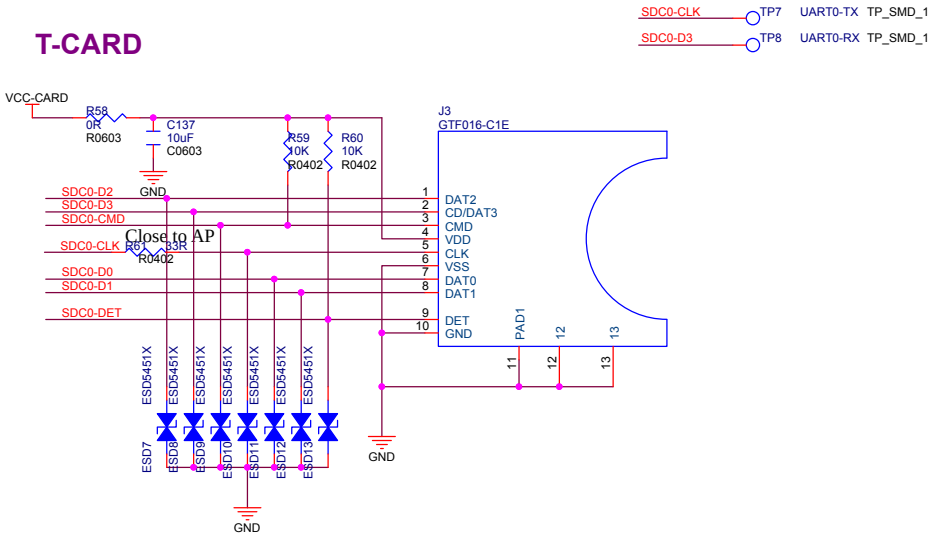
T-CADD/USB

T-CARD



U1G

PF0/SDC0-D1/JTAG-MS1	AB10	SDC0-D1
PF1/SDC0-D0/JTAG-DI1	W13	SDC0-D0
PF2/SDC0-CLK/UART0-TX	AC8	SDC0-CLK
PF3/SDC0-CMD/JTAG-DO1	W9	SDC0-CMD
PF4/SDC0-D3/UART0-RX	AB6	SDC0-D3
PF5/SDC0-D2/JTAG-CK1	AB9	SDC0-D2
PF6	AB8	SDC0-DET

PH0/TWI0-SCK	W11	TWI0-SCK	11
PH1/TWI0-SDA	AA10	TWI0-SDA	11
PH2/TWI1-SCK	AC4	TWI1-SCK	17
PH3/TWI1-SDA	AA9	TWI1-SDA	17
PH4/UART3-TX	AB5	CTP-INT	11
PH5/UART3-RX	AC7	PH5	17
PH6/UART3-RTS	AB4	PH6	17
PH7/UART3-CTS	AC5	PH7	17
PH8/SPDIF-OUT	Y10	PH8	12
PH9	AA8	PH9	17
PH10/MIC-CLK	Y8	LCD-BL-EN	11
PH11/MIC-DATA	AA5	CTP-RST	16

A64

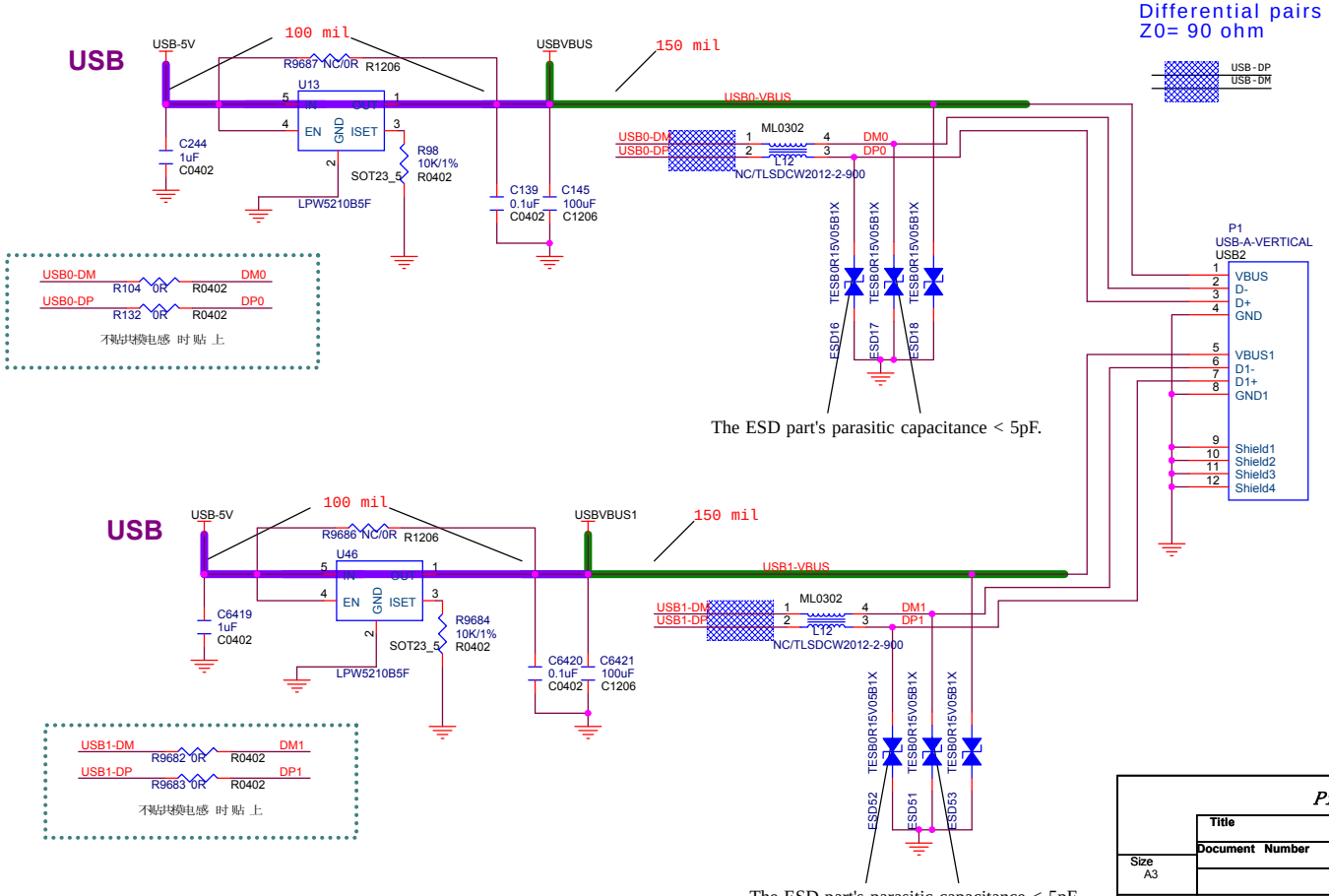
VCC-CARD

5,6 USB0-DM
5,6 USB0-DP
5,6 USB1-DM
5,6 USB1-DP

USB-5V

DCDC1

USB



USB

Pine A64			
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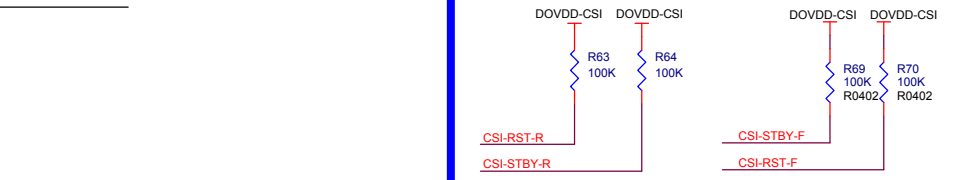
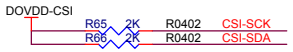
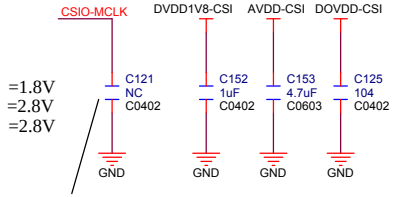
CAMERA

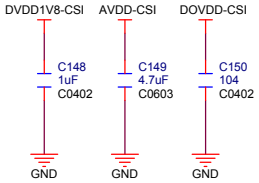






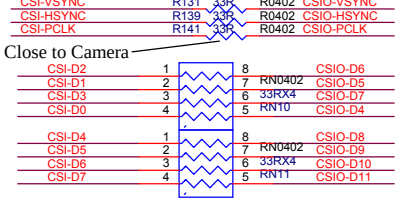
DVDD1V8-CSI =1.8V
DOVDD-CSI =2.8V
AVDD-CSI =2.8V

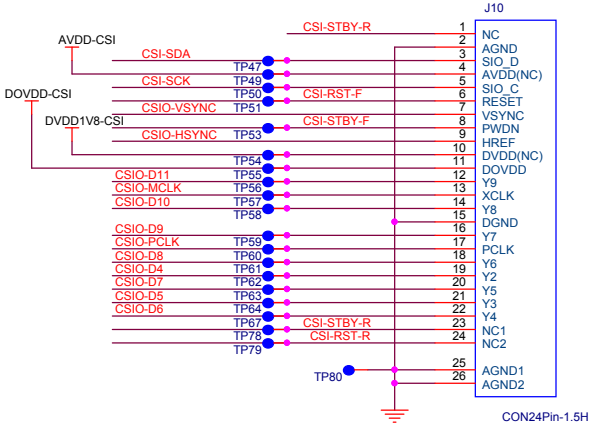
Close to camera.

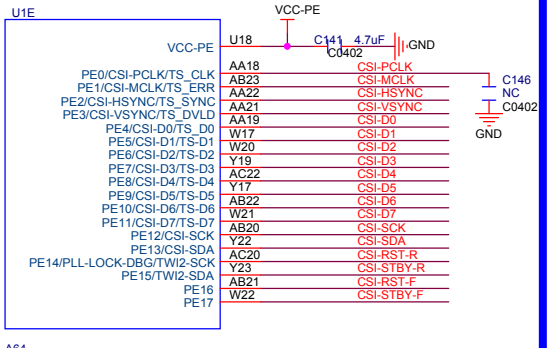


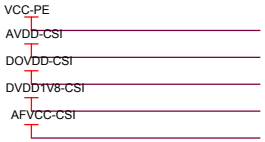
Close to AP

Close to Camera









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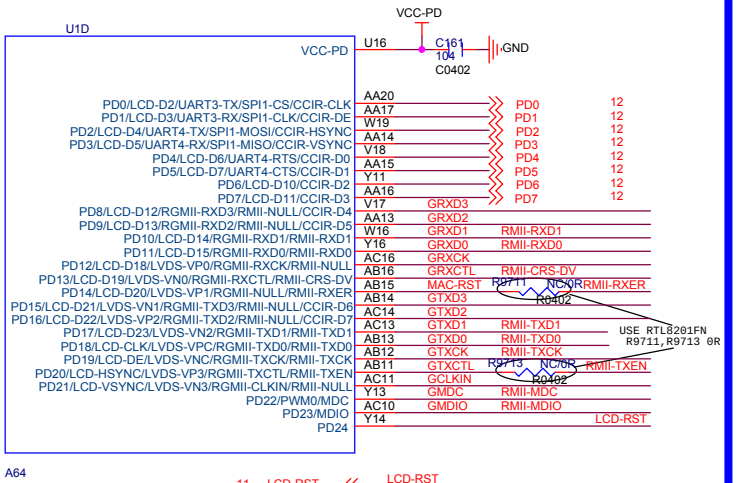
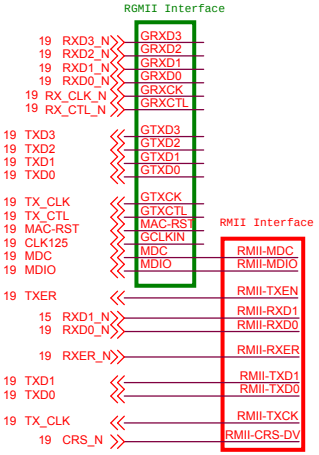
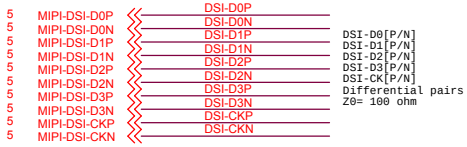
LCD

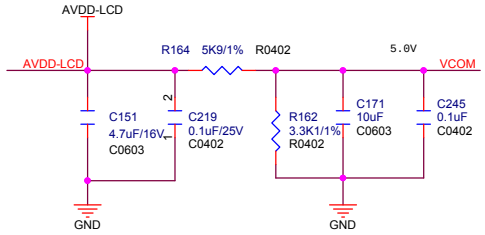


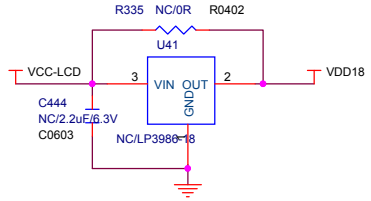
11 LCD-RST <<< LCD-RST

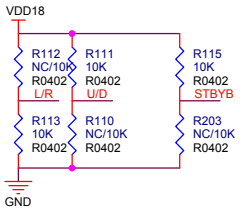


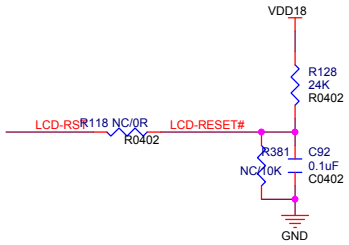


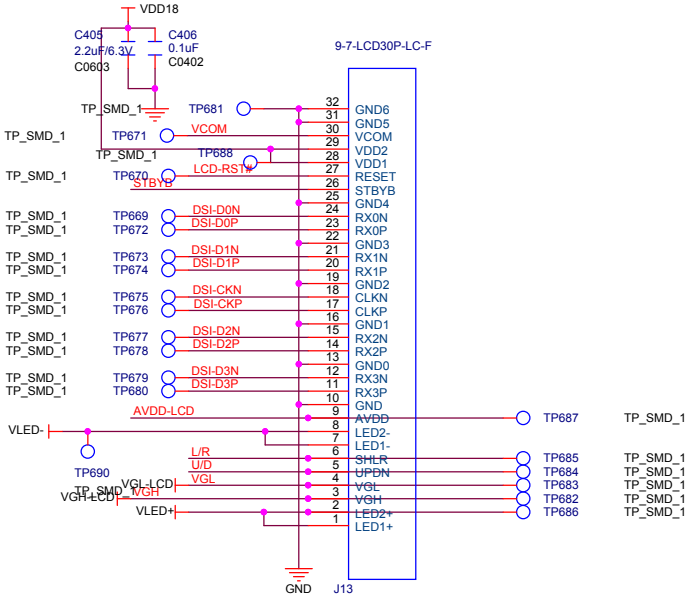
MIPI-LCD

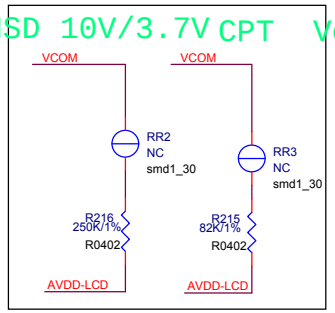












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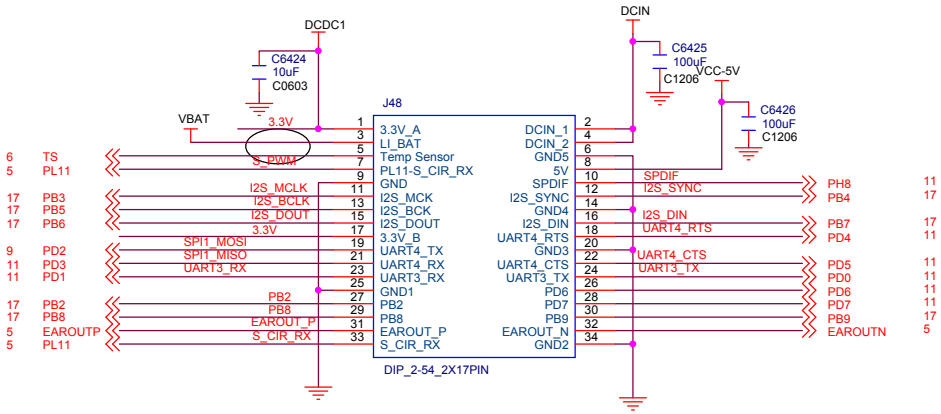
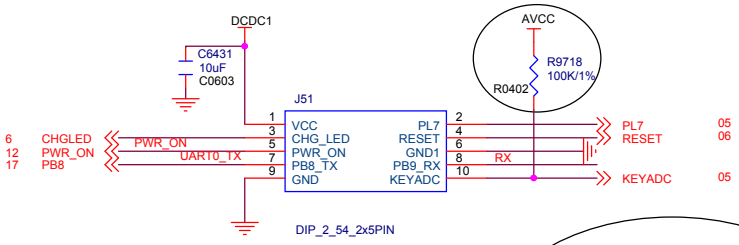
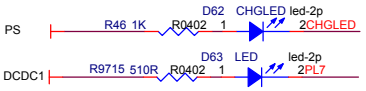
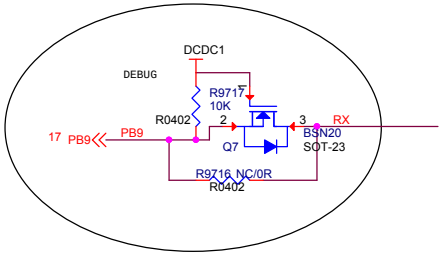
Euler bus









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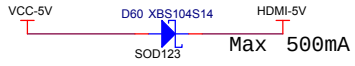
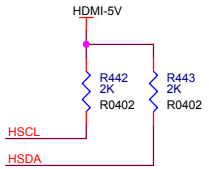
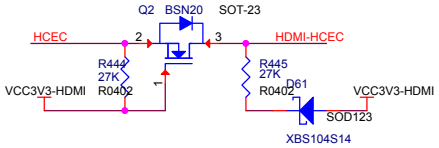
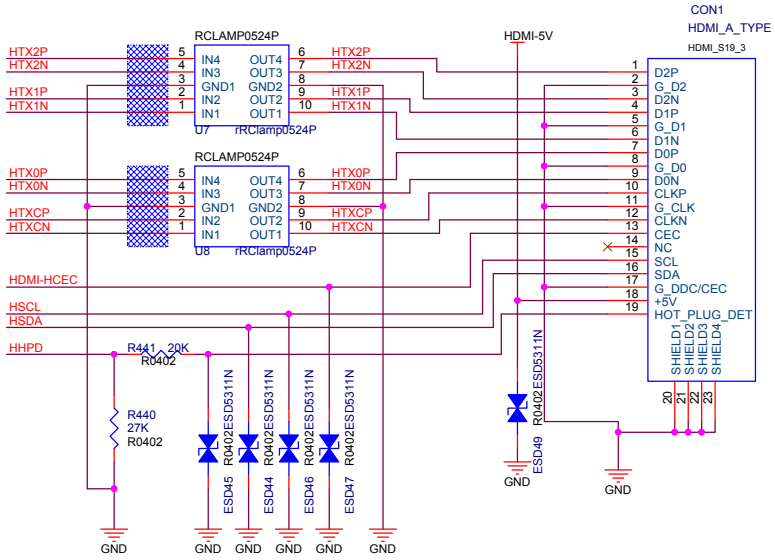
HDMI



Differential pairs
Z0= 100 ohm







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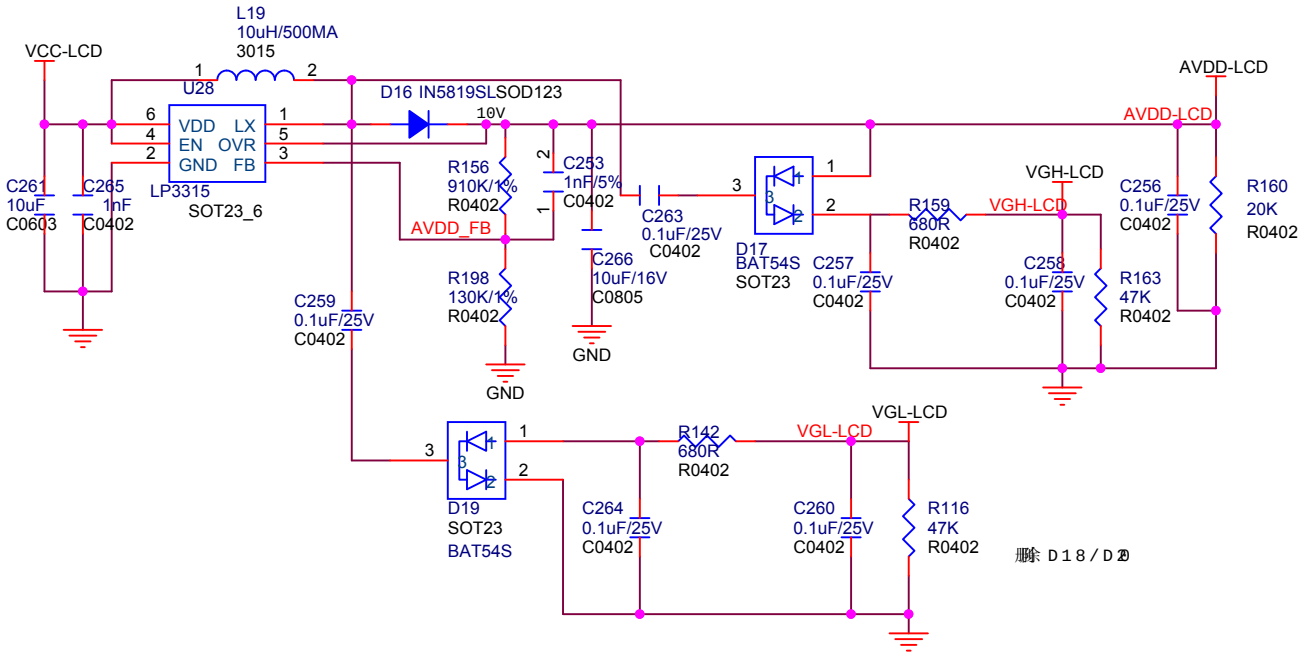
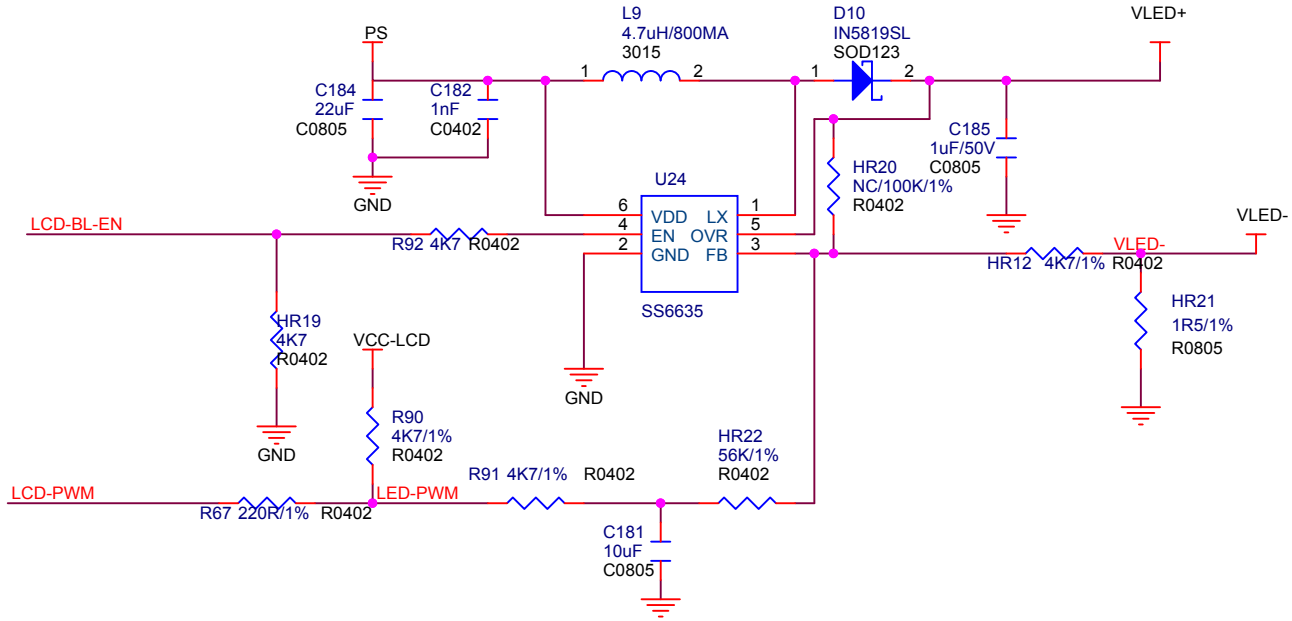
LCD POWER

6 LCD-PWM
6 LCD-BL-EN



Backlight



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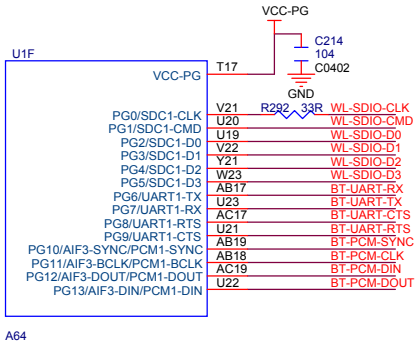
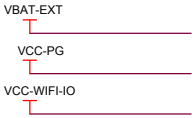
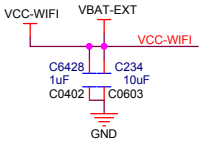
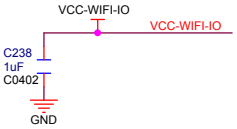
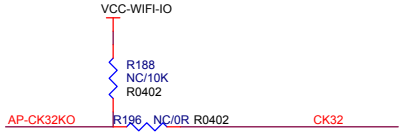
WIFI+BT

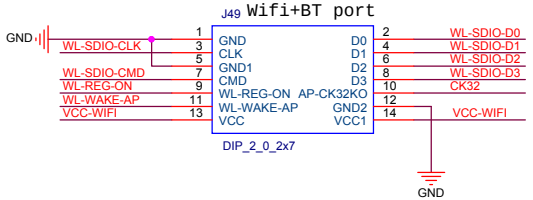


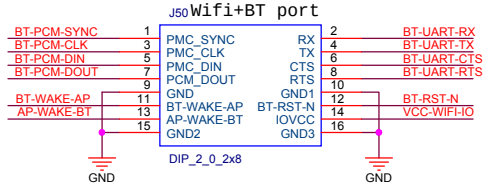












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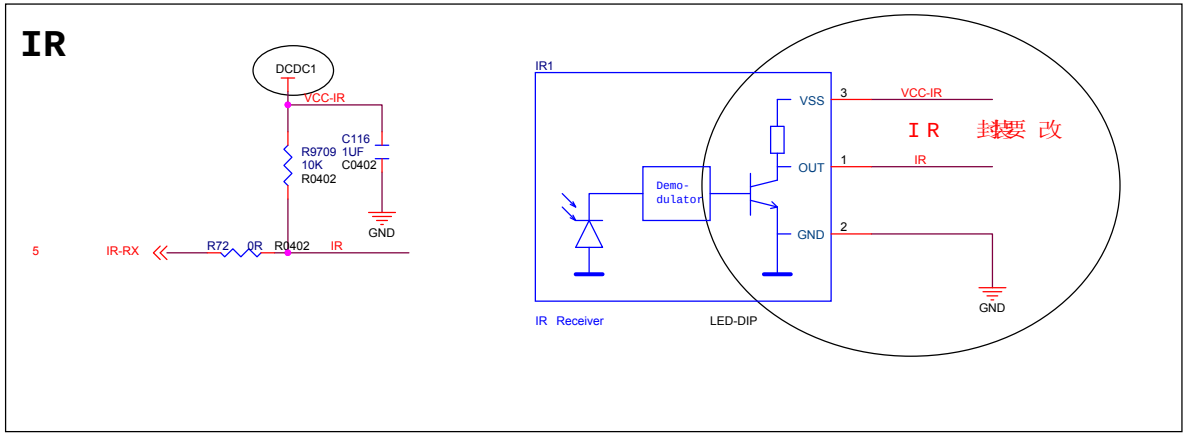
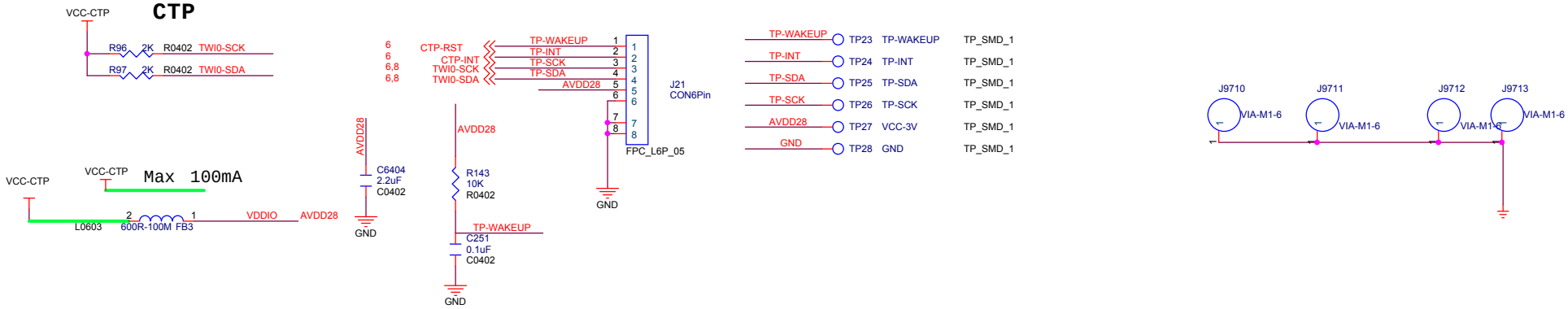
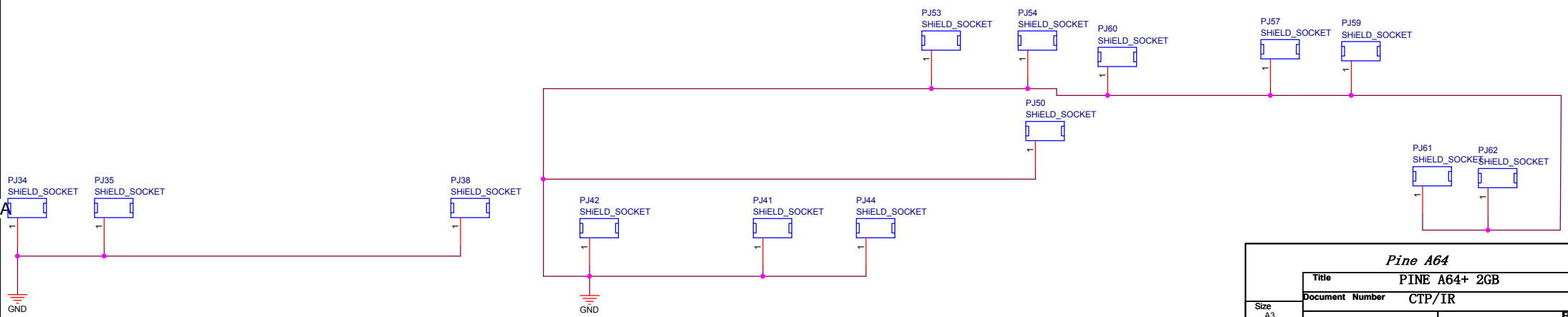
CTP

IR



CTP





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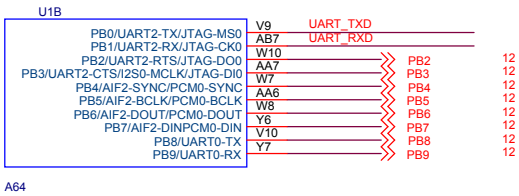
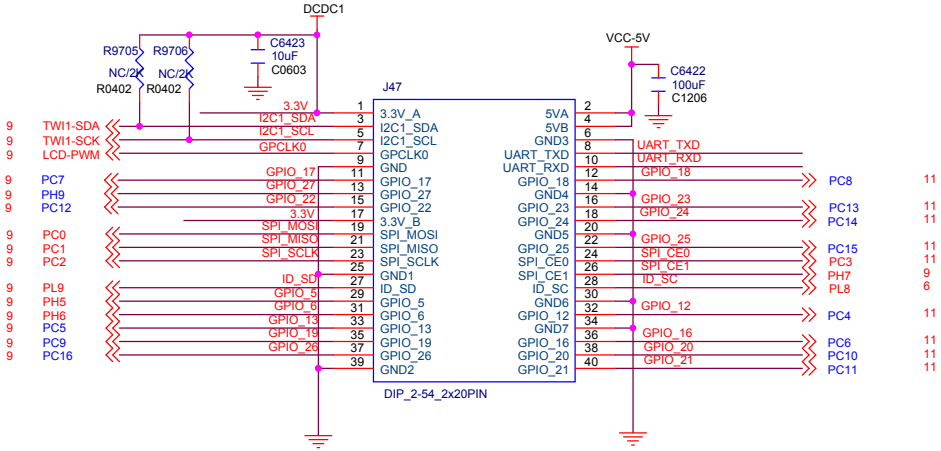
PI-2 bus





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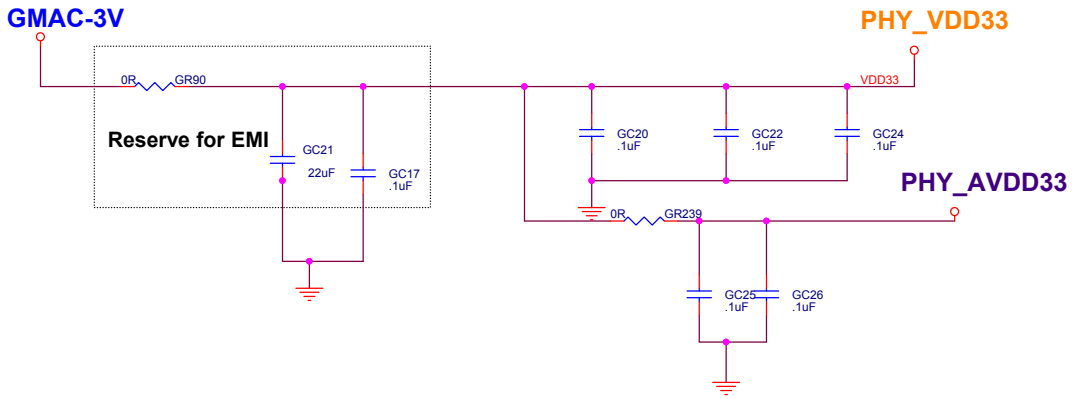
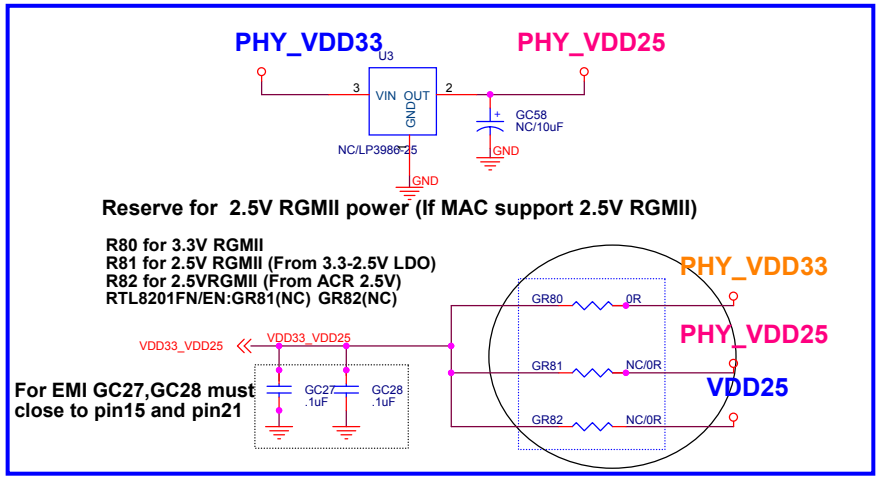


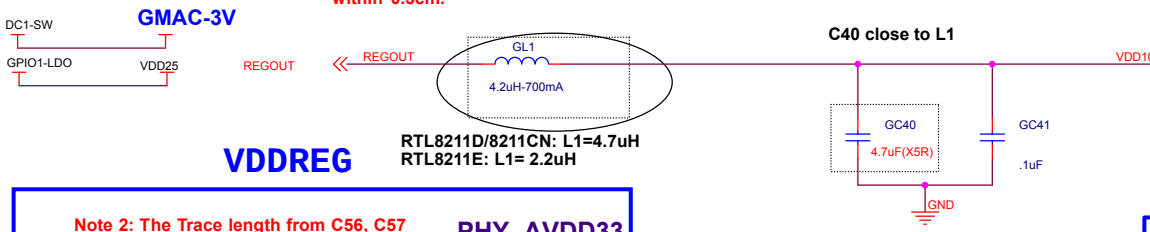


RTL8211CN/D/E	GL1	C56	U10	GR65	GR66	GR122	GC41/GC57
Enable switching regulator	O	O	X	O	X	X	O
Disable switching regulator	X	X	O	X	O	O	X

Note 1: The Trace length between GL1 and Pin 48 must be within 0.5 cm. GC40 and GC41 toG L1 must be within 0.5cm.

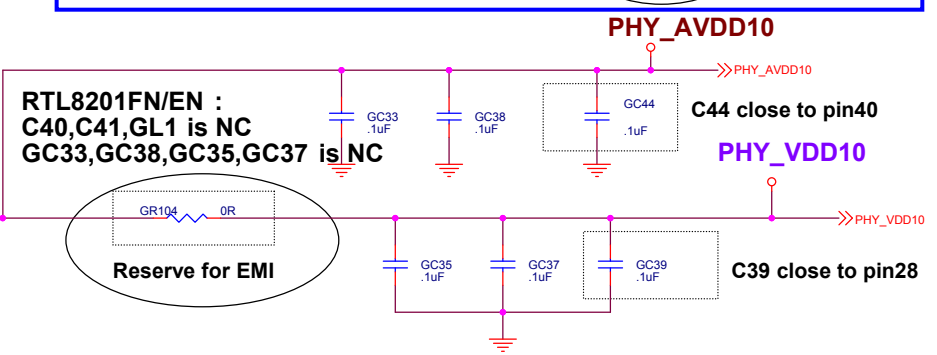
RTL8211D/8211CN:GC40 22uF(X5R)
RTL8211E: GC40 4.7uF(X5R)

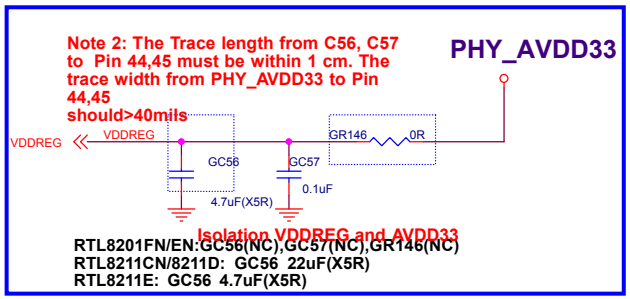
C40 close to L1

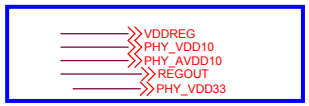


RTL8211D/8211CN: L1=4.7uH
RTL8211E: L1= 2.2uH

VDDREG



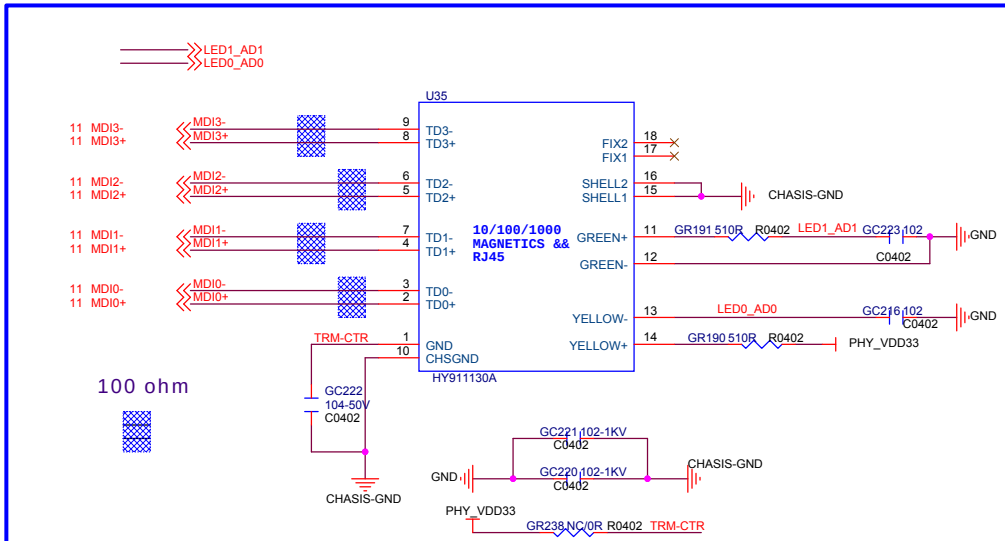




External Power Source

U10,GC69,GC68, GR122,GR120 and GR121 are only used by 8211CN/8211D/8211E application when switching regulator is disabled. For other applications, please remove them.

RESERVE



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RTL8211CN/8211D/8211E/8201FN/8201EN

PME

PHY_VDD33

Note: PME Function
RTL8211D/8211E/ 8201FN only
RTL8201EN/8211CN Pin33 is NC

GR109 4.7K

PME → PME

Interrupt

PHY_VDD33

GR127 for RTL8201EN INT function

CLK125/LED2_RXDLY — GR127 0 — INT → INT

GR106 4.7K

MDC/MDIO

PHY_VDD33

MDC/MDIO

VDD33_VDD25

GR125 NC/0

GR128 0

MDIO — GR38 1.5K

MDIO → MDIO
MDC → MDC

RTL8201FN/EN/8211CN/8211D: GR128(NC)
RTL8211E:GR125(NC)

Configuration Setting

MII/RMII Setting only for RTL8201FN & RTL8201EN PHYAD2
Setting only for RTL8211E

PHY_VDD33

RTL8201FN USE RMII mode

GR46 4.7K — RX_CTL_PHYAD2 — GR47 NC/4.7K

RTL8201FN/RTL8201EN: RMII Signals:
Pull High for RMII mode — REF_CLK - Pin 22
Pull Low for MII mode — CRS_DV - Pin 36
RXD[1:0] - Pin 16, 14
TX_EN - Pin 27
TXD[1:0] - Pin 24, 23
RX_ER - Pin 39

PHY_VDD33

VDD33

PHY_VDD33

GR54 NC/4.7K — MDI3- — GR59 NC/4.7K

RTL8201FN: Pull High for LDO Enable
Pull Low for LDO disable

PHY_VDD33

LED1_AD1
LED0_AD0

GR88 NC/4.7K LED2_RXDLY_ENREG
GR69 NC/4.7K LED2_RXDLY
GR71 4.7K LED1_AD1
GR73 NC/4.7K LED0_AD0
GR87 NC/4.7K
GR70 4.7K
GR72 NC/4.7K
GR74 4.7K

RTL8211D/E: If use 2.5V RGMII please pull down (GR123)RXD0/SELRGV
RTL8211CN/8201EN:GR123,GR124 NC

GR123 NC/4.7K RXD0/SELRGV
GR75 NC/4.7K RXD2/AN0
GR77 NC/4.7K RXD3/AN1
GR85 NC/4.7K RXD1/TXDLY
GR124 4.7K
GR76 4.7K
GR78 4.7K
GR86 4.7K

VDD33_VDD25 → VDD33_VDD25

GND

RTL8211CN/8211D/8211E:
GR76,GR78: Config for all capability
GR71,GR74: PHY Address=01 (8211D/8211CN)
GR46,GR71,R74: PHY Address=001 (8211E)
GR69,GR85: Without TX/RX Delay

RTL8201EN:
GR88:MII Interface
GR87:SNI Interface
GR71,GR74: PHY Address=01
Other resistors are NC

RTL8201FN:
R78 : REF_CLK Input
R77: REF_CLK Output
R69,R71,R74: PHY Address=001
Other resistors are NC

External clock and Crystal

External clock source from OSC or Chipset.

XTAL1 — X5 (GND XIN / XOUT GND) — XTAL2
GC1 27pF — 25M-10PPM CRY-TSX3225 — GC2 27pF

Use external clock:
RTL8201FN/RTL8201EN/8211CN/8211D/8211E: GR105(0 ohm)

Enable/Disable SWREG

PHY_AVDD33

ENSWREG — GR65 0R — GR66 NC/0R

Connect ENSWREG to PHY_AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.

RTL8201FN /EN:
GR65 is Fiber Mode
GR66 is UTP Mode(default)

PHY Reset

GR57 NC0R/VDD33_VDD25 → VDD33_VDD25
GR58 0R PHY_VDD33 → PHY_VDD33
GR55 4.7K
PHYRSTB — GR56 NC/0R PCIRST → MAC-RST
GC54 0.01uF

RTL8211CN: GR58 (NC)
RTL8211D/8211E: GR57 (NC)
RTL8201FN /EN: GR58(NC)

For wake on LAN function, please mount GR55 GC54 and remove GR56

RSET/ENSWREG/CLK125 Co-layout

ENREG/RSET — GR112 NC/0R — ENSWREG
GR113 0R — RSET
GR126 NC/4.7K

RTL8211D/E Pin39 is RSET (GR112,GR126 NC)
RTL8211CN Pin39 is ENSWREG (GR113,GR126 NC)
RTL8201FN/EN Pin39 is RXER (GR113 NC)

CLK125/LED2_RXDLY — GR114 NC/0R — CLK125 → CLK125
GC74 22pF
GR115 0R — LED2_RXDLY

RTL8211D/E / RTL8201FN Pin32 is LED2_RXDLY (GR114 NC)
RTL8211CN Pin32 is CLK125 (G R115 NC)
RTL8201EN Pin32 is interrupt(G R114,GR115 NC)

Reserve for EMI.

LED2_RXDLY_ENREG — GR118 0R — ENSWREG
GR119 NC/0R — LED2_RXDLY

RTL8211CN Pin38 is LED2_RXDLY (GR118 NC)
RTL8211D/E Pin38 is ENSWREG (GR119 NC)
RTL8201FN/EN Pin 38 is Collision Pin(GR118 & GR119 NC)

RSET/CLK125 — GR116 0R — CLK125 → CLK125
GC73 22pF
GR117 NC/0R — RSET

RTL8211D/E Pin46 is CLK125 (GR117 NC)
RTL8211CN Pin46 is RSET (GR116 NC)
RTL8201FN/EN Pin46 is RSET(GR116 NC)

Reserve for EMI.

RTL8211CN / RTL8211D/E / RTL8201EN/FN

PHY_AVDD33
PHY_VDD33
PHY_VDD10

RTL8211D/E:GC45(NC)
RTL8211CN:GC45(NC)

GC45 1uF

AVDD33_CEN — GR83 0
GC47 1uF
GR83 Close to Pin41

U17

RTL8201EN:GR79(NC)
RTL8201FN: GR79,GR84(NC)
RTL8211CN/8211D/8211E:GR84(NC)

GR79 0 (NC)
GR84 4.7K

PGND REGOUT GND RSET/CLK125 VDDREG CKXTAL2 CKXTAL1 AVDD33-1 AVDD10-1 ENREGRSET DVDD33-1
REGOUT RSET/CLK125 VDDREG VDDREG XTAL2 XTAL1 AVDD33_CEN PHY_AVDD10 ENREGRSET LED2_RXDLY ENREG

MDI0+ 1 — MDI[0]+
MDI0- 2 — MDI[0]-
PHY_AVDD10 3 — AVDD10
MDI1+ 4 — MDI[1]+
MDI1- 5 — MDI[1]-
PHY_AVDD33 6 — AVDD33
MDI2+ 7 — MDI[2]+
MDI2- 8 — MDI[2]-
PHY_AVDD10 9 — AVDD10-0
MDI3+ 10 — MDI[3]+
MDI3- 11 — MDI[3]-
TXER 12 — NC

RTL8211CN
RTL8211D/E
RTL8201EN/FN

DVDD10-0 36 — PHY_VDD10_CRS
LED1/PHYAD1 35 — LED1_AD1
LED0/PHYAD0 34 — LED0_AD0
PME 33 — PME
CLK125/LED2_RXDLY 32 — CLK125/LED2_RXDLY
MDIO 31 — MDIO
MDC 30 — MDC
PHYRSTB 29 — PHYRSTB
DVDD10 28 — PHY_VDD10
TXCTL 27 — TX_CTL
TXD3 26 — TXD3
TXD2 25 — TXD2

RXCTL/PHYAD2 RXD0/SELRGV DVDD33 RXD1/TXDLY RXD2/AN0 RXD3/AN1 RXC INT DVDD33-0 TXC TXD0 TXD1
RX_CTL_PHYAD2 13 — RXCTL/PHYAD2
RXD0/SELRGV 14 — RXD0/SELRGV
VDD33_VDD25 15 — DVDD33
RXD1/TXDLY 16 — RXD1/TXDLY
RXD2/AN0 17 — RXD2/AN0
RXD3/AN1 18 — RXD3/AN1
RX_CLK 19 — RXC
INT 20 — INT
VDD33_VDD25 21 — DVDD33-0
TX_CLK 22 — TXC
TXD0 23 — TXD0
TXD1 24 — TXD1

RGMII/RMII

11 MDI3- / 11 MDI3+ ↔ MDI3- / MDI3+
11 MDI2- / 11 MDI2+ ↔ MDI2- / MDI2+
11 MDI1- / 11 MDI1+ ↔ MDI1- / MDI1+
11 MDI0- / 11 MDI0+ ↔ MDI0- / MDI0+

R35,36,37 Only for RTL8201FN/EN

PHY_VDD10_CRS — GR35 0R — CRS_N → CRS_N
LED2_RXDLY_ENREG — GR36 NC/0R — COL_N → COL_N
ENSWREG — GR37 0R — RXER_N → RXER_N

Place filter network close to RX_CLK.
Reserved for EMI

RX_CLK — GR49 22R — RX_CLK_N
GC46 NC

RX_CTL_PHYAD2 — GR48 22R — RX_CTL_N
RXD0/SELRGV — GR50 22R — RXD0_N
RXD1/TXDLY — GR51 22R — RXD1_N
RXD2/AN0 — GR52 22R — RXD2_N
RXD3/AN1 — GR53 22R — RXD3_N

RX_CTL_N → RX_CTL_N
RX_CLK_N → RX_CLK_N
RXD0_N → RXD0_N
RXD1_N → RXD1_N
RXD2_N → RXD2_N
RXD3_N → RXD3_N
TX_CLK → TX_CLK
TX_CTL → TX_CTL
TXER → TXER
TXD0 → TXD0
TXD1 → TXD1
TXD2 → TXD2
TXD3 → TXD3

Close to PHY
Reserve for EMI

RSET

RSET — GR6 2.49K(1%)

Others

VDDREG
PHY_VDD10
PHY_AVDD10
REGOUT
PHY_VDD33

Pine A64

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