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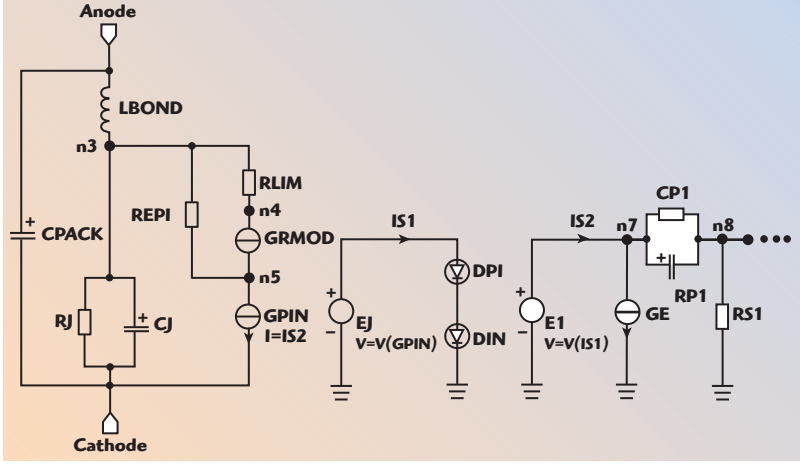
An Advanced PIN-diode Model

This article presents an advanced PIN-diode model, which is based on a model developed by R. Caverly.[1] This model includes the important I-region charge storage phenomenon, which affects the PIN-diode impedance-frequency characteristics and the current-dependent carrier lifetime. While the original model is more advanced than the simple resistance-only models used in many simulators, there are some practical issues that limit its usage. Specifically, the junction capacitance in the original model does not depend on bias or frequency and the operation under reverse bias is not as accurate in simulating the intermodulation products, for example. For the advanced PIN-diode model (PIN-DiodeRC), described here and implemented in APLAC, further improvements and changes have been made in order to create a PIN-diode model as accurate as possible. The enhancements include frequency and bias dependent junction capacitance, improved diode reverse bias operation and improved diode convergence. The model is validated by showing several simulation results, together with the corresponding measured data.

Fig. 1 Equivalent circuit describing the implemented PIN-diode model.



The equivalent circuit describing the model is shown in ***Figure 1***. The junction capacitance frequency dependence is based on an Application Note from Narda.[2] The bias dependent junction capacitance uses the same junction capacitance equations that are implemented in APLAC Diode.[3] While the first (Model Level = 1) PIN-DiodeRC model has several improvements over the original model, it still has a constant junction capacitance. However, the new model (Model Level = 2) introduces a more accurate junction capacitance as well as an improved model convergence.

TECHNICAL DETAILS

Considering the PIN-DiodeRC model, Level = 2, the modeling of the charge storage

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phenomenon is based on the ambipolar carrier transport equation[1]

$$\frac{\partial^2 n(x,t)}{dx^2} = \frac{n(x,t)}{D_a \tau} + \frac{1}{D_a}\frac{\partial n(x,t)}{dt} \quad (1)$$

According to Caverly,[1] from Equation 1, the current flowing through the diode is

$$I(s) = Q(s)\frac{L_a\sqrt{1+s\tau}}{x_m \tau}\tanh\left(\frac{x_m}{L_a}\sqrt{1+s\tau}\right) \quad (2)$$

Where the minimum of the I-region stored charge density, x_m, is given by[1]

$$x_m = \frac{W}{2}\left[1+\frac{2\lambda}{W}\tanh^{-1}\left(\frac{b-1}{b+1}\tanh\left(\frac{W}{2\lambda}\right)\right)\right] \quad (3)$$

In this model, the Padé approximation has been used to transform Equation 2 into a circuit netlist format.[1] This way, the RC network can be realized, resulting in the following values:

RP1 = 1
CP1 = TAU
RS1 = ALFA/3
RP2 = 5
CP2 = TAU/5
RS2 = ALFA/7
RP3 = 9
CP3 = TAU/9
RS3 = ALFA/11
RP4 = 13
CP4 = TAU/13
RS4 = ALFA/15
RP5 = 17
CP5 = TAU/17
RS5 = ALFA/19

where

TAU = model parameter (ambipolar carrier lifetime)
ALFA = TO/TAU
TO = W2/0.00048375
W = model parameter (I-region width)

The PIN-diode junction capacitance frequency dependency is implemented according to[2]

$$C_j = C_{pt}\frac{1+\left(\frac{f}{f_r}\right)^2}{\frac{C_{pt}}{C_d}+\left(\frac{f}{f_r}\right)^2} \quad (4)$$

where

C_{pt} = parameter CJ for the PIN-diode
f_r = dielectric relaxation frequency

$$f_r = \frac{1}{2\pi\rho\varepsilon_r\varepsilon_0} \quad (5)$$

where ρ = RHO and ε_r = EPS are model parameters. The ratio

$$\frac{C_{pt}}{C_d}$$

is equal to the ratio

$$\frac{W_d}{W}$$

where W_d is the diode depletion area width that is given as parameter WD for the model and W is the I-region width. The bias dependency in the junction capacitance is implemented according to[3]

$$C_j = \begin{cases} \dfrac{C_{j0}}{\left(1-\frac{V_d}{V_j}\right)^m}, \text{ when } V_d \le f_c V_j \\ \dfrac{C_{j0}}{(1-f_c)^m}\bullet\left[\dfrac{-m\left(1-\frac{V_d}{V_j}\right)^2}{2(1-f_c)^2}+1+\dfrac{m}{2}\right], \\ \text{when } (2-f_c)V_j > V_d > f_c V_j \\ \dfrac{C_{j0}}{(1-f_c)^m}\bullet e^{\frac{m}{1-f_c}\left(2-f_c-\frac{V_d}{V_j}\right)}, \\ \text{when } V_d \ge (2-f_c)V_j \end{cases} \quad (6)$$

where

C_{j0} = CJ
f_c = FC
M, V_j = VJ are model parameters

The value of the component CJ is the combination of frequency and bias dependent junction capacitances.

The component values for LBOND, CPACK, RP, REPI and RLIM are given to the model as parameters. LBOND and CPACK describe the package parasitics. RP is the junction parallel resistance, REPI is the zero bias resistance and RLIM is the minimum series resistance.

The values of the controlled sources are calculated as follows: the voltage EJ is equal to the voltage across the current source GPIN; voltage E1 is equal to the value of the current IS1.

$$\text{Current GE} = \frac{V(GE)^2}{\text{IKNEE}} \quad (7)$$

where V(GE) is the voltage across the current source GE and IKNEE is a model parameter (current dependent lifetime knee current). For improving the model convergence, V(GE) has been limited according to the function

$$V(GE)^2 \approx 0.25\left(V(GE)+\sqrt{V(GE)^2+4\varepsilon^2}\right)^2 \quad (8)$$

where ε is 10^{-12}. The current GPIN is equal to the current IS2.

$$\text{Current GRMOD} = \frac{2V(GRMOD)V(RP1)}{VM} \quad (9)$$

where V(GRMOD) is the voltage across the current source GRMOD, V(RP1) is the voltage across the resistor RP1 and

$$VM = \frac{10W^2}{TAU} \quad (10)$$

As V(RP1) accounts for a conductance, it should never be negative and thus has been limited according to the function

$$V(RP1) \approx 0.5\left(V(RP1)+\sqrt{V(RP1)^2+4\varepsilon^2}\right) \quad (11)$$

where ε is 10^{-12}. The diodes DPI and DIN are SPICE-compatible diodes, consisting of the parameters IS, IKF, N, BV, IBV and RS.

The emission coefficients η for the diodes are calculated by

$$\eta(DPI) = \frac{N}{1+B} \quad (12)$$

$$\eta(DIN) = \frac{B\bullet N}{1+B} \quad (13)$$

where B and N are model parameters.

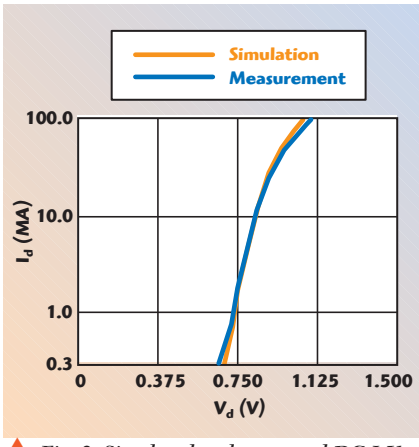

Fig. 2 Simulated and measured DC I-V curves.

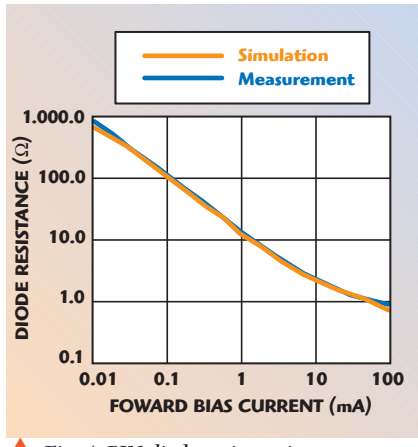

Fig. 4 PIN diode series resistance versus forward bias current at 100 MHz.

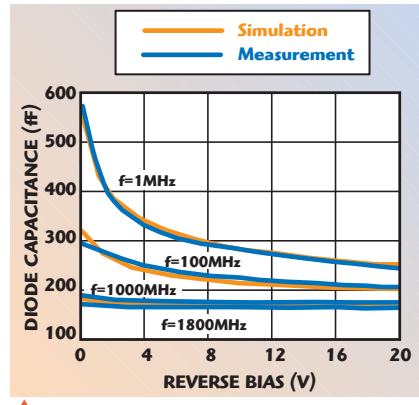

Fig. 6 Diode capacitance versus reverse bias voltage.

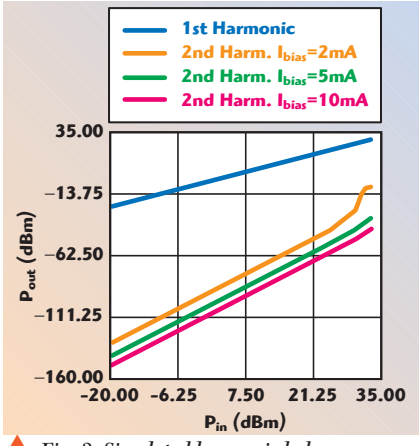

Fig. 3 Simulated harmonic balance power curves for different forward bias currents.

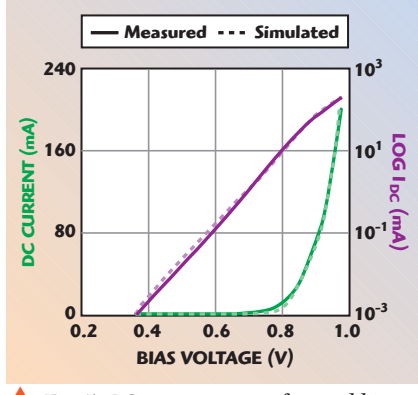

Fig. 5 DC current versus forward bias.

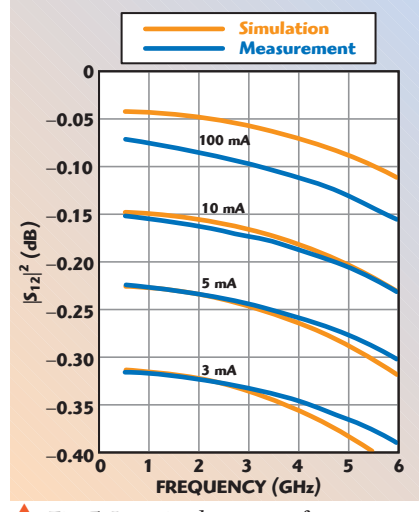

Fig. 7 Insertion loss versus frequency ($Z_O = 50\ \Omega$).

MODEL VERIFICATION

The model has been created in cooperation with a large semiconductor manufacturer in order to assure model suitability for industrial use. The implemented model has already been tested and used in the industry. Next, a series of validation simulations will be presented. APLAC RF Design Tool version 8.00 was used to simulate and analyze the circuit.

SIMULATION RESULTS

PIN-DiodeRC simulation results are compared to measured results (courtesy of STMicroelectronics). ***Figure 2*** shows the DC I-V curve used for parameter extraction, while ***Figure 3*** shows the harmonic balance (HB) power sweep. The agreement is very good between the simulations and measurements.

The next set of figures show the PIN-DiodeRC simulation results compared to the Infineon BAR64-02L PIN-diode data sheet after parameter extraction. ***Figure 4*** shows the PIN-diode resistance versus forward bias current, while ***Figure 5*** shows the PIN-diode linear and logarithmic IV-curves. These curves have been used to fit the DC parameters of the diode, and the agreement is very good. ***Figure 6*** shows the diode capacitance versus reverse bias voltage at four different frequencies. The bias and frequency dependency can be seen clearly here. In particular, the frequency dependence is a feature that most PIN-diode models lack. ***Figure 7*** shows the insertion loss over frequency at four different forward bias current values. The agreement is good except for the highest bias current, which is due to the fact that the modeled PIN-diode resistance is more inaccurate at high currents.

The model parameters for this component are:

MODEL_LEVEL = 2
IS = 5.7125729E-010
N = 1.8454024E+000
B = 1.0837905E+000
IKF = 1.0553000E-002
IBV = 1.0298667E-009
BV = 7.4925428E+001
RP = 3.0116584E+007
RS = 7.6197640E-002
W = 5.0000000E-005
WD = 0.1000000E-006
REPI = 1.8895941E+003
RLIM = 2.0690918E-003
TAU = 2.2424389E-006
IKNEE = 1.8830056E-003
EPS = 1.1700000E+001
RHO = 7.1660057E-001
CJ = 7.8064905E-016
VJ = 7.6935733E-001
M = 4.6710106E-001
FC = 4.4097700E-001
CPACK = 1.6282420E-013
LBOND = 3.0393336E-010

CONCLUSION

Developed from a model introduced by R. Caverly, a more complex and accurate PIN-diode model has been created and validated. Significant enhancements include frequency and bias dependent junction capacitance, along with improvements

in the diode reverse bias operation and the diode convergence. ■

References

1. R.H. Caverly, N.V. Drozdovski, L.M. Drozdovskaia and M.J. Quinn, "Spice Modeling of Microwave and RF Control Diodes," *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, August 8–11, 2000.
2. Application Note for PIN-diodes, Narda Microwave-East.
3. APLAC RF Design Tool 8.00 Reference Manual, Vol. II, Analog Components, APLAC Solutions Corp., October 2004.

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