DESIGN OF SIMPLE DC VOLTAGE STABILIZER

A PROJECT REPORT SUBMITTED IN THE PARTIAL FULFILLMENT OF ELECTRONICS DESIGN LAB PROJECT AT NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA

By:

Electronics and Design Lab., Group-1

Kirtidipan Behera (110EC0159)

Debashish Shanti (110EC0182)

Subhajit Sahu (110EC0181)

Under the Supervision of:

Prof. S. K. Das

Professor-in-charge of Electronics Design Lab

Department of Electronics and Communication,

National Institute of Technology, Rourkela

ACKNOWLEDGEMENT

This project is an original work carried out by the team members. It could have never been possible to complete this without the endless support of Prof. S. K. Das, our Professor-in-charge of the Electronics and Design Lab, as well as our Faculty Advisor. We would also like to thank all our friends for their support in the implementation of the circuit, demonstrated in this project.

Electronics and Design Lab., Group-1

Kirtidipan Behera (110EC0159)

Debashish Shanti (110EC0182)

Subhajit Sahu (110EC0181)

ABSTRACT

A DC Voltage Stabilizer is an electrical / electronic device which provides a constant voltage output even when the input voltage supply is variable. Hence, in a sense, the device “stabilizes” the input power supply to provide a constant voltage output, which is sometimes, a critical requirement in certain cases. Ex- DC rectified voltage obtained from the AC Supply, often contains 50 Hz frequency component which may affect the communication between two electronic devices. Ex- Power supply noise in digital circuits could increase the clock jitter leading to increased error rate in digital systems, especially high-speed communication systems (ex- PCI Express applications).

CIRCUIT DIAGRAM

The DC Voltage Stabilizer {1} designed in this project is a simple and easy-to-implement electronic device. It is fed by a power supply which can be variable, and here it has been assumed that a DC voltage source connected in series with an AC voltage would demonstrate similar effects. The Load is assumed to be simple resistor for simplicity.

A reference battery connected to the device (voltage stabilizer) determines the output voltage. However, only a very small current (in nano-ampere range) is taken from the battery. The voltage stabilizer takes current from the power supply, stabilizes it with respect to the battery, and then supplies it to the load.

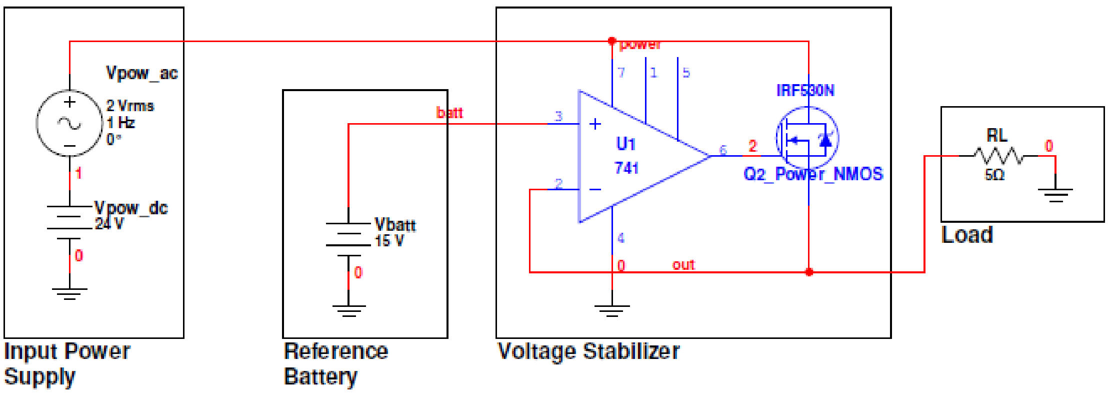

Fig. 1 – Circuit Diagram of the DC Voltage Stabilizer designed in this project *(simulated in MultiSim)*

COMPONENTS USED

- OpAmp IC 741.
- Power NMOS IRF530N.

OTHER REQUISITES

- Variable Power Supply.
- Reference Battery.
- Load.

SIMULATION

Simulation of the circuit was carried out in MultiSim. The DC value of power supply was set to 24V {1}, and the AC value was set to 2V RMS. Then the following two simulations were carried out:

(i) Transient Analysis {2}, with voltage of reference battery set to 15V. Both, input power supply and the output voltage were monitored.

(ii) DC Sweep Analysis {3}, with voltage of reference battery being changed from 0V to 24V. Output voltage was monitored.

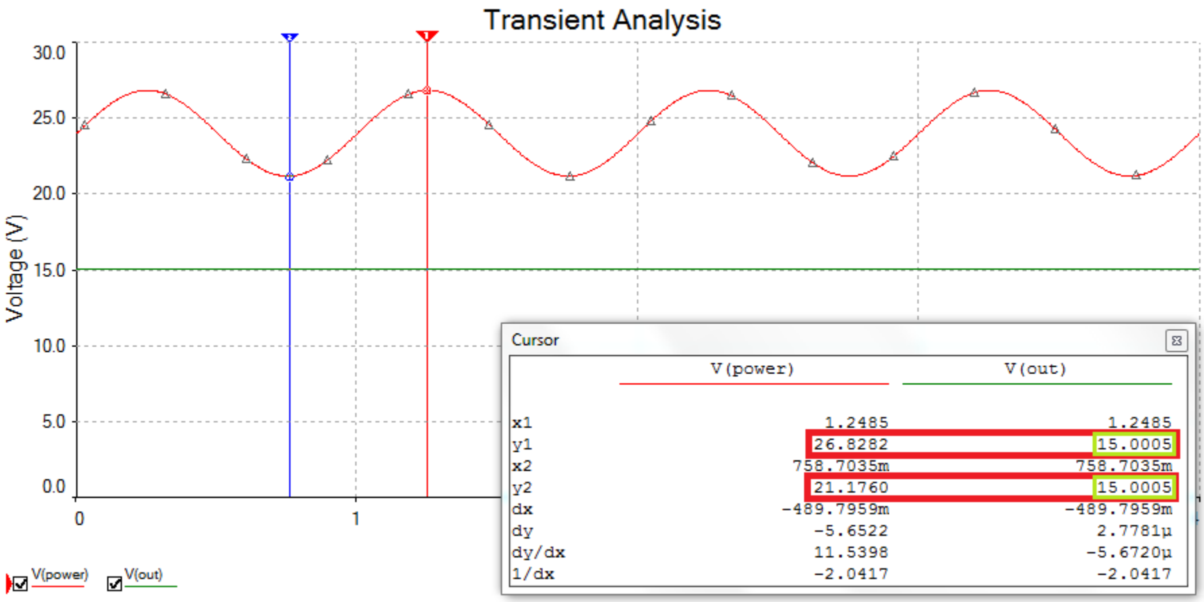

Fig. 2 – Transient Analysis of the DC Voltage Stabilizer; power supply has 24V DC component and 2V RMS AC component. The voltage of Reference battery is set to 15V.

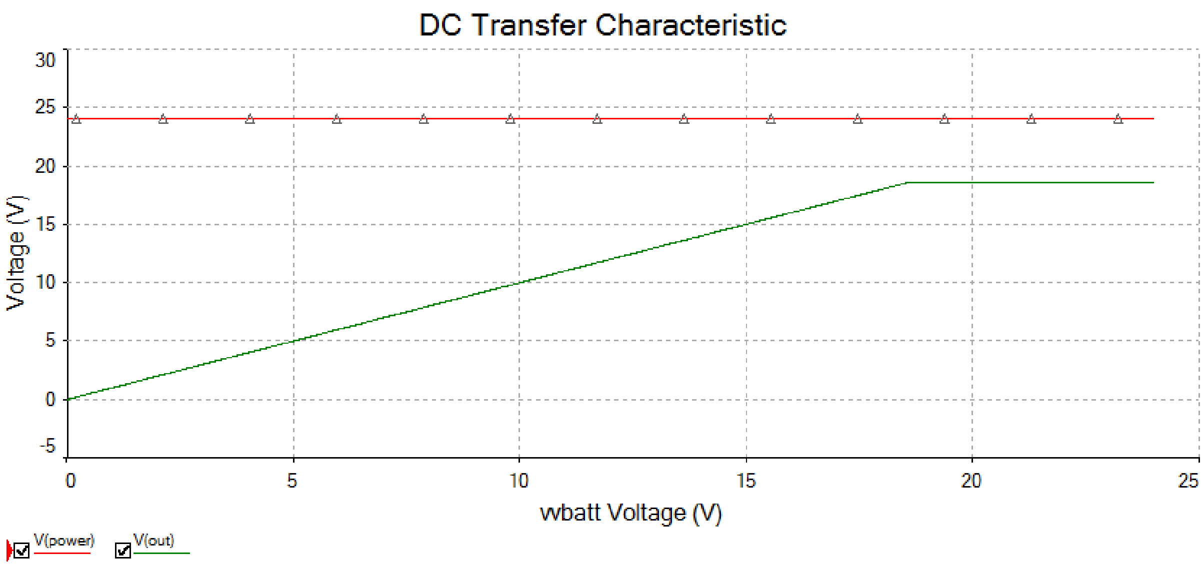

Fig. 2 – DC Sweep Analysis of the DC Voltage Stabilizer; power supply has 24V DC component and 2V RMS AC component. The voltage of Reference battery is changed from 0V to 24V.

WORKING

The working of the DC voltage stabilizer described here can be understood when the Operational Amplifier in {1} is not assumed to be ideal, so that it has a definite slew rate. It is also assumed that the OpAmp can be used with variable supply voltage, and works normally (i.e. the supply voltage is within its working range).

The OpAmp in {1}, which works as a comparator, compares the voltage at the output with the voltage of the reference battery. The output terminal of the OpAmp is connected to the gate terminal of a power NMOS, which is used as a current valve to control the flow of current through it, and thus through the load. Since the current flowing through the load can be controlled, hence the voltage is controlled since voltage is proportional to current. However, the voltage at the output is constant since the comparator uses voltage for comparison.

Initially, when the circuit is powered, the output voltage of the circuit is still 0V. Since the output voltage (connected to "-" terminal of OpAmp) is less than the reference battery voltage the comparator starts to increase its output voltage (which can at max. be the power supply voltage to the OpAmp,; this slow increase in output voltage of the OpAmp is due to its finite slew rate), which in turn partially switches "on" the power NMOS (whose gate is connected to the output of the OpAmp). This happens as long as the output voltage of the circuit is less than the reference voltage.

Once, the output voltage crosses (increases beyond) the reference voltage, the output of the OpAmp slowly falls down (which is again due to its finite slew rate) until the output voltage is just slightly below the reference voltage. Once again the OpAmp increases the output voltage. In fact, due to a finite slew rate, the OpAmp maintains a finite output voltage at its output terminal which turns “on” the power NMOS sufficiently so that the output voltage of the DC voltage stabilizer matches that to the reference battery voltage).

The comparator works well even with a varying power supply voltage only because the voltage of the reference battery is fixed and hence comparing with it produces a stable output similar to the reference. Had the reference battery been replaced with a potential divider, the output of the device would no more be stable since the voltage output of the potential divider would be varying because of the voltage varying power supply.

It is shown in {4} how the device starts initially.

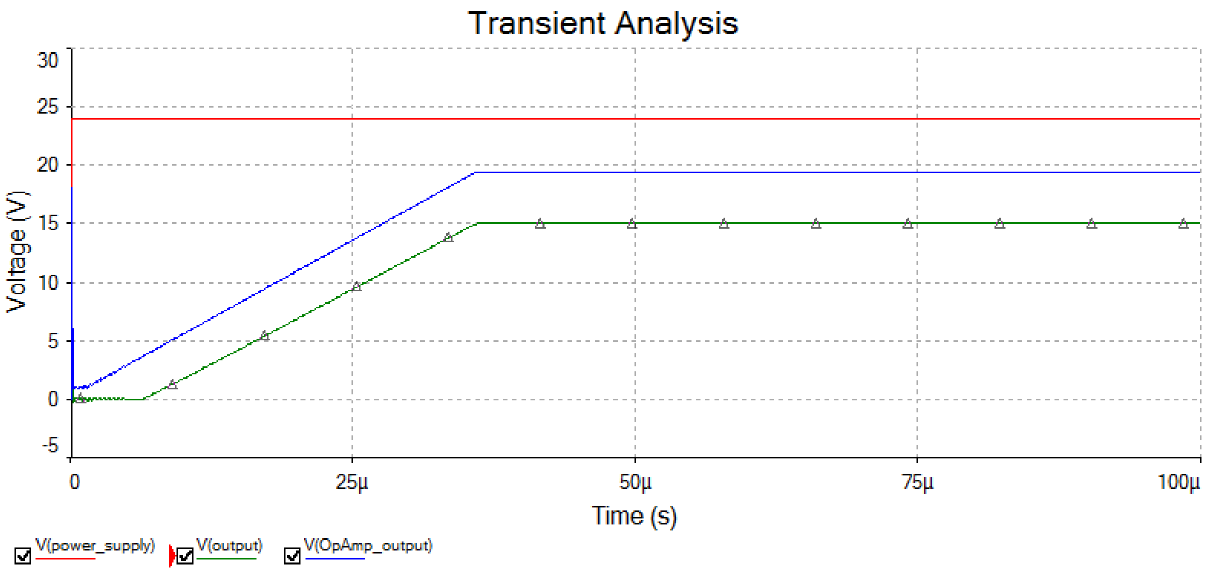

Fig. 4 – Initial starting time of the DC voltage stabilizer

CONCLUSION

The circuit designed in this project demonstrates a simple and easy to implement circuit for voltage stabilization. However, it lacks a lot of features than the voltage stabilizers available today. Modern voltage stabilizers are very efficient, allow a very large load current, and can also boost the output voltage to the required value, even if the supply voltage is less. However, designing such circuits require a sufficient knowledge, technical people working together, and of course, a lot of experience. What we have done is this project is just like a seat belt to an aeroplane. However, it was a great learning experience to be able to build a DC voltage stabilizer of our own.