Schematic Checklist for PCB built for CC3135 device

Below checklist is for VBAT power supply (2.1V to 3.6V)

Domain	Items	Pin Associated	Recommended Connection	BOM Description	Recommended parts
Slow Clock	Oscillator (Optional)	51 and 52	1. The 'Out' pin of the oscillator should be connected to 'Pin 51' of the device, 'RTC_XTAL_P' 2. The 'Supply' pin of the oscillator should be connected to VBAT (same as device supply) 3. 'Pin 52' of the device, 'RTC_XTAL_N' should be pulled high through 100K resistor 4. The clock has to be CMOS logic level	1. Frequency 32.768KHz 2. Frequency stability across -40C and 85C	Micro Crystal AG : OV-7604-C7
	XTAL		1. XTAL should be connected across 'Pin 51' and 'Pin 52' 2. Provide load capacitors (10pF) at both the pins of the XTAL. This is based on TI board layout. 3. Tuning of the load capacitance may be needed based on customer board layout.	1. Frequency 32.768KHz, ESR < 150K Ohm, load capacitance < 20pF	ABS07-32.768KHZ-T
Fast Clock	XTAL	22 and 23	1. XTAL should be connected across 'Pin 22' and 'Pin 23' 2. Provide load capacitors (6.2pF) at both the pins of the XTAL. This is based on TI board layout. 3. Tuning of the load capacitance may be needed based on customer board layout.	1. Frequency 40MHz, ESR < 60 Ohms, Load cap < 12pF	Epson : Q24FA20H00396 TXC : 8Z40000055 or 8Y40072002
RF 2.4GHz	Filter	31	1. 2.4G filter should be connected at Pin #31. The filter part number should match exactly with TI recommendation or meet the specs from the datasheet.	Refer datasheet for attenuation requirements	DEA202450BT-1294C1-H (EPCOS/TDK)
RF 2.4GHz	Antenna & Matching	31	An antnena is required for the RF signal to radiate. Any 50 Ohms antenna with the bandwidth extending from 2.4 to 2.5 GHz could be used with the device. Provide matching network option for the antenna as shown in the picture.	Antenna impedance : 50 Ohms VSWR : 1:2 Bandwidth : 2.4GHz - 2.5GHz Pattern : Omini-directional Peak gain : 2dBi	2. Recommended antenna:M830520 (Ethertronics) 3. Recommended antenna matching network for the AH316M antenna: Series cap (2.2 pF): GRM1555C1H2R2BA01D Shunt Inductor (3.9 nH): LQG15HS3N9S02D **Note:** These component values will vary when implementing on a customer board. Please perform Antenna matching to ensure optimal performance.
RF - 5 GHz	Switch	27 and 28	A switch is required for the 5 GHz TX and RX signals to radiate. The switch part number should match exactly with TI Recommendation or meet specs from the datasheet	Refer to datasheet for switch specifications	Recommended switch: RTC6608OSP

RF - 5 GHz	Switch	34 and 35	The SOP0 And SOP1 Pins also are used to control the switch in the 5 GHz path. Please Connect SOP0 to the first switch control pin (VC1) and SOP1 to the second (VC2). 100pF capacitors should be added to reduce noise.	De-coupling Capacitor = 100 pF	Recommended Cap = GRM31CR60J107ME39L
RF- 5 GHz	Filter	27 and 28	After the switch, a 5 GHz filter is needed. The filter part number should match exactly with TI Recommendations or meet specs from the datasheet	Refer to datasheet for filter specifications	Recommended Filter: DEA165538BT-2236B1-H
RF - 5 GHz	Antenna & Matching	27 and 28	An antenna is required for the RF signal to radiate. You will need to use a 50 Ohms antenna with the bandwidth extending from 4.9 GHz to 5.95 GHz. Provide matching network option for the antenna as referenced on the CC3235x-LAUNCHXL	Antenna impedance : 50 Ohms VSWR : 1:2 Bandwidth : 4.9GHz - 5.95GHz Pattern : Omini-directional Peak gain : 2dBi	Recommended Antenna: M830520 (Ethertronics)
RF - 2.4 GHz and 5 GHz (OPTIONAL)	Antenna & Matching	27,28,31	Another option is to use the same antenna for both 5 GHz and 2.4 GHz. An antenna is required for the RF signal to radiate. Also, a Diplexer is required for proper isolation between RF signals. Any 50 Ohms antenna supporting Dual Band bandwidth extending from 2.4-2.5 GHz and 4.9- 5.95GHz could be used with the device. Provide matching network option for the antenna.	Antenna impedance : 50 Ohms VSWR : 1:2 Bandwidth : 2.4GHz - 2.5GHz and 4.9 GHz to 5.95 GHz Pattern : Omini-directional Peak gain : 2dBi	Recommended Antenna:M830520 (Ethertronics) Recommended Diplexer: DPX165950DT-8148A1
Power	ANA DCDC IN	37	1. Should be connected to VBAT 2. Provide de-coupling capacitor (4.7uF)	De-coupling capacitor = 4.7uF, 6.3V	Recommended PN: CL05A475MQ5NRNC
	PA DCDC IN	39	1. Should be connected to VBAT 2. Provide de-coupling capacitor (4.7uF) 3. Provide de-coupling capacitor (.6 pF)	De-coupling capacitor = 4.7uF, 6.3V De-coupling capacitor = .6pF	Recommended PN (4.7uF): CL05A475MQ5NRNC Recommended PN (.6pF): GJM0335C1ER60BB01D Place the .6 pF cap as close to the pin as possible. Please see our Layout Design Guide for more information.
	DIG DCDC IN	44	1. Should be connected to VBAT 2. Provide de-coupling capacitor (4.7uF) 3. Provide de-coupling capacitor (.5 pF)	De-coupling capacitor = 4.7uF, 6.3V De-coupling capacitor = .5pF	Recommended PN (4.7uF): CL05A475MQ5NRNC Recommended PN (.5pF): GJM0335C1ER50BB01D Place the .5 pF cap as close to the pin as possible. Please see our Layout Design Guide for more information.
	VIO	54 and 10	1. Should be connected to VBAT 2. Provide de-coupling capacitor (0.1uF)	De-coupling capacitor = 0.1uF, 10V	Recommended PN: LMK105BJ104KV-F
	VDD_PLL	24	1. Add de-coupling capacitor (0.1uF)	De-coupling capacitor = 0.1uF, 10V	
	VDD_RAM	49	1. Add de-coupling capacitor (0.1uF)	De-coupling capacitor = 0.1uF, 10V	
	VDD_FLASH	47	**Leave this pin un-connected. There is no harm if connected to VBAT or 3.3V.**	Optional 0.1uF decap	
	VDD_DIG	9, 43 and 56	1. Provide 2.2uH inductor at DIG DCDC Out (Pin 43) 2. DIG DCDC output should be connected to VDD DIG (Pin 9 and Pin 56). 3. Provide de-coupling capacitors (0.1uF) to both VDD DIG pins (Pin 9 and Pin 56).	1. De-coupling capacitor = 10uF, 6.3V 2. De-coupling capacitor = 0.1uF, 10V 3. Inductor 2.2uH, DCR < 0.3 Ohm, Isat > 0.8A, Tol : 20R%	Recommended PN: GRM188R60J106ME47D Recommended PN: LMK105BJ104KV-FRecommended PN for 2.2uH inductor: LQM2HPN2R2MG0L (Lower ESR and Higher Current Rating)

	VDD_PA	33, 40, 41 and 42	1. DCDC_PA_SW_P (Pin 40) and DCDC_PA_SW_N (Pin 41) should be connected through 1uH inductor 2. PA DCDC Out (Pin 42) should be connected to VDD_PA_IN (Pin 33). 3. Provide de-coupling capacitor (22uF and 1uF) as shown in picture	1. De-coupling capacitor = 22uF, 4V min 2. De-coupling capacitor = 1uF, 10V 3. Inductor 1uH, DCR < 0.1 Ohm, Isat > 1.5A, Tol < 20%	Recommended PN for 22uF: AMK107BBJ226MAHT Recommended PN for 1uF: GRM155R61A105ME15D Recommended PN for 1uH inductor: LQM2HPN1R0MJ0L (Lower ESR and Higher Current Rating)
	VDD_ANA	25, 36, 38 and 48	1. ANA DCDC Out (Pin 38) should be provided with 2.2uH inductor in series. 2. ANA DCDC Out (Pin 38) should be connected to VDD_ANA (Pin 48), LDO IN1 (Pin 36) and LDO IN2 (Pin 25). 3. Provide de-coupling capacitors, 0.1uF to VDD_ANA (Pin 48), LDO IN1 (Pin 36) 4. Provide de-coupling capacitors .2 pF on LDO_IN2(Pin 25) and .6pF on LDO_IN1(Pin 36) 4. Provide a 10uF capacitor to LDO IN1 (Pin 36)	1. De-coupling capacitor = 10uF, 6.3V 2. De-coupling capacitor = 0.1uF, 10V 3. De-coupling capacitor = .2pF 4. de-coupling capacitor = .6pF 5. Inductor 2.2uH, DCR < 0.3 Ohm, Isat > 0.8A, Tol : 20R%	Recommended PN: GRM188R60J106ME47D Recommended PN: LMK105BJ104KV-F Recommended PN (.2pF): GJM0335C1ER20BB01D Recommended PN (.6pF): GJM0335C1ER60BB01D 3. Recommended PN for 2.2uH inductor: LQM2HPN2R2MG0L (Lower ESR and Higher Current Rating)
Digital	Flash_SPI	11, 12, 13 and 14	1. Please connect CS# (Flash) to device 'Pin 14', DOUT (Flash) to DIN (Dev Pin 13), DIN (Flash) to DOUT (Dev Pin 12) and Clock (Flash) to CLK (Dev Pin 11) 2. Provide 0.1uF de-coupling capacitor for the supply of the flash 3. 8Mbit part is recommended	Size >= 16Mbit Operating voltage : 2.3V to 3.6V	Use only the recommended PN: ISSI IS25LQ016B or Macronix MX25R1635F. Macronix part works at a wider voltage from 1.65V to 3.6V and consumes lower current in hibernate.
	Reset	32	1. Reset circuitry should be connected to 'Pin 32' of the device 2. Add RC circuit for the Power On Reset (R=100K and C=1uF)	R=10K and C=10uF R=100K and C=1uF	
	Reserved for Antenna Selection for future version	29 and 30	NC		
	Reserved	16, 17, 19 and 20	Add 100K pull-down on pin 19. Leave the rest un-connected	100K	
	SOP	21, 34 and 35	1. 100K pull down resistor to GND should be provided to pins 21, 34 and 35 2. Please place a .6 pF cap close to the pin.	Resistors and 100K Cap: .6pF	recommended PN (.6pF): GJM0335C1ER60BB01D
	UART	50, 55, 57 and 61	1. Pin 55 should be TX (Device). Add 100K pull up to VBAT. Add external test points 2. Pin 57 should be RX (Device). Add 100K pull up to VBAT to allow lowest current in hibernate. Add external test points Pin 55 and 57 are needed for flashing the firmware for development devices and must for production upgrade of ROM units: a. Security certificates b. Web Pages c. ROM Patches d. RF Testing e. Configuration files (AP SSID / etc.) 3. Pin 50 should be RTS (Device): Add external test points. Add 100K pull down. If this pin is used as a UART host interface there must be a pull down. If this pin is not used at all there must be no pull down on this pin to avoid elevated leakage current in LPDS mode. 4. Pin 61 should be CTS (Device): Add external test points	Resistor 100K Test points	
	Debug Pins	58, 59, 60 and 62	1. Pin 58 and pin 59: Add external test points 2. Pin 60: Add external test points 3. Pin 62: Add external test points Pin 60 and 62 are for logging.	Test points	

	nHIB	2	1. nHIB has to be connected to the HOST (MCU) for implementing hibernate function. 2. Ensure that the line does not float at any time, even when the MCU enters sleep state. Add external pull-up/down if required by the MCU to keet the IO state retained in sleep mode.	Resistor 10K	
	Host_SPI	5, 6, 7, 8 and 15	1. Device pin 8 should be CS# 2. Device pin 5 should be Clock 3. Device pin 6 should be DIN (device side) 4. Device pin 7 should be DOUT (device side) 5. Add 100K pull down resistor to SPI_DOUT (pin #7) 6. Add 10K pull down resistor to HOSTINTR (pin #15) and connect to HOST (MCU)	Resistor 100K	
	Others	1	Add option to pull down (100K). Leave DNP by default.	Resistor 100K	
		18, 26, 27, 28, 45, 46, 53, 63 and 64	NC		
		3,4	Add option to pull down (100K).	These are optional pull-downs. No issues if these lines are left floating.	
Ground	GND PAD	65	Electrical and thermal connection. Must be connected to GND		
Production Line Requirements			1. The following pins should be brought out to test points for flash programming. **Pin # Description** Pin 57 UART RX Pin 55 UART TX Pin 32 nRESET 2. Ensure that while programming, the RX (pin #57) and TX (pin #55) are NOT driven by any other circuit. Note that the nHIB pin should be pulled high for the flash programming. Both nHIB and nRESET can be used for the programming. If one is used, the other should be pulled to Vcc.		
Direct flash access			The following pins need to be brought on to a header,connector or Test point to be able to access the serial flash for In-circuit programming Pin# 11, 12, 13, 14 (Flash SPI lines) Pin# 32 (nRESET) Vcc, GND Ensure that the programmer can hold the CC3135 device in RESET mode while accessing the s-flash. nHIB pin should be held high during the entire programming phase.		

Power Budget for CC3120 and CC3220	
a	Board shall be designed to source 450mA for 24 msec for 3.3V
b	Board shall be designed to source 670mA for 24 msec for 2.2v
c	Board shall be designed to source 700mA for 24 msec for 1.85v
d	The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.

Special consideration during Hiobernate and RESET	
a	All the I/O pins will float while in Reset state. Please ensure pull-ups/pull-downs are available on board to maintain the state of the I/O if required by the system.