

# DRV8836 Dual Low-Voltage H-Bridge IC

## 1 Features

- Dual-H-Bridge Motor Driver
  - Capable of Driving Two DC Motors or One Stepper Motor
  - Low MOSFET On-Resistance: HS + LS 305 mΩ
- 1.5-A Maximum Drive Current Per H-Bridge
- Configure Bridges Parallel for 3-A Drive Current
- 2-V to 7-V Operating Supply Voltage
- Flexible PWM or PHASE/ENABLE Interface
- Low-Power Sleep Mode With 95-nA Maximum Supply Current
- Dedicated nSLEEP Input Pin
- Tiny 2.00-mm × 3.00-mm WSON Package

## 2 Applications

- Battery-Powered:
  - DSLR Lenses
  - Consumer Products
  - Toys
  - Robotics
  - Cameras
  - Medical Devices

## 3 Description

The DRV8836 provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device has two H-bridge drivers, and can drive two DC motors or one stepper motor, as well as other devices like solenoids. The output driver block for each consists of N-channel power MOSFET configured as an H-bridge to drive the motor winding. An internal charge pump generates gate drive voltages.

The DRV8836 supplies up to 1.5-A of output current per H-bridge. It operates on a power supply voltage from 2 V to 7 V.

PHASE/ENABLE and IN/IN interfaces can be selected which are compatible with industry-standard devices. A low-power sleep mode is provided which turns off all unnecessary logic to provide a very low current state.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

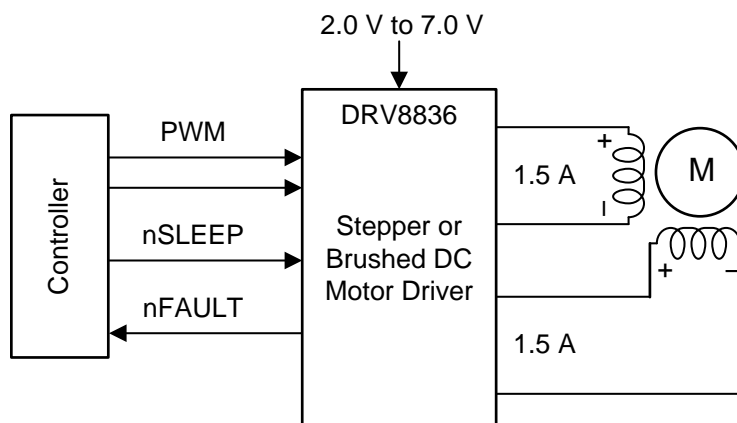
The DRV8836 is packaged in a tiny 12-pin WSON package (Eco-friendly: RoHS and no Sb/Br).

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)   |
|-------------|-----------|-------------------|
| DRV8836     | WSON (12) | 2.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Simplified Schematic



## Table of Contents

|  |          |  |           |
|--|----------|--|-----------|
| <b>1 Features</b> .....                        | <b>1</b> | 7.4 Device Functional Modes.....                                 | <b>9</b>  |
| <b>2 Applications</b> .....                    | <b>1</b> | <b>8 Application and Implementation</b> .....                    | <b>11</b> |
| <b>3 Description</b> .....                     | <b>1</b> | 8.1 Application Information.....                                 | <b>11</b> |
| <b>4 Revision History</b> .....                | <b>2</b> | 8.2 Typical Application .....                                    | <b>11</b> |
| <b>5 Pin Configuration and Functions</b> ..... | <b>3</b> | <b>9 Power Supply Recommendations</b> .....                      | <b>13</b> |
| <b>6 Specifications</b> .....                  | <b>4</b> | 9.1 Bulk Capacitance .....                                       | <b>13</b> |
| 6.1 Absolute Maximum Ratings .....             | <b>4</b> | <b>10 Layout</b> .....   | <b>13</b> |
| 6.2 ESD Ratings.....                           | <b>4</b> | 10.1 Layout Guidelines .....                                     | <b>13</b> |
| 6.3 Recommended Operating Conditions.....      | <b>4</b> | 10.2 Layout Example .....  | <b>14</b> |
| 6.4 Thermal Information .....                  | <b>4</b> | 10.3 Thermal Considerations .....                                | <b>14</b> |
| 6.5 Electrical Characteristics.....            | <b>5</b> | <b>11 Device and Documentation Support</b> .....                 | <b>16</b> |
| 6.6 Timing Requirements .....                  | <b>6</b> | 11.1 Community Resources.....                                    | <b>16</b> |
| 6.7 Typical Characteristics .....              | <b>7</b> | 11.2 Trademarks .....  | <b>16</b> |
| <b>7 Detailed Description</b> .....            | <b>8</b> | 11.3 Electrostatic Discharge Caution.....                        | <b>16</b> |
| 7.1 Overview .....                             | <b>8</b> | 11.4 Glossary .....  | <b>16</b> |
| 7.2 Functional Block Diagram .....             | <b>8</b> | <b>12 Mechanical, Packaging, and Orderable Information</b> ..... | <b>16</b> |
| 7.3 Feature Description.....                   | <b>9</b> |  |           |

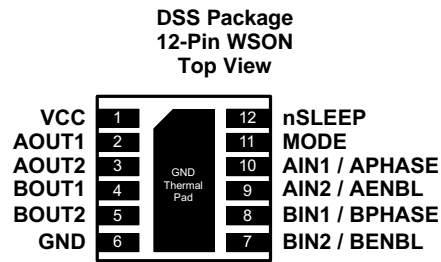
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (January 2014) to Revision C  | Page     |
|---|----------|
| <ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul> | <b>1</b> |

| Changes from Revision A (September 2013) to Revision B   | Page     |
|--|----------|
| <ul style="list-style-type: none"> <li>Added <math>t_{OCR}</math> and <math>t_{DEAD}</math> parameters to <i>Electrical Characteristics</i> .....</li> </ul> | <b>5</b> |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN              |     | I/O <sup>(1)</sup> | DESCRIPTION                   | EXTERNAL COMPONENTS OR CONNECTIONS  |
|------------------|-----|--------------------|-------------------------------|---|
| NAME             | NO. |                    |                               |   |
| POWER AND GROUND |     |                    |                               |   |
| GND, Thermal pad | 6   | —                  | Device ground                 |   |
| VCC              | 1   | —                  | Device and motor supply       | Bypass to GND with a 0.1-μF (minimum) ceramic capacitor   |
| CONTROL          |     |                    |                               |   |
| AIN1/APHASE      | 10  | I                  | Bridge A input 1/PHASE input  | IN/IN mode: Logic high sets AOUT1 high<br>PH/EN mode: Sets direction of H-bridge A<br>Internal pulldown resistor  |
| AIN2/AENBL       | 9   | I                  | Bridge A input 2/ENABLE input | IN/IN mode: Logic high sets AOUT2 high<br>PH/EN mode: Logic high enables H-bridge A<br>Internal pulldown resistor |
| BIN1/BPHASE      | 8   | I                  | Bridge B input 1/PHASE input  | IN/IN mode: Logic high sets BOUT1 high<br>PH/EN mode: Sets direction of H-bridge B<br>Internal pulldown resistor  |
| BIN2/BENBL       | 7   | I                  | Bridge B input 2/ENABLE input | IN/IN mode: Logic high sets BOUT2 high<br>PH/EN mode: Logic high enables H-bridge B<br>Internal pulldown resistor |
| MODE             | 11  | I                  | Input mode select             | Logic low selects IN/IN mode<br>Logic high selects PH/EN mode<br>Internal pulldown resistor                       |
| nSLEEP           | 12  | I                  | Sleep input                   | Active low places part in low-power sleep state<br>Internal pulldown resistor                                     |
| OUTPUT           |     |                    |                               |   |
| AOUT1            | 2   | O                  | Bridge A output 1             | Connect to motor winding A  |
| AOUT2            | 3   | O                  | Bridge A output 2             |   |
| BOUT1            | 4   | O                  | Bridge B output 1             | Connect to motor winding B  |
| BOUT2            | 5   | O                  | Bridge B output 2             |   |

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

|   | MIN                | MAX       | UNIT |
|---|--------------------|-----------|------|
| Power supply voltage, VCC   | −0.3               | 7         | V    |
| Digital input pin voltage   | −0.5               | VCC + 0.5 | V    |
| Peak motor drive output current                                   | Internally limited |           | A    |
| Continuous motor drive output current per H-bridge <sup>(3)</sup> | −1.5               | 1.5       | A    |
| T <sub>J</sub> Operating junction temperature                     | −40                | 150       | °C   |
| T <sub>stg</sub> Storage temperature                              | −60                | 150       | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values pertain to network ground terminal.
- (3) Power dissipation and thermal limits must be observed.

### 6.2 ESD Ratings

|  | VALUE  | UNIT  |
|--|--|-------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|  | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

T<sub>A</sub> = 25°C (unless otherwise noted)

|   | MIN | MAX             | UNIT |
|---|-----|-----------------|------|
| V <sub>CC</sub> Device power supply voltage             | 2   | 7               | V    |
| V <sub>IN</sub> Logic level input voltage               | 0   | V <sub>CC</sub> | V    |
| I <sub>OUT</sub> H-bridge output current <sup>(1)</sup> | 0   | 1.5             | A    |
| f <sub>PWM</sub> Externally applied PWM frequency       | 0   | 250             | kHz  |

- (1) Power dissipation and thermal limits must be observed.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | DRV8836    | UNIT |
|-------------------------------|--|------------|------|
|                               |  | DSS (WSON) |      |
|                               |  | 12 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 50.4       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 58         | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 19.9       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.9        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 20         | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 6.9        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

 $T_A = 25^{\circ}\text{C}$ ,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

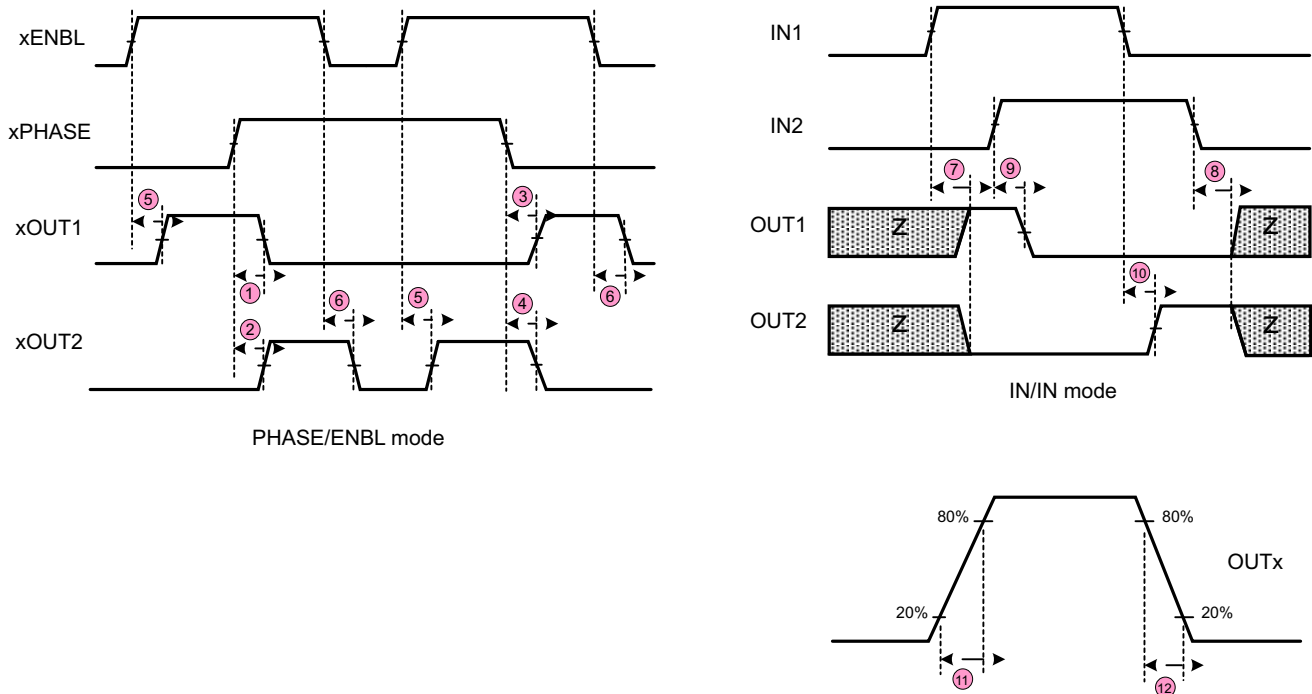
| PARAMETER           |                                   | TEST CONDITIONS   | MIN                   | TYP | MAX                       | UNIT |
|---------------------|-----------------------------------|---|-----------------------|-----|---------------------------|------|
| POWER SUPPLY        |                                   |   |                       |     |                           |      |
| I <sub>VCC</sub>    | VCC operating supply current      | f <sub>PWM</sub> = 50 kHz, no load                                    |                       | 1.7 | 2.5                       | mA   |
| I <sub>CCQ</sub>    | VCC sleep mode supply current     | nSLEEP = 0 V, all inputs 0 V  |                       | 40  | 95                        | nA   |
|                     |                                   | V <sub>CC</sub> = 3 V, nSLEEP = 0 V, all inputs 0 V                   |                       | 10  |                           |      |
| V <sub>UVLO</sub>   | VCC undervoltage lockout voltage  | V <sub>CC</sub> rising  |                       |     | 2                         | V    |
|                     |                                   | V <sub>CC</sub> falling   |                       |     | 1.9                       |      |
| LOGIC-LEVEL INPUTS  |                                   |   |                       |     |                           |      |
| V <sub>IL</sub>     | Input low voltage                 |   |                       |     | 0.25 ×<br>V <sub>CC</sub> | V    |
| V <sub>IH</sub>     | Input high voltage                |   | 0.5 × V <sub>CC</sub> |     |                           | V    |
| I <sub>IL</sub>     | Input low current                 | V <sub>IN</sub> = 0   | –5                    |     | 5                         | μA   |
| I <sub>IH</sub>     | Input high current                | V <sub>IN</sub> = 3.3 V   |                       |     | 50                        | μA   |
| R <sub>PD</sub>     | Pulldown resistance               |   |                       | 100 |                           | kΩ   |
| H-BRIDGE FETS       |                                   |   |                       |     |                           |      |
| R <sub>DS(ON)</sub> | HS + LS FET on resistance         | V <sub>CC</sub> = 3 V, I <sub>O</sub> = 800 mA, T <sub>J</sub> = 25°C |                       | 370 | 420                       | mΩ   |
|                     |                                   | V <sub>CC</sub> = 5 V, I <sub>O</sub> = 800 mA, T <sub>J</sub> = 25°C |                       | 305 | 355                       |      |
| I <sub>OFF</sub>    | OFF-state leakage current         |   |                       |     | ±200                      | nA   |
| PROTECTION CIRCUITS |                                   |   |                       |     |                           |      |
| I <sub>OCP</sub>    | Overcurrent protection trip level |   | 1.6                   |     | 3.5                       | A    |
| t <sub>DEG</sub>    | Overcurrent deglitch time         |   |                       | 1   |                           | μs   |
| t <sub>OCR</sub>    | Overcurrent protection retry time |   |                       | 1   |                           | ms   |
| t <sub>DEAD</sub>   | Output dead time                  |   |                       | 100 |                           | ns   |
| t <sub>TSD</sub>    | Thermal shutdown temperature      | Die temperature   | 150                   | 160 | 180                       | °C   |

## 6.6 Timing Requirements<sup>(1)</sup>

 $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $R_L = 20\ \Omega$ 

| NO. |   | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1   | $t_1$ Delay time, xPHASE high to xOUT1 low  |     | 210 | ns   |
| 2   | $t_2$ Delay time, xPHASE high to xOUT2 high |     | 150 | ns   |
| 3   | $t_3$ Delay time, xPHASE low to xOUT1 high  |     | 150 | ns   |
| 4   | $t_4$ Delay time, xPHASE low to xOUT2 low   |     | 210 | ns   |
| 5   | $t_5$ Delay time, xENBL high to xOUTx high  |     | 150 | ns   |
| 6   | $t_6$ Delay time, xENBL high to xOUTx low   |     | 150 | ns   |
| 7   | $t_7$ Output enable time                    |     | 210 | ns   |
| 8   | $t_8$ Output disable time                   |     | 210 | ns   |
| 9   | $t_9$ Delay time, xINx high to xOUTx high   |     | 125 | ns   |
| 10  | $t_{10}$ Delay time, xINx low to xOUTx low  |     | 125 | ns   |
| 11  | $t_R$ Output rise time                      | 20  | 188 | ns   |
| 12  | $t_F$ Output fall time                      | 8   | 30  | ns   |

(1) Not production tested – ensured by design



**Figure 1. Timing Requirements**

## 6.7 Typical Characteristics

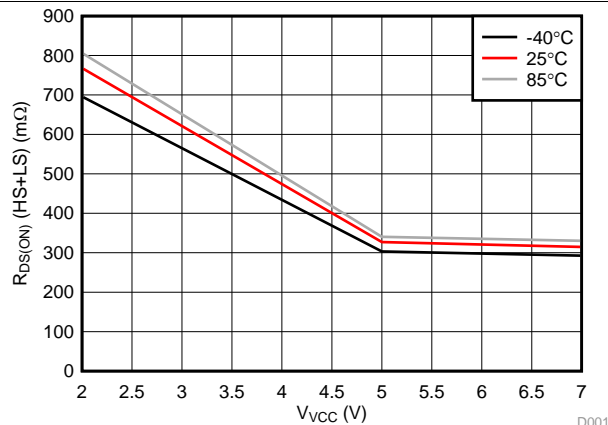


Figure 2.  $R_{DS(on)}$  (HS + LS)

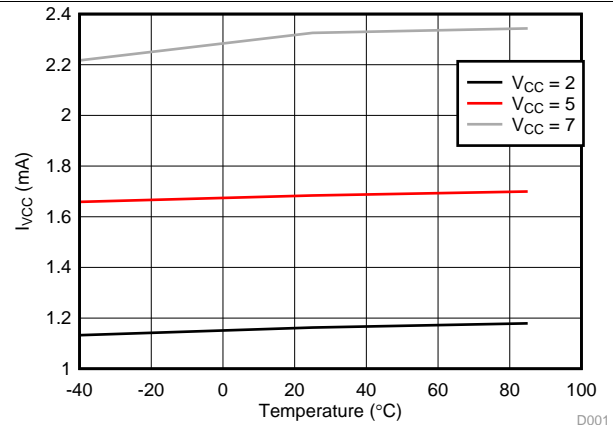


Figure 3.  $V_{CC}$  Operating Current, fPWM = 50 kHz, No Load

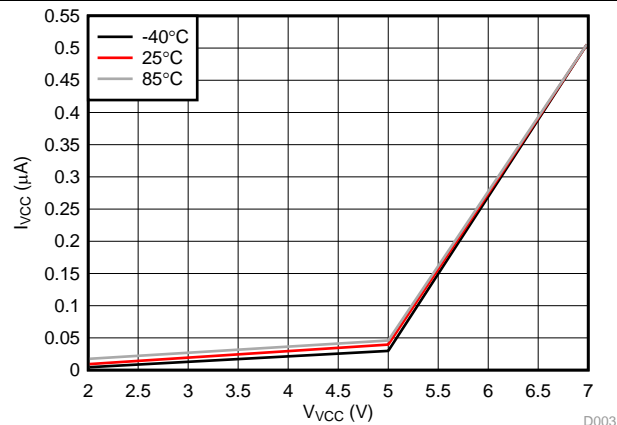


Figure 4.  $V_{CC}$  Sleep Current





## 7.3 Feature Description

### 7.3.1 Sleep Mode

If the nSLEEP pin enters a logic-low state, the DRV8836 enters a low-power sleep mode. In this state all unnecessary internal circuitry is powered down.

### 7.3.2 Power Supplies and Input Pins

There is a weak pulldown resistor (approximately 100 kΩ) to ground on the input pins.

### 7.3.3 Protection Circuits

The DRV8836 is fully protected against undervoltage, overcurrent, and overtemperature events.

#### 7.3.3.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge disable. After approximately 1 ms, the bridge re-enables automatically.

Overcurrent conditions on both high and low side devices, like a short to ground, supply, or across the motor winding results in an overcurrent shutdown.

#### 7.3.3.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge disable. Once the die temperature has fallen to a safe level operation automatically resumes.

#### 7.3.3.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all circuitry in the device disables, and internal logic resets. Operation resumes when VCC rises above the UVLO threshold.

**Table 1. Device Protection**

| FAULT                   | CONDITION     | ERROR REPORT | H-BRIDGE | INTERNAL CIRCUITS | RECOVERY           |
|-------------------------|---------------|--------------|----------|-------------------|--------------------|
| VCC undervoltage (UVLO) | $VCC < VUVLO$ | None         | Disabled | Disabled          | $VCC > VUVLO$      |
| Overcurrent (OCP)       | $IOUT > IOCP$ | None         | Disabled | Operating         | tOCR               |
| Thermal shutdown (TSD)  | $TJ > TTSD$   | None         | Disabled | Operating         | $TJ < TTSD - THYS$ |

## 7.4 Device Functional Modes

The DRV8836 is active when the nSLEEP pin is set to a logic high. When in sleep mode, the H-bridge FETs disable (Hi-Z).

**Table 2. Device Operating Modes**

| OPERATING MODE    | CONDITION               | H-BRIDGE  | INTERNAL CIRCUITS           |
|-------------------|-------------------------|-----------|-----------------------------|
| Operating         | nSLEEP high             | Operating | Operating                   |
| Sleep mode        | nSLEEP low              | Disabled  | Disabled                    |
| Fault encountered | Any fault condition met | Disabled  | See <a href="#">Table 1</a> |

### 7.4.1 Bridge Control

Two control modes are available in the DRV8836: IN/IN mode and PHASE/ENABLE mode. IN/IN mode is selected if the MODE pin is driven low or left unconnected; PHASE/ENABLE mode is selected if the MODE pin is driven to logic high. The following tables show the logic for these modes.

**Table 3. IN/IN Mode**

| MODE | xIN1 | xIN2 | xOUT1 | xOUT2 | FUNCTION<br>(DC MOTOR) |
|------|------|------|-------|-------|------------------------|
| 0    | 0    | 0    | Z     | Z     | Coast                  |
| 0    | 0    | 1    | L     | H     | Reverse                |
| 0    | 1    | 0    | H     | L     | Forward                |
| 0    | 1    | 1    | L     | L     | Brake                  |

**Table 4. PHASE/ENABLE Mode**

| MODE | xENABLE | xPHASE | xOUT1 | xOUT2 | FUNCTION<br>(DC MOTOR) |
|------|---------|--------|-------|-------|------------------------|
| 1    | 0       | X      | L     | L     | Brake                  |
| 1    | 1       | 1      | L     | H     | Reverse                |
| 1    | 1       | 0      | H     | L     | Forward                |

## 8 Application and Implementation

### NOTE

The information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

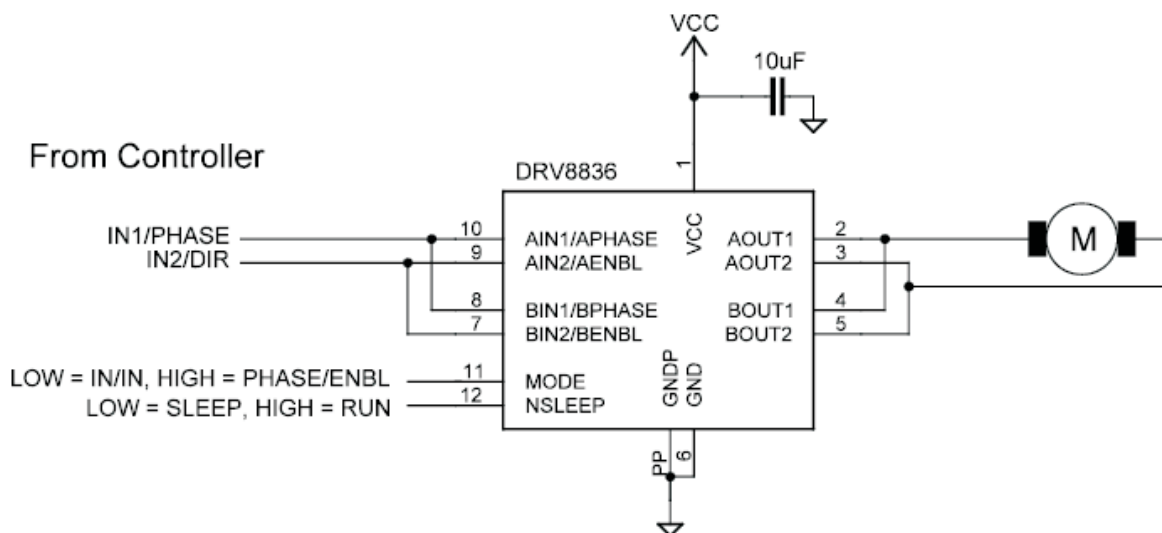
### 8.1 Application Information

The DRV8836 is used in one or two motor control applications. When configured in parallel, the DRV8836 provides double the current to one motor.

### 8.2 Typical Application

The two H-bridges in the DRV8836 can be connected in parallel for double the current of a single H-bridge. [Figure 5](#) shows the connections.

The following design is a common application of the DRV8836.



**Figure 5. Parallel Mode Connections**

#### 8.2.1 Design Requirements

The design requirements are shown in [Table 5](#).

**Table 5. Design Requirements**

| DESIGN PARAMETER         | REFERENCE | EXAMPLE VALUE |
|--------------------------|-----------|---------------|
| Motor voltage            | VCC       | 4 V           |
| Motor RMS current        | IRMS      | 0.3 A         |
| Motor startup current    | ISTART    | 0.6 A         |
| Motor current trip point | ILIMIT    | 0.5 A         |

## 8.2.2 Detailed Design Procedure

The following design procedure can be used to configure the DRV8836 in a brushed motor application.

### 8.2.2.1 Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

### 8.2.2.2 Low-Power Operation

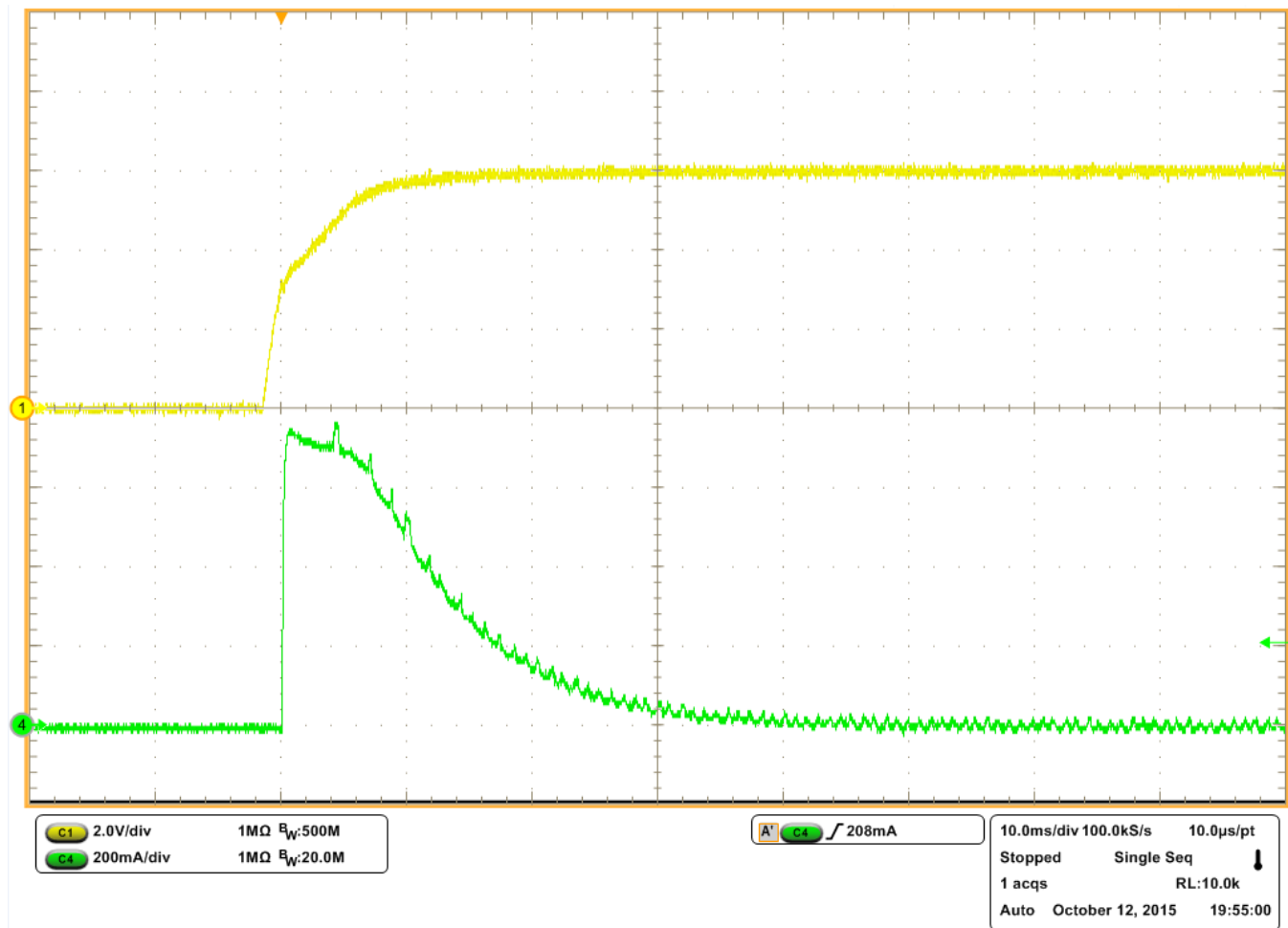
When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

## 8.2.3 Application Curve

The following scope captures motor startup as V<sub>CC</sub> ramps from 0 V to 6 V. Channel 1 is V<sub>CC</sub>, and Channel 4 is the motor current of an unloaded motor during startup. The motor used is a NMB Technologies Corporation OOB7PA12C, PPN7PA12C1. As V<sub>CC</sub> ramps the current in the motor increases until the motor speed builds up. The motor current then reduces for normal operation.

Inputs are set as follows:

- Mode: IN/IN
- AIN1: High
- AIN2: Low



**Figure 6. Motor Startup With No Load**

## 9 Power Supply Recommendations

### 9.1 Bulk Capacitance

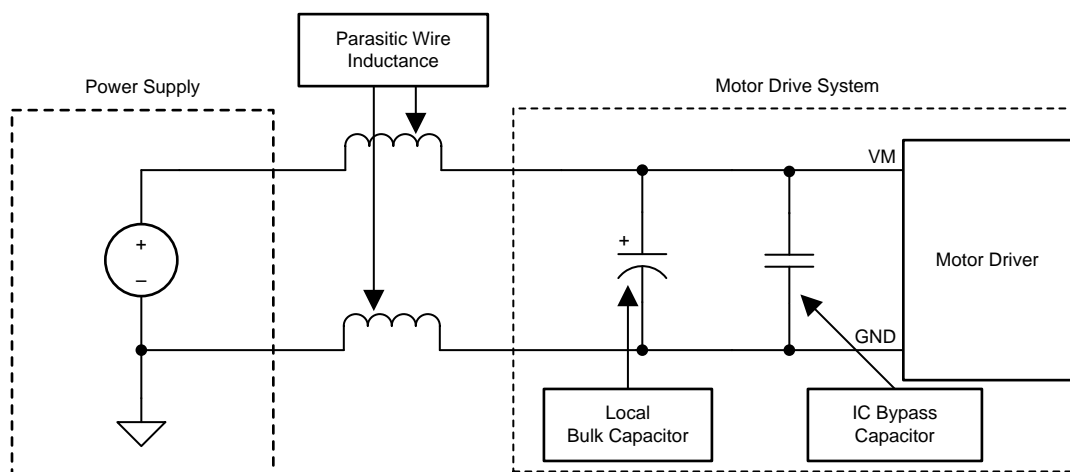
The appropriate local bulk capacitance is an important factor in motor drive system design. More bulk capacitance is generally beneficial but may increase costs and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate current changes from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.



**Figure 7. Bulk Capacitor**

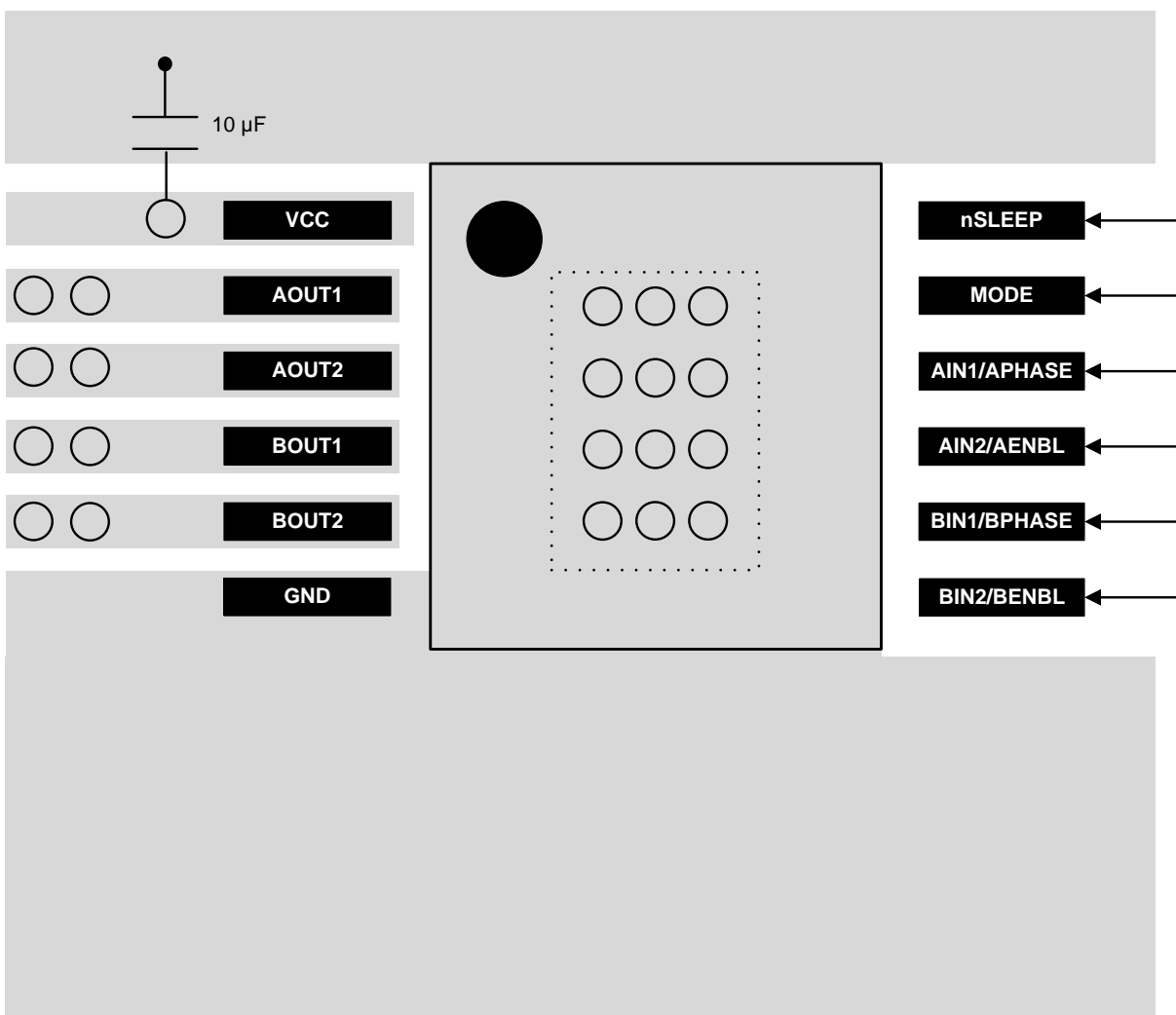
## 10 Layout

### 10.1 Layout Guidelines

The VCC pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-μF rated for VCC. This capacitor should be placed as close to the VCC pin as possible with a thick trace or ground plane connection to the device GND pin.

The VCC pin must bypass to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8836.

## 10.2 Layout Example



**Figure 8. Layout Recommendation**

## 10.3 Thermal Considerations

The DRV8836 has thermal shutdown (TSD) as described in [Thermal Shutdown \(TSD\)](#). If the die temperature exceeds approximately 150°C, the device disables until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or an ambient temperature that is too high.

### 10.3.1 Power Dissipation

The power dissipated in the output FET resistance or  $R_{DS(on)}$  dominates the power dissipation in the DRV8836. The average power dissipation when running both H-bridges can be roughly estimated by [Equation 1](#):

$$P_{TOT} = 2 \times R_{DS(on)} \times (I_{OUT(RMS)})^2$$

where

- $P_{TOT}$  is the total power dissipation,  $R_{DS(on)}$  is the resistance of the HS plus LS FETs, and  $I_{OUT(RMS)}$  is the RMS output current being applied to each winding.  $I_{OUT(RMS)}$  is equal to approximately 0.7x the full-scale output current setting. The factor of 2 comes from the fact that there are two H-bridges. (1)

The maximum amount of power dissipated in the device is dependent on ambient temperature and heatsinking.

## Thermal Considerations (continued)

### NOTE

$R_{DS(ON)}$  increases with temperature. As the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

### 10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For more information on PCB design, refer to TI application report [SLMA002](#), *PowerPAD™ Thermally Enhanced Package*, and TI application brief [SLMA004](#), *PowerPAD™ Made Easy*, available at [www.ti.com](http://www.ti.com).

In general, the more copper area that can be provided, the more power can be dissipated.

## 11 Device and Documentation Support

### 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DRV8836DSSR      | ACTIVE        | WSO          | DSS                | 12   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 85    | 836                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV8836DSSR | WSO          | DSS             | 12   | 3000 | 180.0              | 8.4                | 2.25    | 3.25    | 1.05    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS

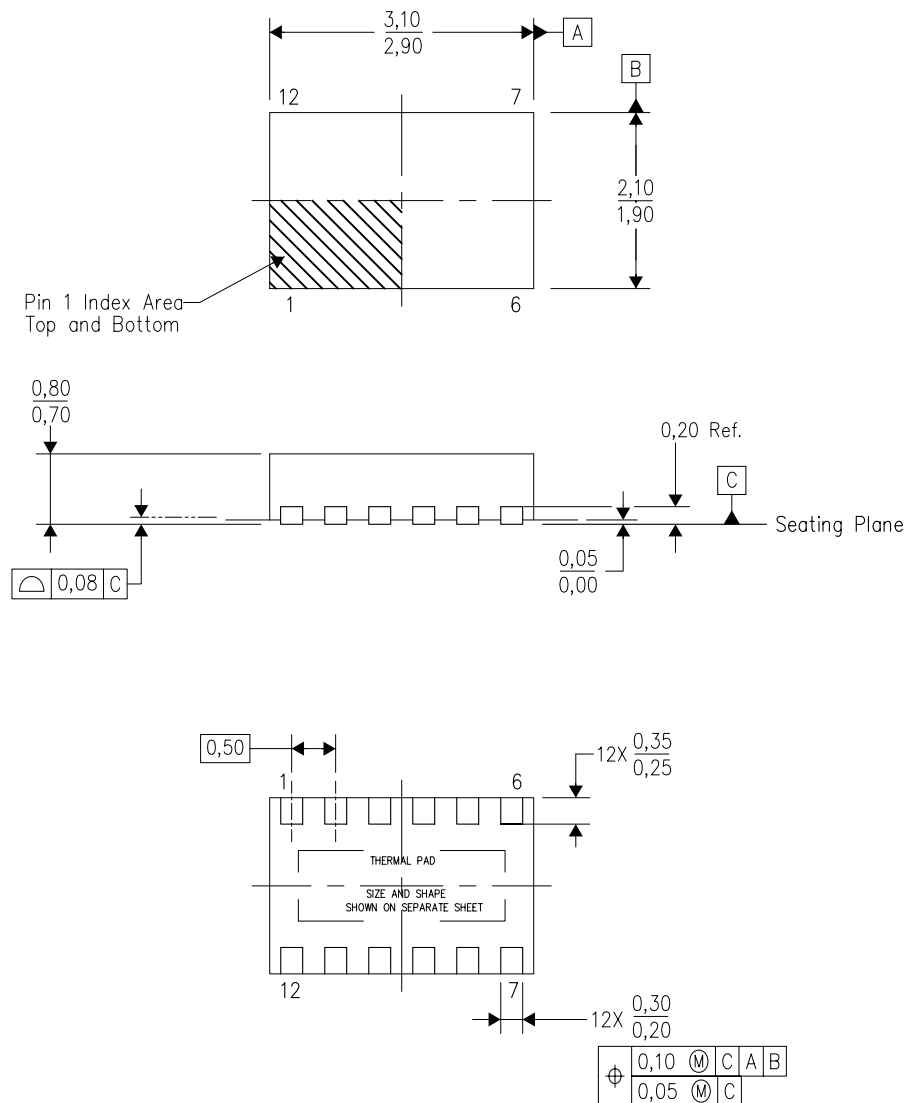


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV8836DSSR | WSON         | DSS             | 12   | 3000 | 210.0       | 185.0      | 35.0        |

DSS (R-PWSON-N12)

PLASTIC SMALL OUTLINE NO-LEAD



4209244/C 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

DSS (R-PWSON-N12)

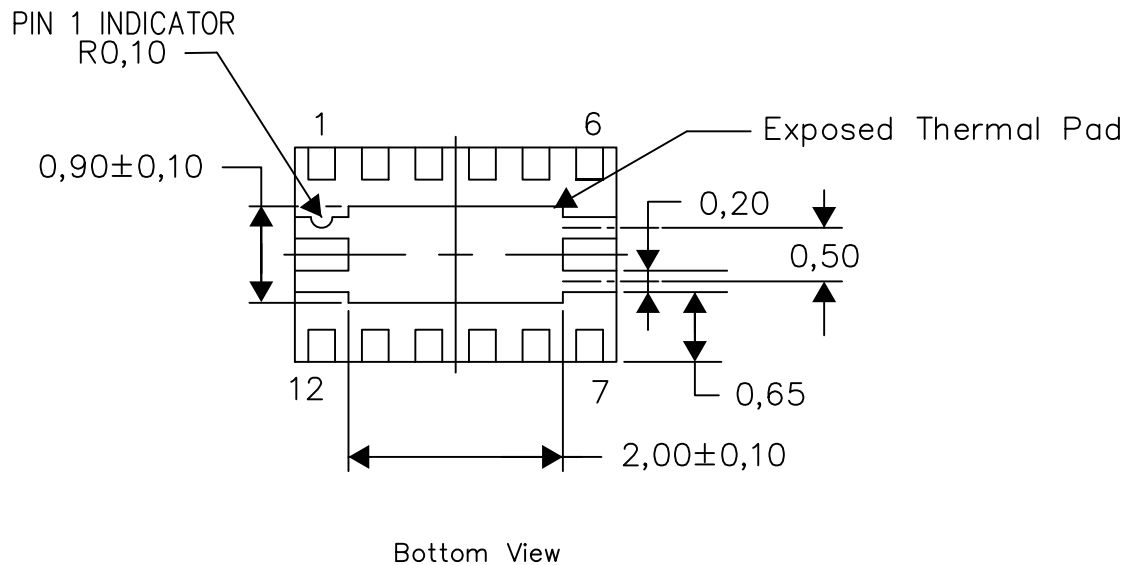
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



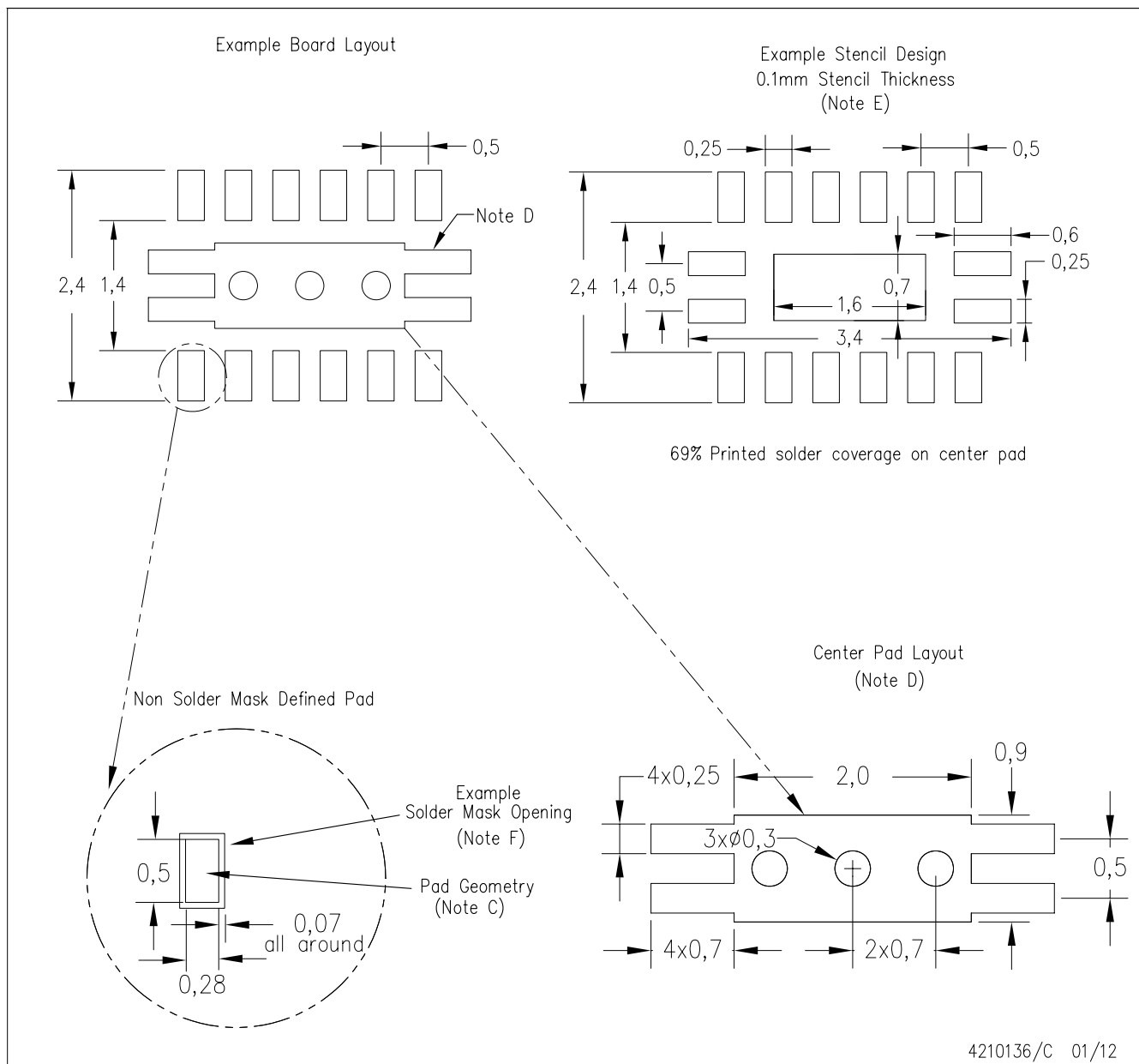
Exposed Thermal Pad Dimensions

4210135-2/D 02/16

NOTE: All linear dimensions are in millimeters

DSS (R-PWSON-N12)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

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| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
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| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
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| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
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