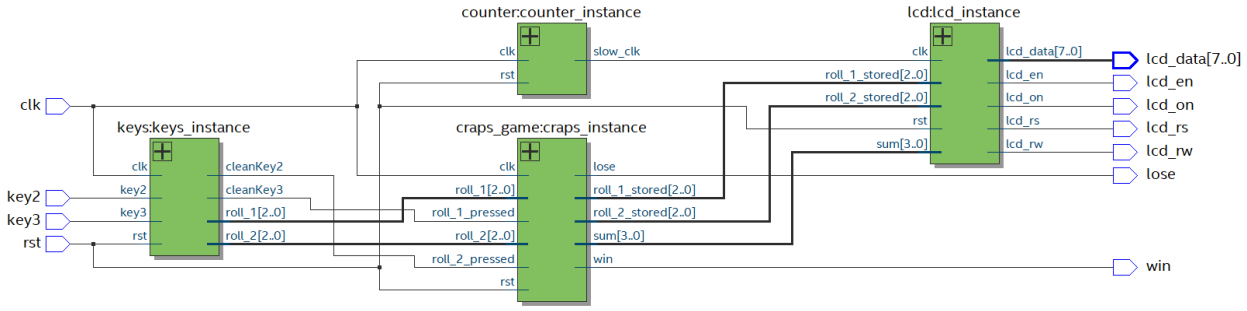
Craps Game Lab

Functionality:

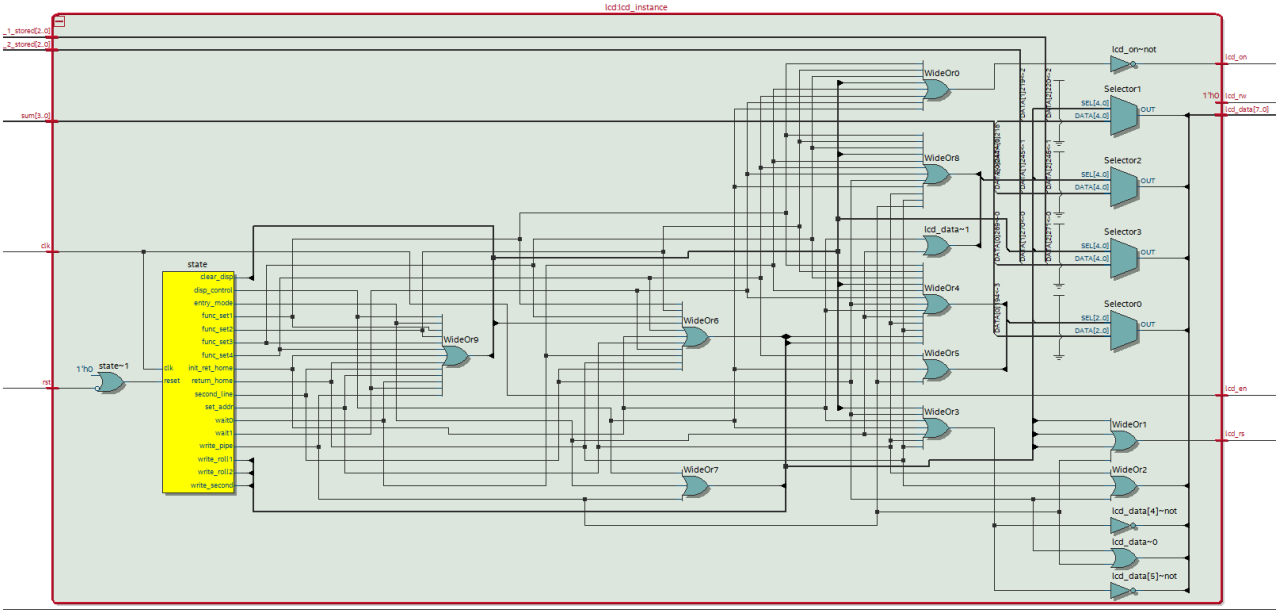
Inputs	
KEY3	Dice roll 1
KEY2	Dice roll 2
KEY0	Reset

Outputs	
LCD	Displays the current sum and dice roll values
LEDG0	Lose light – if on you lost, off otherwise
LEDG1	Win light – if on you won, off otherwise

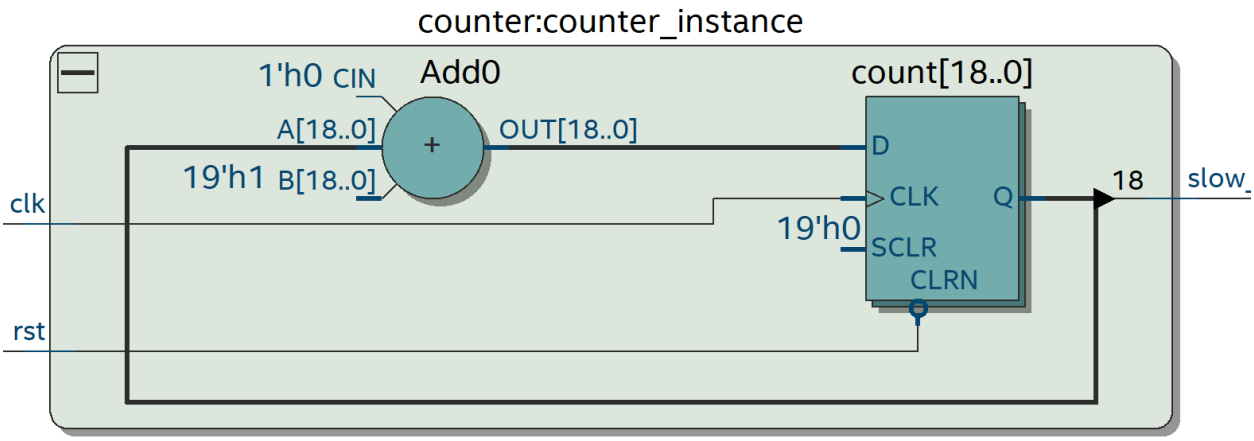
Top Level Schematic



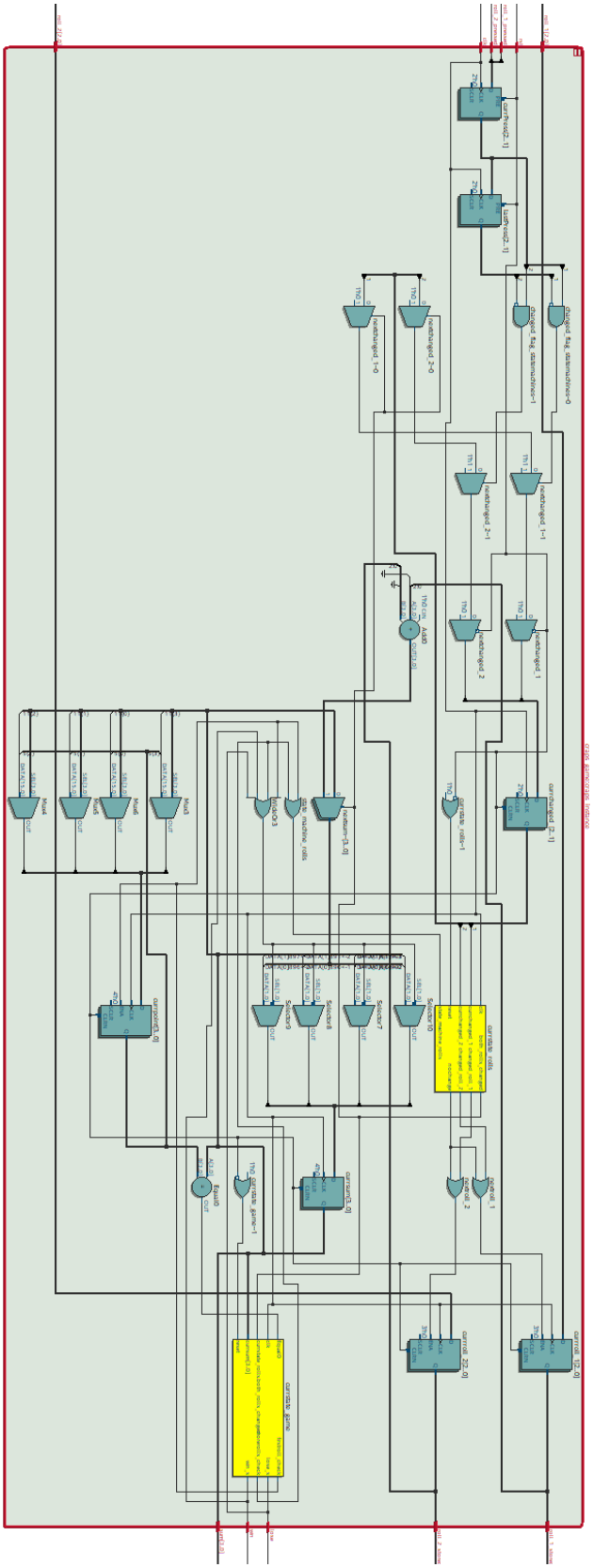
LCD Schematic (displays the rolls and the current sum)



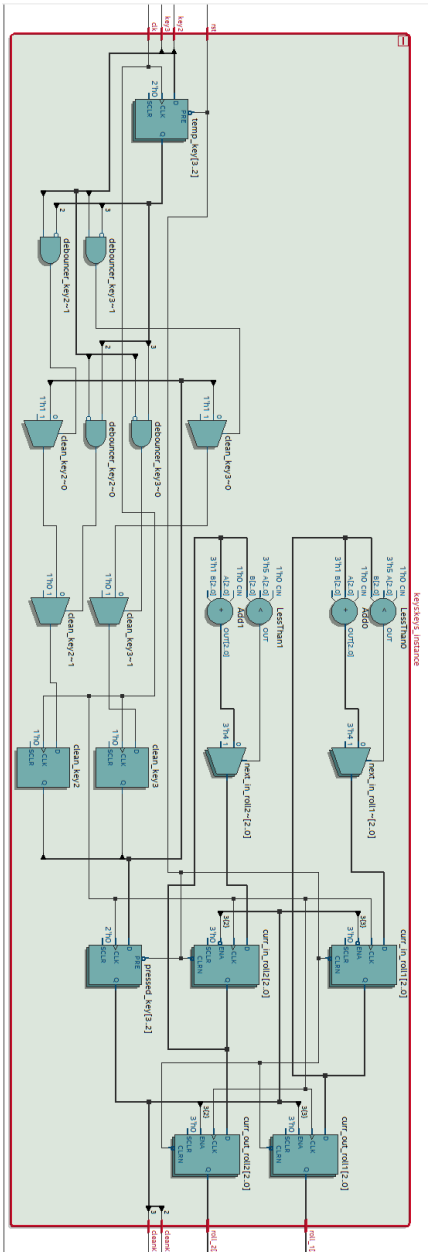
Counter Schematic (slows down clock for LCD)



Craps_game Schematic (decides state of the game)



Keys Schematic



Performance and Specs

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Nov 08 11:36:42 2022
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Standard Edition
Revision Name	Lab5
Top-level Entity Name	toplevel
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	113 / 114,480 (< 1 %)
Total registers	84
Total pins	18 / 529 (3 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Flow Elapsed Time

<<Filter>>

	Module Name	Elapsed Time	Average Processors Used	Peak Virtual Memory	Total CPU Time (on all processors)
1	Analysis & Synthesis	00:00:09	1.0	4840 MB	00:00:20
2	Fitter	00:00:13	1.0	6196 MB	00:00:22
3	Assembler	00:00:03	1.0	4680 MB	00:00:02
4	Timing Analyzer	00:00:01	1.0	4918 MB	00:00:02
5	Total	00:00:26	--	--	00:00:46

Parallel Compilation

<<Filter>>

	Processors	Number
1	Number detected on machine	20
2	Maximum allowed	10
3		
4	Average used	1.00
5	Maximum used	10
6		
7	Usage by Processor	% Time Used
1	Processor 1	100.0%
2	Processors 2-10	0.0%

Analysis & Synthesis Summary

<<Filter>>

Analysis & Synthesis Status	Successful - Tue Nov 08 11:36:24 2022
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Standard Edition
Revision Name	Lab5
Top-level Entity Name	toplevel
Family	Cyclone IV E
Total logic elements	124
Total registers	84
Total pins	18
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimated Total logic elements	124
2		
3	Total combinational functions	92
4	Logic element usage by number of LUT inputs	
1	-- 4 input functions	33
2	-- 3 input functions	22
3	-- <=2 input functions	37
5		
6	Logic elements by mode	
1	-- normal mode	72
2	-- arithmetic mode	20
7		
8	Total registers	84
1	-- Dedicated logic registers	84
2	-- I/O registers	0
9		
10	I/O pins	18
11		
12	Embedded Multiplier 9-bit elements	0
13		
14	Maximum fan-out node	rst~input
15	Maximum fan-out	82
16	Total fan-out	569
17	Average fan-out	2.68