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Lab 1, Building an RC Low Pass Filter (Hardware)

Theory:

Figure 1 shows how the voltage divider equation works for two resistors in series. Figure 2 shows the equation to calculate percent error. Figure 3 shows the equation for the transfer function of a low pass filter and how the cut-off angular frequency is 1/(RC).

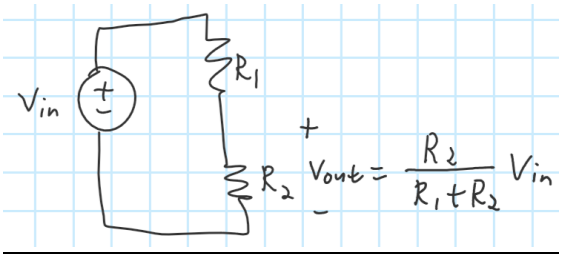


Figure 1

$$\%\ error = \frac{measured - ideal}{ideal} \cdot 100$$

Figure 2

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 + sRC}$$

Figure 3

Analysis and Design:

Picking R1 as 2200 Ohms and R2 as 6800 Ohms and an input voltage of 12 V would yield an output voltage of 9.07 V, as shown in Figure 4. Then for the low pass filter, with using R as a 100 Ohms and C as 10 micro-Farads, the work for finding the cutoff frequency is shown in Figure 5. And the theoretical amplitude of the output voltage, given an input of 1 V, would be 0.016 V as the magnitude gain for the circuit would be 0.016, as shown in the work in Figure 6.

$$9.07\,V = \frac{6800}{2200 + 6800} \cdot 12$$

Figure 4

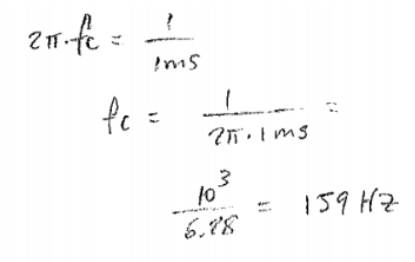


Figure 5

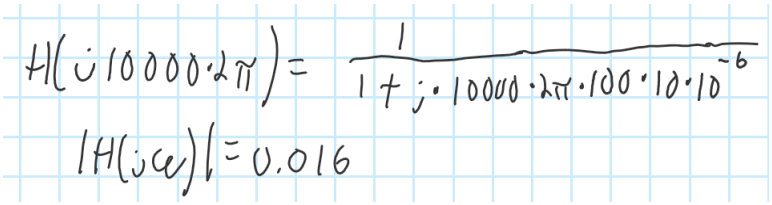


Figure 6

Laboratory Procedure:

Applying a voltage source to measure output at R2 at the specified value for it, R1, and Vin as shown in the above section. Measured the cut-off frequency and make a Bode plot of the low pass filter as per the values of R and C in the above section and what the amplitude of the output voltage for an input of a sine wave at 1V amplitude and 10KHz is.

Data Collection:

The output voltage is 9.07 V on R2, see Figure 7.

	Channel 1
DC	9.066 V
True RMS	9.066 Ṽ
AC RMS	2 mṼ

Figure 7

Figure 8 contains the output wave from a square waveform that varies from 0V to 1V and has a frequency of 1 kHz. This resulting waveform does indeed match my expectation as when the input is 1V the capacitor is charging and when the input is 0V the capacitor is discharging all exponentially. The measured cutoff frequency is 108.51 Hz, see the Bode plot in Figure 9. And the output voltage for the sine wave is 38.566 mV, see Figure 10.

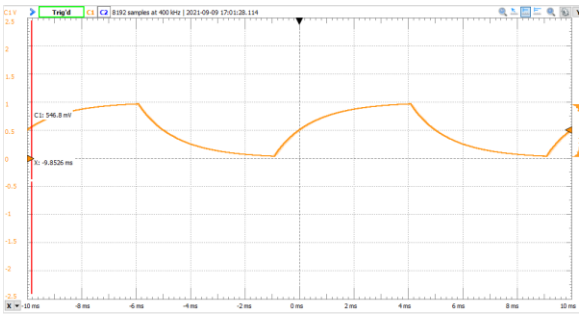


Figure 8

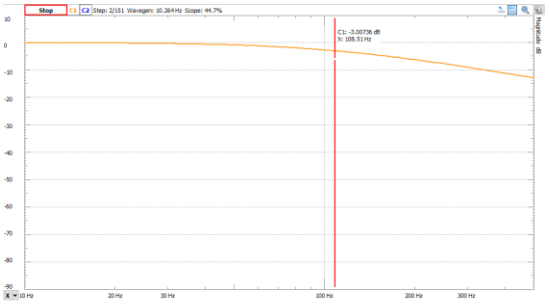


Figure 9

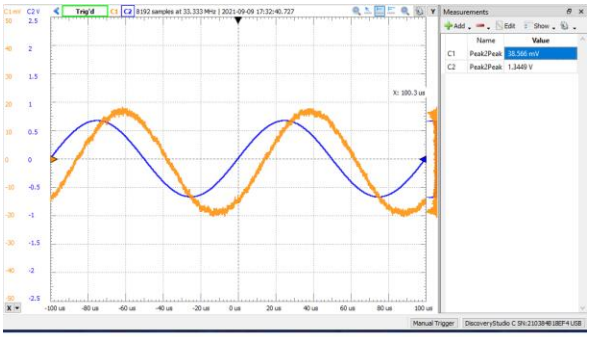


Figure 10

Data Analysis:

The percent error for the voltage divider is around 0%. And the percent error of the time constant for the RC circuit is 47.4%.

Summary and Interpretation of Result:

The voltage divider is quite accurate because of how the circuit is simple. However, the low pass filter is not really accurate due to the selected high capacitance that is parasitic. Overall though this lab taught me how to use the waveform generator, network analyzer, voltmeter, and oscilloscope all on the waveform app and board.

Lab 2, Modeling and simulating op. amp based circuits (LTSPICE)

Theory:

Figure 1 contains the transfer function for a low pass filter with A0 being the gain from a dependent voltage source and wp being the bandwidth frequency. Figure 2 contains the sub-circuit for an operational amplifier. Also, a non-inverting amplifier will have a gain = R2/R1 + 1.

$$T(s) = \frac{A0}{1 + \frac{s}{\omega_p}}$$

Figure 1

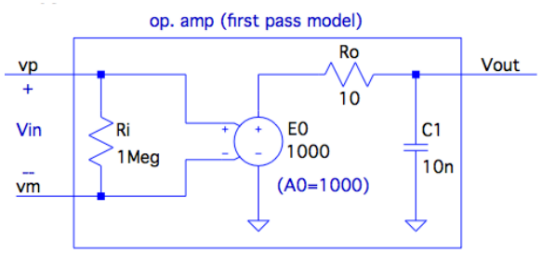


Figure 11

Analysis and Design:

For the operational amplifier model in Figure 2 component values used are Ri = 1M Ohms, Ro = 10 Ohms, and A0 = 1000, and the bandwidth is 1.6 MHz, please see the calculations for that value in Figure 4. That yielded the bode plot in Figure 3.

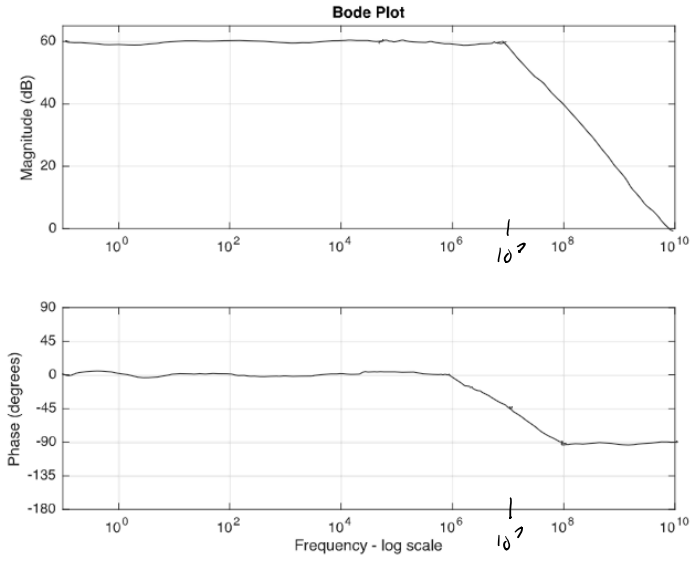


Figure 12

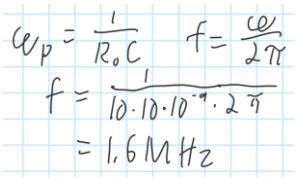


Figure 13

Figure 5 shows a non-inverting amplifier made with the operation amplifier model in Figure 2. The calculated gain is 10 which is 20 dB and the bandwidth is 160 MHz, the calculation for that value is in Figure 6.

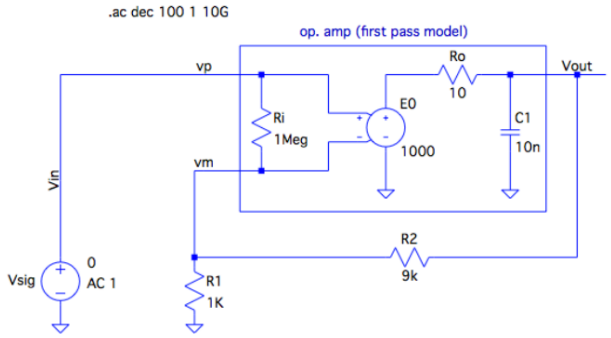


Figure 14

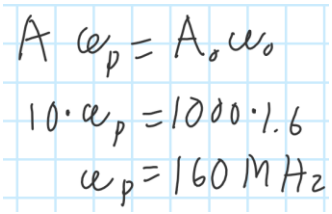


Figure 15

Figure 7 shows the non-inverting amplifier but with a load resistor which the output goes through and the Vsig is changed to be instead a DC voltage of 1V. In this circuit below, according to the calculations in Figure 8, Vout = 9.804 V, V(vm) = 804 mV, I(Ri) = -981.4 mA, I(R1) = I(R2) = 1 mA, I (RL) = 980.4 mA.

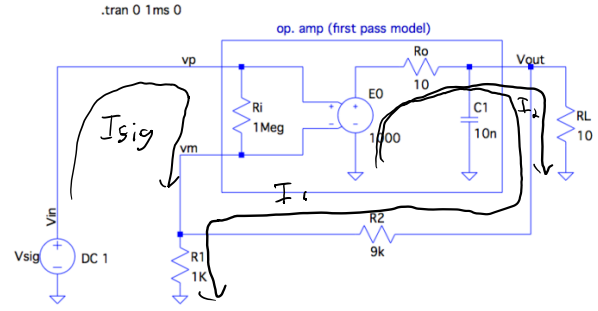


Figure 16

$$-V_{sig} + V_{in} + R_1 I_1 = 0$$
$$-1000 V_{in} + R_0 (I_1 + I_2) + (R_1 + R_2) I_1 = 0$$
$$-1000 V_{in} + R_0 (I_1 + I_2) + R_2 I_2 = 0$$
$$V_{in} + 1000 I_1 = 1$$
$$-1000 V_{in} + (10000 + 10) I_1 + 10 I_2 = 0$$
$$-1000 V_{in} + 10 I_1 + 20 I_2 = 0$$
$$V_{in} = 0.0196\ V \qquad I_2 = 0.9804\ A$$
$$I_1 = 0.0010\ A$$

Figure 17

Figure 9 shows how Ri, the input resistance is changed to 1 k Ohms. Vout/Vin is not expected to change because of this as Ri just measures the Vin for the dependent voltage source, so the current through Ri would adjust accordingly. If Rsig changes to 1 k Ohms then Vout/Vin would change. This is because the voltage for the dependent voltage source is less, so the output voltage is less, however, vin is the same as the current adjusts. And thus the calculated gain is 54 dB.

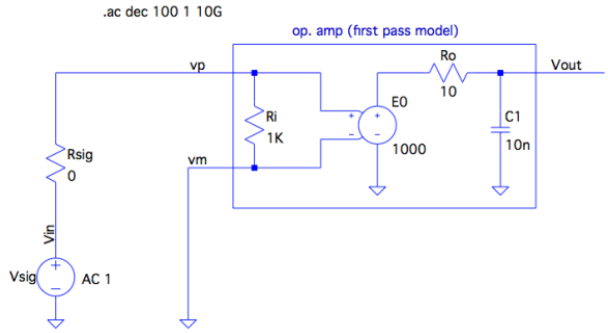


Figure 18

Laboratory Procedure:

Simulate the circuits in Figure 2, Figure 6, and Figure 9 in LTSpice and display their Bode Plots of Vout/Vin.

Data Collection:

As seen in Figure 10 is how LTSpice plotted the magnitude and phase of the circuit in Figure 2.

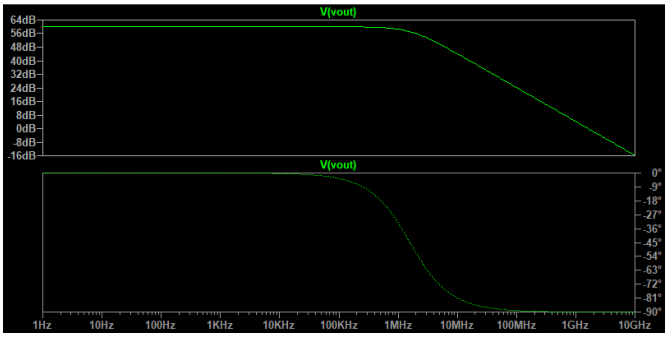


Figure 19

As seen in Figure 11 is how LTSpice plotted the magnitude and phase of the circuit in Figure 16. And from that, the gain was found to be 20 dB and the bandwidth was found to be 158.4 MHz.

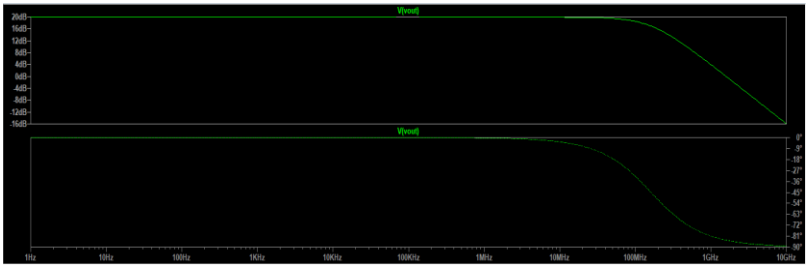


Figure 20

Running a TRAN analysis in LTSpice for the circuit in Figure 17 yielded Vout = 9.80 V, V(vm) = 980.4 mV, I(Ri) = 0, I(Ro) = -981.3 mA, I(R1) = 980.4 µA, I(R2) = 980.4 µA, and I(RL) = 980 mA. If Ro increases to 100 Ohms then Vout would decrease as Ro is ideally supposed to be zero. And the circuit simulated again with the new value of Ro yields Vout = 9.01 V, therefore, to indeed match my intuition about why Vo decreased.

As seen in Figure 12 is how LTSpice plotted the magnitude and phase of the circuit in Figure 19. And from that, the gain was found to be 60 dB. And when Rsig was changed to be 1 K Ohms the gain was found to be 54 dB.

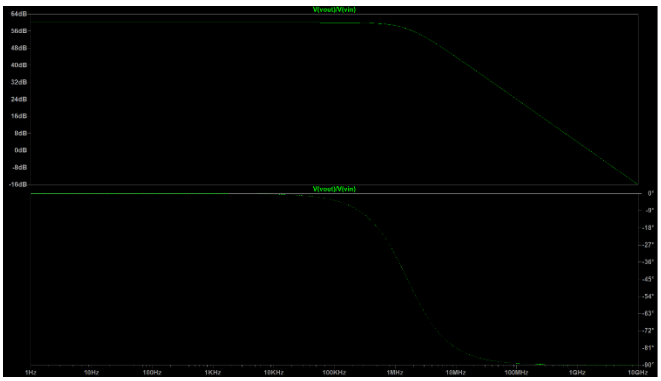


Figure 21

Data Analysis:

For the circuit in Figure 3, the calculated quantities match the LTSpice simulated values well within 10-20%.

Summary and Interpretation of Result:

Overall this lab taught how to use LTSpice to realize amplifier circuits and how the value of the circuit in LTSpice is indeed as accurate as the calculated theoretical values. Then, the circuits can be analyzed through Bode Plots or TRANS analysis. Finally, what happens if the amplifiers were more “non-ideal” was recorded with changing resistor values.

Lab 3, Building an op-amp based non-inverting amplifier and an integrator (Hardware)

Theory:

Figure 1 shows the pinout of the LM-741 which is the output from the operational amplifier circuit inside of it.

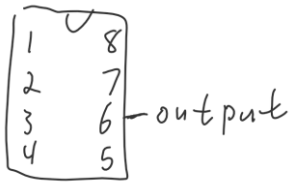


Figure 1

Analysis and Design:

Figure 2 is the schematic of a non-inverting amplifier that provides a voltage gain of 10. And if R1 = 1 k Ohms then R2 = 9.1 k Ohms

Figure 2

Figure 3 is the schematic of an inverting integrator amplifier.

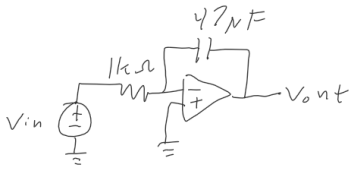


Figure 3

Figure 4 contains calculations for the voltage that is outputted at half the period, which yields a value of 1.06 V, and as seen in Figure 5 the output will linearly go to this voltage and then back to 0 periodically.

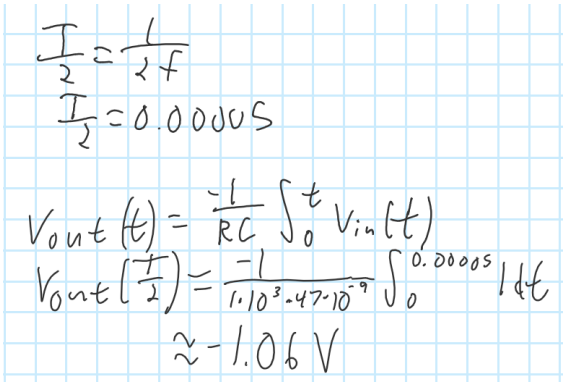


Figure 4

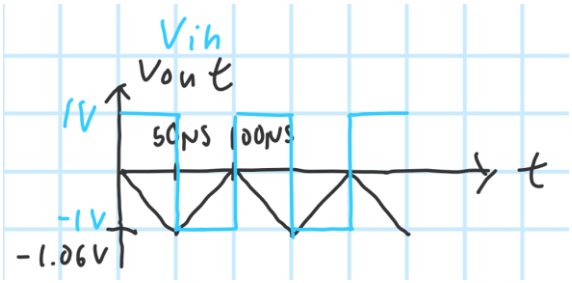


Figure 5

Laboratory Procedure:

In this lab, a non-inverting amplifier was built, as shown in Figure 3, and make a Bode Plot using the network analyzer. Then an input of a sinusoidal signal with frequency = 1 kHz and amplitude 1V peak and then 2V peak will be used. Lastly, an integrator, as shown in Figure 4, will be built and input a 10 kHz square waveform with a 1V peak.

Data Collection:

Figure 6 contains the Bode Plot for the non-inverting amplifier. The measured gain is 15 dB and the measured bandwidth is 23 kHz.

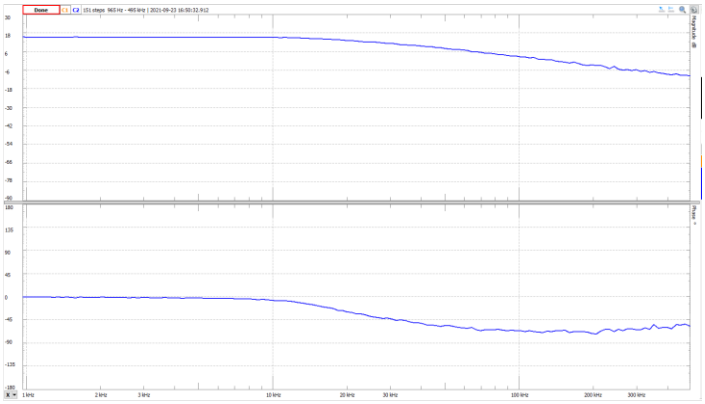


Figure 6

Figure 7 contains the output of the non-inverting amplifier from a sinusoidal input with an amplitude of 1V and frequency of 1kHz. And the measured gain is 10.

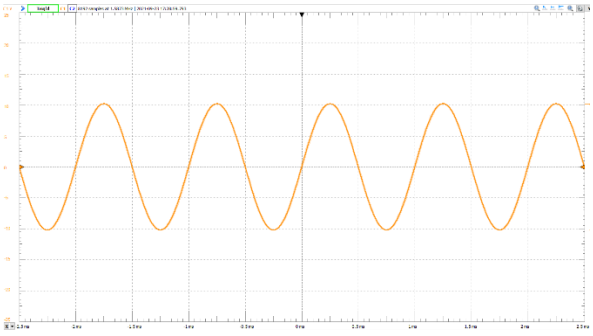


Figure 7

Figure 8 contains in orange the output of the non-inverting amplifier from a sinusoidal input with an amplitude of 2V and frequency of 1KHz, in blue. And the measured gain is 5.5.

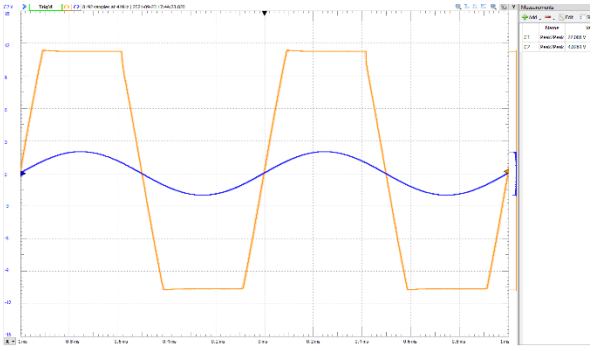


Figure 8

Figure 9 contains in orange the output of the non-inverting amplifier from a sinusoidal input with an amplitude of 1V and frequency of 100 kHz, in blue. And the measured gain is 1.5.

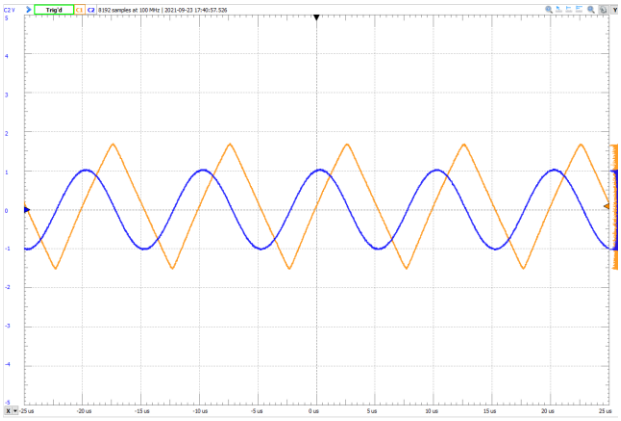


Figure 9

Figure 10, disregarding the scaling on this graph, contains how the output wants to migrate to the rail voltage of 11V. And this is because of the DC imperfection in the circuit in which the capacitor will build up enough voltage to behave like an open circuit. And thus the operational amplifier will operate in open loop

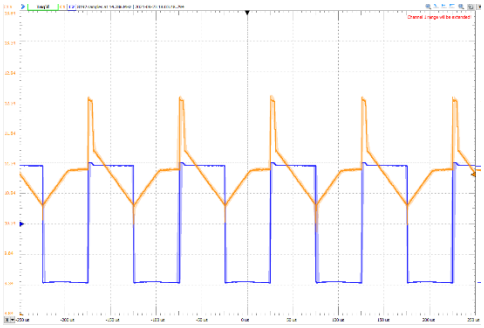


Figure 10

Figure 11 contains the Vout and Vin of a resistor in parallel with the capacitor to correct the problem. Then the measured peak magnitude of the output triangle wave is 1.6 V.

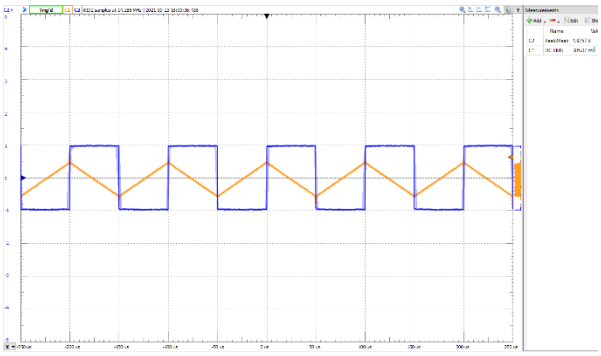


Figure 11

Data Analysis:

The non-inverting amplifier gain in for an input of 2V only had a gain of 5.5 (22/4 both values are peak to peak voltages) and not the calculated 10 because of how the output voltage clips +/-11V as only a voltage of +/-12V is supplied to the operational amplifier. And compared to the ideal inverting integrator amplifier's expected peak magnitude of 1.06 V, the corrected circuit's magnitude is 1.6 V. This mismatch is due to the resistor added in parallel as this circuit is therefore not an ideal integrator but a low pass filter.

Summary and Interpretation of Result:

Overall this experiment taught how there are physical constraints to devices that are not apparent in theory but manifest themselves in actual testing of the circuit, like the voltage clipping in the non-inverting amplifier and ramping to the rail voltage in the inverting amplifier circuit.

Lab 4: Diodes' Characterization (LTSPICE & Hardware)

Theory:

Figure 1 shows the equation relating the voltage across a diode to the current through it. Then, Figure 2 shows how this equation models the forward and reverse bias region. However, the equation does not model the breakdown/Zener region, nor does it model the region where the transistor blows up. Also, shown according to Figure 1 and on Figure 2 is how the curve will change depending on temperature.

$$I_D = I_S\left(e^{\frac{V_D}{V_T}} - 1\right) \qquad V_T = \frac{kT}{q}$$

Figure 1

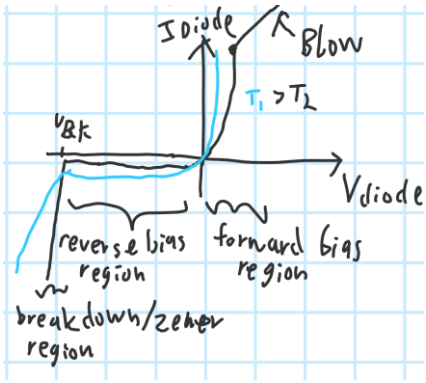


Figure 2

Analysis and Design:

Figure 3 shows a circuit in LTSpice that contains a D1N4148 diode and will be used to measure the current through the diode with a varying voltage input.

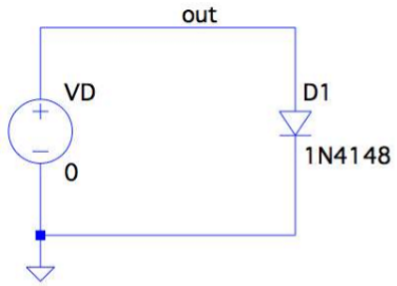


Figure 3

Figure 4 shows a plot of ID vs VD in the forward and reverse region at the room temperature of 27 deg C.

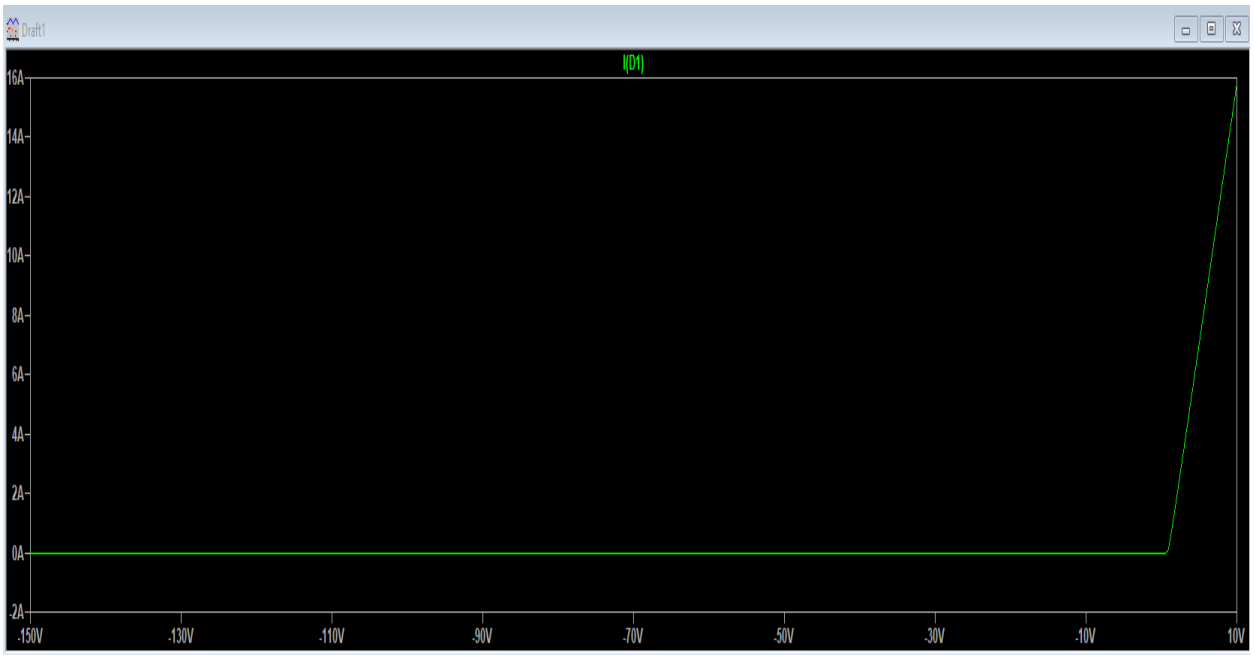


Figure 4

In LTSpice the default temperature (TNOM) used by the SPICE simulation is 27 deg C, the unit of temperature used by SPICE is deg C, using DC analysis for plotting the ID vs VD curve of the diode will be needed, [0,1] is a reasonable range of VD values to plot the ID characteristic, and the SPICE directive ".dc VD -10 10 0.1" will be used to obtain the plot. When comparing qualitatively the plots with the information provided by the diode Data Sheet, the model provided does seem to capture the forward and reverse region behavior adequately but not the reverse breakdown region.

Laboratory Procedure:

In this lab ".model D1N4148 D (IS=0.1PA, RS=16, CJO=2PF TT=12N BV=100 IBV=0.1PA)" is used compared to the default one provided by LTSPICE. Then the ID vs. VD characteristic of the diode in forward, reverse, and reverse breakdown region at three different temperatures: -50 centigrade, 27 centigrade, and 50 centigrade are plotted. After that, the reverse breakdown voltages will be measured.

Data Collection:

In the figures, Red is 50 deg C, Blue is 27 deg C, and Green is -50 deg C. Figure 5 is the breakdown region, Figure 6 is the forward region, and Figure 7 is the reverse region.

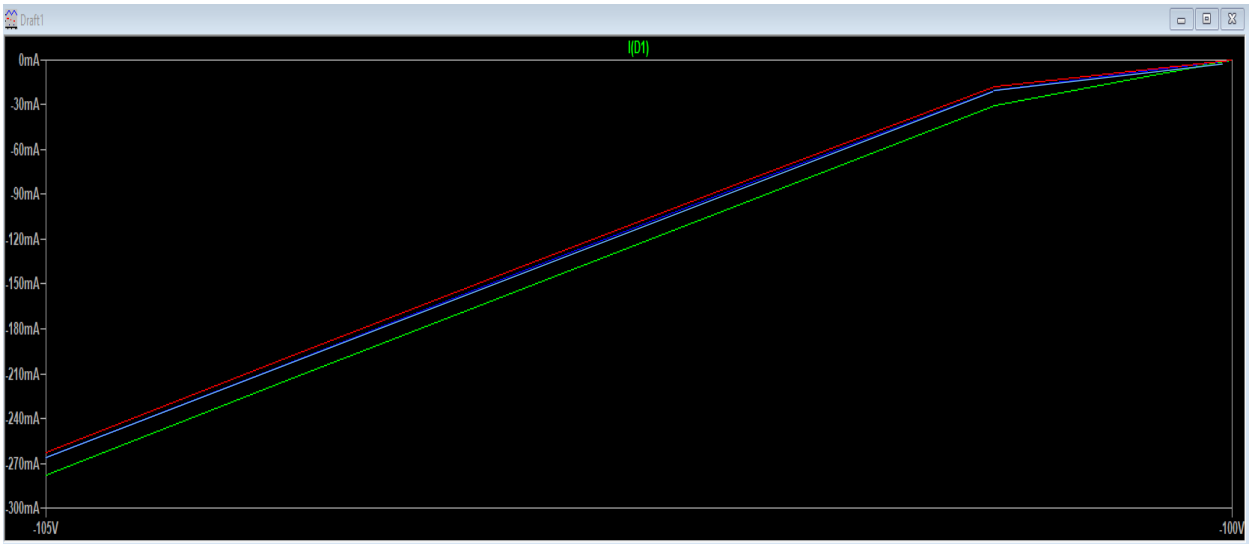


Figure 5

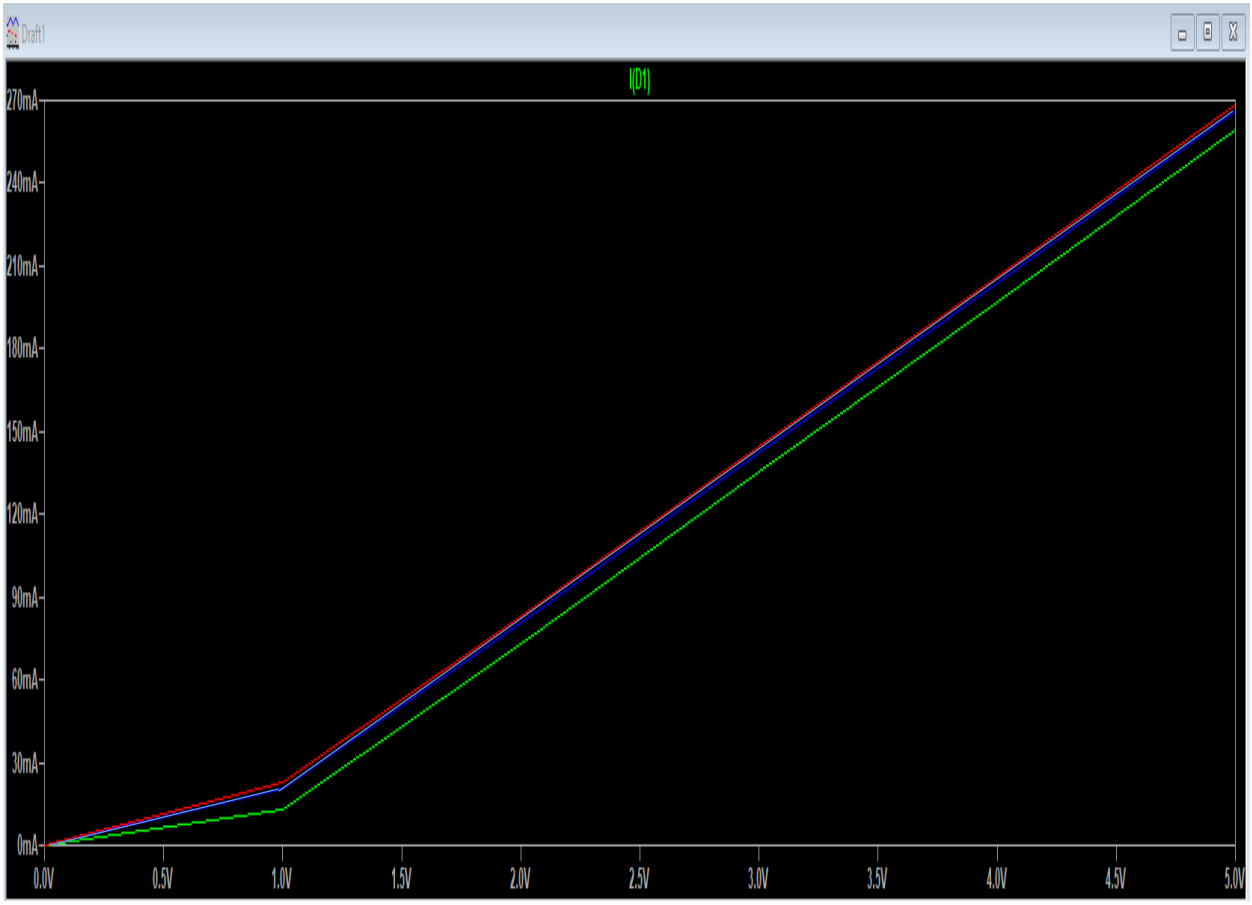


Figure 6

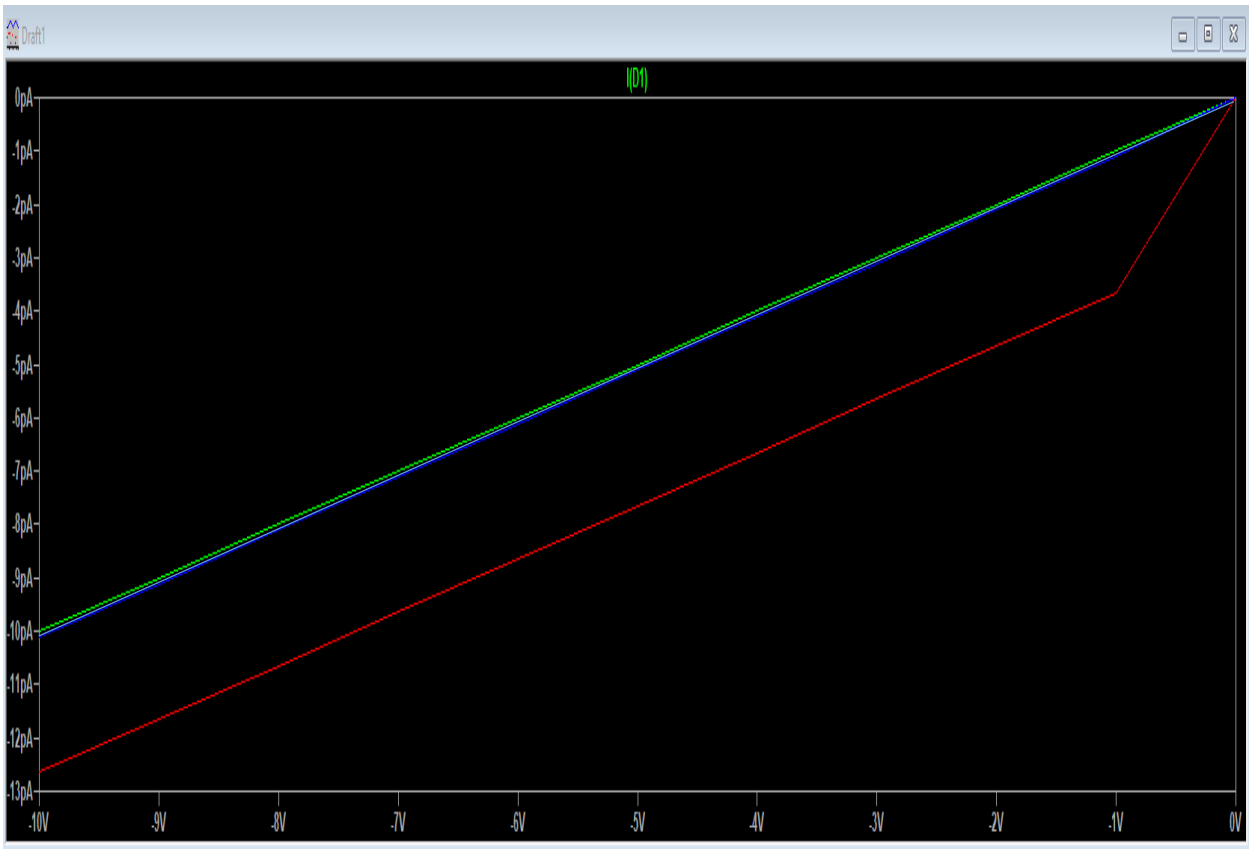


Figure 7

Data Analysis:

Figure 8 contains the equation used to calculate the forward temperature coefficient. This was applied to the graphs by picking 2.64 V and 2.60 V at 27 deg C and 50 deg C at the current 120 mA. Then the change in those values and the resulting coefficient value are shown in Figure 9. Comparing that to the theoretical coefficient value of -2mV/deg C led to a percent error of -15%.

$$dV_D/dT \approx \Delta V_D/\Delta T.$$

Figure 8

Diode	Temperature coeff. [units]	I_D [units]	ΔV_D [units]	ΔT [units]
1N4148	-1.7 mV/°C	120 mA	0.04 V	-23 °C

Figure 9

From the reverse breakdown region graph, in Figure 5, the breakdown voltage increases in magnitude when temperature increases.

Diode Type	V_{BR} [units] at –50 °C	V_{BR} [units] at 27 °C	V_{BR} [units] at 50 °C
1N4148	-100.4 V	-100.5 V	-100.6 V

Figure 10

Summary and Interpretation of Result:

Overall this experiment showed how the voltage and current across a diode in the forward, reverse, and breakdown region changes with temperature.

Lab 5: Designing and constructing a Zener based regulator (Hardware)

Theory:

The model in Figure 1 is a Zener diode voltage regulator that will provide a relatively constant voltage output despite input variations from the voltage source. Figure 2 shows the equation used to calculate what resistance R in Figure 1 should be. Then Figure 3 shows how to find the voltage and current through the Zener diode with the intersection of the breakdown voltage curve and the curve of the current through resistor R when RL is infinity.

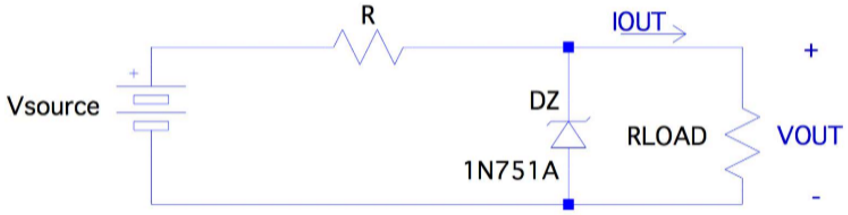


Figure 1

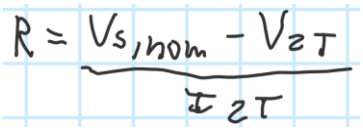


Figure 2

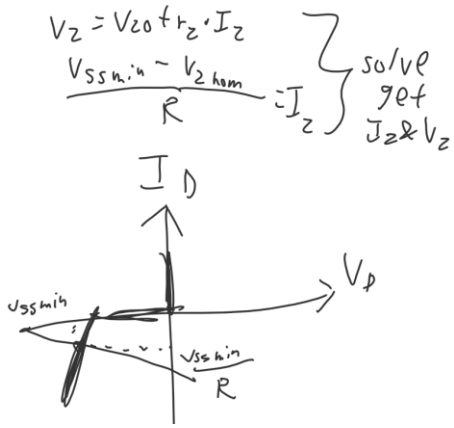


Figure 3

Analysis and Design:

Figure 4 shows how the voltage source will be set up such that the Vminus can change so VAB will be in between 12 V and 17 V. V_{ZT} = 5.1 V and I_{ZT} = 20 mA are the nominal voltage and current of IN751A, the nominal Zener resistance of the IN751A is 17 Ohms, and the value of R as 340 Ohms (12-5.1 / 0.02 = 345 Ohms and there is physically no 345 Ohm resistor) was selected for the design. Figure 5 shows the maximum current and voltage across the Zener diode as RL is infinity and Vsource varies from 12V to 17V, Figure 6 shows the piecewise model used for the Zener diode, the max amount of current through the regulator (Zener and resistor), if the load is accidentally shorted, is 50 mA (17 V/ 340 Ohms), and 0 A flow through the Zener in this circumstance.

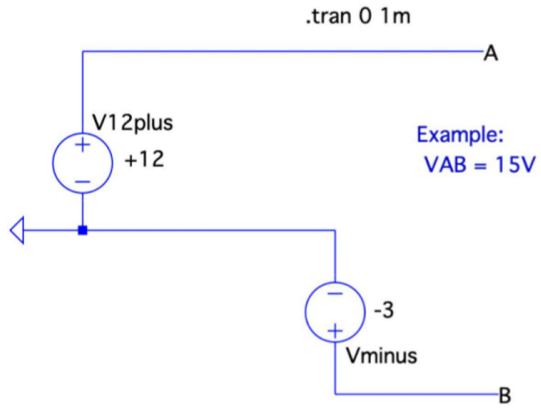


Figure 4

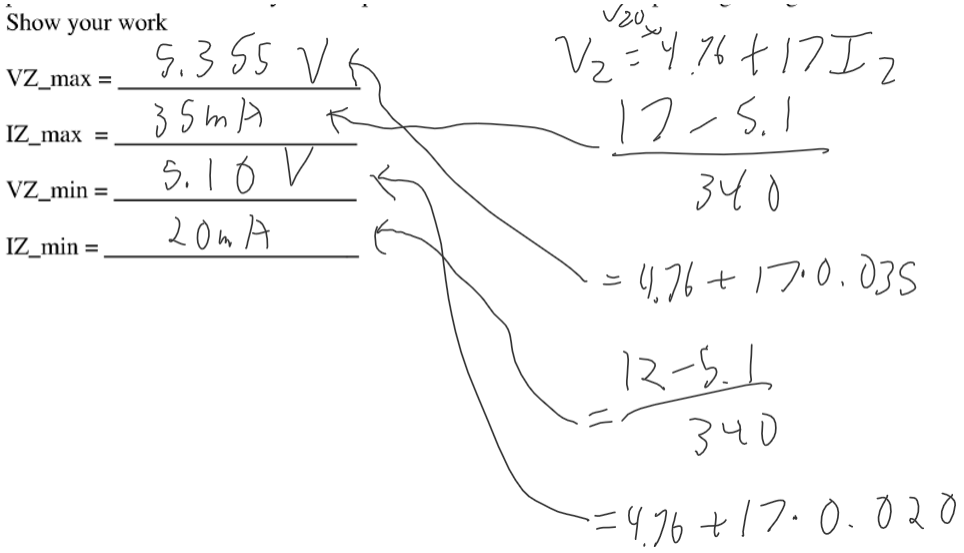


Figure 5

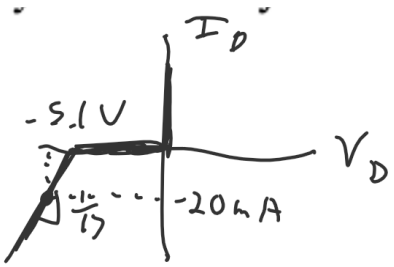


Figure 6

Laboratory Procedure:

The circuit shown in Figure 1 was built and specified by the values found in the previous section. In the first part of the lab, a load resistance of 240 Ohms and infinite resistance (which is just an open circuit) all with an R value of 340 Ohms was used, and the voltage source was varied between 12V and 17V to see how the output voltage changes. Then a source voltage of 17V will be used to vary the load

current by changing the load resistor from infinite resistance to 240 Ohms the output current and voltage were measured. After, the same process was done for 12V.

Data Collection:

Figure 7 shows the Vsource and Vout data for a load resistance of 240 Ohms and R value of 340 Ohms and Figure 8 shows the plot of that. Figure 9 shows the Vsource and Vout data for an infinite resistance (an open circuit where the load resistor area is) and Figure 10 shows the plot of that. Figure 11 shows the changing of RLoad for a Vsource of 17V to measure its Iout and Vout and Figure 12 is the plot of that. Then Figure 13 shows the changing of RLoad for a source of 12V to measure its Iout and Vout and Figure 14 is the plot of that.

V_{source} [V]	V_{OUT} [V]
12	4.781
13	5.09
14	5.1615
15	5.1885
16	5.205
17	5.216

Figure 7

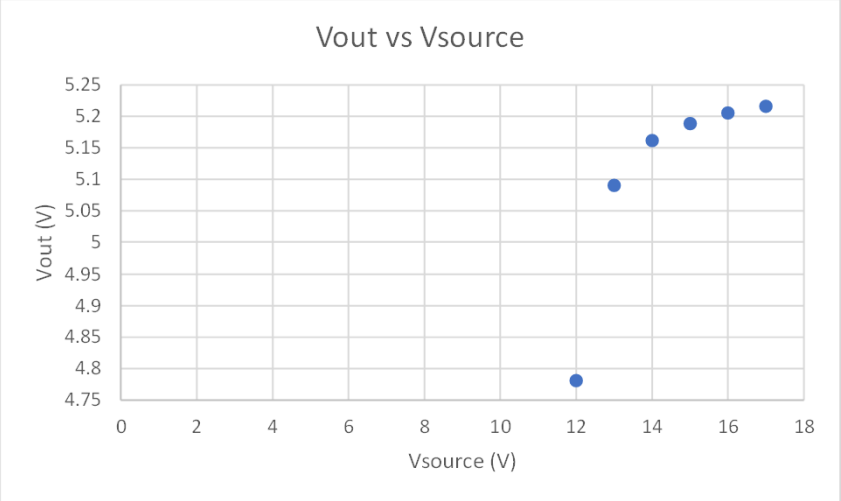


Figure 8

V_{source} [V]	V_{OUT} [V]
12	5.244
13	5.252
14	5.264
15	5.272
16	5.282
17	5.291

Figure 9

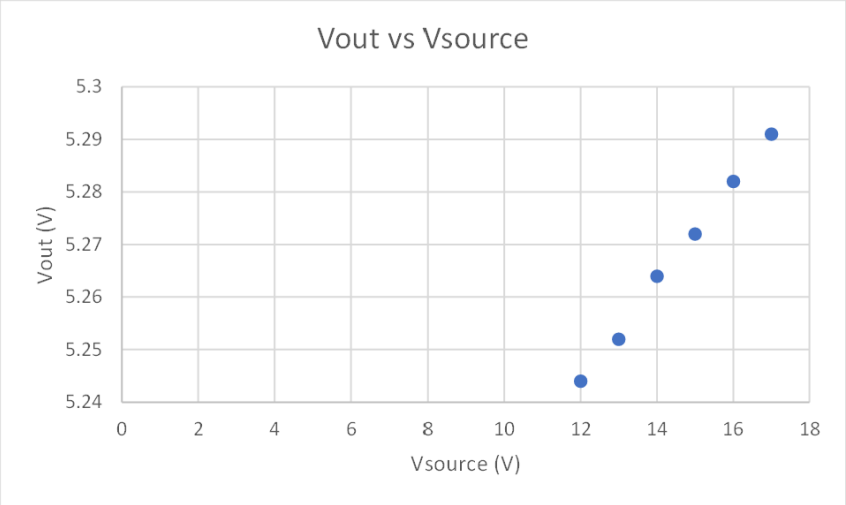


Figure 10

R_{LOAD} [Ω]	I_{OUT} [mA]	V_{OUT} [V]
∞	0	5.291
10000	0.536	5.283
2200	2.463	5.279
1000	5.340	5.269
240	20	4.781

Figure 11

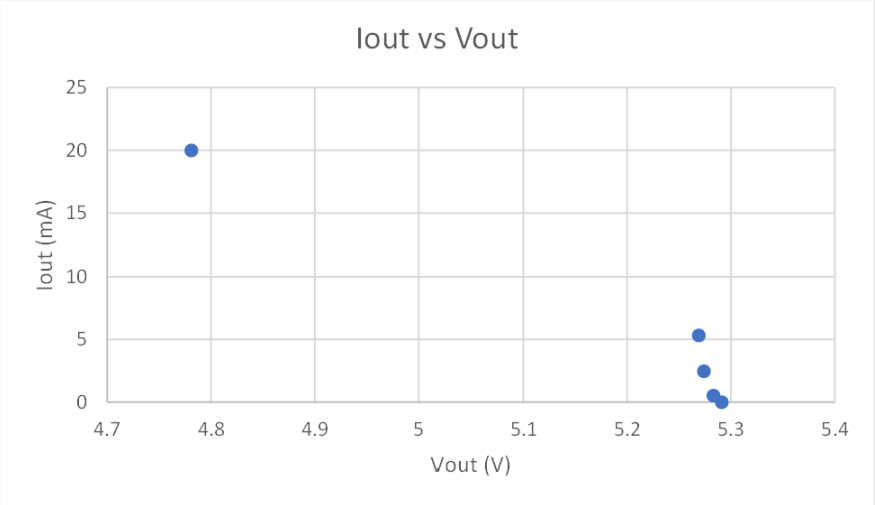


Figure 12

R_{LOAD} [Ω]	I_{OUT} [mA]	V_{OUT} [V]
∞	0	5.244
10000	0.530	5.264
2200	2.442	5.248
1000	5.288	5.241
240	22	5.216

Figure 13

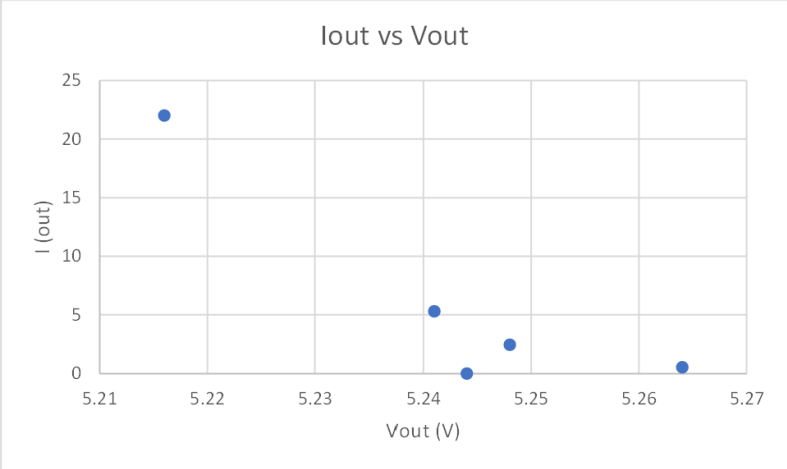


Figure 14

Data Analysis:

Figure 15 shows how to calculate the Line regulation and Figure 16 is the calculation of it from a Vsource of 15V and 14 V and its Vout in Figure 9. Figure 17 shows how to calculate the Load regulation and Figure 18 is the calculation of it from an RLoad of infinity and 240 Ohms and its Iout and Vout in Figure 13.

Line regulation ≡ ΔVout/ΔVsource ×100

Figure 15

$$\frac{5.272 - 5.264}{1} \cdot 100 = 0.8\%$$

Figure 16

Load regulation ≡ $|V_{out,noload} - V_{out,fullload}| / |I_{L,noload} - I_{L,fullload}| = |\Delta Vout| / |\Delta IL|$
LOAD REGULATION IS COMPUTED ASSUMING Vsource IS FIXED AT ITS MAX VALUE.

Figure 17

$$= \frac{|5.291 - 4.781|}{|10 - 0.020|} = 25.5\,\Omega$$

Figure 18

Summary and Interpretation of Result:

Overall this experiment showed how a Zener diode voltage regulator circuit indeed does keep a relatively constant voltage despite a varying Vsource and this effectiveness is shown in the calculated line regulation value. Also, the circuit is tested with different load resistance values and its effectiveness to regulate despite these changes is shown in the calculated load regulation value.

Lab 6: Designing a Power Supply (LTSPICE)

Theory:

Figure 1 shows how an AC voltage input gets its magnitude reduced with a power transformer. Then it goes through a diode rectifier to make the negative part of the voltage wave positive. That gets filtered by an in parallel capacitor and then the voltage ripples become constant through the voltage regulator. The circuit as a whole is how an AC signal gets converted to a DC one.

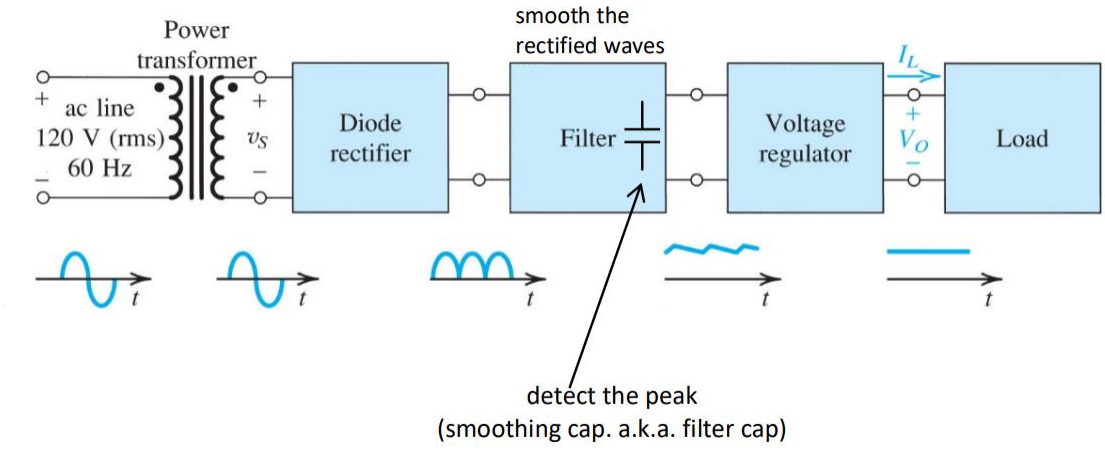


Figure 1

Analysis and Design:

Figure 2 shows how to build a Zener diode subcircuit and then you would transform that into SPICE directives to represent the model. Figure 3 shows how to build a transformer with inductors and SPICE directives. With that, Figure 4 shows how to calculate the needed two inductor values such that the voltage amplitude will be stepped down from 120 V to 12 V. Figure 5 shows the calculated capacitor value to get the desired 1V ripple and Figure 6 shows how to calculate the R resistance for the voltage regulator. All those calculated components are put together and shown in Figure 7.

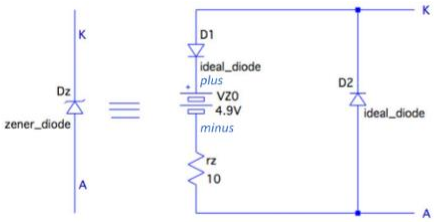
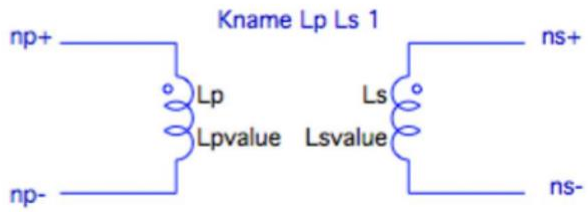


Figure 2



```
Lp np+ np- Lpvalue
Ls ns+ ns- Lsvalue
Kname Lp Ls 1
```

Figure 3

$$\frac{V_p}{V_s} = \frac{I_s}{I_p} = \frac{N_p}{N_s} = \sqrt{\frac{L_p}{L_s}}$$

$$\frac{120}{12} = \sqrt{\frac{L_p}{L_s}}$$

$$\frac{10}{1} = \sqrt{\frac{L_p}{L_s}}$$

$$\frac{L_p}{L_s} = \frac{100\ mH}{1\ mH}$$

Figure 4

$$R_L C = \frac{(V_m - V_R/2)}{V_R} \cdot T$$

$$R_L C = \frac{12 - \frac{1}{2}}{1} \cdot \frac{1}{60}$$

$$R_L C = 0.2$$

IF $R_L = 200\ \Omega$ $C = 1mF$

Figure 5

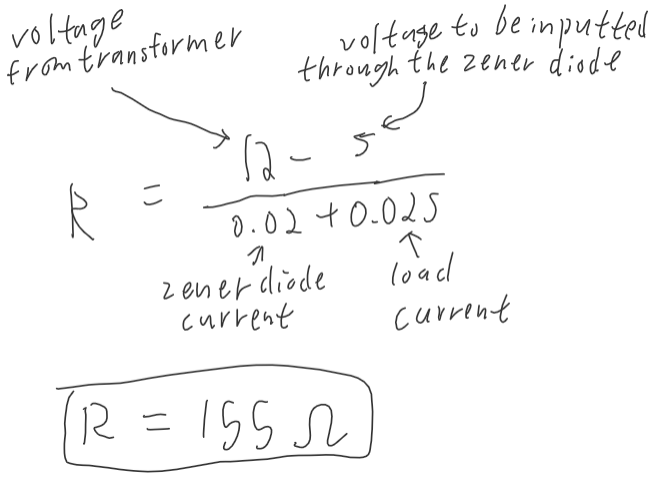


Figure 6

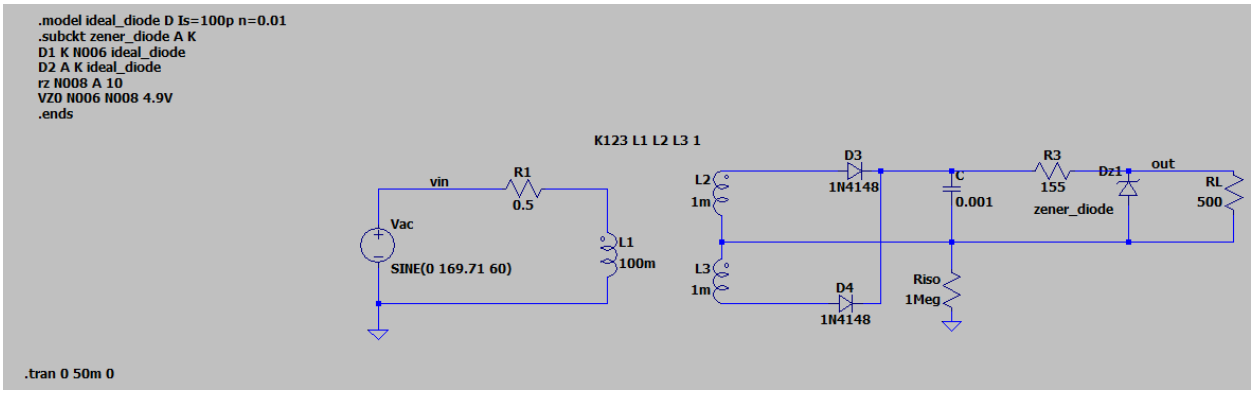


Figure 7

Laboratory Procedure:

Trans analysis was used to simulate input for a certain amount of time and this input and the resulting output were then measured in this amount of time.

Data Collection:

Figure 8 shows the output waveform for RL = 200 Ohms, Figure 9 shows the output waveform for RL = 250 Ohms, and Figure 10 shows the output waveform for RL = 500 Ohms.

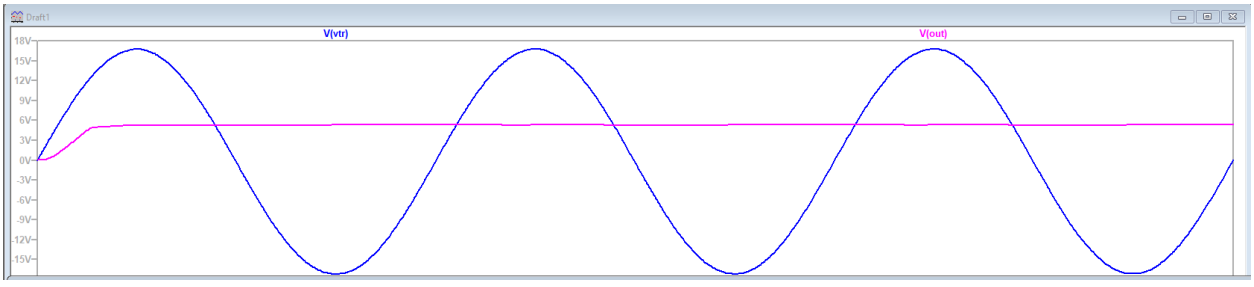


Figure 8

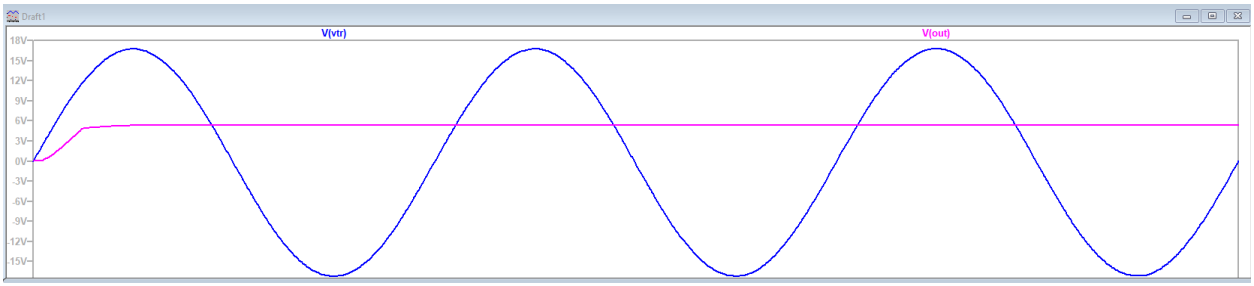


Figure 9

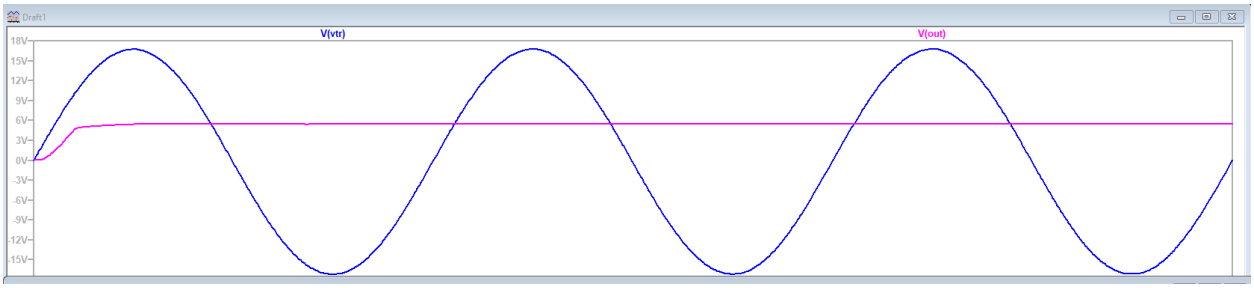


Figure 10

Data Analysis:

If the load gets shorted the system will not get damaged. This is because the voltage will be constant, not rippling, but the voltage will not be regulated as the diode is in the reverse region now, as most of the current flows through the short.

Summary and Interpretation of Result:

Overall, this experiment shows how to model a DC power supply in LTSpice and how to calculate component values for the desired behavior.

Lab 7: Characterizing the 2N7000 nMOST in your kit (Hardware)

Theory:

Figure 1 shows how the voltage across the gate and source of a MOSFET transistor relates to the current through its drain when in saturation mode. Then Figure 2 Shows the pinouts of a 2N7000 transistor.

$$ID\_n \approx 0.5\ K\_n\ (VGS\_n - Vth\_n)^2$$

Figure 1

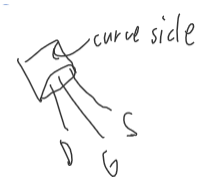


Figure 2

Analysis and Design:

Figure 3 shows what values the threshold voltage could be between and the resulting average voltage. Also in that figure, the average voltage, the equation from Figure 1, and a VGS value of 4 V, and an ID value of 0.5 A are all used to calculate Kn. Figure 4 shows how to calculate VTHn and Kn through two sets of measurements. Then in Figure 5 is shown the circuit that will be built. With that, Figure 6 shows calculations for what VGS values to use for measurements. For calculating ID = (VDD – VDS)/R, VDS is chosen to be 6V and 8V for the transistor to be in the saturation (not the triode region or too high such that it could clip), and R is chosen such that ID will not be too large but large enough to allow VGS to be larger than VTH. Although the calculations led to a VGS around 2.2 V, 2.4V and 2.3V, which are around those values, were decided to be used instead.

0.8 V ≤ Vth_n ≤ 3.0 V

Vth_n (avg) = 1.9 V

K_n = 0.23 A/V²

$0.5 = 0.5\ K_n (4 - 1.9)^2$

Figure 3

$$I_{D\_n1} = 0.5\,k_n (V_{GS\_n1} - V_{th\_n})^2$$
$$I_{D\_n2} = 0.5\,k_n (V_{GS\_n2} - V_{th\_n})^2$$
$$\frac{(V_{GS\_n1} - V_{th\_n})^2}{I_{D\_n1}} = \frac{(V_{GS\_n2} - V_{th\_n})^2}{I_{D\_n2}}$$
$$\frac{V_{GS\_n1} - V_{th\_n}}{\sqrt{I_{D\_n1}}} = \frac{V_{GS\_n2} - V_{th\_n}}{\sqrt{I_{D\_n2}}}$$
$$\frac{V_{GS\_n1}}{\sqrt{I_{D\_n1}}} - \frac{V_{th\_n}}{\sqrt{I_{D\_n1}}} = \frac{V_{GS\_n2}}{\sqrt{I_{D\_n2}}} - \frac{V_{th\_n}}{\sqrt{I_{D\_n2}}}$$
$$\frac{V_{GS\_n1}}{\sqrt{I_{D\_n1}}} - \frac{V_{GS\_n2}}{\sqrt{I_{D\_n2}}} = \frac{V_{th\_n}}{\sqrt{I_{D\_n1}}} - \frac{V_{th\_n}}{\sqrt{I_{D\_n2}}}$$
$$V_{th\_n} = \frac{\frac{V_{GS\_n1}}{\sqrt{I_{D\_n1}}} - \frac{V_{GS\_n2}}{\sqrt{I_{D\_n2}}}}{\left(\frac{1}{\sqrt{I_{D\_n1}}} - \frac{1}{\sqrt{I_{D\_n2}}}\right)}$$
$$k_n = \frac{I_{D\_n1}}{0.5\,(V_{GS\_n1} - V_{th\_n})^2}$$

Figure 4

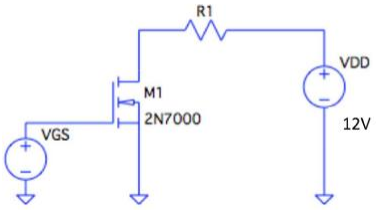


Figure 5

$$I_D = \frac{12 - 6}{470}$$
$$\downarrow$$
$$0.013 = 0.5 \cdot 0.23 (V_{GS} - 1.9)^2$$
$$V_{GS} = \sqrt{\frac{0.13}{0.5 \cdot 0.23}} + 1.9$$
$$V_{GS} = 2.2\,V$$
$$0.0085 = 0.5 \cdot 0.23 (V_{GS} - 1.9)^2$$
$$V_{GS} = 2.2\,V$$

Figure 6

Laboratory Procedure:

The calculated VGS values above are used in the circuit in Figure 5 and then the resulting VDS and ID values will be measured.

Data Collection:

Figure 7 shows the VGS and R1 values used and the measured VDS and ID values.

Measurement #1:

VGS = 2.4 V

R1 = 470 Ω

VDS = 8.3 V

ID = 7.3mA

Measurement #2:

VGS = 2.3 V

R1 = 470 Ω

VDS = 10.2 V

ID = 3.8mA

Figure 7

Data Analysis:

Figure 8 shows the calculations from the values found in Figure 7 and the equations in Figure 4. Figure 9 shows how these calculated values compare with these values from the datasheet.

$$V_{th\_n} = \frac{\frac{2.4}{\sqrt{0.0073}} - \frac{2.3}{\sqrt{0.0038}}}{\frac{1}{\sqrt{0.0073}} - \frac{1}{\sqrt{0.0038}}}$$

$$V_{th\_n} = 2.04\,V$$

$$k_n = \frac{0.0073}{0.5(2.4-2.04)^2}$$

$$k_n = 0.11$$

Figure 8

Parameter	*Estimated [units]*	*Data Sheet [units]*	*% Error*
K_n	0.11	0.23	−52.2
Vth_n	2.04	1.9	7.4

Figure 9

Summary and Interpretation of Result:

This experiment showed how physically a circuit operates in the saturation region and the calculated Vthn and Kn values will be used in a future transistor experiment.

Lab 8 - Designing and Analyzing a MOS based Amplifier (LTSPICE)

Theory:

To operate an NMOS transistor in the saturation region for amplification purposes constant VGS and VDS values must be applied such that VGS > VTH and VDS > VGS – VTH.

Analysis and Design:

Figure 1 shows the circuit to be built in LTSpice. With that, Figure 2 shows how to calculate the operating ID, VDS, and VGS values for a given RD value and given transistor parameters, in Figure 3. Also, Figure 4 shows the Spice directive used to set parameters for the transistor. After that, Figure 5 shows how gm, ro, and Av will be calculated.

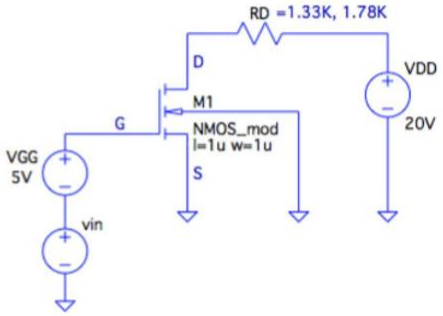


Figure 1. nMOST amplifier

a. RD=1.33KΩ

ID,Q = 9mA $= \frac{\beta}{2}(V_{GS}-V_{TH})^2 = \frac{0.002}{2}(5-2)^2$

VDS,Q = 8.03 V $= 20 - 11.97$

VGS,Q = 5V $0.009 \cdot 1330$

b. RD=1.78KΩ

ID,Q = 9mA

VDS,Q = 3.98V $= 20 - 0.009 \cdot 1780$

VGS,Q = 5V

Figure 2

Vth=2V and $\beta = \mu$ Cox W/L = 2mA/V².

Figure 3

.MODEL MOS. NMOS NMOS(kp = 20m, Vto = 2, lambda = 0)

Figure 4

Symbolic expression for gm: $\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$

Symbolic expression for ro: $\frac{1}{\lambda I_{DS}}$ cause $\lambda = 0.01$

Symbolic expression for Av: $A_V = -g_m(r_o \,//\, R_D)$

Figure 5

Laboratory Procedure:

In this lab ID vs VD plots based on different lambda values were created and load lines were drawn for different values of RD. After that, the Spice directive ".op" will be used to find the operating point VGS, VDS, and ID, and also gm, ro, and Av. Lastly, a triangle wave will be inputted with a 5 V DC voltage at the gate to see its output voltage with the different values of RD.

Data Collection:

Figure 6 is the ID vs VD plot for lambda=0 and Figure 7 is the plot for lambda=0.01V^-1. Figure 8 shows the load lines for RD values of 1.78 kOhms (red curve) and 1.33 kOhms (green curve). After that, Figure 9 shows the operation point values for VGS, VDS, and ID. With those values, Figure 10 shows the calculated gm, ro, and Av values compared to the Spice found values in Figure 11. Figure 12 and Figure 13 show the output voltage for RD values of 1.33 kOhms and 1.78 kOhms respectively.

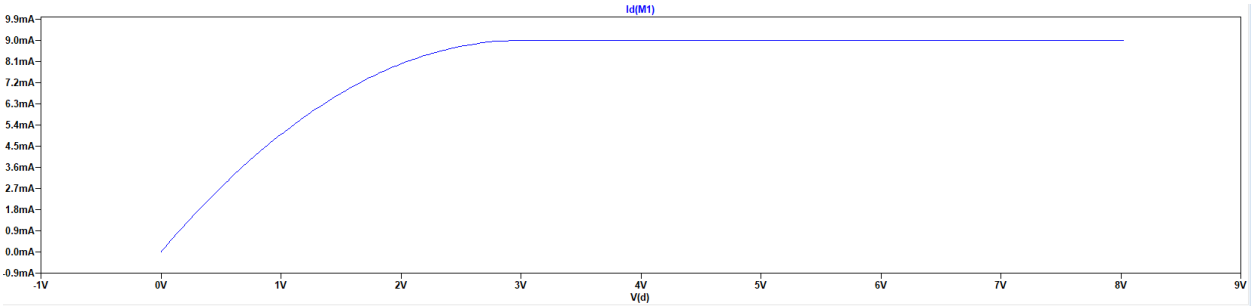


Figure 6

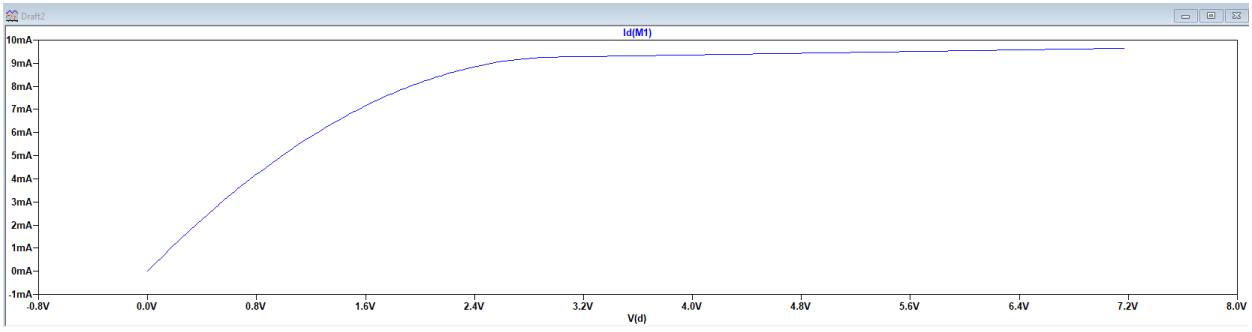


Figure 7

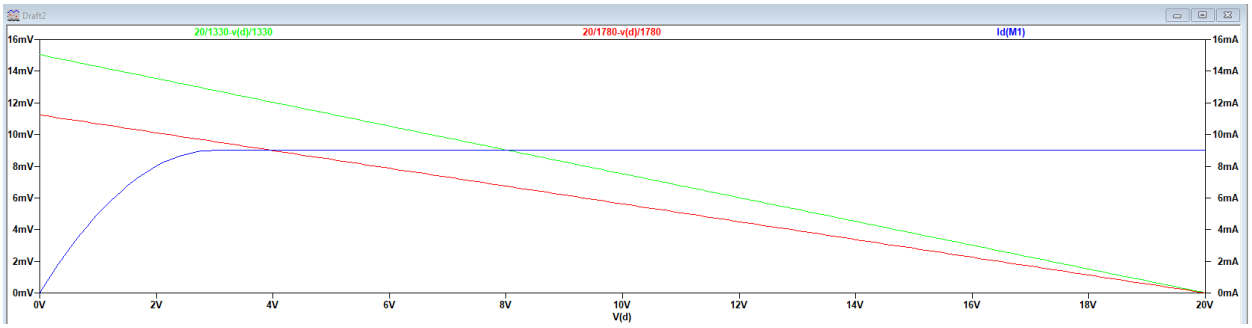


Figure 8

		Q_1 (R_D=1.33KΩ)	Q_2 (R_D=1.78KΩ)
VGS,Q	=	5 V	5 V
VDS,Q	=	8.03 V	3.98
ID,Q	=	9mA	9mA

Figure 9

		Q_1 (R_D=1.33KΩ)	Q_2 (R_D=1.78KΩ)
gm	=	0.006 Ω⁻¹	0.006 Ω⁻¹
ro	=	11 ‖ 11 Ω	11 ‖ 11 Ω
Av	=	7.13	9.21

Figure 10

		Q_1 (R_D=1.33KΩ)	Q_2 (R_D=1.78KΩ)
gm	=	0.00643 Ω⁻¹	0.00621 Ω⁻¹
ro	=	10 362.69 Ω	10 741.14 Ω
Av	=	7.638	9.521

Figure 11

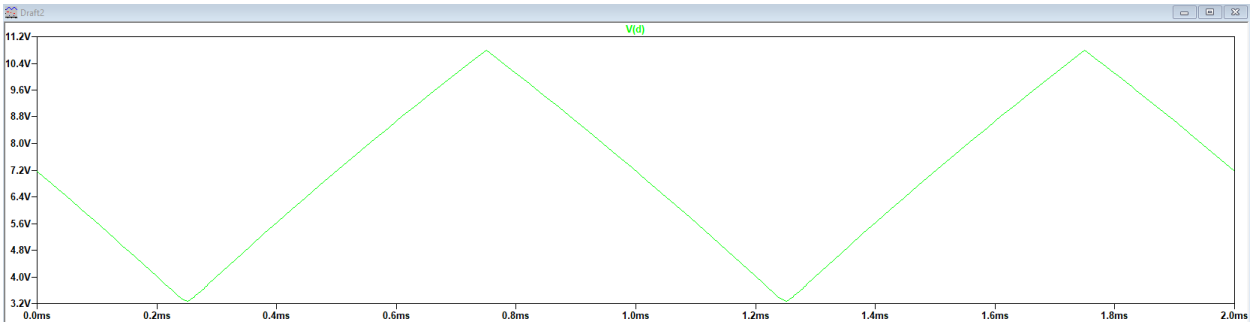


Figure 12

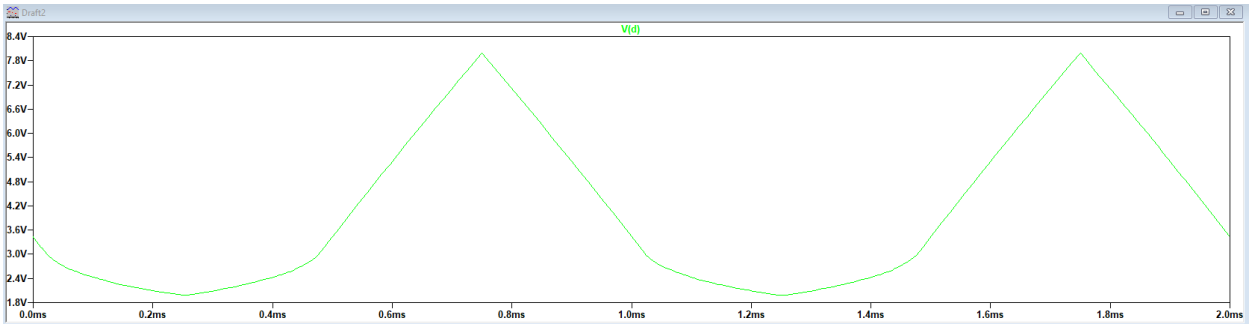


Figure 13

Data Analysis:

As shown in Figure 8 the MOST operation mode will be saturation at the location of the DC operating point if the drain resistance RD is 1.33 kOhms however if the drain resistance is increased to 1.78 kOhms then the MOST operation mode will be in triode.

As shown in Figure 12 for RD as 1.33 kOhms, the operation mode is in saturation and thus the signal will be amplified. However, in Figure 13 for RD as 1.78 kOhms the operation mode is in triode and thus the MOSFET will act as a resistor and attenuate the signal.

Summary and Interpretation of Result:

This experiment showed how a lambda value can add a slope to the saturation region of an ID vs VD plot of a transistor. Also how to find the operating point and corresponding transistor parameters for different RD values. Then those RD values are used to show the voltage amplification for saturation and attenuation for triode.

Lab 9: Designing and building common source stages (with and w/o degeneration)

Theory:

Figure 1 shows a common source amplifier with biasing. R1 and R2 lessen the biasing voltage from VDD, RS makes the system robust against process and temperature variations as it is allowing feedback, and the big capacitors make it such that the biasing voltage and current will not go across it unless a small signal is applied to keep the circuit biased.

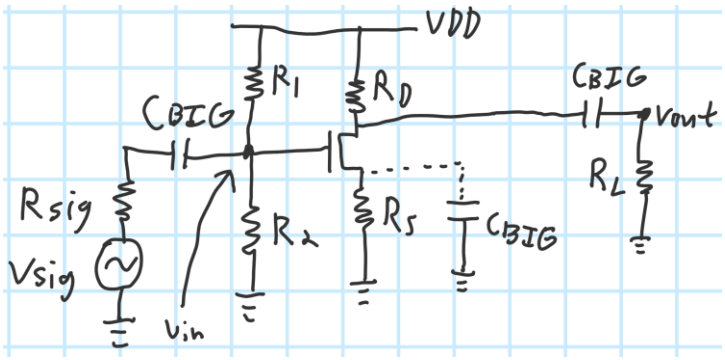


Figure 1

Analysis and Design:

Figure 2 shows the bias circuit that will be built, and Figure 3 shows the component and transistor (2N7000) parameter values for the circuit with ID=7mA, VD=8V, VS=1V, and how the gate resistors (R1 and R2) should be larger than RS by at least a factor of 10. With that, Figure 4 shows the completed circuit in LTSpice. Figure 5 shows the "complete" circuit of the CS amplifier in both configurations (with a capacitor across RS and without a capacitor across RS). Figure 6 shows the AC small-signal circuit without a bypass capacitor across RS and Figure 7 is with.

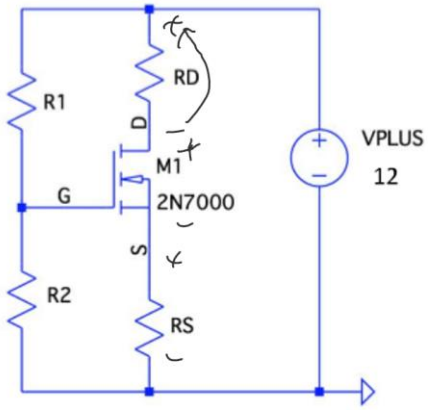


Figure 2

VTH = 2.04 V

β = 0.11 A/V^2

VDSAT = VGS – VTH = 0.35 V

VGS = 2.39 V

R1 = 10kΩ

R2 = 3.9kΩ

RD = 570Ω

RS = 150Ω

gm = 0.0385 Ω^{-1}

Figure 3

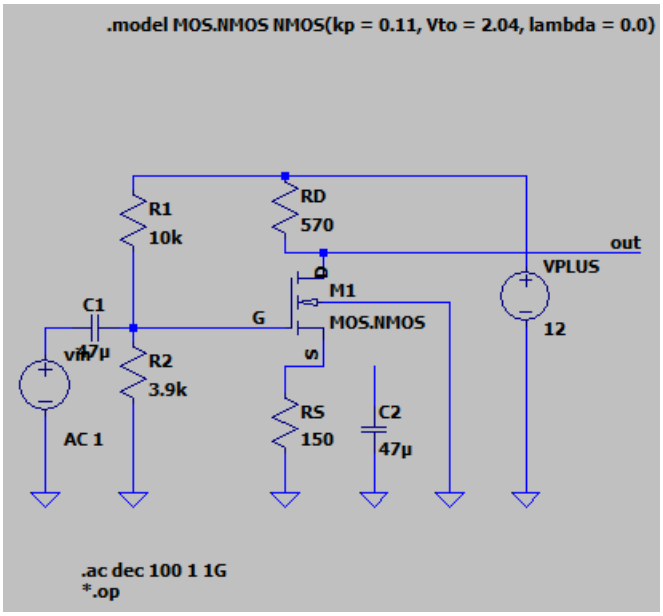


Figure 4

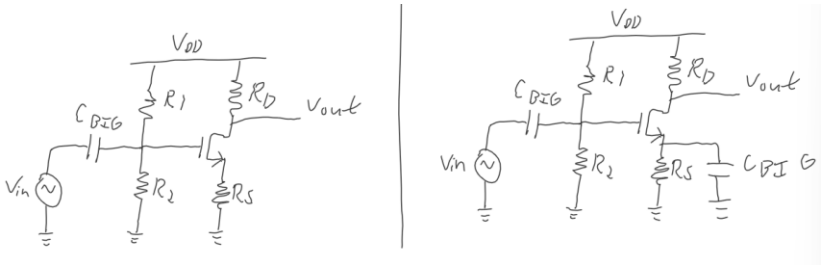


Figure 5

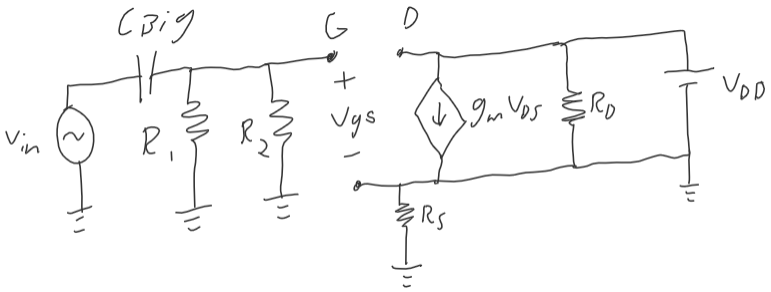


Figure 6

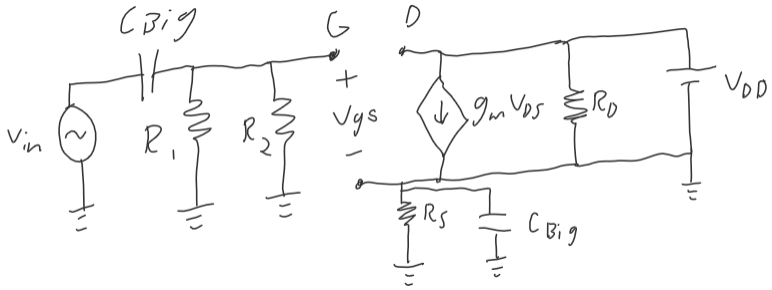


Figure 7

Laboratory Procedure:

The circuits in Figure 4 will be built in LTSpice and then will go through ".ac" analysis to measure the gain and ".op" analysis to find the biasing values: ID, VGS, VTH, and gm. Also, the calculated gains, found by the equations in Figure 8, were compared to the simulated values. After all that, the physical circuit was built, and its biasing values were measured. Then an AC signal will be applied to the gate (through a large coupling capacitor) to make a Bode Plot from 100Hz to 10MHz using the network analyzer tool.

$$\text{AV (w/o bypass cap)} = \frac{g_m R_D}{1 + g_m R_S}$$

$$\text{AV (w bypass cap)} = g_m R_D$$

Figure 8

Data Collection:

Figure 9 shows the theoretical and simulated gain and how they compare, and Figure 10 is the result from the ".op" analysis for the biasing values. This is with Figure 11 as the Bode Plot for the CS without a bypass cap across RS (Gain in dB = 10.1) and Figure 12 with a bypass cap (Gain in dB = 26.7). After all this, the bias circuit is built physically and all the measured node voltages (VD, VG, and VS) and used resistor values are shown in Figure 13. Then based on the measurements the computed gm of the

transistor is 0.0385 Ohms^-1. Figure 14 shows the Bode Plot of the Network Analyzer for the circuit without the large capacitor across RS and Figure 15 shows the Bode Plot with the capacitor.

Configuration	Theoretical Gain (Hand calculation)	Simulated Gain (SPICE)	% Error
CS w/o bypass cap across RS	3.2	3.2	0
CS w bypass across RS	21.9	21.7	-0.9

Figure 9

Parameter	SPICE	Hand Calculation
Id	0.08655 A	0.007 A
Vgs	2.38 V	2.39 V
Vds	7.29 V	7 V
Vth	2.04 V	2.04 V
Gm	0.0379 Ω^{-1}	0.0385 Ω^{-1}

Figure 10

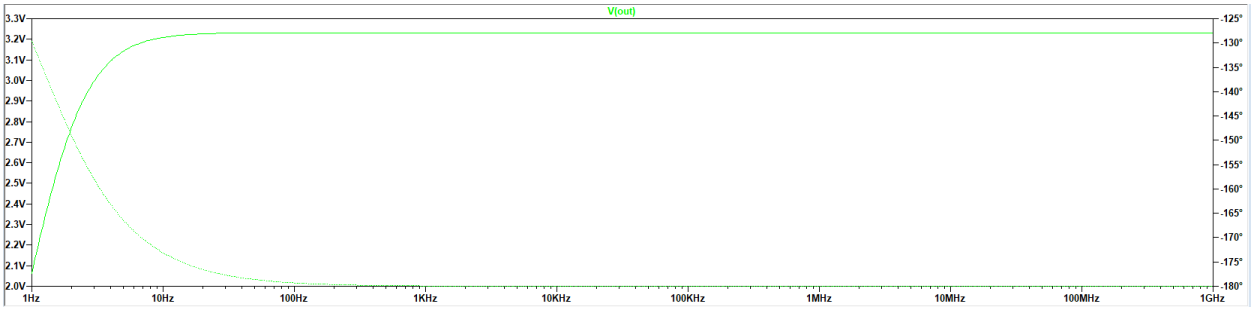


Figure 11

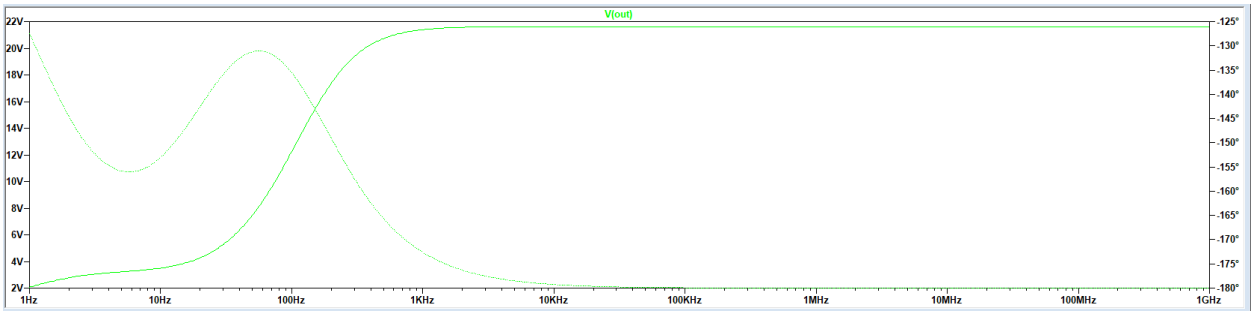


Figure 12

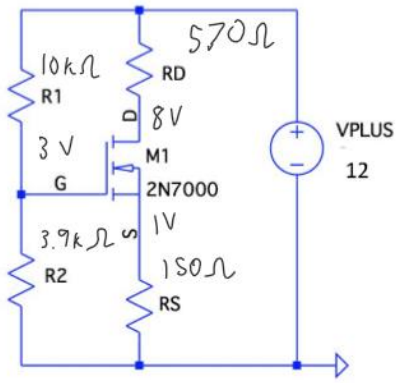


Figure 13

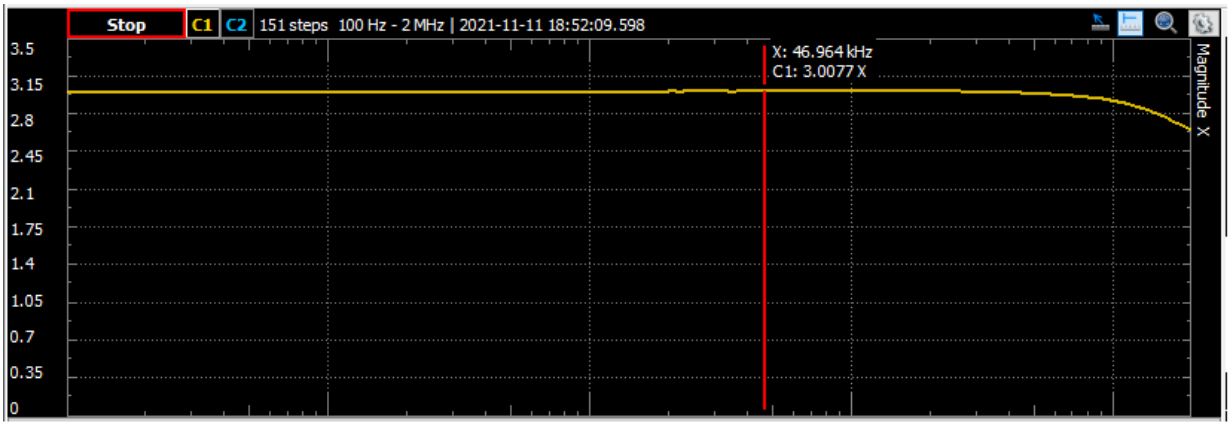


Figure 14

Figure 15

Data Analysis:

In Figure 14 the amplitude output did not get clipped however the frequency cannot be too high. Therefore the bandwidth can be measured before this drop in amplitude. Lastly, for Figure 15 a 100mV amplitude wave had to be applied as in the previous attempts it was too high and thus the output would get clipped. Because the frequency cannot be too low or high, the two bandwidth values were measured where the gain is around constant.

Summary and Interpretation of Result:

This experiment taught how to build a MOSFET amplifier circuit in simulation and physically to be able to bias it and measure gain in both. Some difficulties encountered with the physical circuit were how there had to be prevention of clipping when running the network analyzer and how a large capacitor had to be put where vout is measured. Overall though the physical gain does somewhat match the theoretical and simulated gain but is different probably due to the transistor not having the parameters expected and component values not exactly being what they are expected to be.