Single Cycle CPU Design

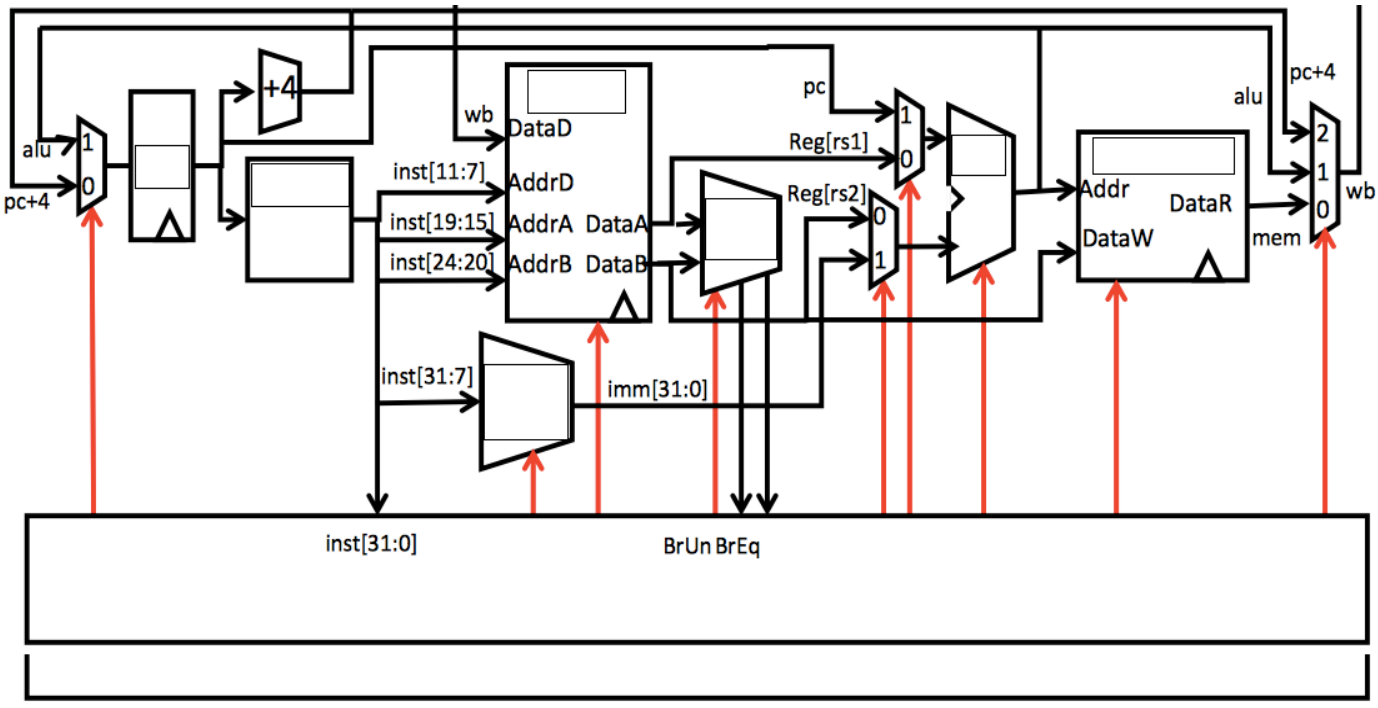
Here we have a single cycle CPU diagram. Answer the following questions:

1. Name each component.

2. Name each datapath stage and explain its functionality.

Stage	Functionality

3. Provide data inputs and control signals to the next PC logic.



Single Cycle CPU Control Logic

Fill out the values for the control signals from the previous CPU diagram.

Instrs.	Control Signals									
	BrEq	PCSel	ImmSel	BrUn	ASel	BSel	ALUSel	MemRW	RegWEn	WBSel
add										
ori										
lw										
sw										
beq										
jal										

(Put an X if the signal doesn't matter)

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers.

Single Cycle CPU Performance Analysis

The delays of circuit elements are given as follows:

Stage	IF	ID	EX	MEM	WB
Delay	200	100	200	200	100

1. Mark the stages the following instructions use and calculate the time to execute.

Instruction	IF	ID	EX	MEM	WB	Total
add						
lw						
sw						
xori						
beq						
jal						

2. Which instruction(s) exercises the critical path?

3. What is the fastest you could clock this single-cycle datapath?

4. Why is a single cycle CPU inefficient?

5. How can you improve its performance? What is the purpose of pipelining?