Elena Corpuz

1. i. a. add
   ii. b. PC + 4
   iii. c. bits 00_2
   iv. b. bne
   v. d. WB

2. Reg Dst: 1
   Reg Write: 1
   ALU Src: 0
   Mem Read: 1
   Mem Write: 0
   Mem to Reg: 1

   Read Reg 1: $t2
   Read Reg 2: $t1
   Write Reg: $t1

3. 50% = P Not Taken
   25% = bL state

   each choice has 2 options

   1e ~~total~~ options

   accuracy 33 %.

4. i. RAW: I1(I1 + I2)
RAR: I1 + I3
WAR: I3
WAW: I1 I4

ii.
add
sw
lw ← hazard
nop
add

* = Hazard

iii.
add
sw
nop
lw
nop
add

5.

#	address	H/M	set 0	set 0	set 1	set 2	set 2	set 3	set 3
0	0	M	M[0]						
1	8	M	M[0]						
2	0	H			M[1]				
3	6	M	M[0]						
4	7	M	M[0]						
5	2	M	M[0]						
6	6	H			M[1]				
7	10	M	M[0]						
8	11	M	M[0]						
9	3	M	M[0]						

6. $32 - 16 - 4 = 12$

7. miss rate of instruction 5%
miss rate of data 2%

CPI = 2 w/o stalls
200 cycles for all penalties

$CPI_{stall} / CPI_{perfect}$

How much faster?

1 penalty = +200 cycles

frequency = 30%

2% faster b/c the miss rate in the cache is already 2% thus if we lose this it increase our speed

miss 2 × 200 = +400 cycles to total
miss 5 × 200 = +1000 cycles to total

When we start missing our cycles also go down which result in the faster processor

Ultimately
- 7% miss rate
+ CPI (more)
- cycles b/c no penalties

8. final TLB

#	Valid	tag	#Page
0	1	6	3
1	0	4	9
2	1	3	6
3	1	2	7

$2^{10} \cdot 4$

1

1024

4

4096

mod

final Page table

#	Valid	Page / DISK
0	1	6
1	1	5
2	0	DISK
3	0	DISK
4		
5	1	8
6	0	DISK
7	1	10
8	1	3
9	0	DISK
10	1	12
11	0	DISK
12	0	DISK
	1	13