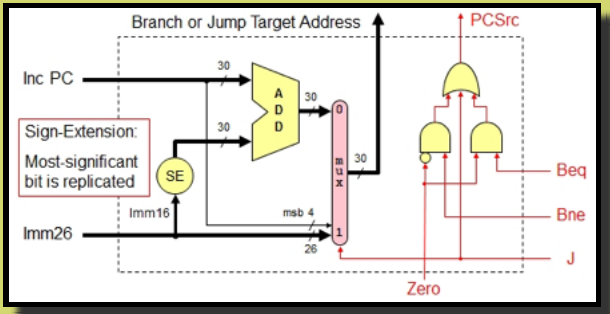
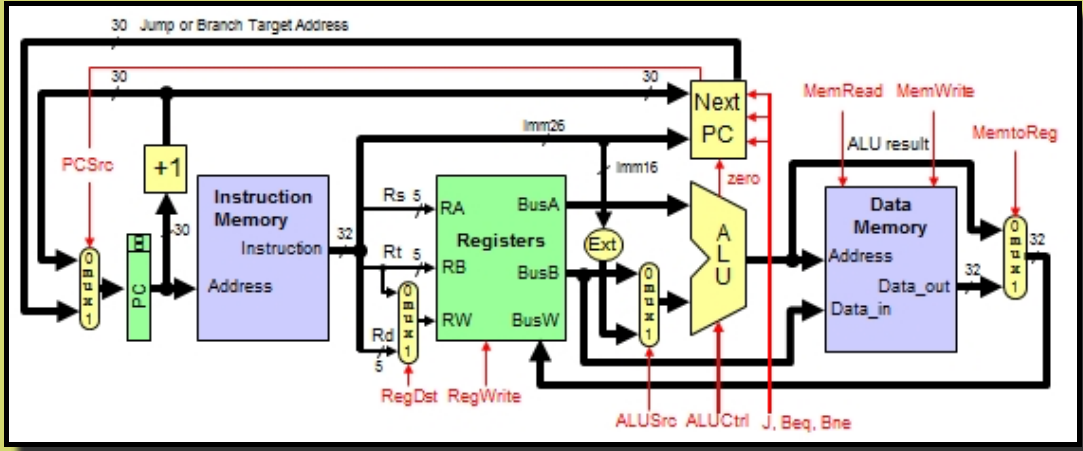


Due date: On or before Monday, April 27, 2020
Absolutely no copying others’ works

Name: _____

- The purpose of homeworks is for students to practice for the exams without others’ help, so the penalty of mistakes will be minor.
- Without practicing for the exams properly, students would not be able to do well on the exams.

- Use the figures in slides, instead of the textbook, to answer the questions in this homework.
- The following figures are from the Slide [12.10](#) and will be used in this homework:



I. Problems in this homework assume that logic blocks needed to implement a processor’s datapath have the following latencies (time needed to do their work):

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend
180 ps	60 ps	30 ps	110 ps	110 ps	240 ps	10 ps

[†]Note that the block “Shift-Left-2” is dropped since it is used in the textbook, but not in the slides.

1. (06%) If the only thing we need to do in a processor is fetch consecutive instruction as shown in the middle figure in the Slide [11.8](#), what would the cycle time be?

[†]Hint: The cycle time is the time for the critical (longest-latency) path.

2. (23%) Consider a datapath similar to the one in the figures in the Slide [12.10](#), but for a processor that only has one type of instruction: unconditional PC-relative branch. What would the cycle time be for this (single-cycle) datapath?

[†]Comment: Unconditional PC-relative branch is a branch without using the register files and is always taken.

[‡]Comment: Jump is a J-type instruction and unconditional PC-relative branch is an I-type one.

[§]Hint: The cycle time is the time for the critical (longest-latency) path.

3. (23%) Repeat the previous question, but this time we need to support only conditional PC-relative branches.

[†]Hint: The cycle time is the time for the critical (longest-latency) path.

4. (06%) Which kinds of instructions require the logic block (or resource), (immediate/sign) extender, in the datapath?

5. (06%) For which kinds of instructions (if any) is the (immediate/sign) extender on the critical (longest-latency) path?

6. (20%) Assuming that we only support bne and add instructions, discuss how changes in the given latency of the (immediate/sign) extender affect the cycle time of the processor. Assume that the latencies of other resources do not change.

II. For the problems in this exercise, assume that there are no pipeline stalls and that the breakdown of executed instructions is as follows:

add	addi	not	beq	lw	sw
25%	10%	0%	30%	20%	15%

[†]Hint: This is single-cycle implementation. That is each instruction finishes its execution in one clock cycle.

1. (06%) In what fraction of all cycles is the data memory used?

2. (10%) In what fraction of all cycles is the input of the sign-extend circuit needed? What is this circuit doing in cycles in which its input is not needed?