THE CMS HGCAL DETECTOR FOR HL-LHC UPGRADE

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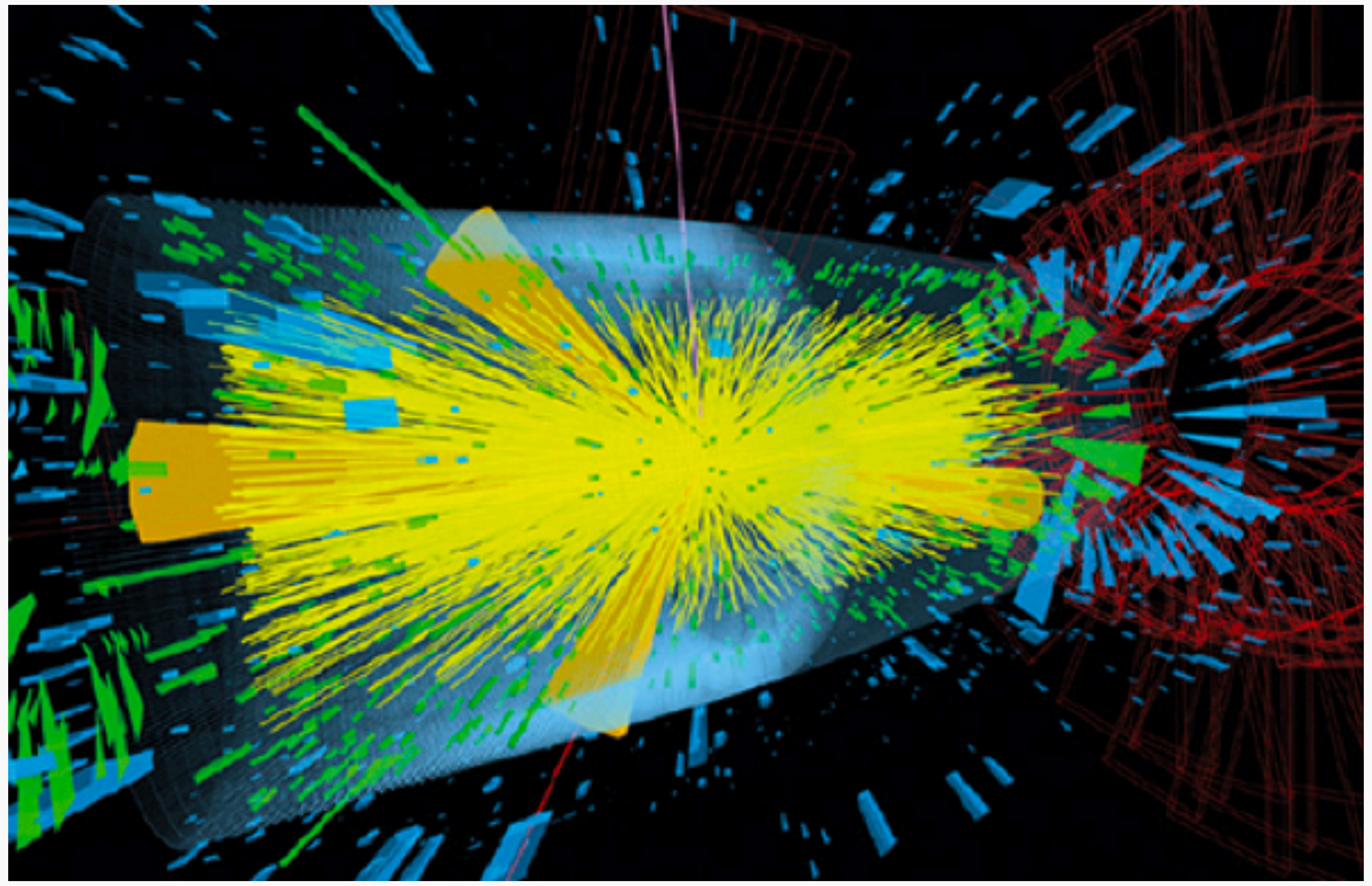
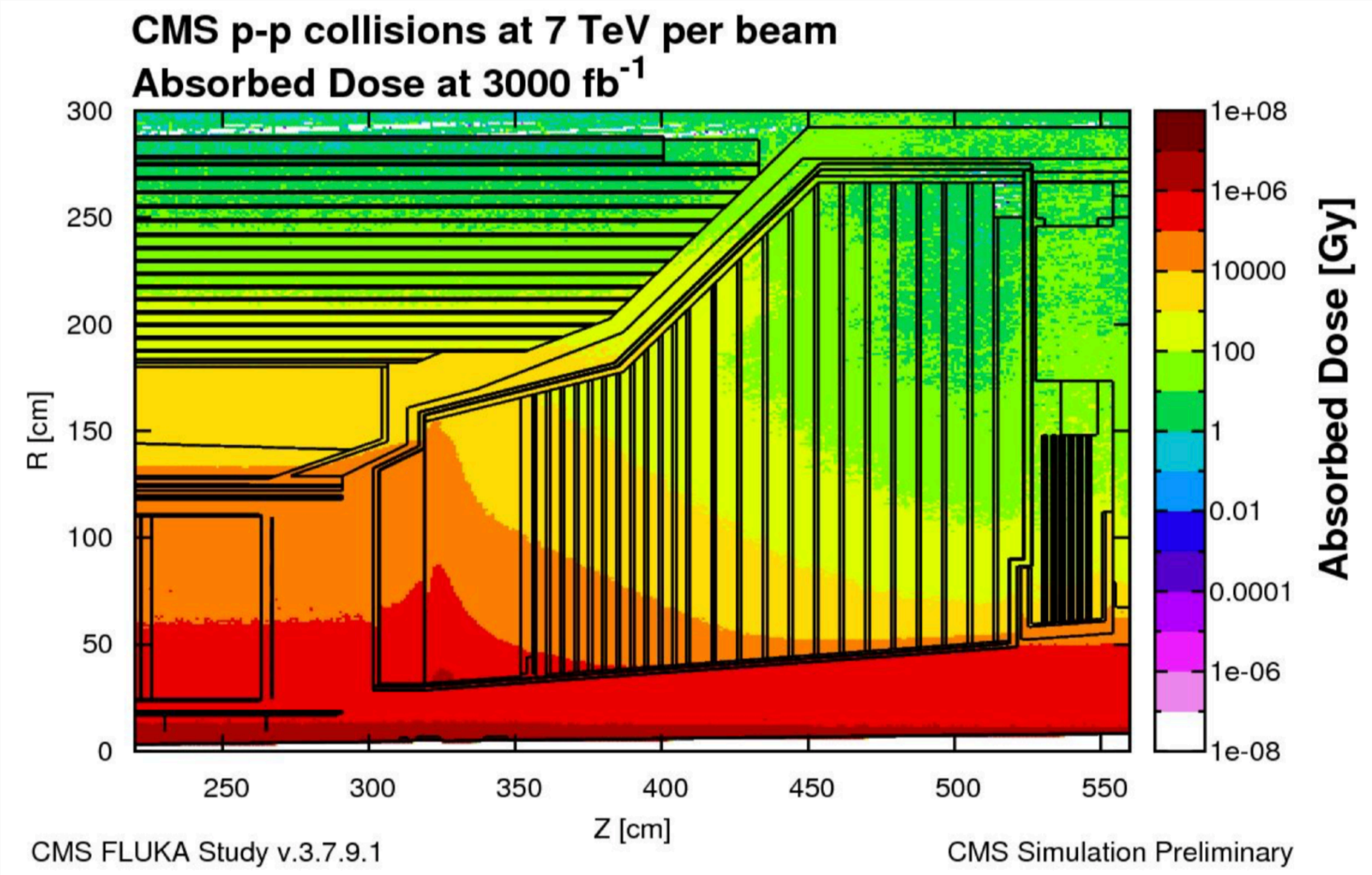
on behalf of the CMS Collaboration

CMS CALORIMETER ENDCAP FOR THE HL-LHC



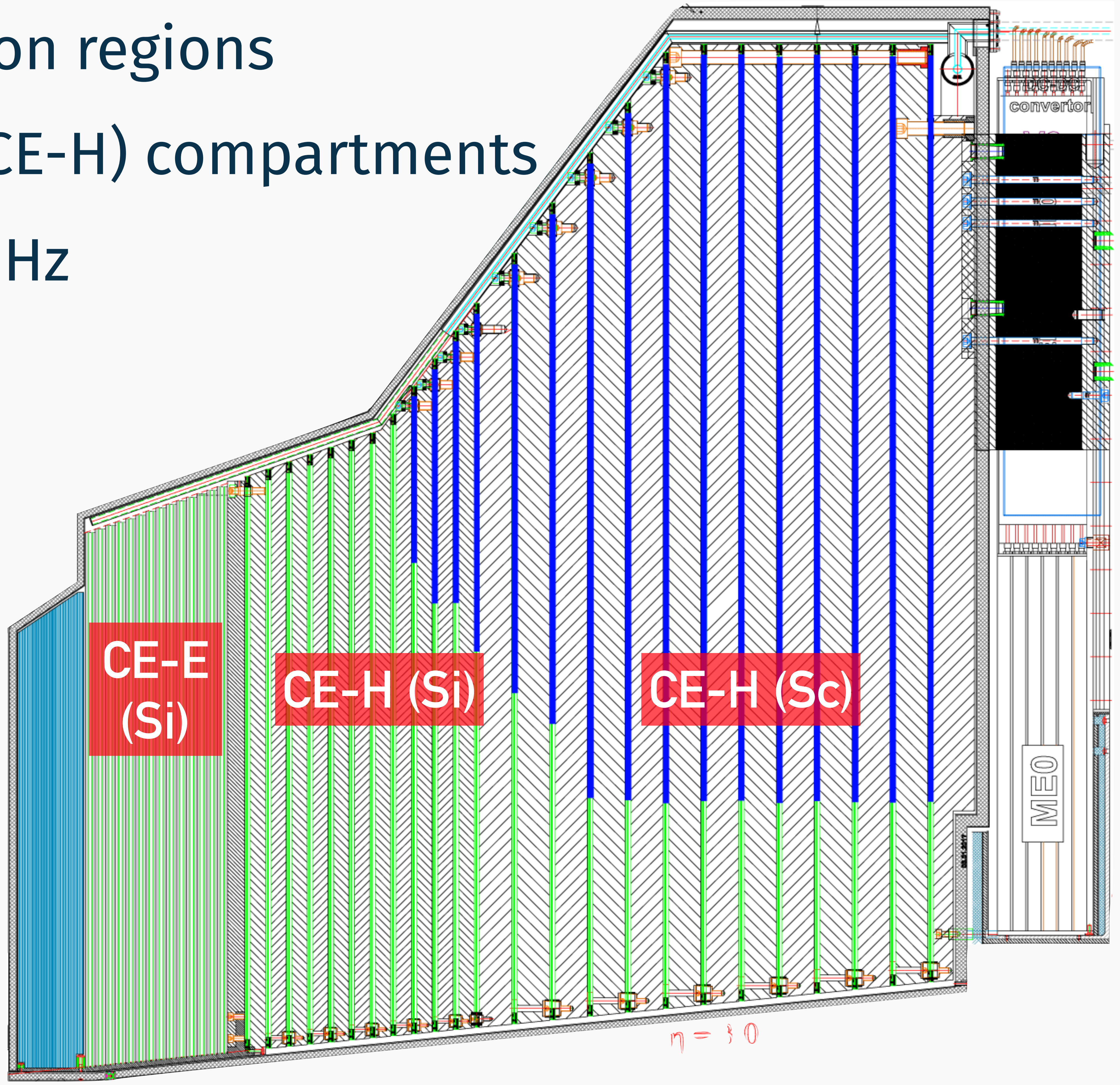


- CMS Phase-2 Upgrades are required to cope with the HL-LHC demanding environment of high radiation levels and large pileup <200> PU
- Current endcap calorimeters will need to be replaced
  - Preserve or even improve sensitivity in the interesting and busy forward region for VBS/VBF
  - The High Granularity Calorimeter (HGCAL) will become the new Calorimeter Endcap (CE):
    - Radiation hard technology based on a mix of silicon and scintillator detectors
    - High transverse and longitudinal granularity + timing (5D!) for enhanced particle flow reconstruction and ID/pileup mitigation

THE CMS HIGH GRANULARITY CALORIMETER

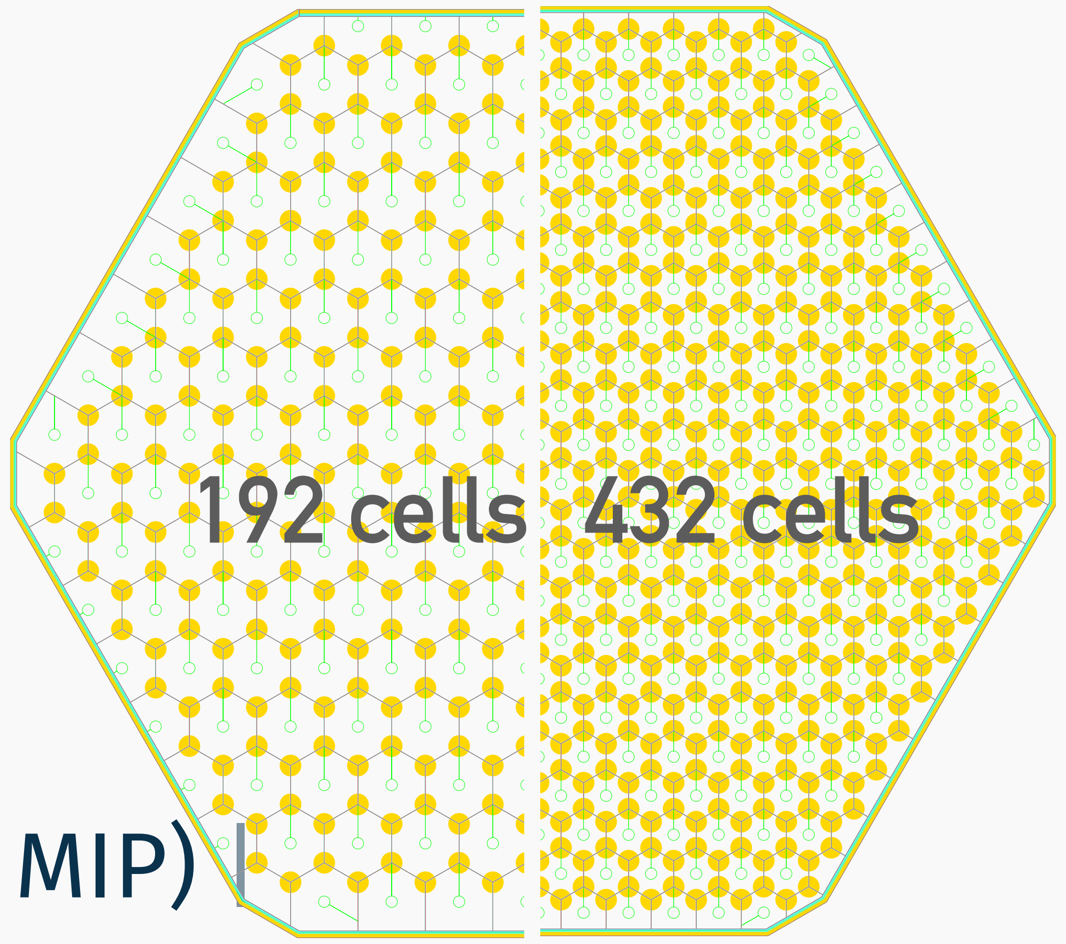
- The high luminosity and high granularity are a big challenge for the detector design:
  - Silicon/scintillator detectors in the high/low radiation regions
  - 28 layers in the ECAL (CE-E) + 24 layers in the HCAL (CE-H) compartments
  - Triggering and reading data of >6M channels at 40 MHz

Endcap coverage: $1.5 < \lvert\eta\rvert < 3.0$		
Total	Silicon sensors	Scintillator
Area	600 m²	500 m²
Number of modules	27 000	4 000
Cell size	0.5 — 1 cm²	4 — 30 cm²
N of channels	6 000 000	400 000
Power	Total at end of HL-LHC: ~180 kW @ -30°C	

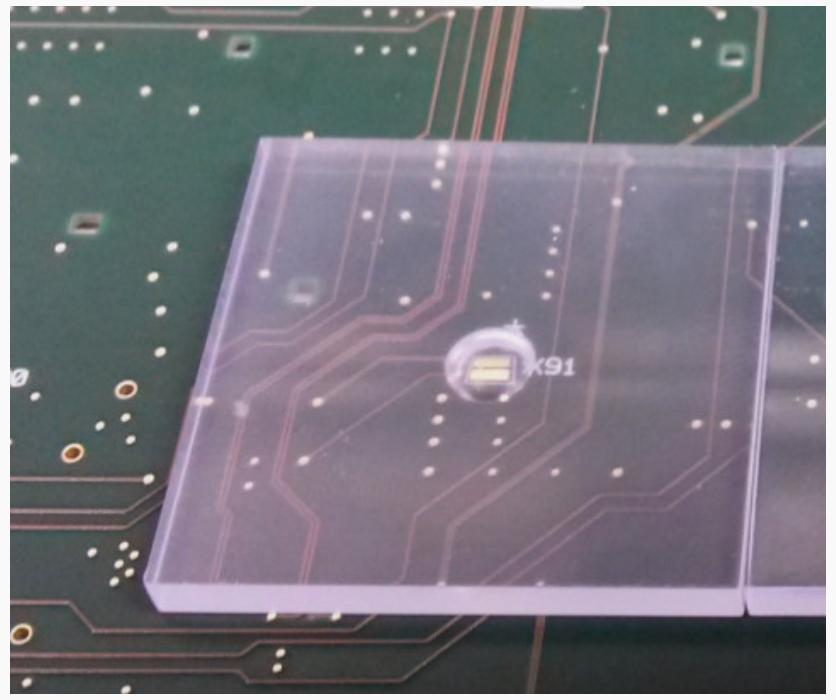


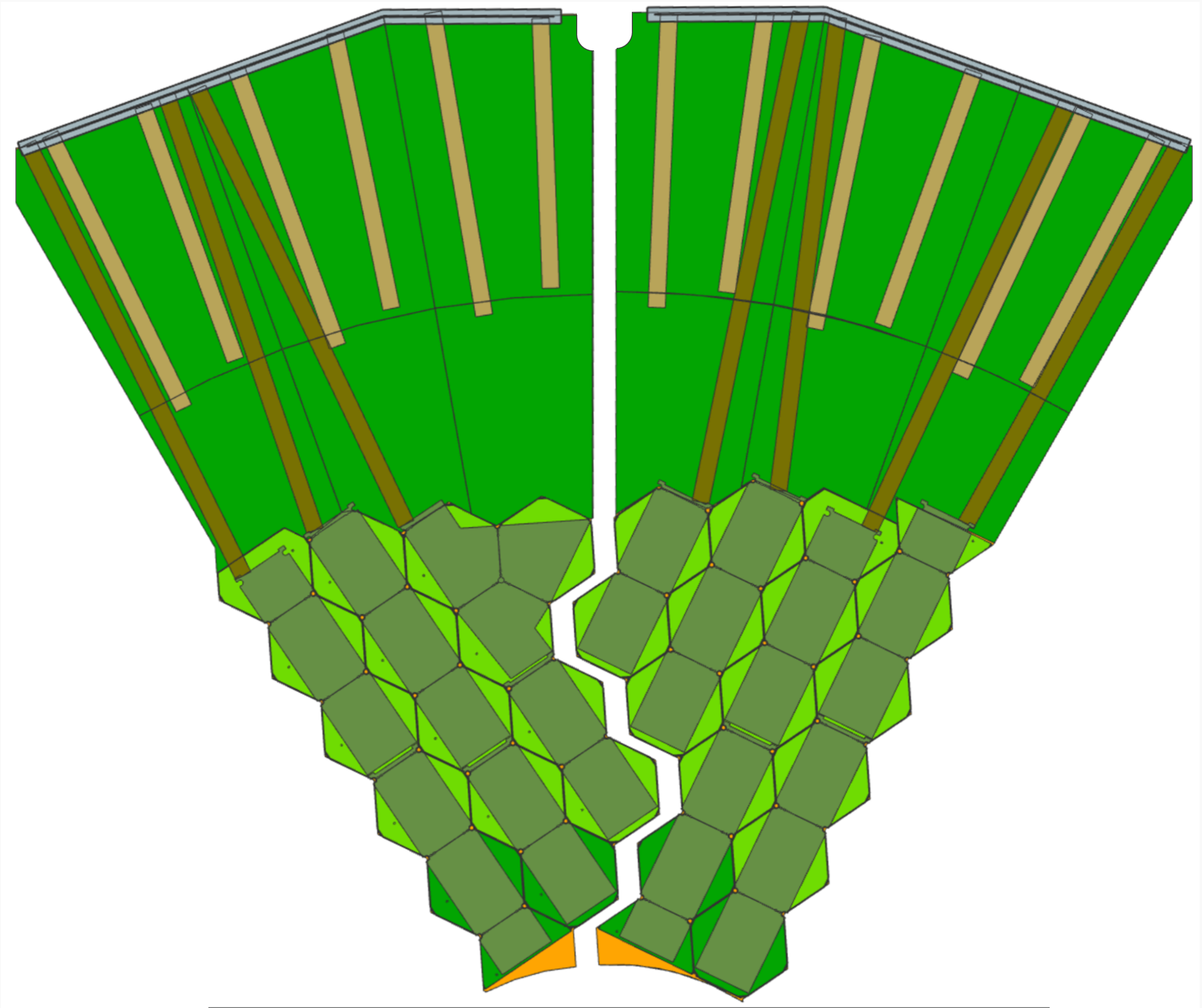
KEY INGREDIENTS OF HGCAL

- Active elements:
  - 8” hexagonal silicon wafers p/n-type | thickness: 120/200/300 um | 192/432 cells | HV bias up to 1kV
  - SiPM-on-tile scintillator readout (à la CALICE AHCAL)
- Electronics:
  - Front-End ASIC: rad. hard | low noise | high dynamic range (1-1000 MIP) | timing measurement | < 15 mW/ch consumption
    - High range with low power due to time-over-threshold (TOT)
    - Time-of-arrival (TOA) method with time precision of 20 ps
  - Trigger data from ASICs (300 TB/s) fed through concentrators to the back-end system (2 TB/s) in multi-stage approach
- Engineering:
  - 30º/60º cassettes tiled with hexagonal silicon modules and partially mixed with scintillator tile boards
  - Full detector volume cooled to -30ºC



Silicon sensors

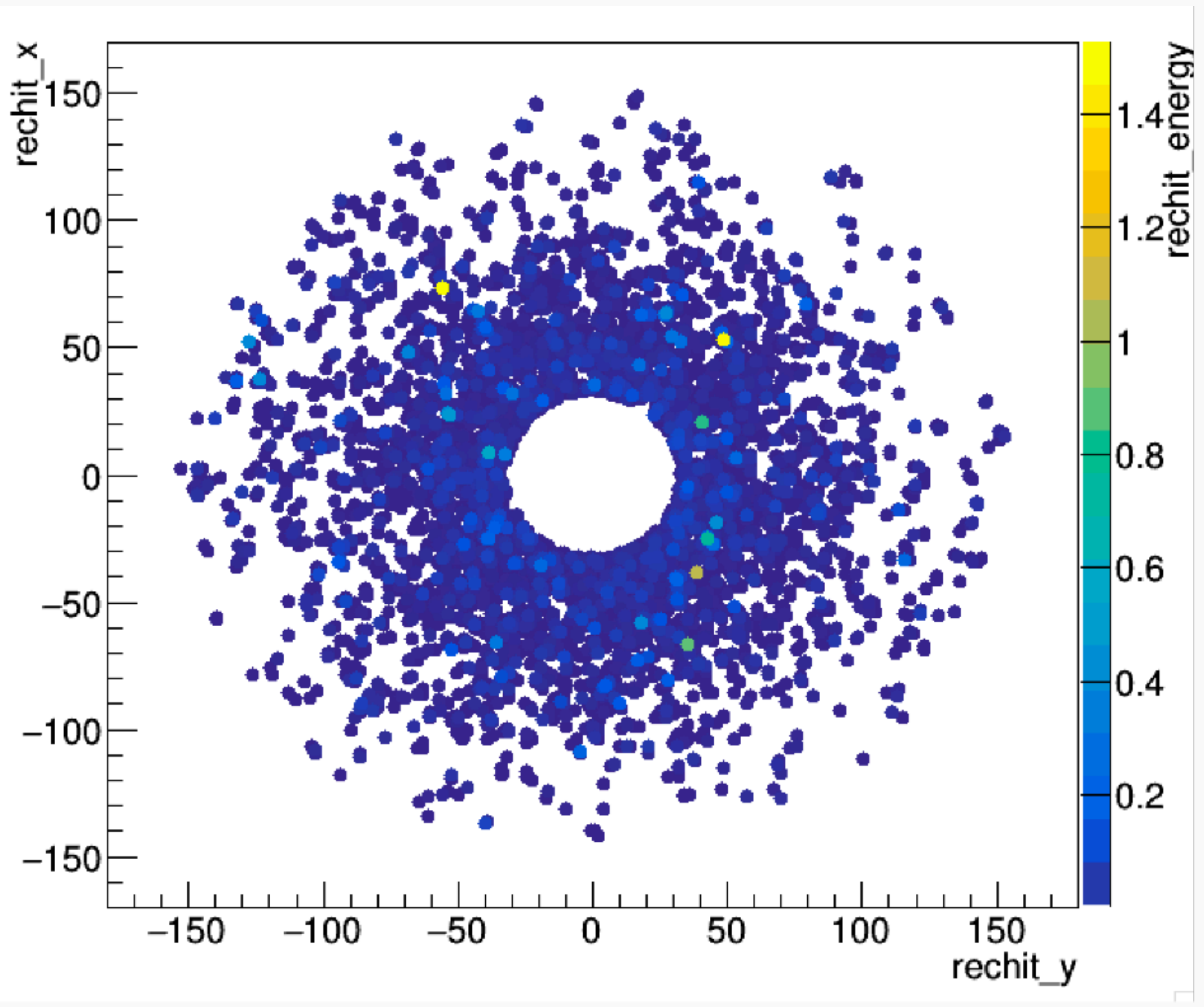

SiPM-on-tile (AHCAL)


Si+Sci mixed cassette

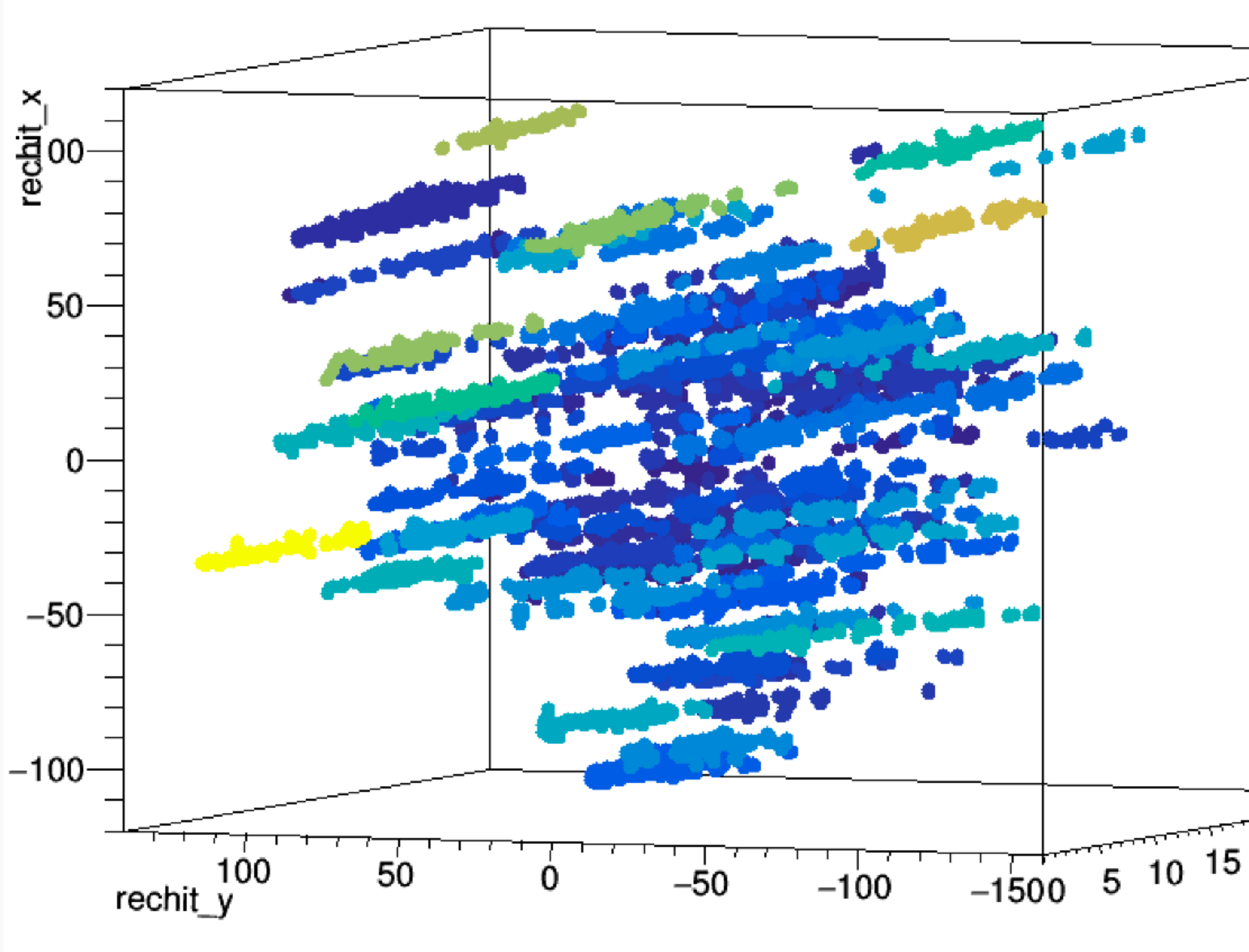
PHYSICS PERFORMANCE

PHYSICS PERFORMANCE

- The high occupancy and pileup are both big challenges for the particle reconstruction
  - But HGCAL is an 5D imaging calorimeter: 3D position, energy and time
    - ➤ Ultimate detector to perform Particle Flow
- The very first step is the clustering of the hits. Currently, the clustering is done in two steps:
  - 2D clustering in every layer using an energy density-based imaging algorithm
  - 3D clustering in an IP-pointing cylinder
- Great opportunity for novel tracking, clustering and imaging techniques as DBSCAN and CNNs!



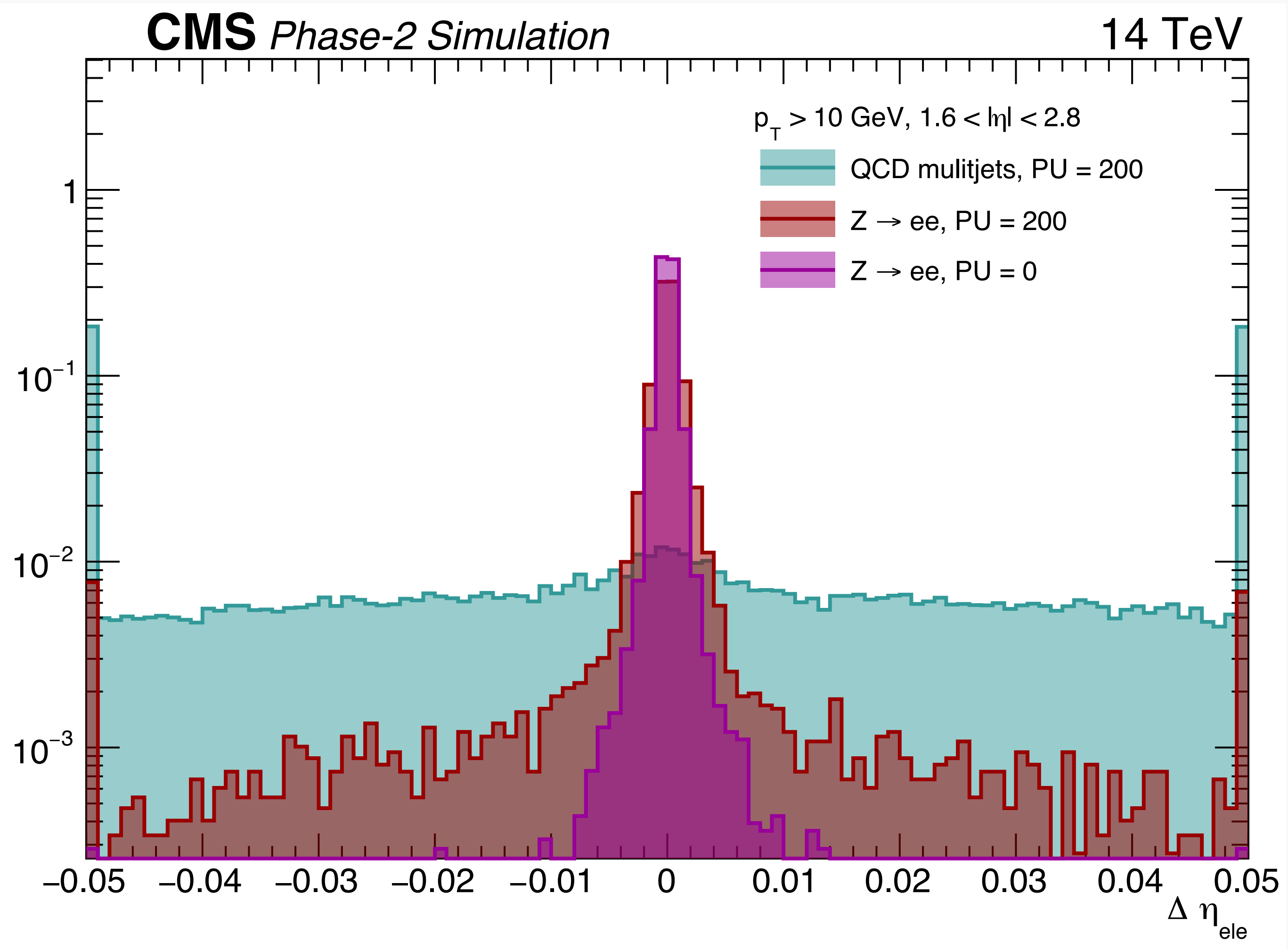
All hits in layer 1 for a 200 PU event



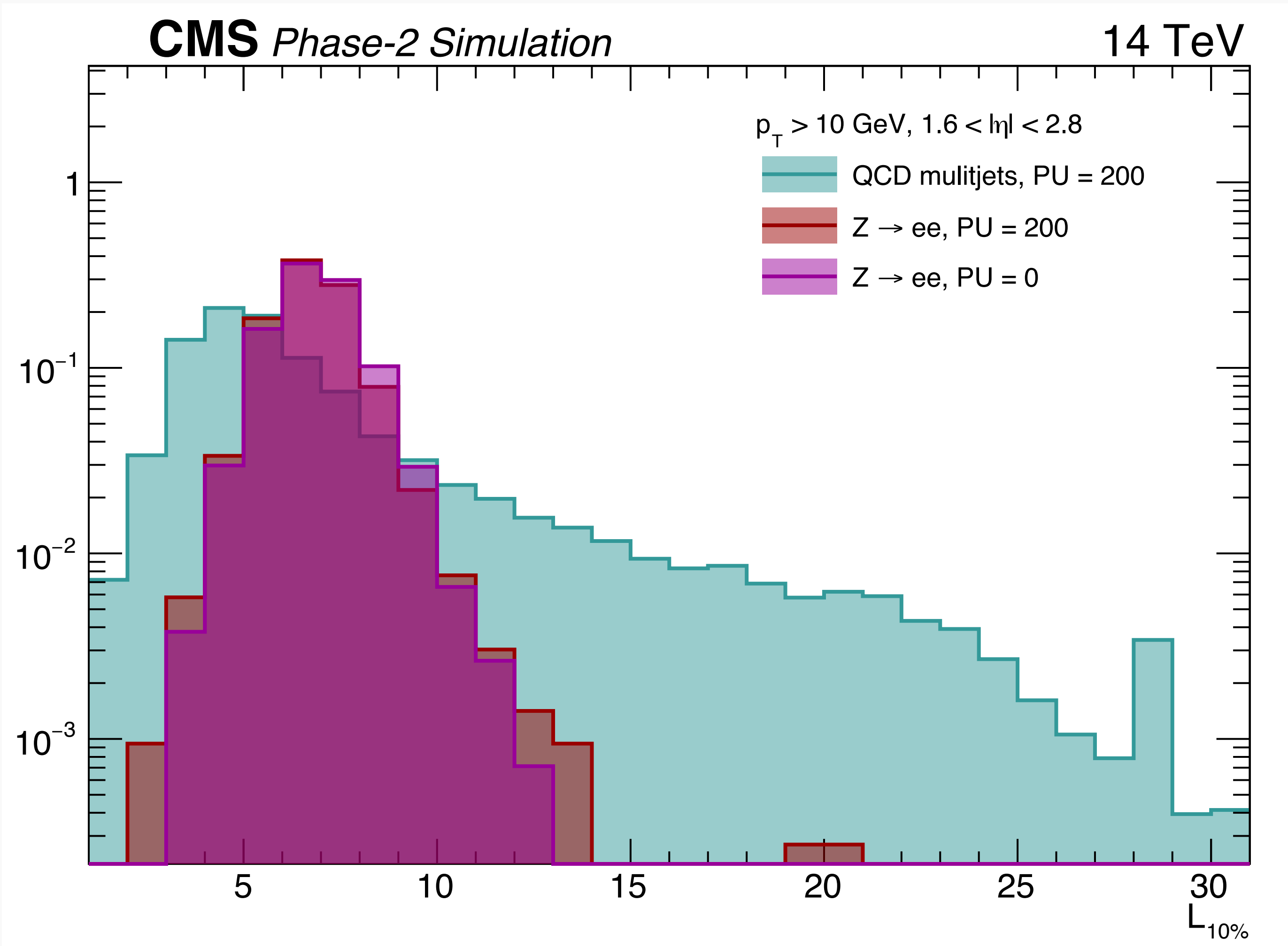
Clustered hits for clusters with pt > 1 GeV

ELECTRON IDENTIFICATION

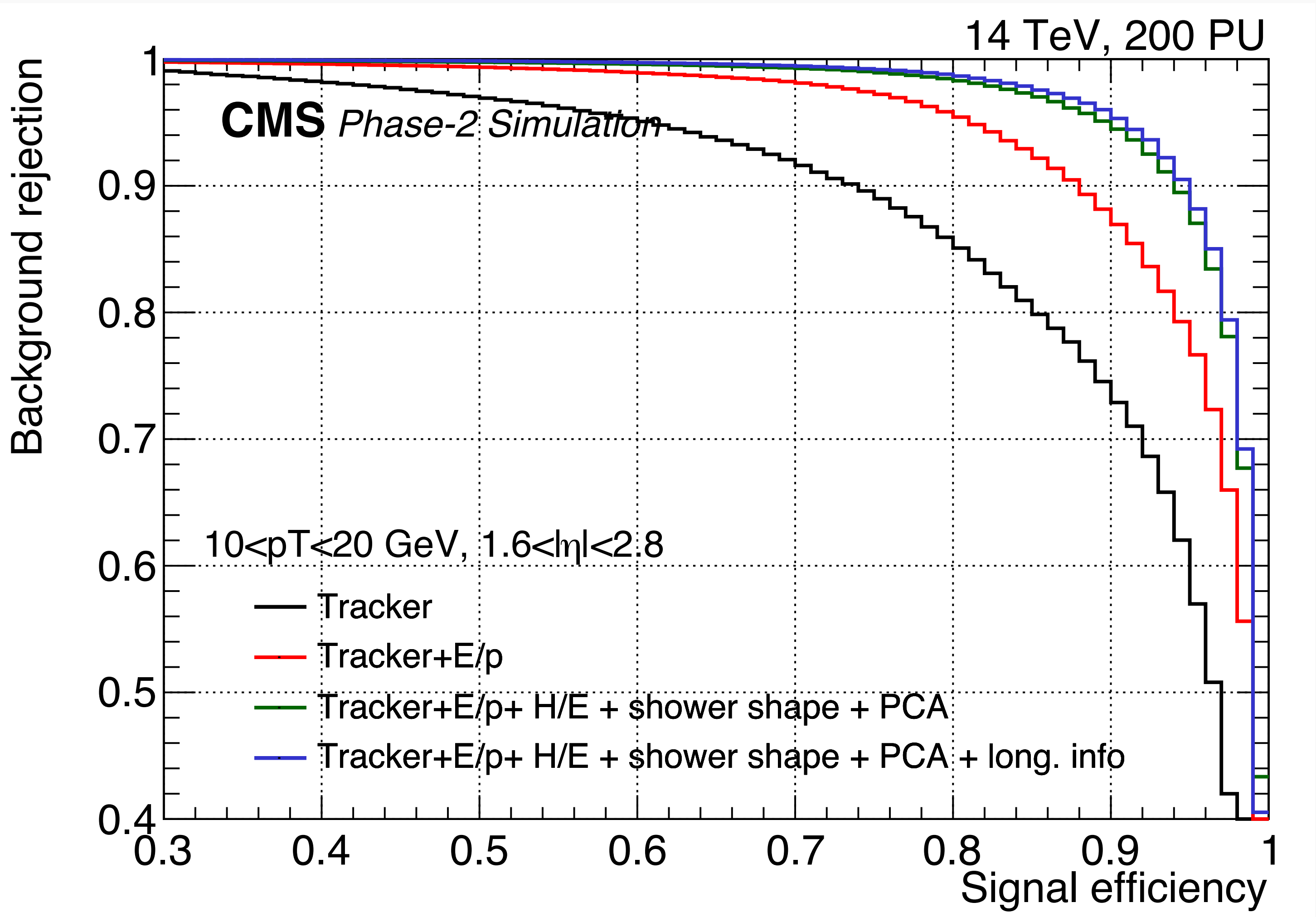
- Electrons are a ‘standard candle’ for Particle Flow:
EM showers are compact ($R_{Moliere}$ ~ 3 cm), of known shape and associated with a track
  - 3D information allows reconstruction of the shower axis (e.g. using Principal Component Analysis) and the measurement of shower shapes with an unprecedented precision
  - Axis pointing improves rejection of PU photons with respect to bremsstrahlung



Track-cluster deltaEta



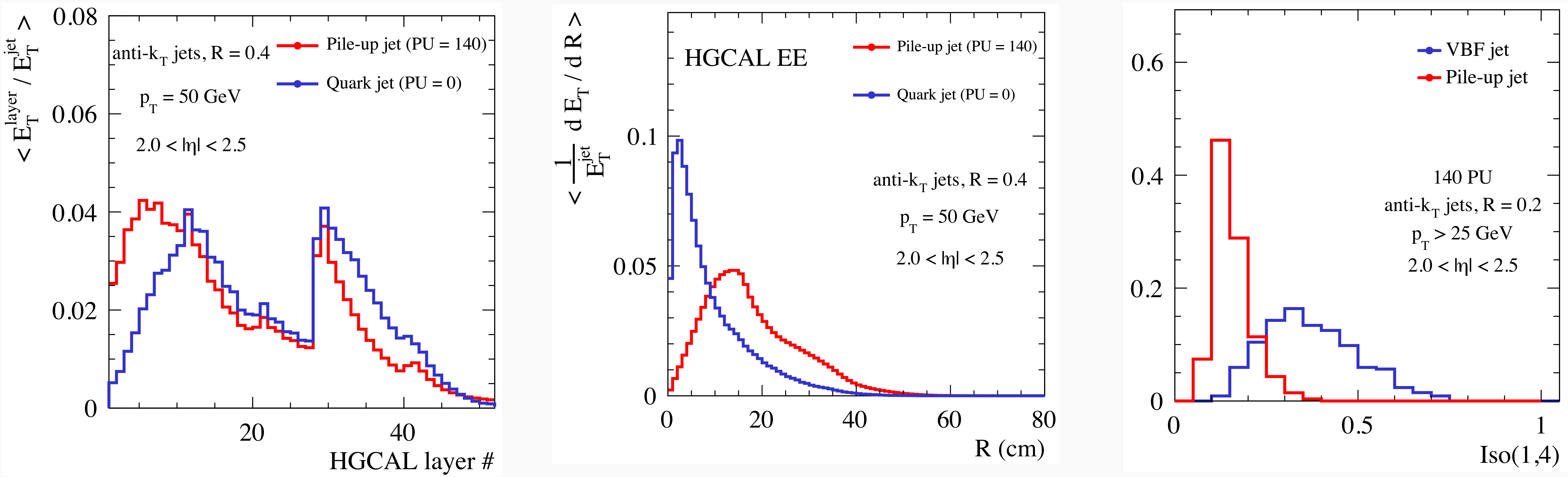
First layer with 10% energy fraction



Electron ID for p_T in 10-20 GeV

JET IDENTIFICATION

- The high granularity allows for the separation of pileup jets with shape variables
  - Pileup jets start to develop earlier in the calorimeter and are wider
  - Promising for resolving boosted topologies as VBF jets, top tagging, etc.



Longitudinal energy profile

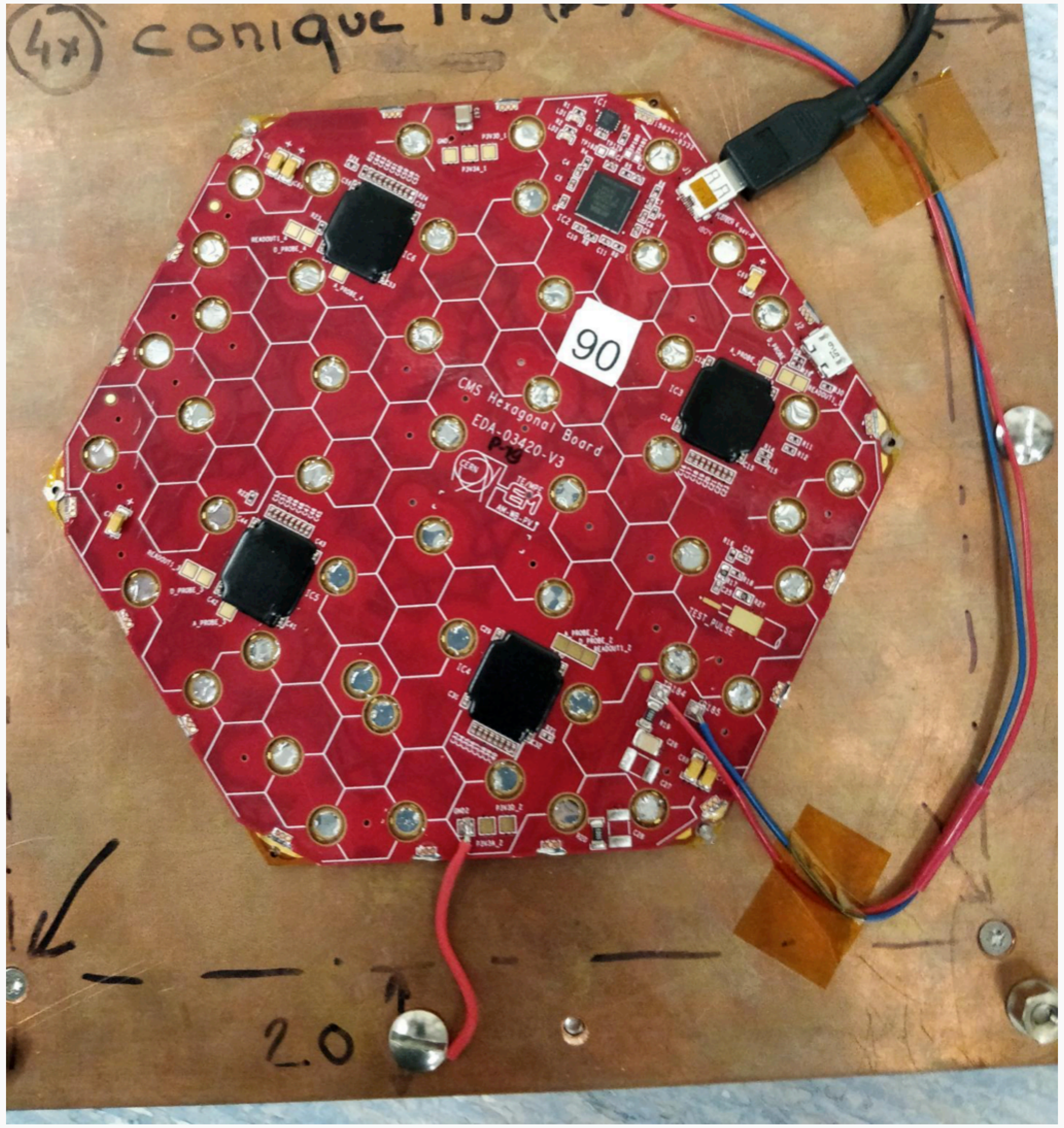
Radial jet profiles in the CE-E

VBF vs PU jet isolation

BEAM TESTS

BEAM TESTS

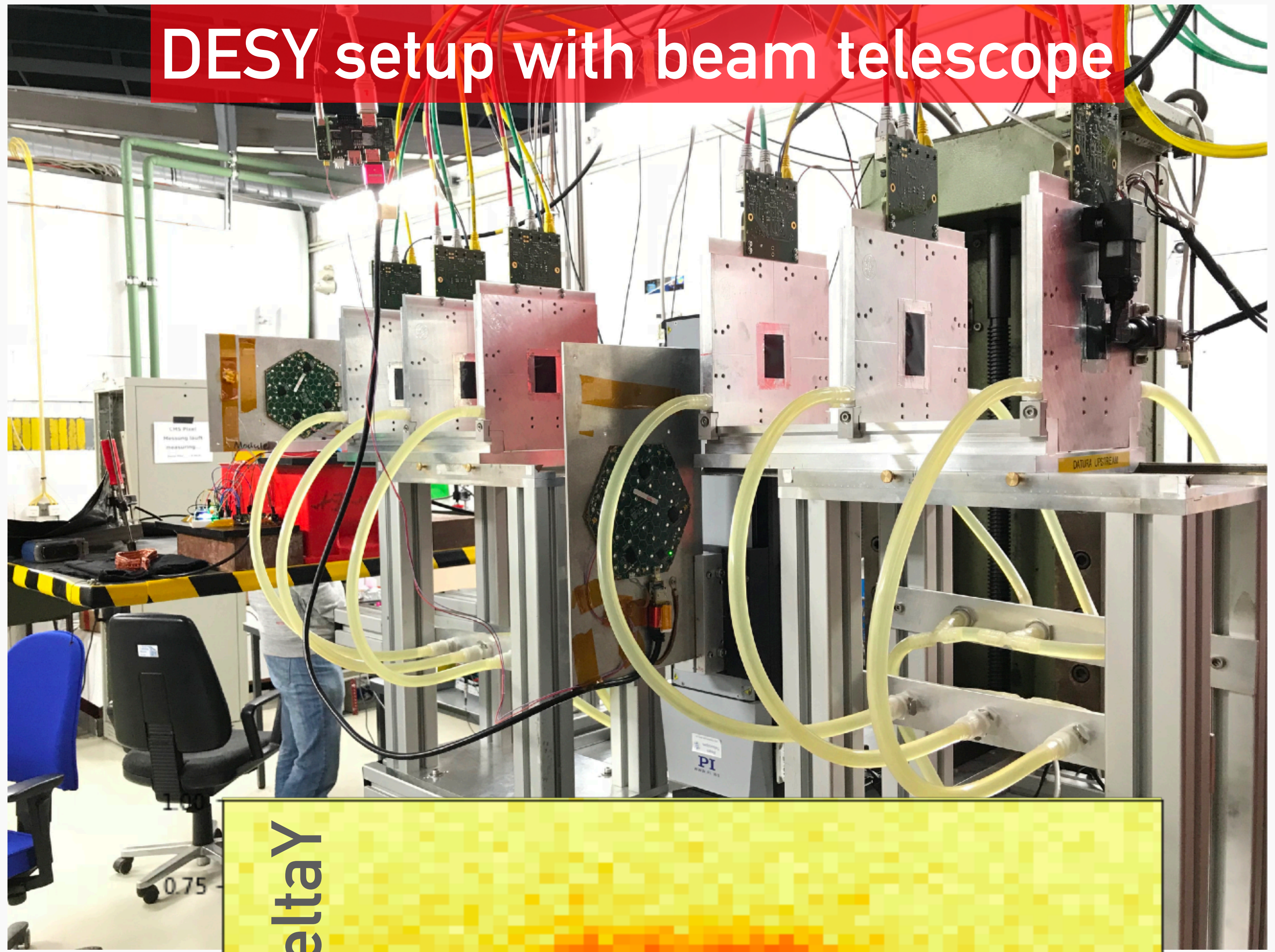
- Several beam tests performed in 2016-2018
- Main objectives for beam tests:
  - Physics performance of the CE-E and CE-H silicon / scintillator parts
  - Verification of the MC simulation
  - Validation of basic FE ASIC architecture in beam conditions: TOT and TOA
  - Technological prototyping of the detector modules
  - System test development in parallel

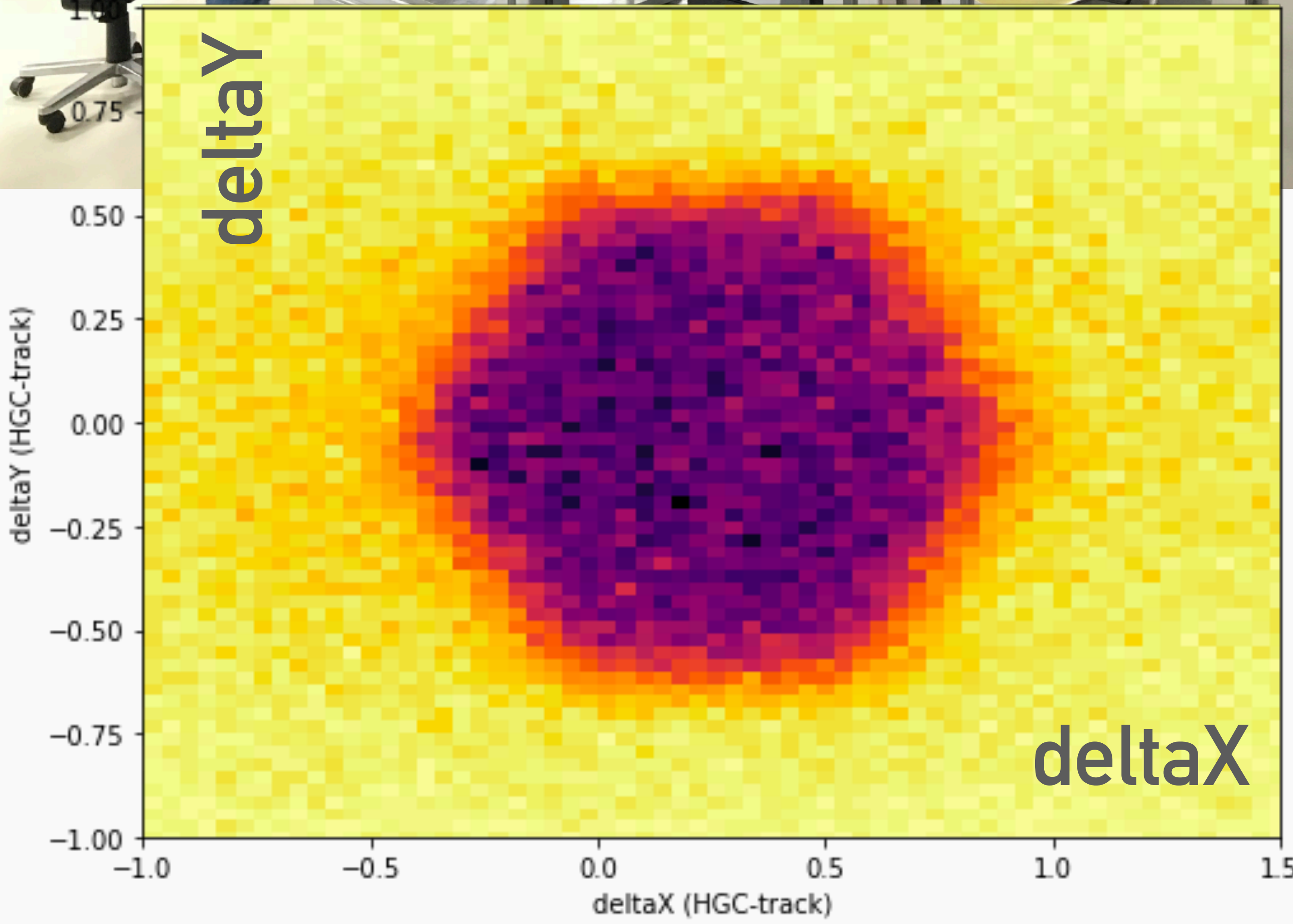


6” hexagonal silicon module prototype

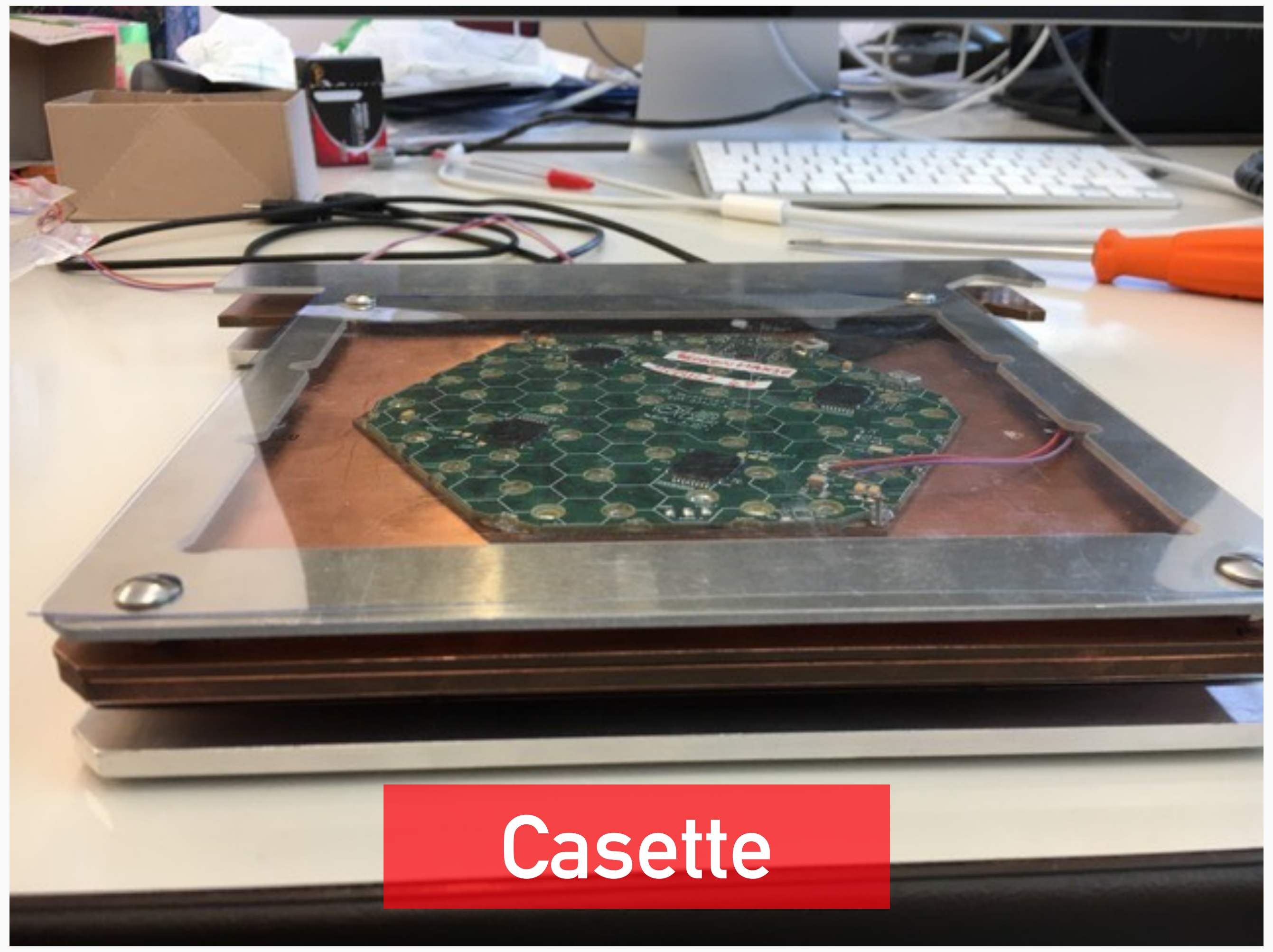
RECENT TEST BEAMS

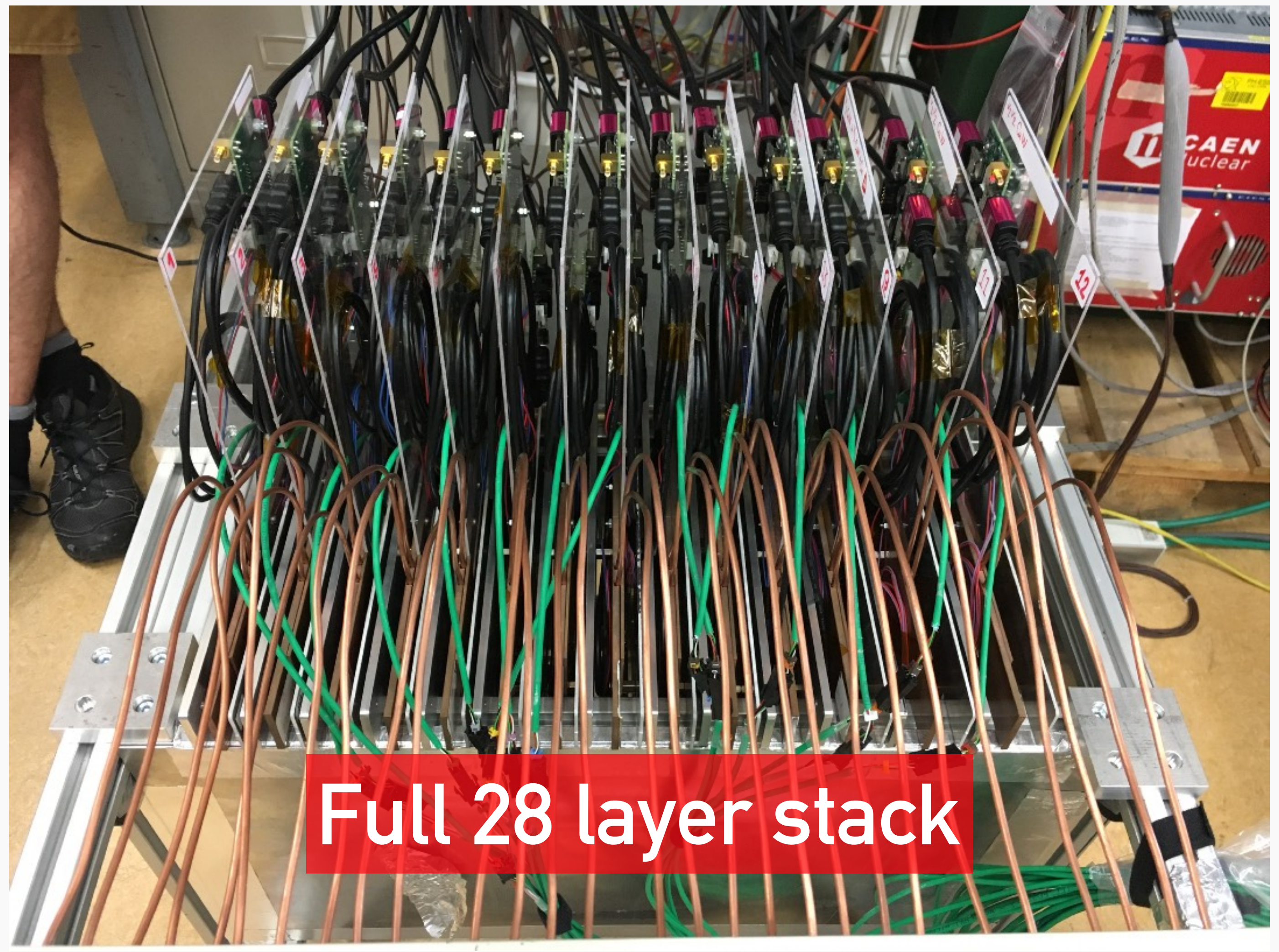
- DESY: March 2018
  - Studies of single module response using low energy electrons (1-6 GeV) as MIPs and in showers
  - AIDA beam telescope for precision tracking (σ_{xy} ~ 10 µm)
- CERN: June 2018
  - Full CE-E depth prototype with 28 modules arranged in double-sided cassettes with integrated cooling
  - Studies of electrons (and pions) in with E = 10-150 GeV


DESY setup with beam telescope



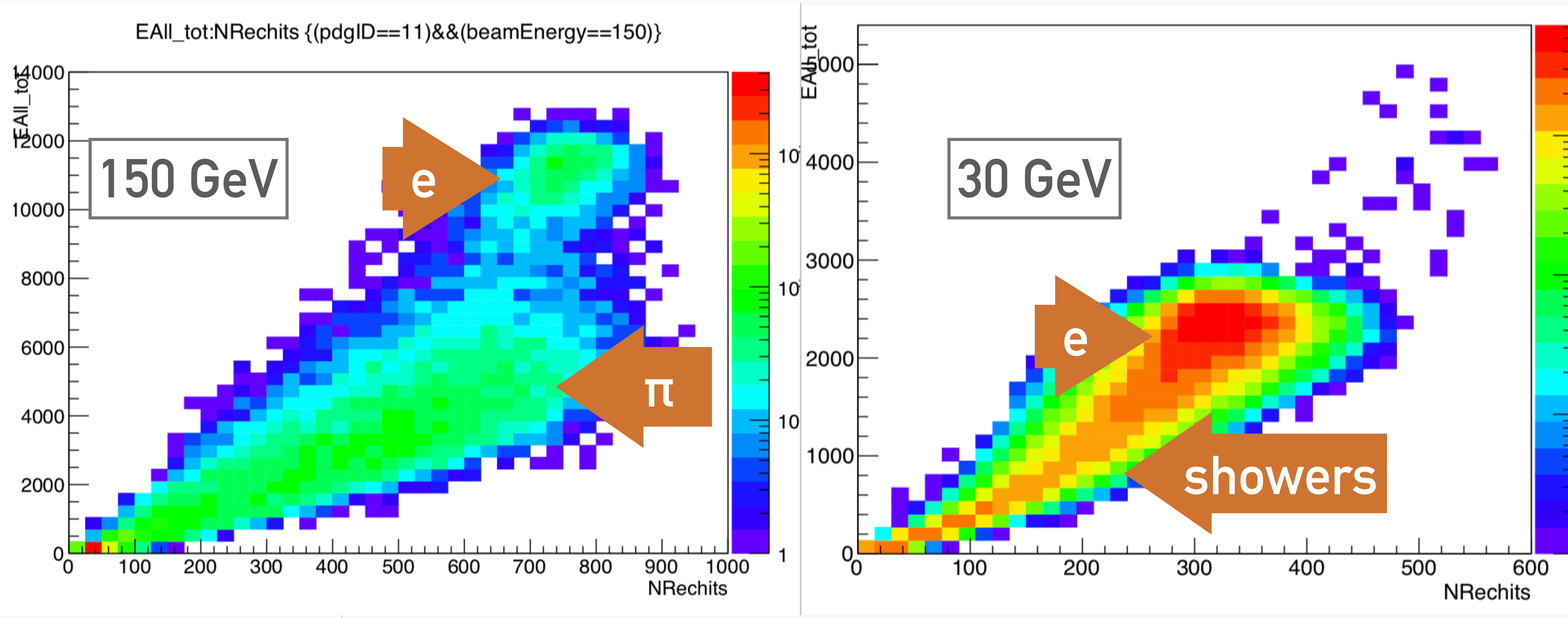
Track - HGC cell position


Casette

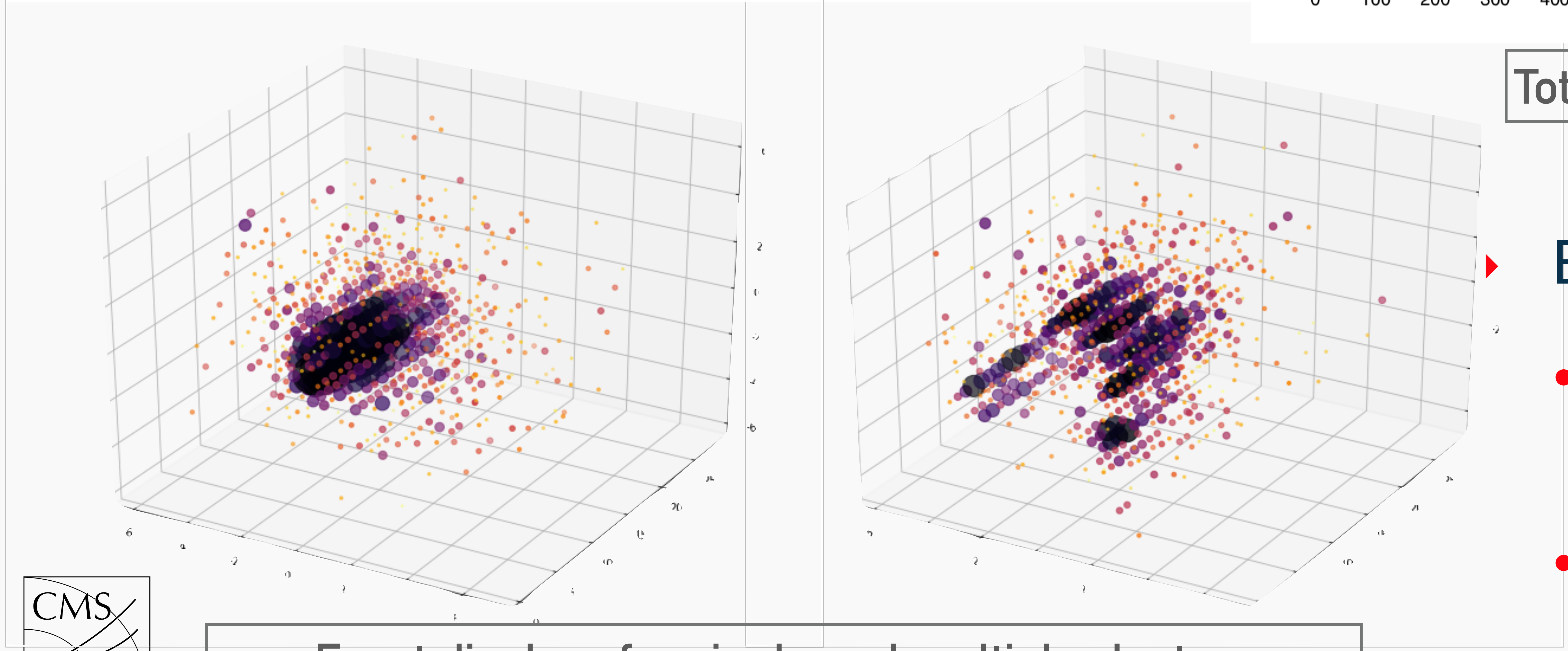

Full 28 layer stack

CERN BEAM TEST IN JUNE 2018

- Significant π contamination of electron beam at high energies *[expected]*
  - 99% purity < 80 GeV; <10% for 150 GeV
  - Consistent with simulated e/pi mix
  - Studying mitigation by ID variables



Total uncalibrated energy vs number of hits

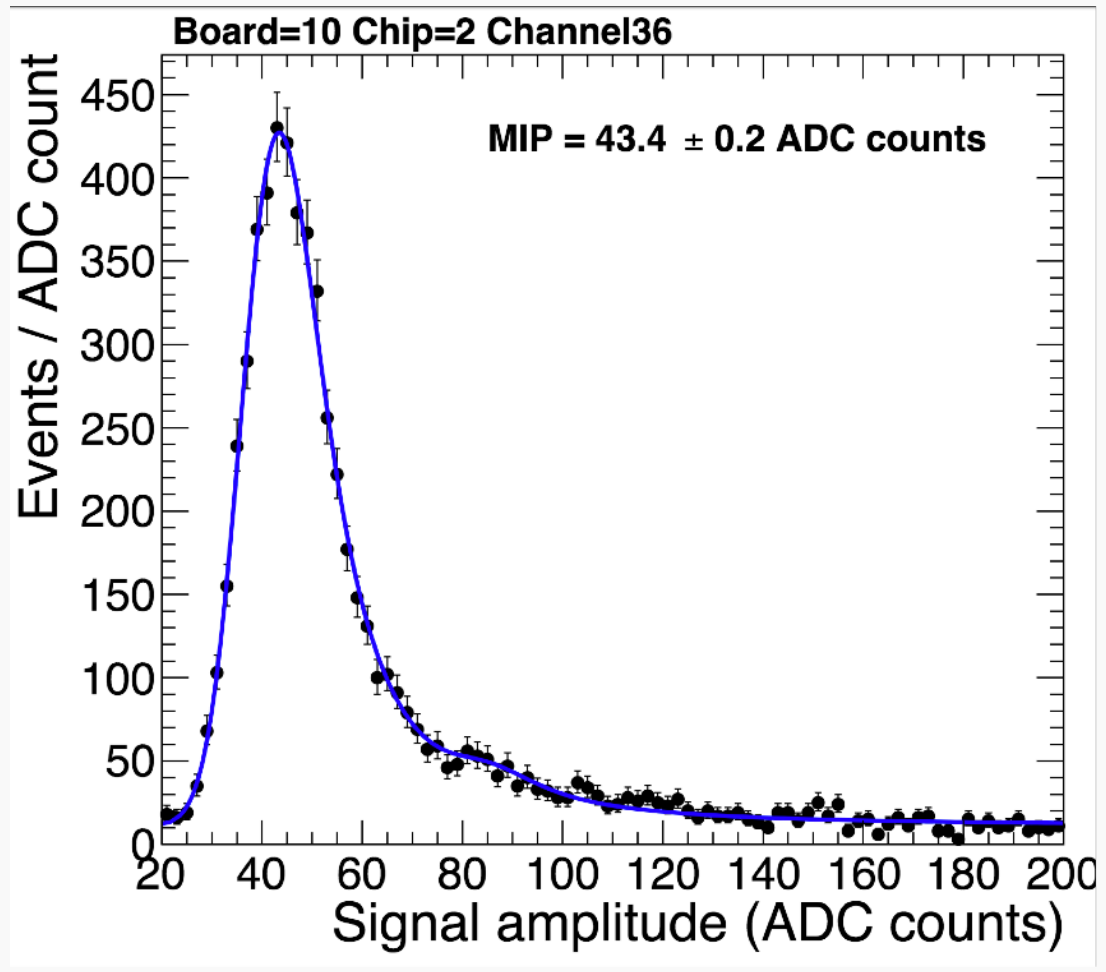


Event displays for single and multiple clusters

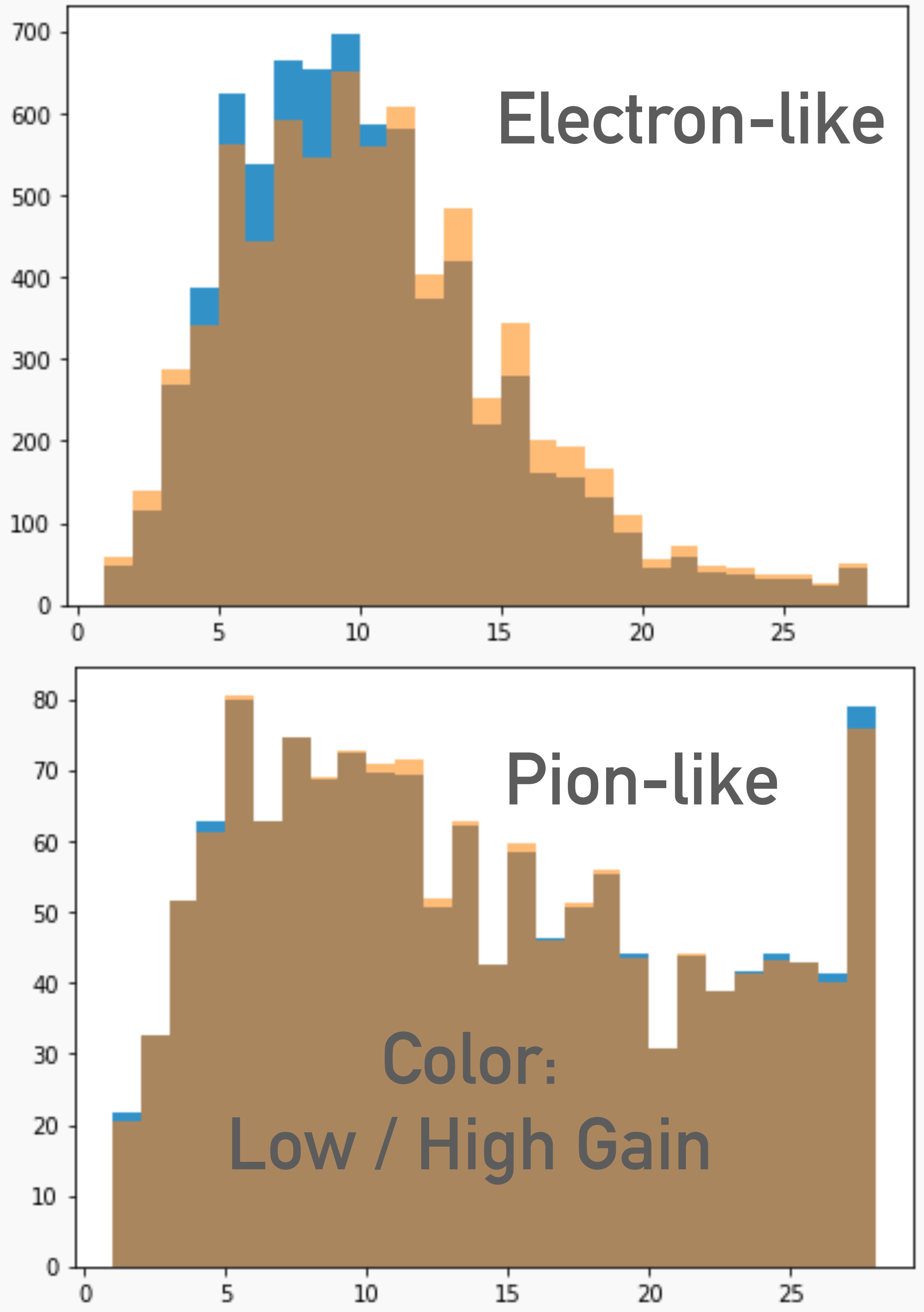
- Early showering electrons *[unexpected]*
  - Requires cleaning of data and limits statistics for E measurement,
  - … but provides interesting data for pattern recognition/clustering!

CERN BEAM TEST IN JUNE 2018

- Preliminary results:
  - Clean MIP spectra for calibration
  - Longitudinal shower shapes distinguishable for electrons/pions
  - Energy reconstruction works well even with preliminary calibration
  - Basic agreement with Geant4 simulation for energy and multiplicity

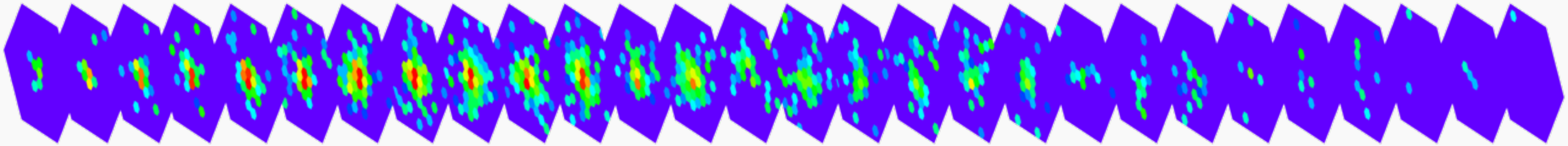


Muon MIP spectrum for a single channel



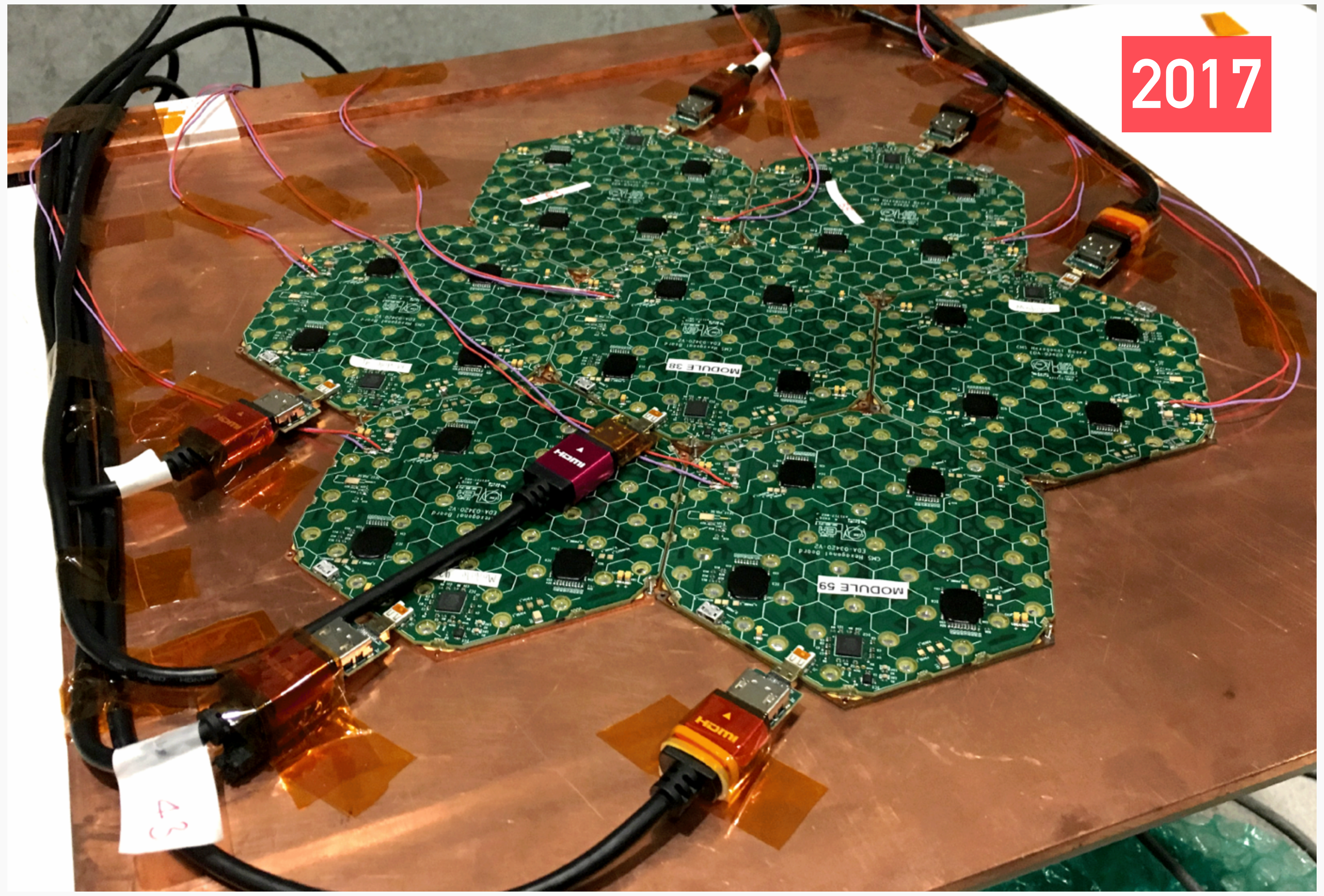
Longitudinal energy profiles

Event display for an 80 GeV electron

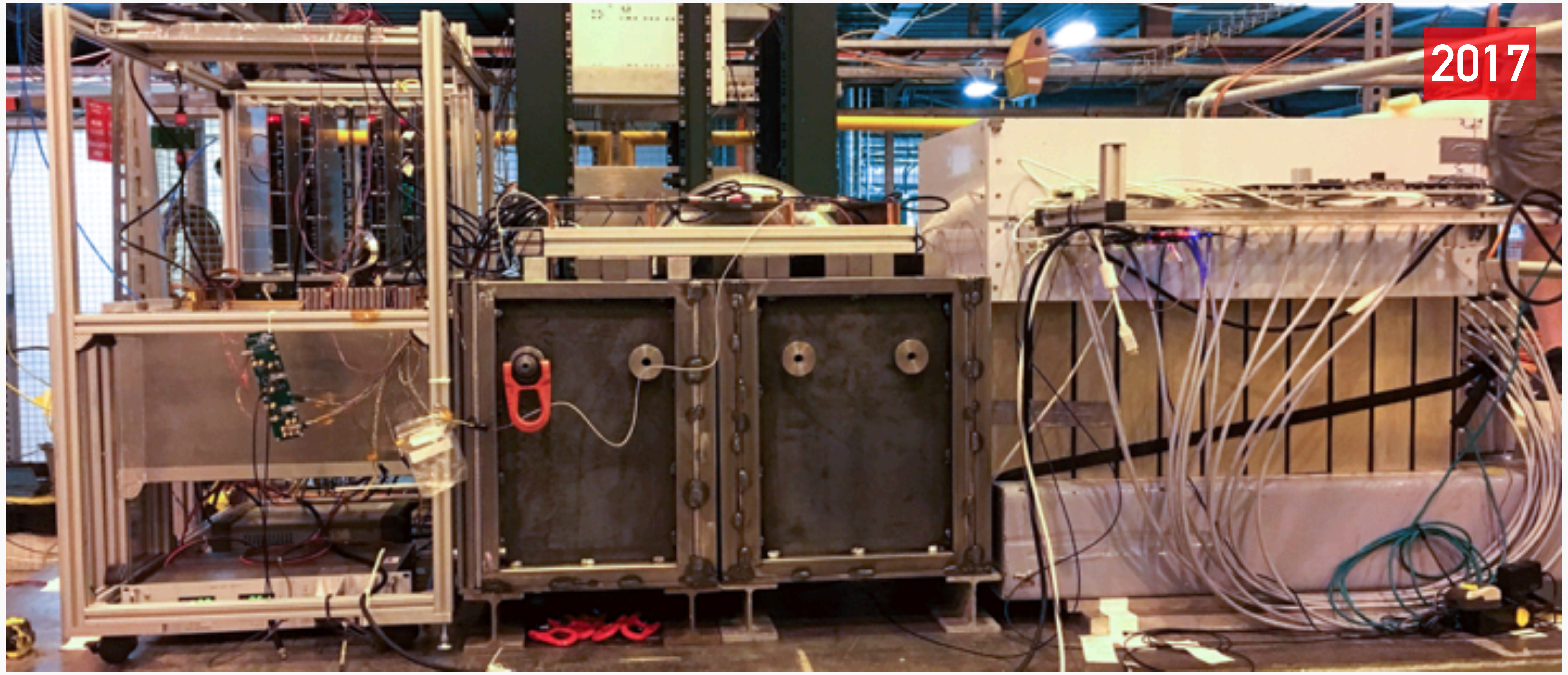


ONGOING ACTIVITIES TOWARDS OCTOBER 2018 TB

- Next CERN beam test in October 2018:
  - Silicon: CE-E + 12 layer CE-H (7 modules/layer) | Scintillator: CALICE AHCAL
  - Setup as in 2017, but with ~100 modules in total vs. 20 in 2017
  - Aiming at exploiting the full potential of the test system (including timing)



CE-H plate with 7 modules



CE-E stack | CE-H stack | AHCAL

SUMMARY

SUMMARY

- CMS High Granularity Calorimeter is a very challenging detector
  - Harsh radiation environment, high pileup & occupancy
  - Large number of channels, low noise, large dynamic range, high speed, low power …

CERN European Organization for Nuclear Research
Organisation européenne pour la recherche nucléaire

CERN-LHCC-2017-023
CMS-TDR-17-007
22 Dec 2017

CMS

The Phase-2 Upgrade of the
CMS Endcap Calorimeter
Technical Design Report

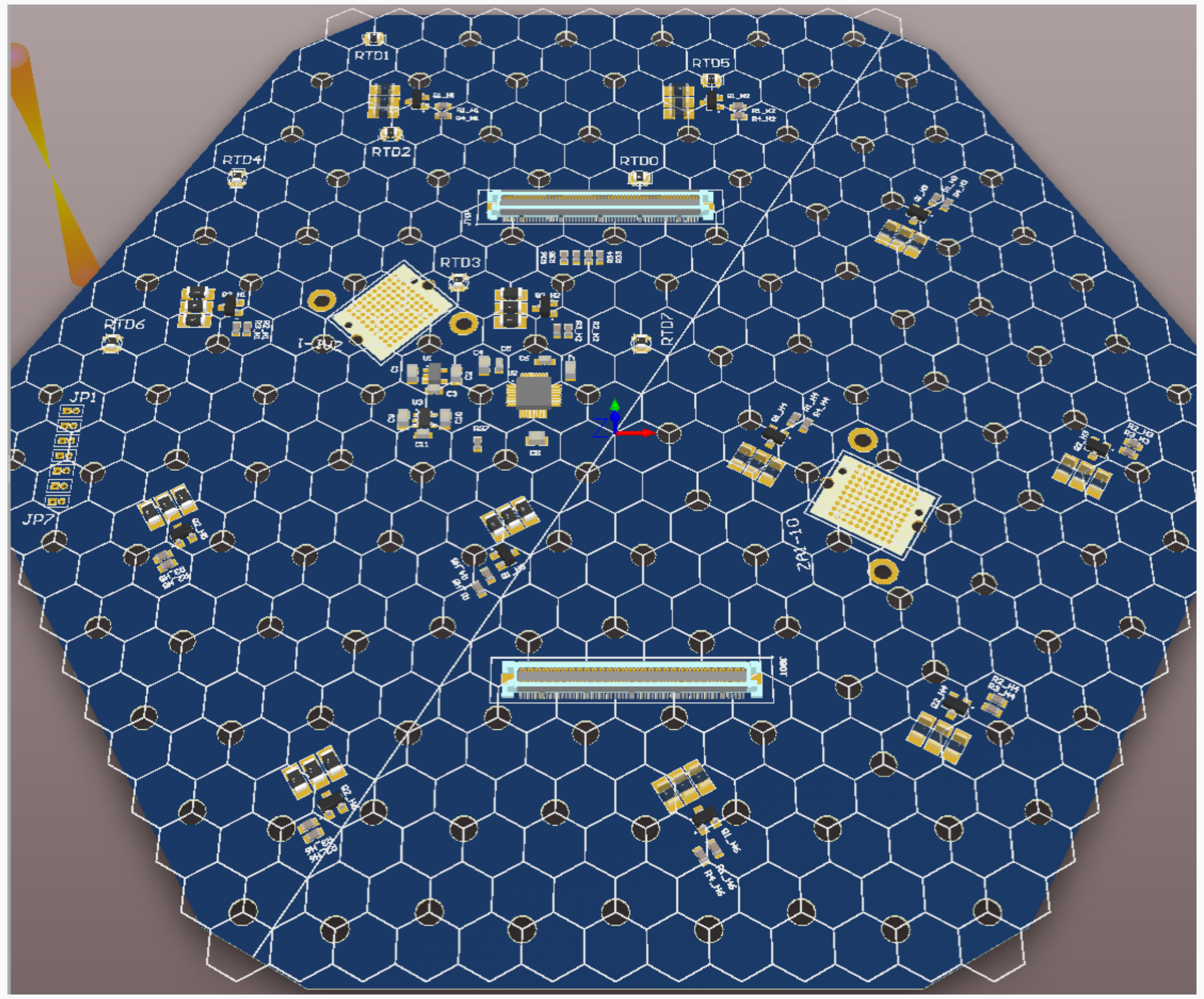
- TDR approved in April 2018: cds.cern.ch/record/2293646
- 5D (3D position + energy + time) measurement of showers provides unique opportunities in particle reconstruction for identification and pileup mitigation
- Ongoing test beam campaign to validate technology and physics performance
- Engineering Design Review to review full design scheduled for mid 2020

BACKUP

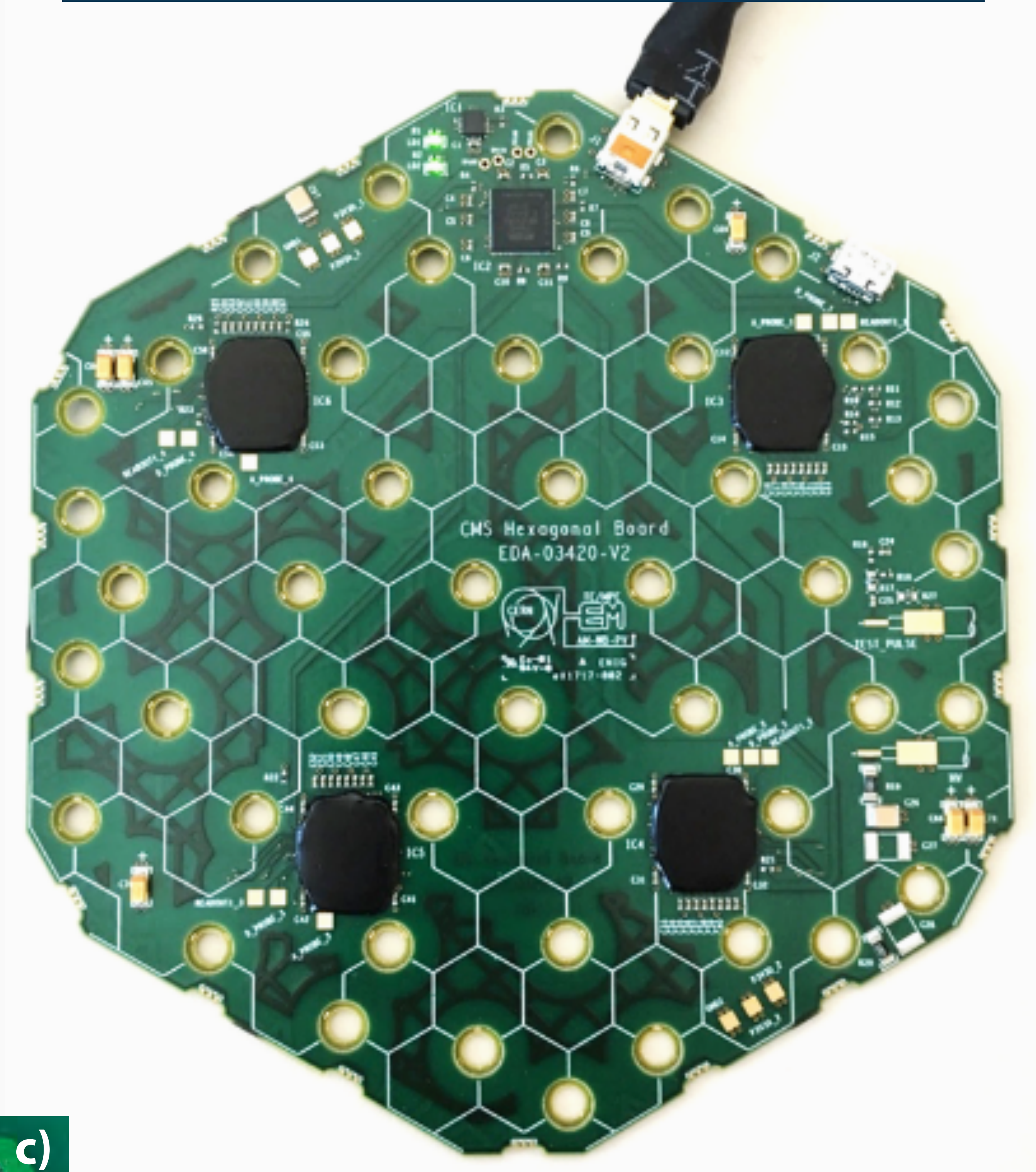
FRONT-END ELECTRONICS

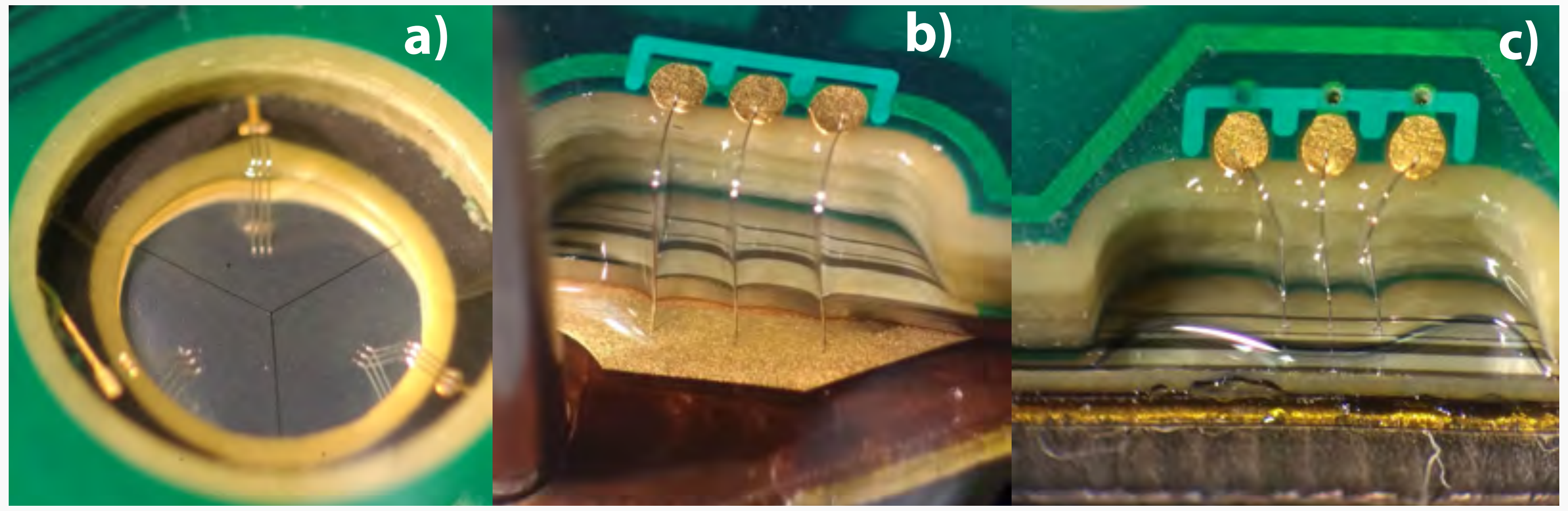
- Detector modules with 2 PCBs
  <u>< 6mm thick</u>:
  1. PCB: “hexaboard”
     Wire-bonds to Si-sensor
     and very-FE ASICs
  2. PCB: Motherboard for
     powering, data concentration,
     trigger generation and
     bi-directional communication
- Trigger/data transfer:
  low-power GBT links (lpGBT)

Hexaboard design for HGCROC



Hexaboard PCB for Test Beam

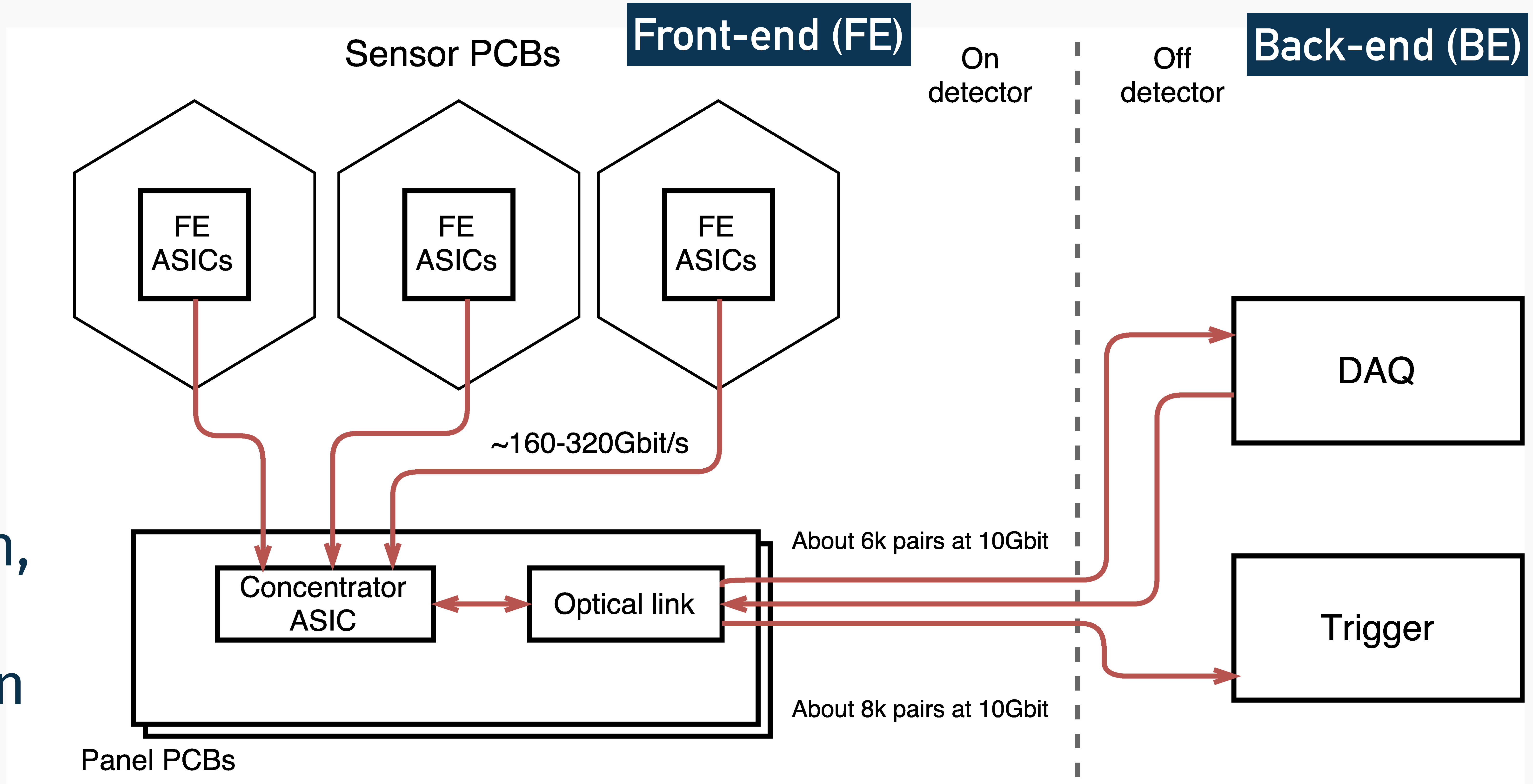




Wire-bonds from Silicon to 1. PCB

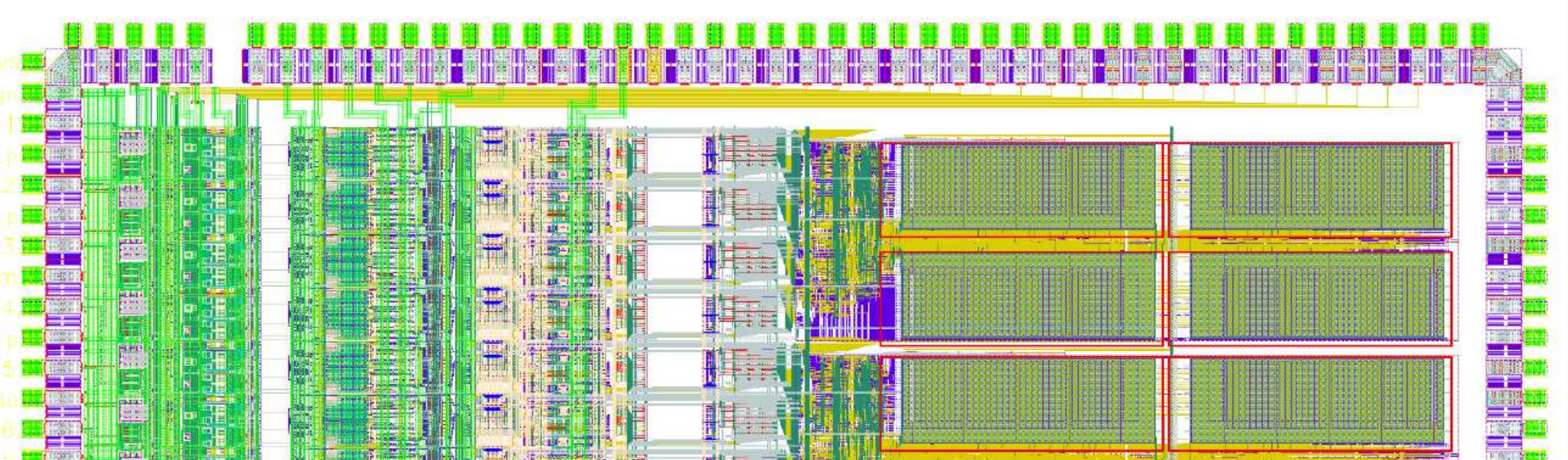
FRONT-END ELECTRONICS

- Detector modules with 2 PCBs <u>< 6mm thick</u>:
  1. PCB: “hexaboard”
     Wire-bonds to Si-sensor and very-FE ASICs
  2. PCB: Motherboard for powering, data concentration, trigger generation and bi-directional communication
- Trigger/data transfer: low-power GBT links (lpGBT)



VERY FRONT-END ASIC

- At the heart of the detector electronics is the front-end readout ASIC
- The design and environment of the HGCAL pose several requirements
  - System on chip: charge, time, digitization, data and trigger processing, ZS …
  - Low power: < 15 W/channel
  - Low noise: < 2000 e^-
  - High radiation: 10^{16} n_{eq} (1MeV eq.)/cm^2
  - High speed readout: > 1 Gb/s
  - Same ROC for Si&SiPM



- Signal: high dynamic range: 0–10 pC
  - Charge: 0–100 fC [11 bits]
  - Time over Threshold: 0.1–10 pC [12 bits]
- Timing information: Time of Arrival with 25 ps resolution > 50 fC [12 bits]

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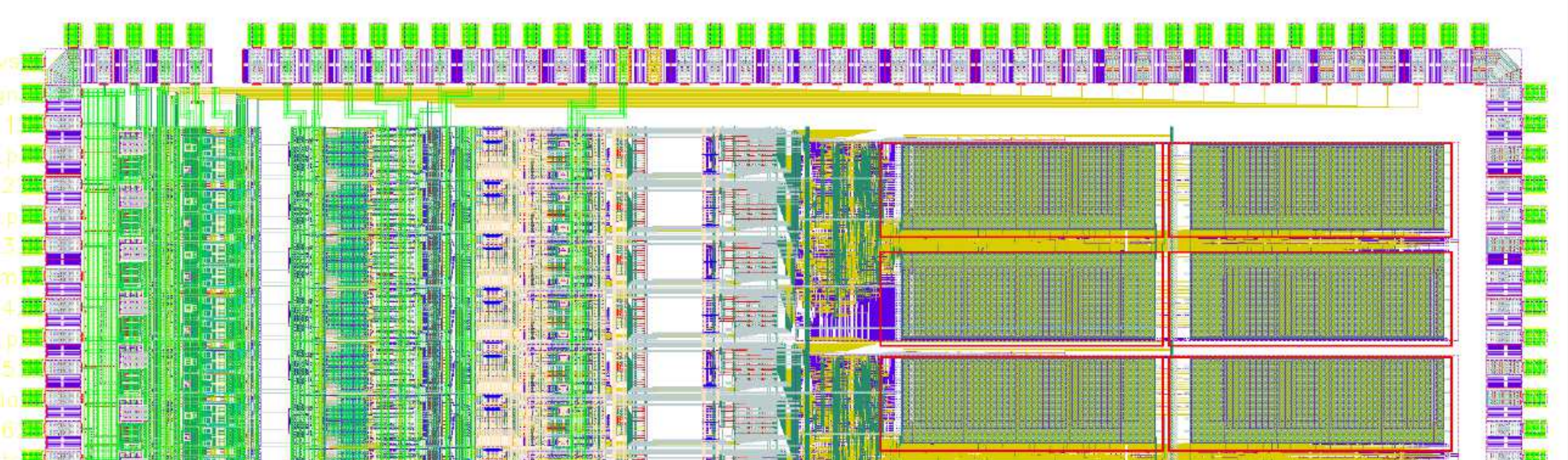

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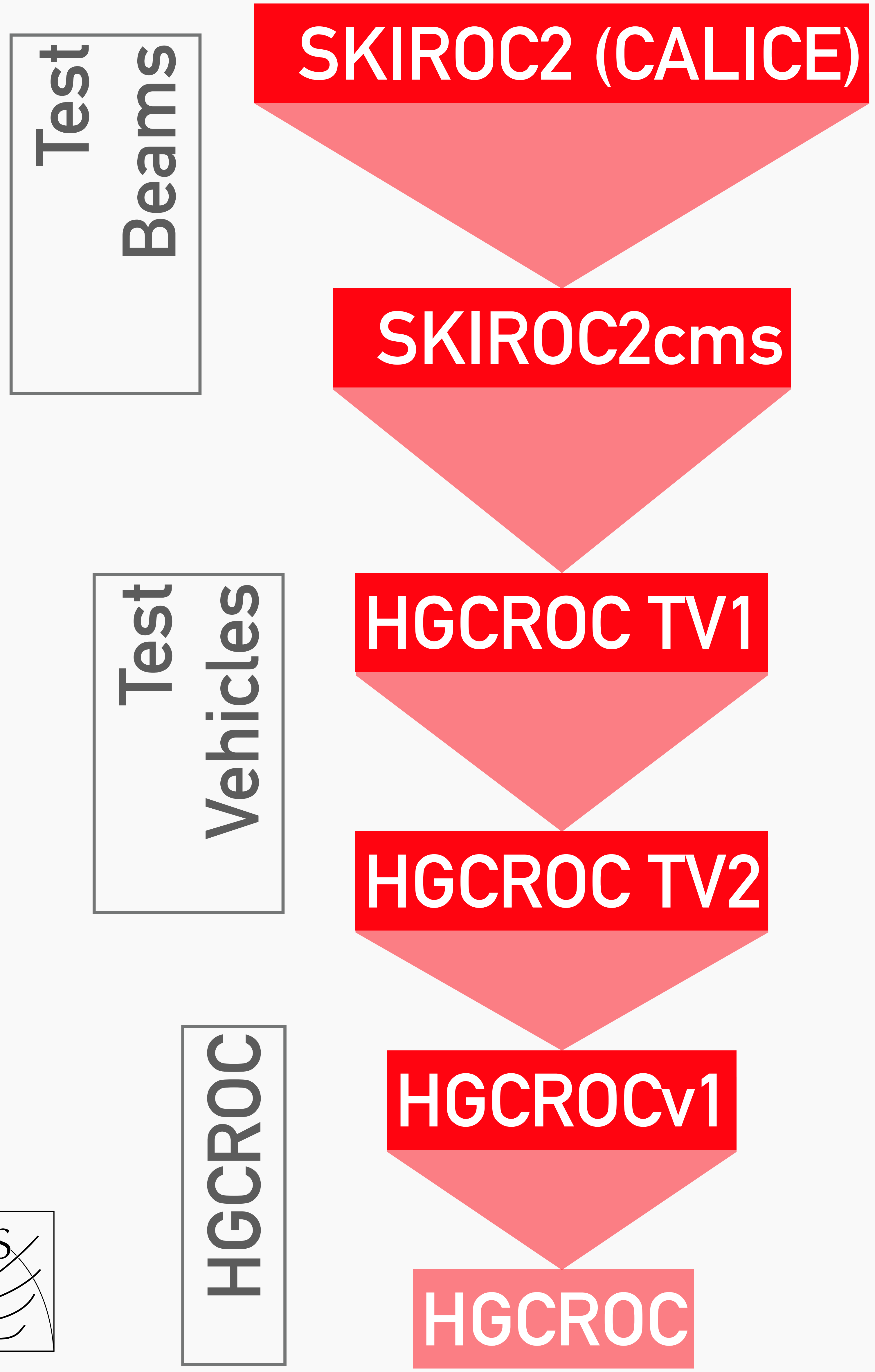
HGCAL ASIC EVOLUTION: FROM SKIROC TO HGCROC

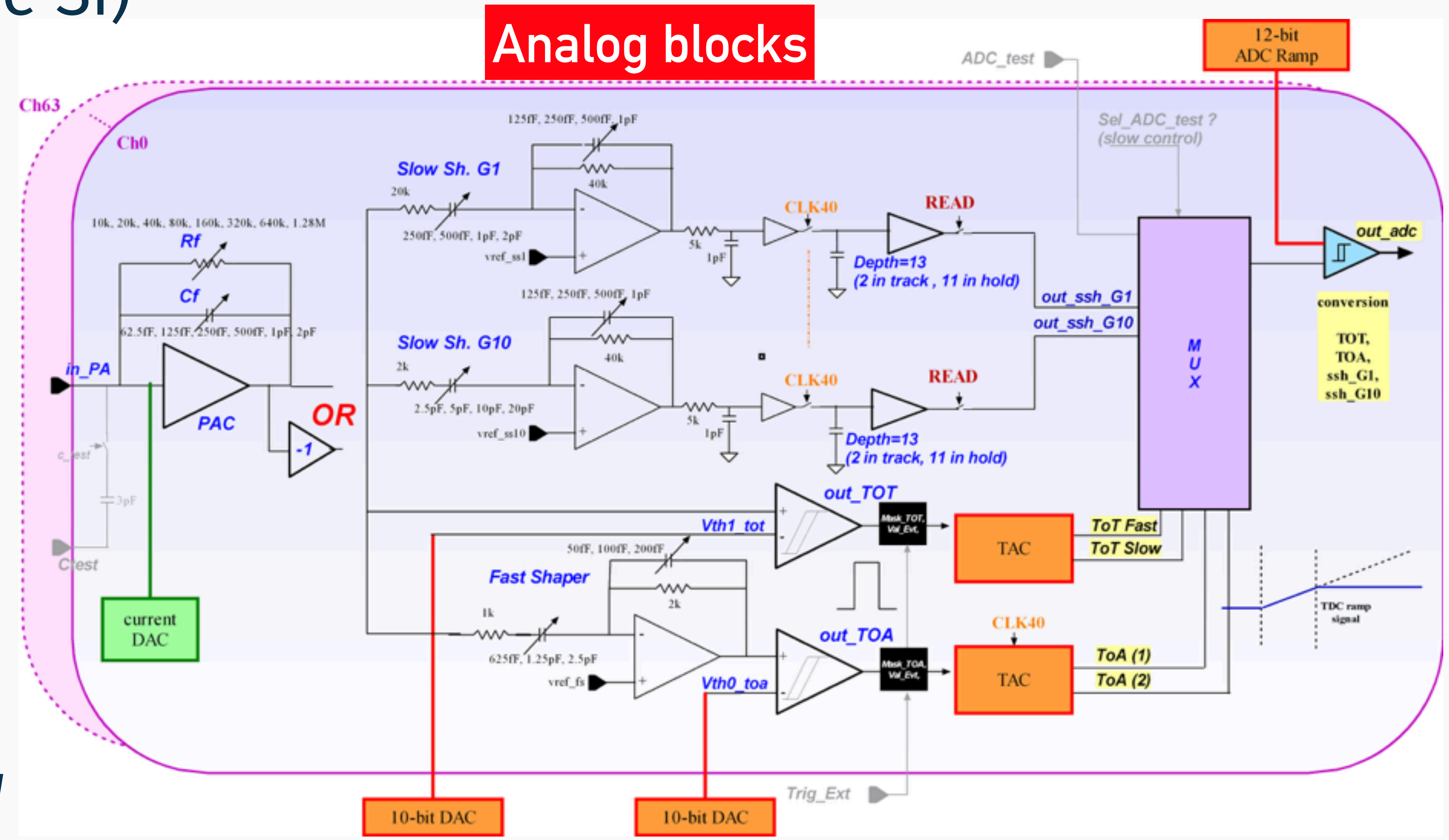


- SKIROC2:
  - ASIC used by CALICE in the SiW ECAL
  - Dedicated 64 channel Si-detector readout ASIC, SiGe 350 nm
- SKIROC2cms: *submitted and received in 1Q of 2016*
  - Modification for test beams with CMS-like running conditions
  - 40 MHz clock and sampling, Gain + ToA + ToT
- Test Vehicle 1: *submitted in May 2016, received in August 2016*
  - First HGCROC test vehicle in CMOS 130 nm architecture
  - Dedicated to preamplifier studies
- Test Vehicle 2: *submitted in December 2016, received in May 2017*
  - Dedicated to analog channel study for TDR
- HGCROCv1: *submitted in July 2017, expected in October 2017*
  - All analog and mixed blocks; many simplified digital blocks

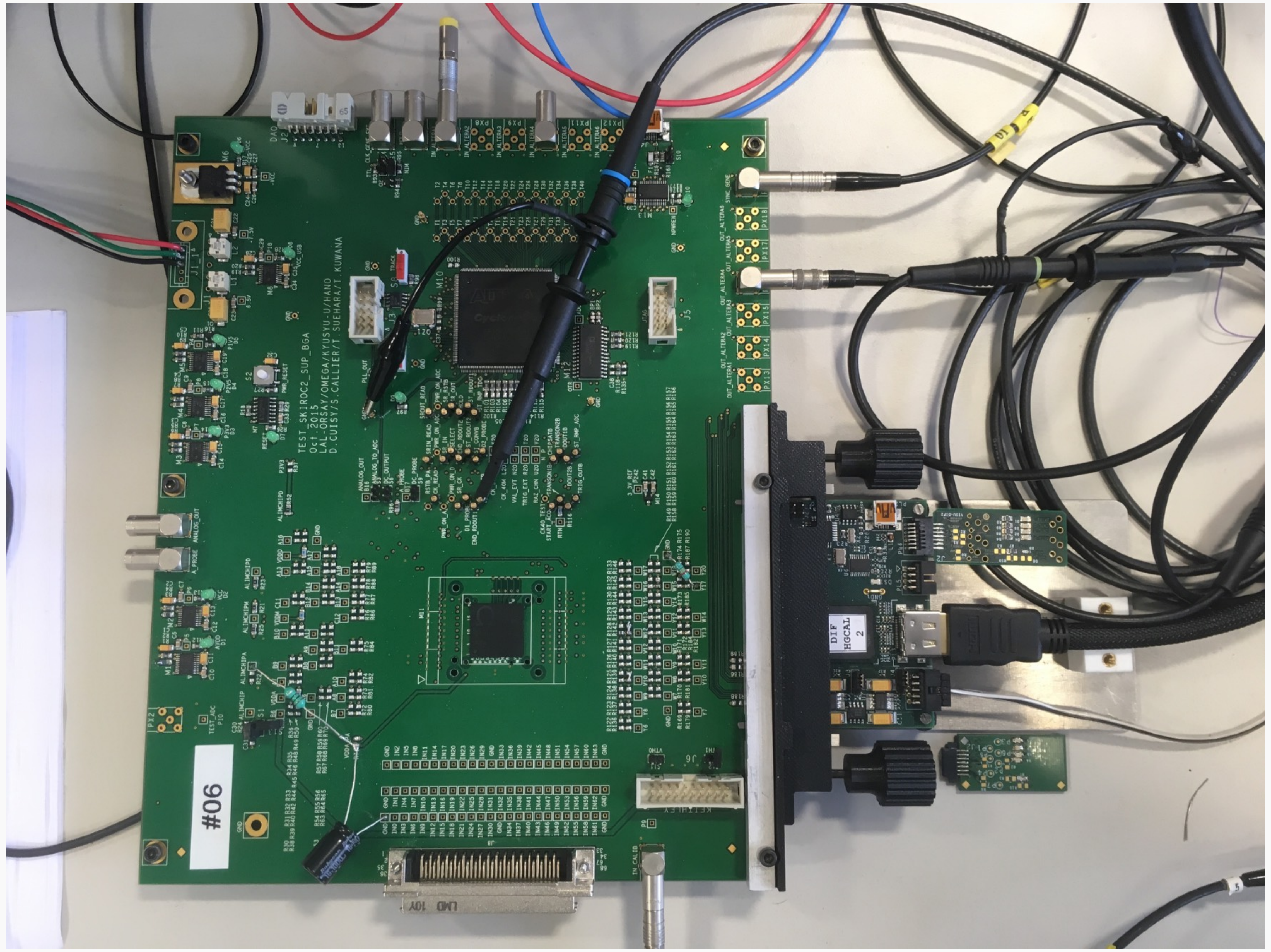
➡ **Final HGCROC submission by mid 2019!**

SKIROC2CMS: ASIC FOR BEAM TESTS [Q1 2016]

- Modified 64ch CALICE SKIROC2 specially for test beam use
- Dual polarity preamplifier (for p- or n-type Si)
- 40 MHz clock and 25 ns sampling
- ADC: low and high (x10) gain
  - Slow shaper with 40ns shaping time
  - 300ns in rolling analog memory
- Time-of-Arrival — *proof of principle!*
  - Fast shaper (5 ns)
- Time-over-Threshold — *proof of principle!*
  - For large signals directly from the preamplifier
- TDC (TAC) for TOA & TOT (~20 ps binning, ~50ps jitter)



SKIROC2CMS: ASIC FOR BEAM TESTS

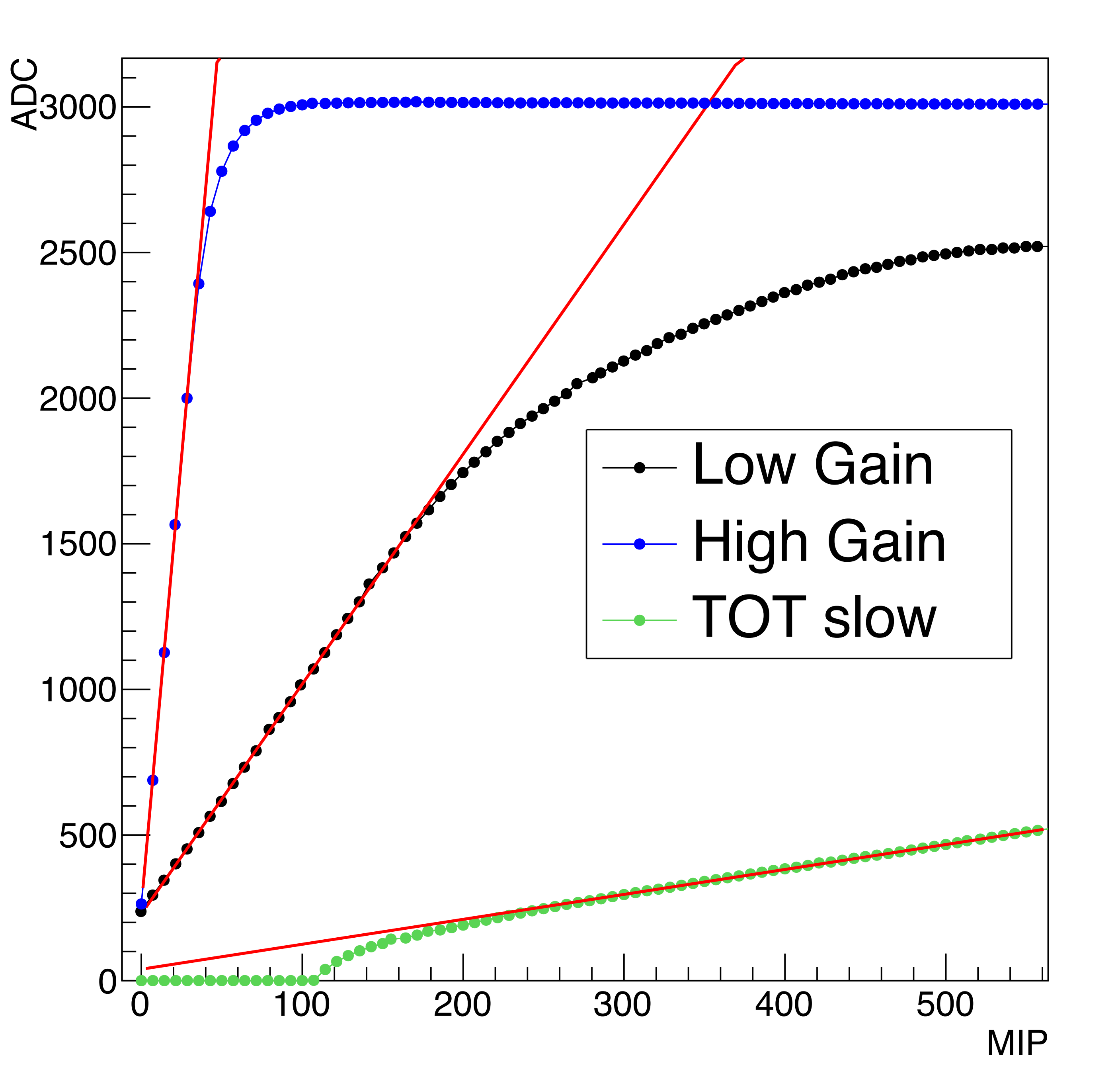


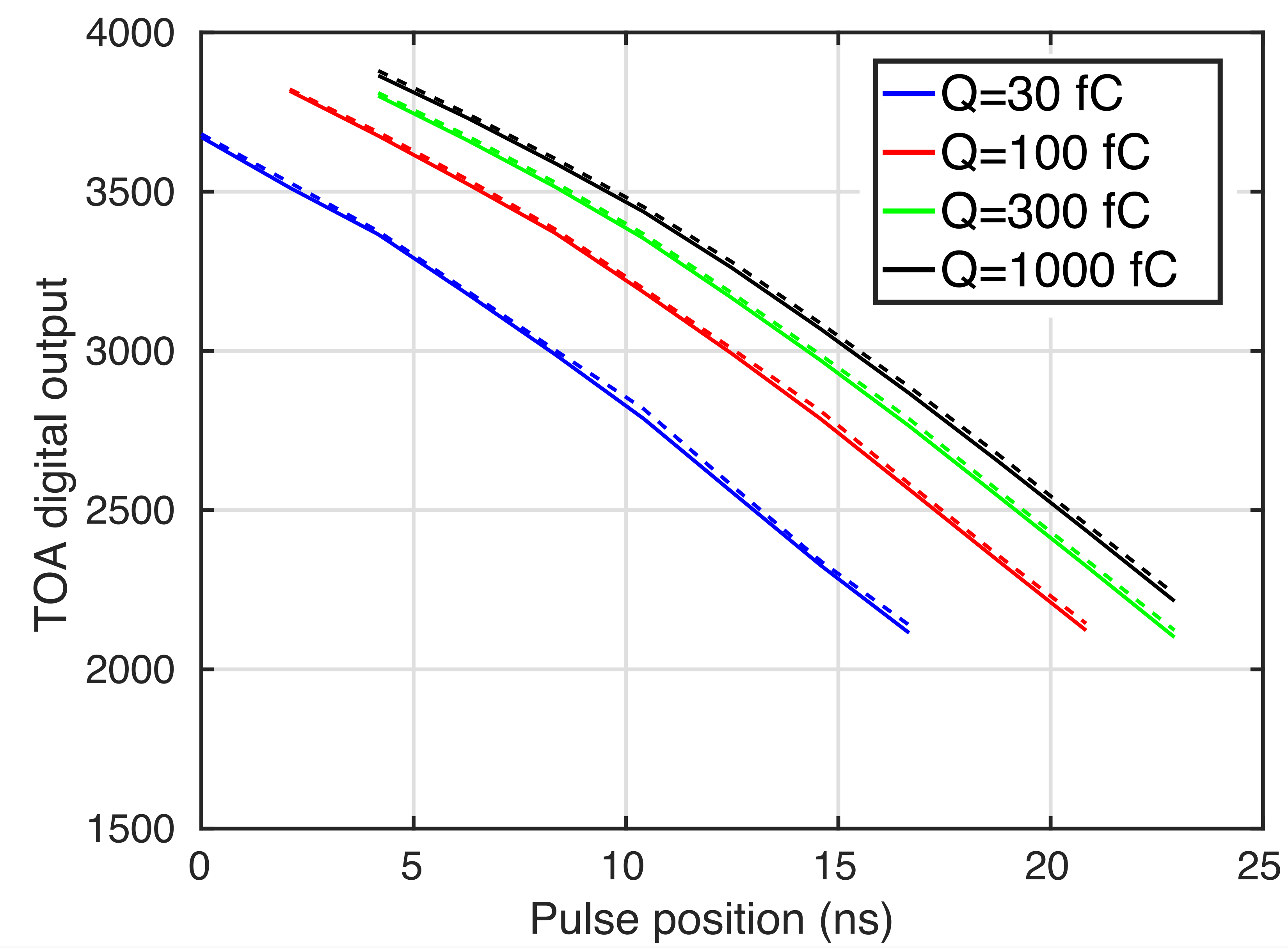
ASIC test board

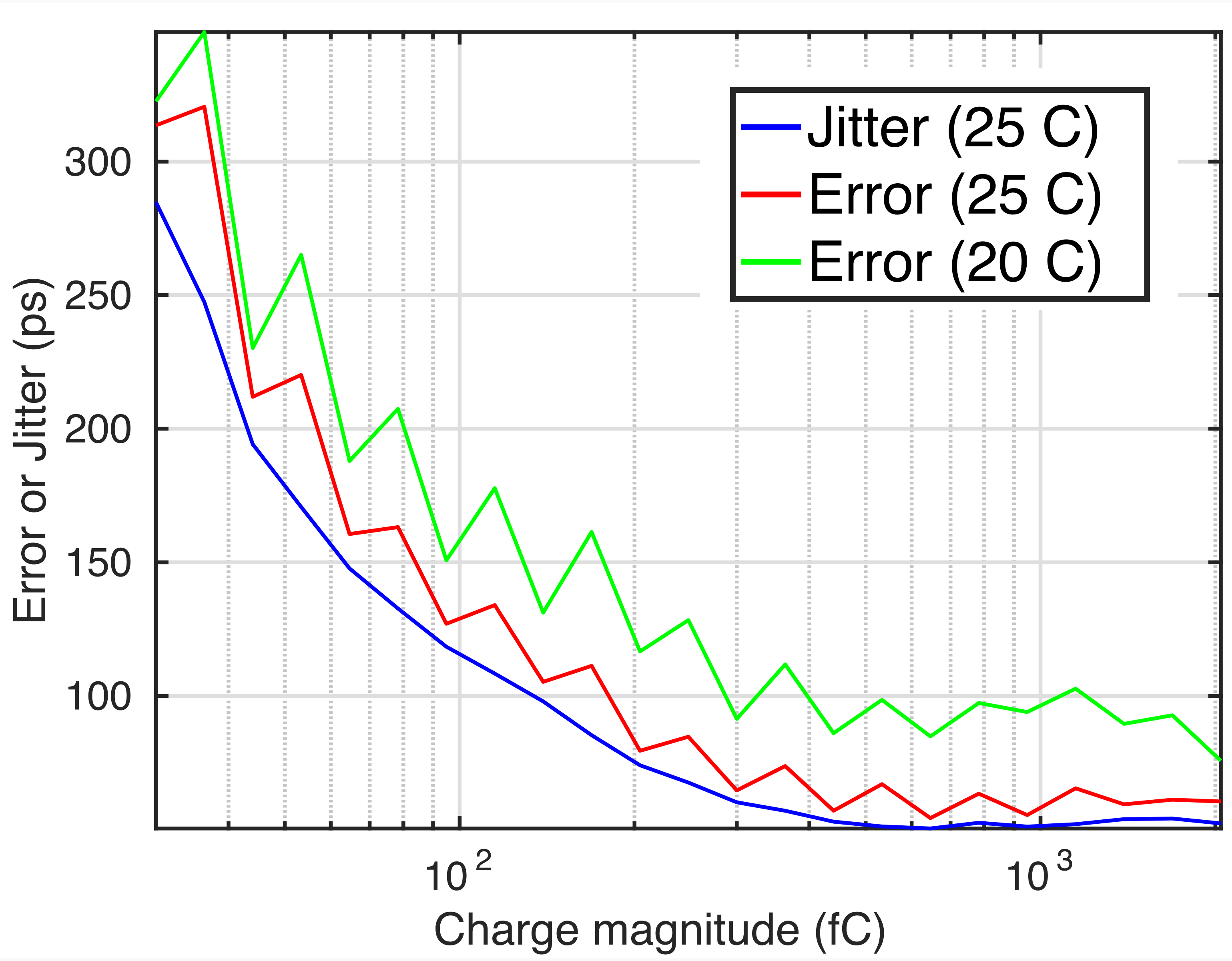
- Extensive tests of the SKIROC2cms ASIC have been performed
  - Gain and TOT linearity, noise, pedestals
  - TOA transfer characteristics, efficiency, time-walk, jitter
  - Temperature stability
- On single-ASIC test board and hexaboard
- More details about the TB performance in tomorrow's talk by Thorben Quast

SKIROC2CMS: ASIC FOR BEAM TESTS

- ADC and TOT linearity:
  - HG/LG linear until 500 fC
  - TOT linear for 500fC — 10pC
- Noise for gain: ~ 3500 e^-
- TOA performance:
  - Off-line correction for time-walk possible
  - Constant term: 50 ps
  - Noise term: 10ns/Q(fC) [expected ~4ns/Q]



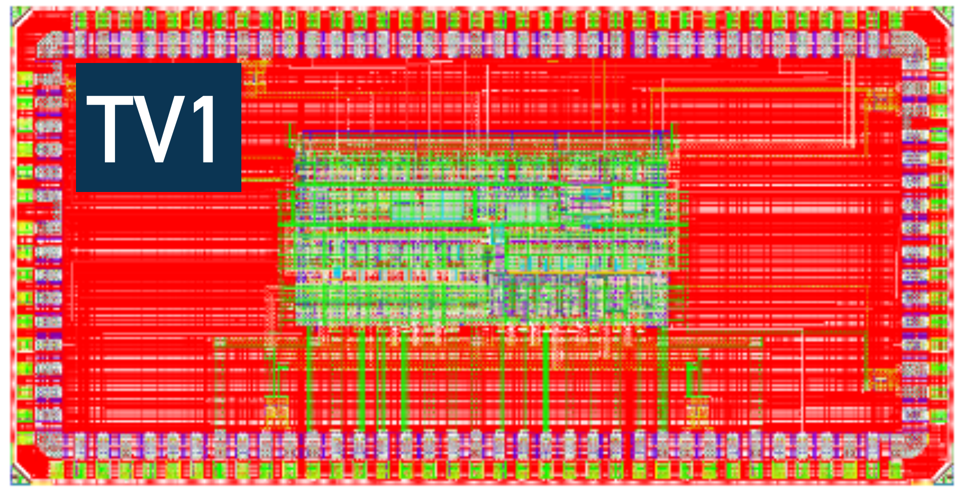




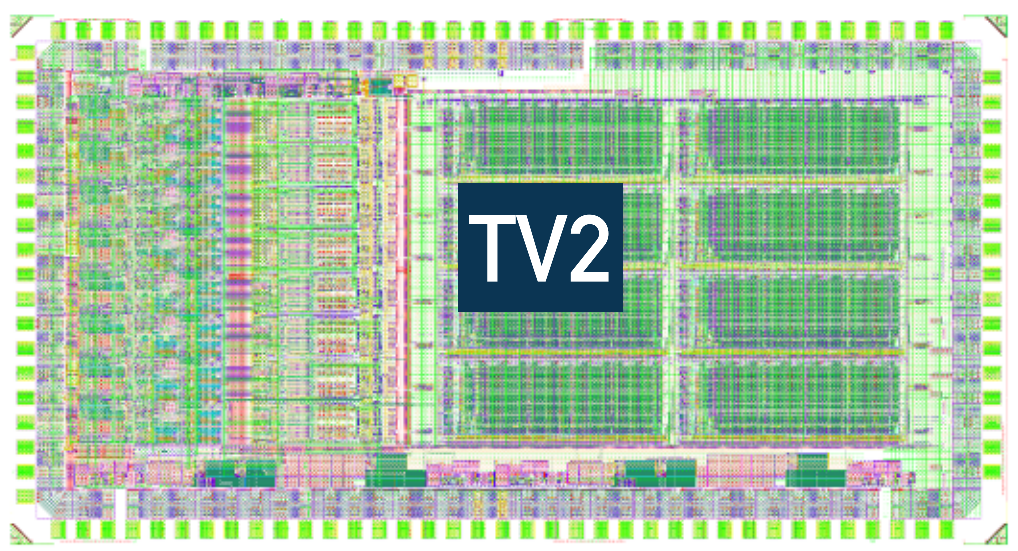
* Jagged shape is due to imperfect interpolation between characterisation measurements.

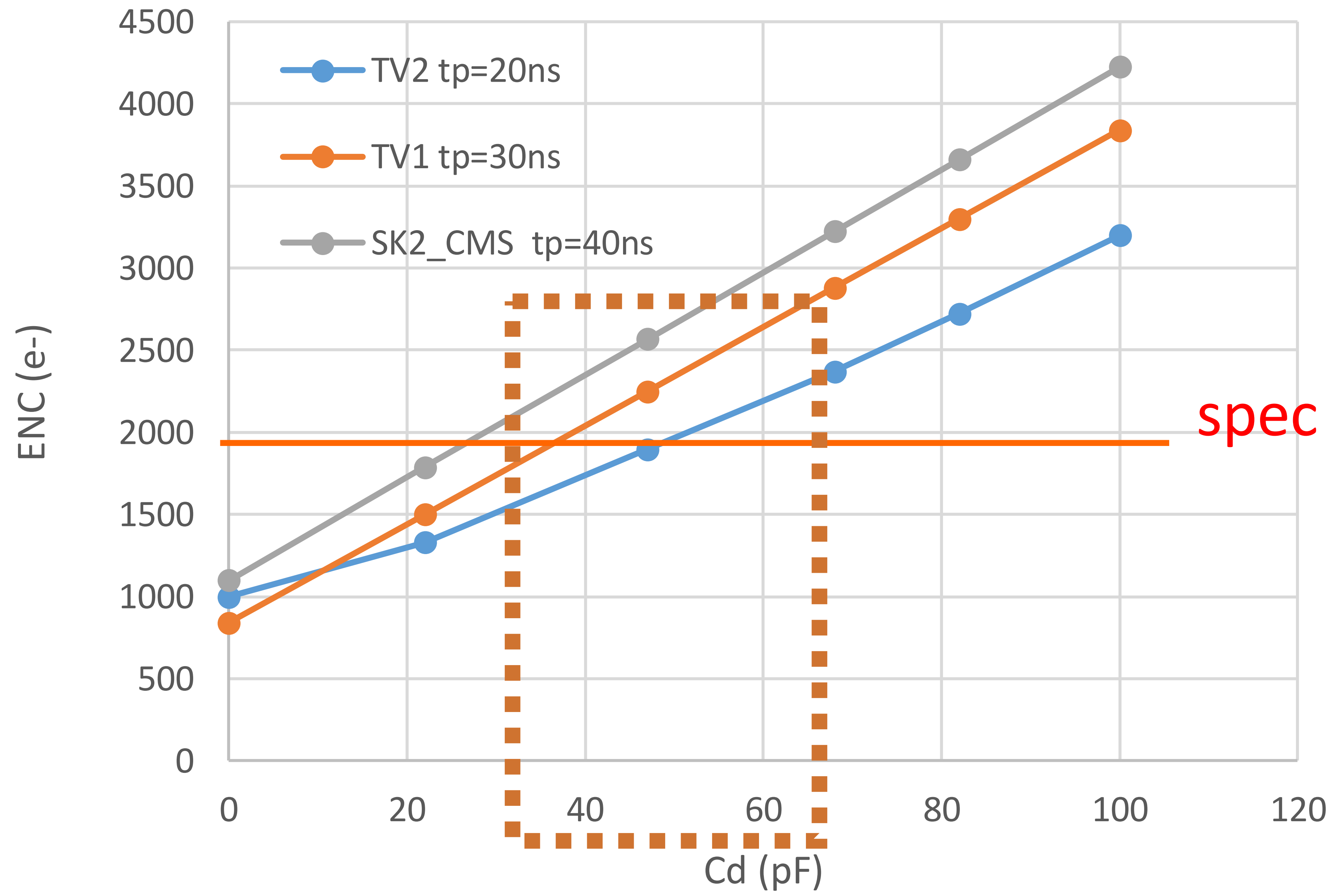
TEST VEHICLES FOR HGCROC [Q4 2016 – Q1 2017]

- CMOS 130 nm:
  rad hard technology
- 6 positive + 6 negative input preamplifiers
- 1 baseline channel
- 4 discriminators for TOT
- CR-RC shapers: HG and LG
- Digital part for noise coupling tests



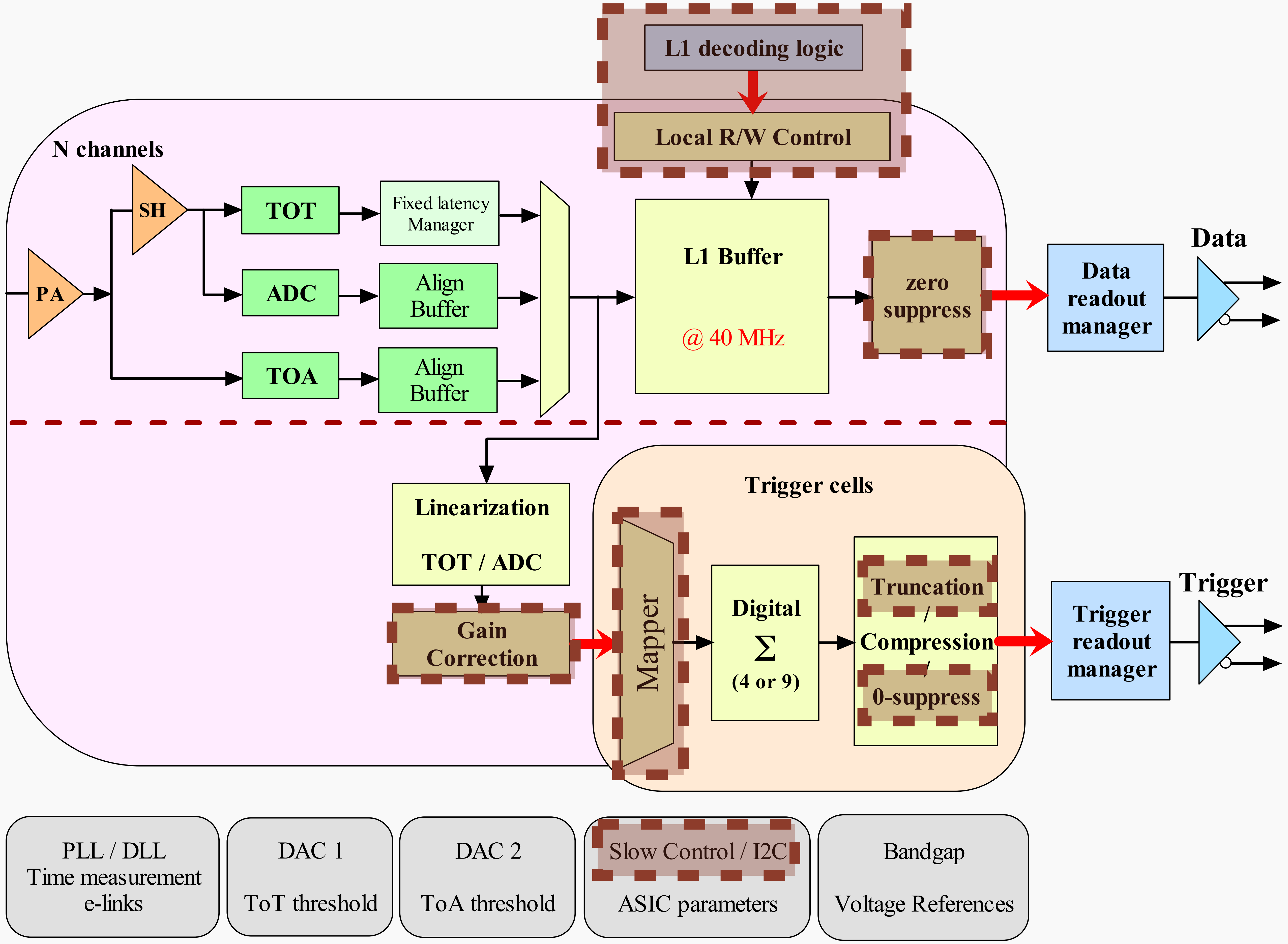
- Groups 8 channels with variants of ADC and shapers
- Positive preamps
- Global 10b-DAC
- 11 bits SAR-ADC, 32x512 RAM





- Building blocks successfully tested
- Noise in TV2 as in specification

HGCROCv1 [Q3 2017]



- 32 channels for development/cost
- Dual polarity (for p- or n-type silicon)
- TOA, TOT with 2 variants: low power or DLL
- 11-bit SAR ADC @ 40MHz
- Simplified Trigger path: no ZS, only 4 sums
- Data readout @ 320MHz
- Slow Control with triple voting (shift register like SK2-CMS)
- Digital blocks with simplified architecture
- Services: bandgap, PLL, 10b DAC

*Not yet included

- No interface to GBT/concentrator yet

HGCAL TRIGGER FLOW

Front-end

HGCROC
~300 Tb/s
Concentrator
~40 Tb/s

- Resolution and granularity reduction, formation of trigger cells (TC)
- Selects fraction of trigger cells (threshold or fixed number of highest energy TC)

Back-end
Trigger primitive
generator

TPG Stage 1
~20 Tb/s
TPG Stage 2
~2 Tb/s

- Dynamical 2D clustering of trigger cells per layer
- Formation of 3D clusters — trigger primitives (TP)

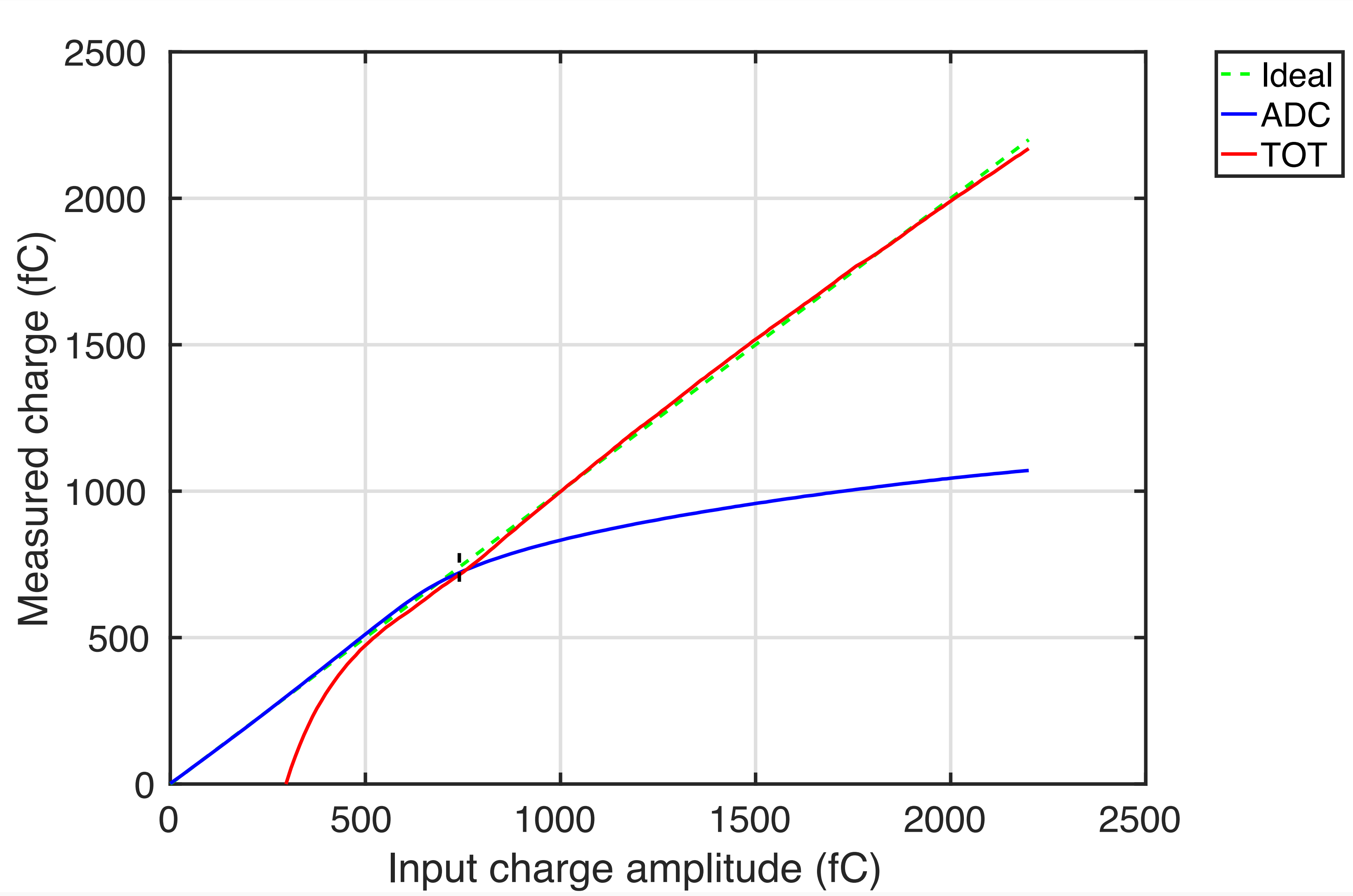
CMS
Trigger

Correlator
Global trigger

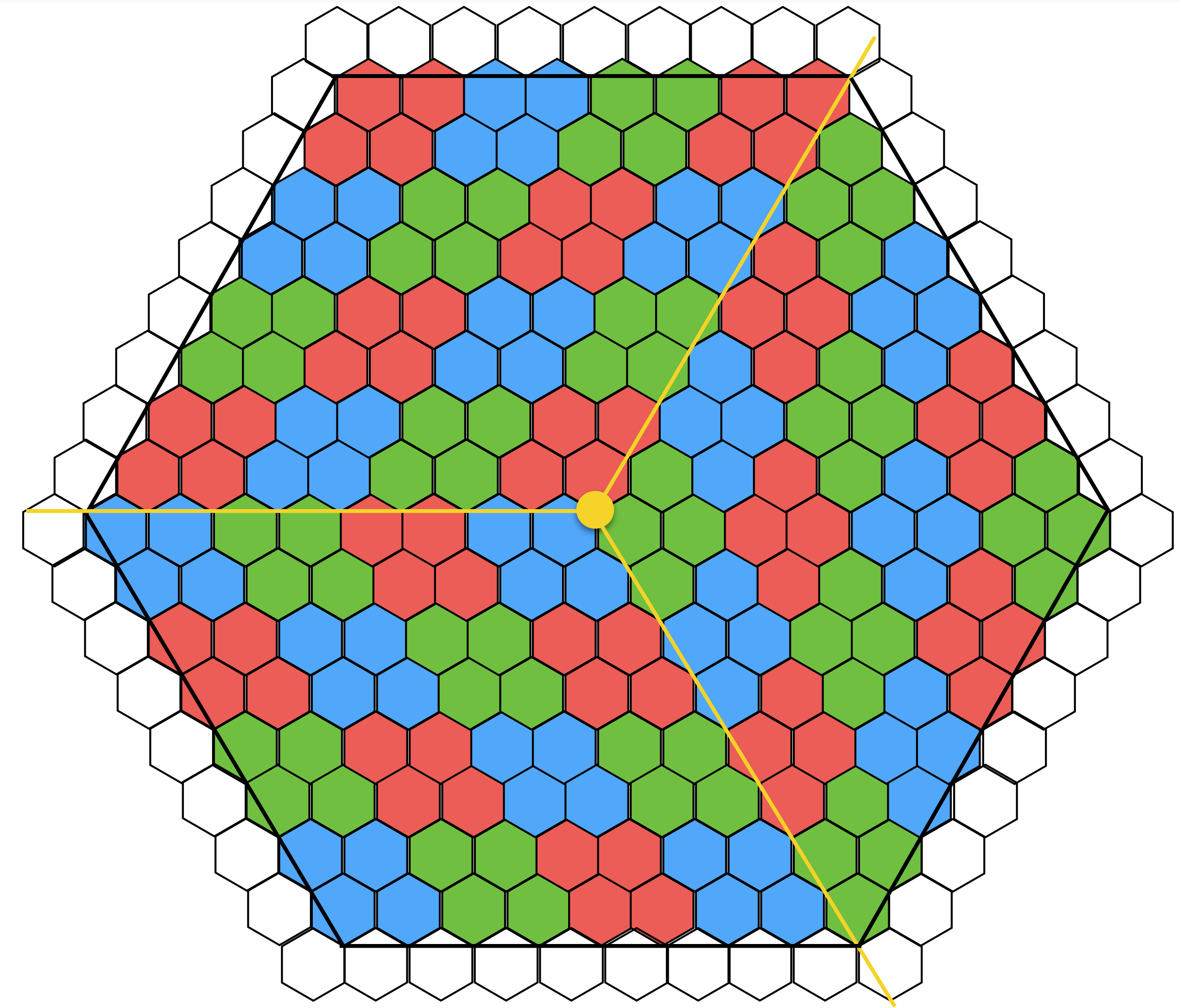
- L1 trigger correlator with input from track trigger
- Central CMS L1 trigger

TRIGGER: HGCROCv1

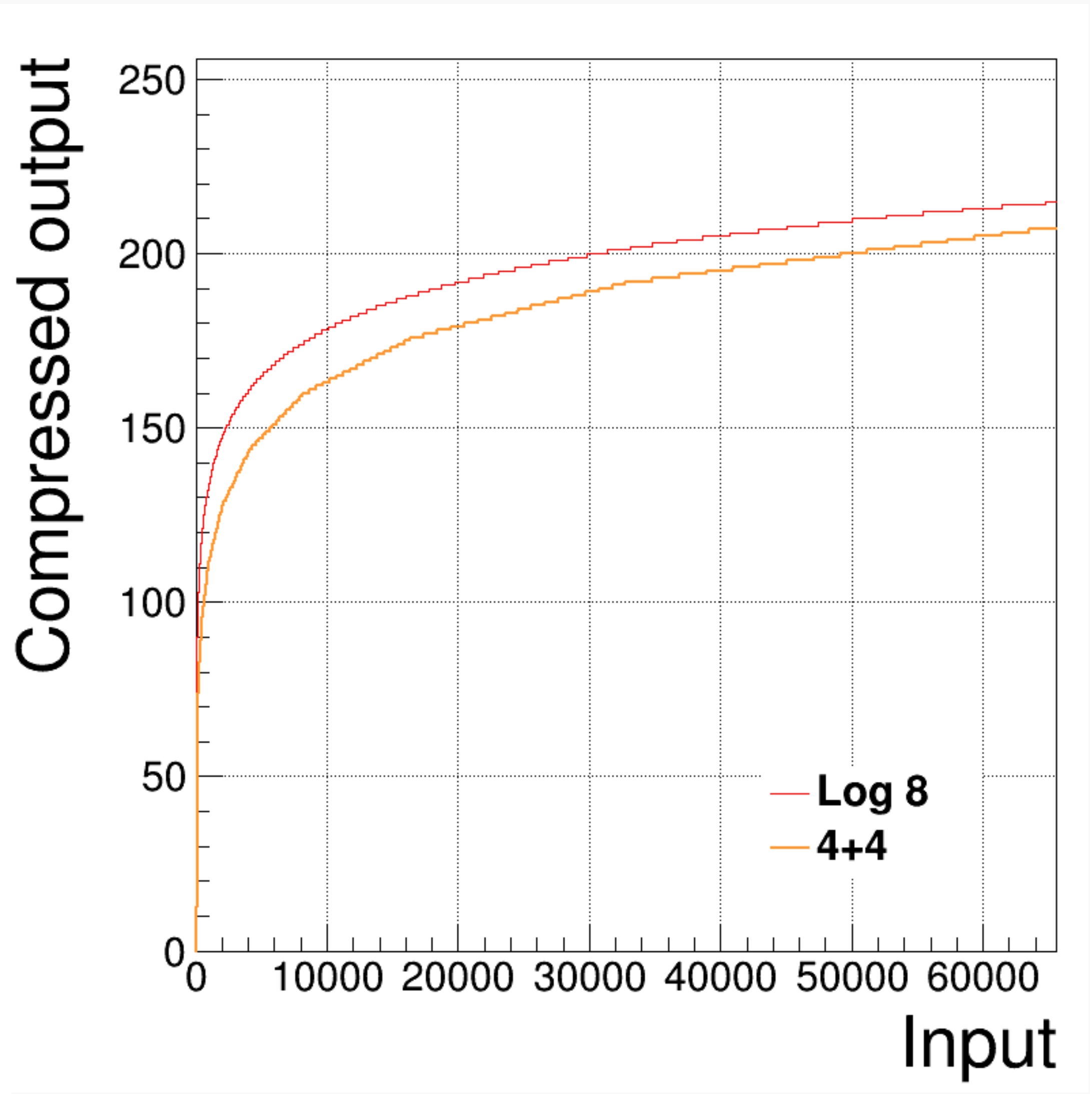
- Reduced energy resolution:
  - ADC/TOT linearization: automatic switching
  - Digitized charge data:
    - Gain: 11-bit ADC ➔ LSB @ 0.1 fC
    - TOT: 12-bit TDC ➔ LSB @ 2.5 fC
  - Compensate LSB ratio (~25) ➔ 17 bits
- Reduced granularity:
  - 4 (9) cells per Trigger Cell (48 per wafer)
  - Sum of 4 channels ➔ 17+2 bits
- Compression:
  - 4+4 encoding ➔ 8 bits



ADC/TOT linearisation



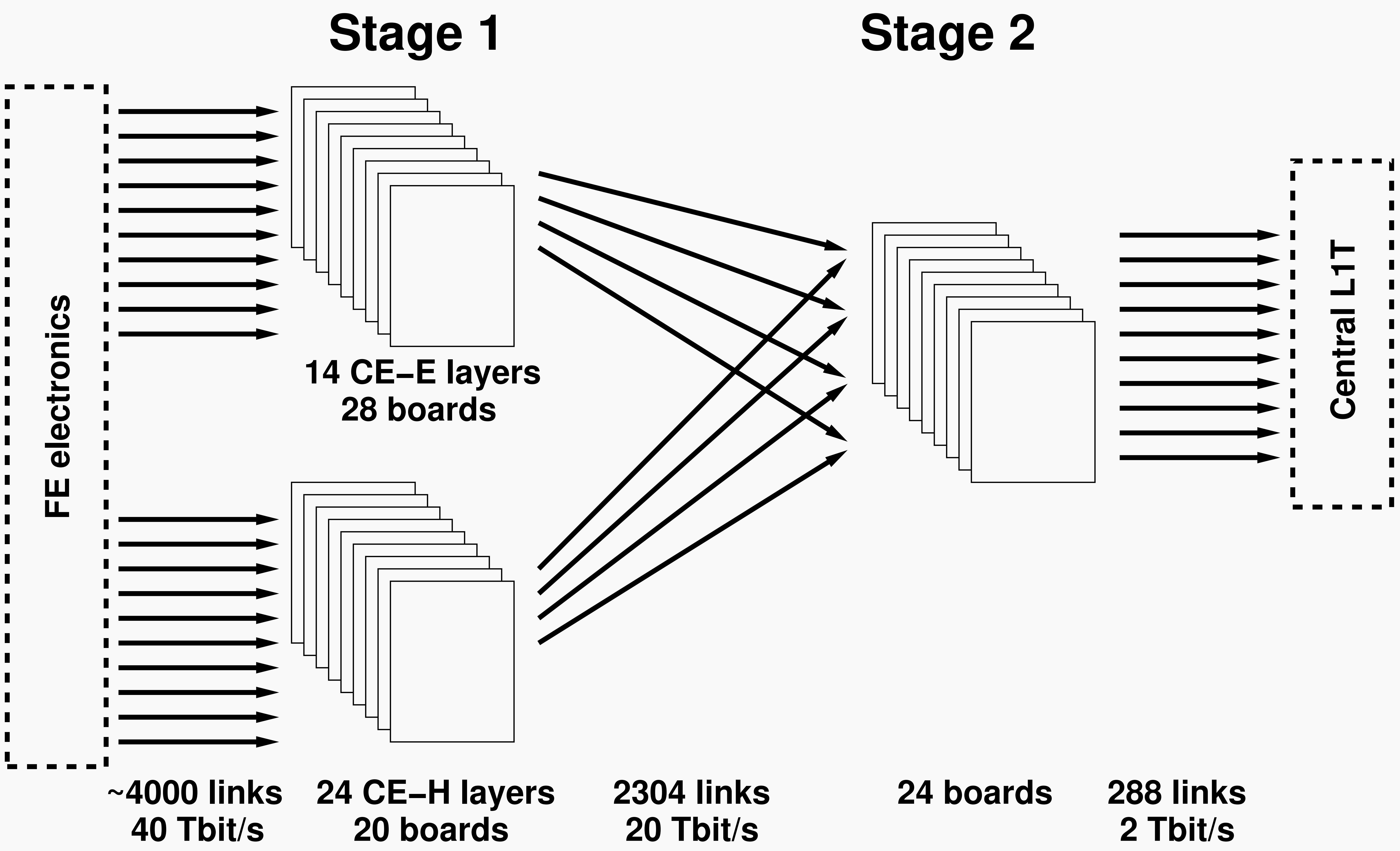
Trigger Cells



Data compression

BACK-END: TRIGGER PRIMITIVE GENERATOR

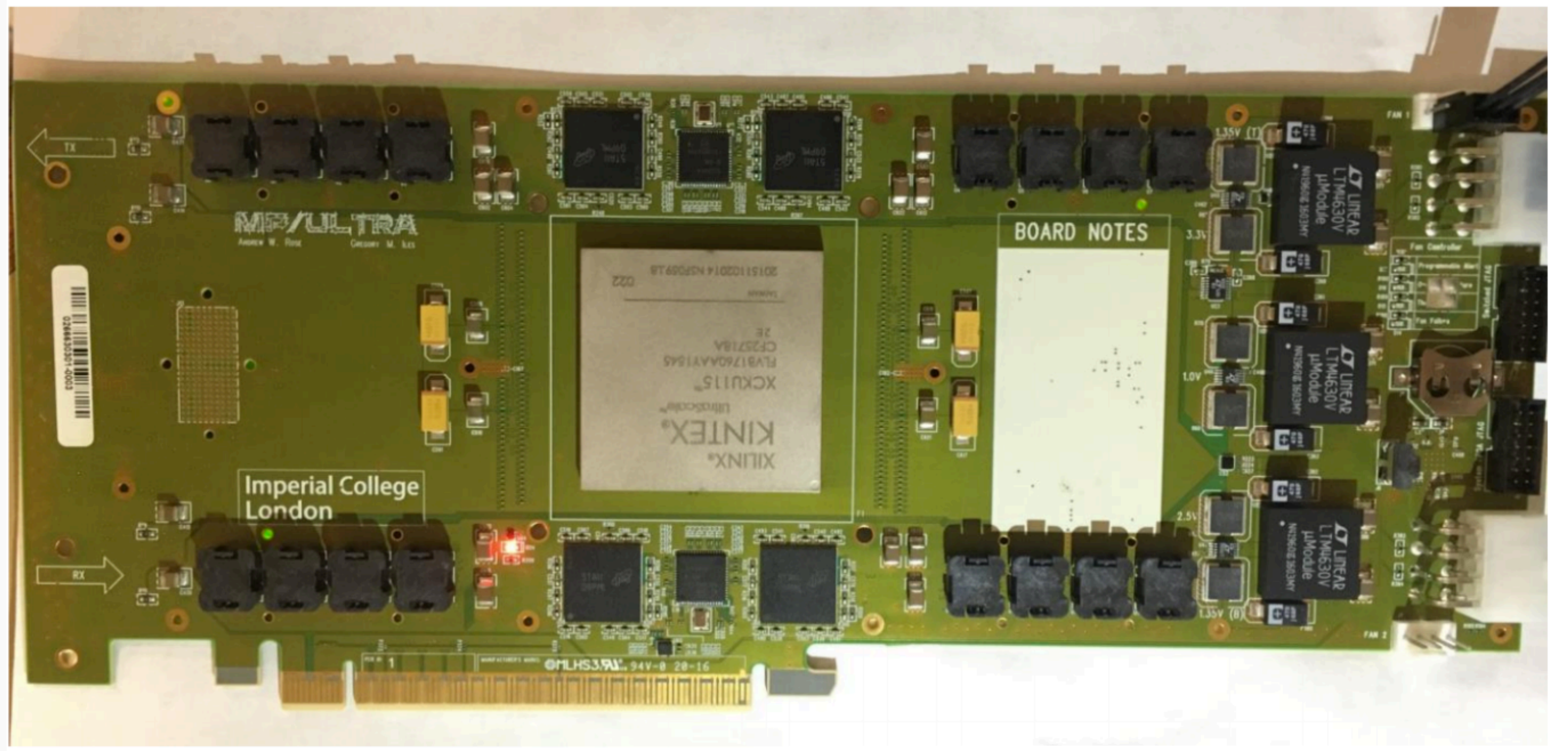
- Stage 1:
  - Dynamical clustering based on the Nearest Neighbour TCs generates **2D clusters** in each trigger layer
- Stage 2:
  - Creation of **3D-clusters** exploiting the longitudinal development of the shower using the projected position of each 2D cluster to identify its direction



- The Stage 1 –> Stage 2 data transmission is **x24 time-multiplexed** in order for all data from one endcap to be processed by one single FPGA

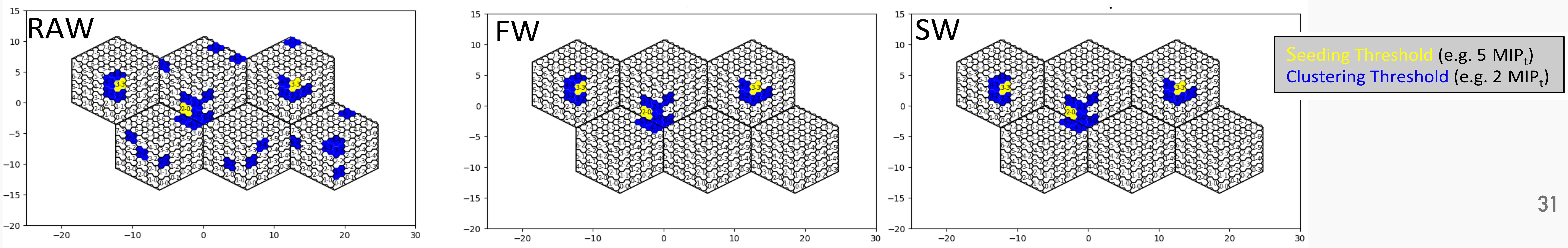
BACK-END: TPG HARDWARE

- Both DAQ and TPG require boards with high I/O and significant processing power
- Aim to use generic boards developed for the whole CMS trigger and DAQ systems, not only HGCAL
  - ATCA format
  - ~100 I/O links up to 16 or 25 Gbit/s in and out
  - Ultrascale(+) FPGA(s) for processing



MPUltra - up to 96 links in and out, each ~16 Gb/s

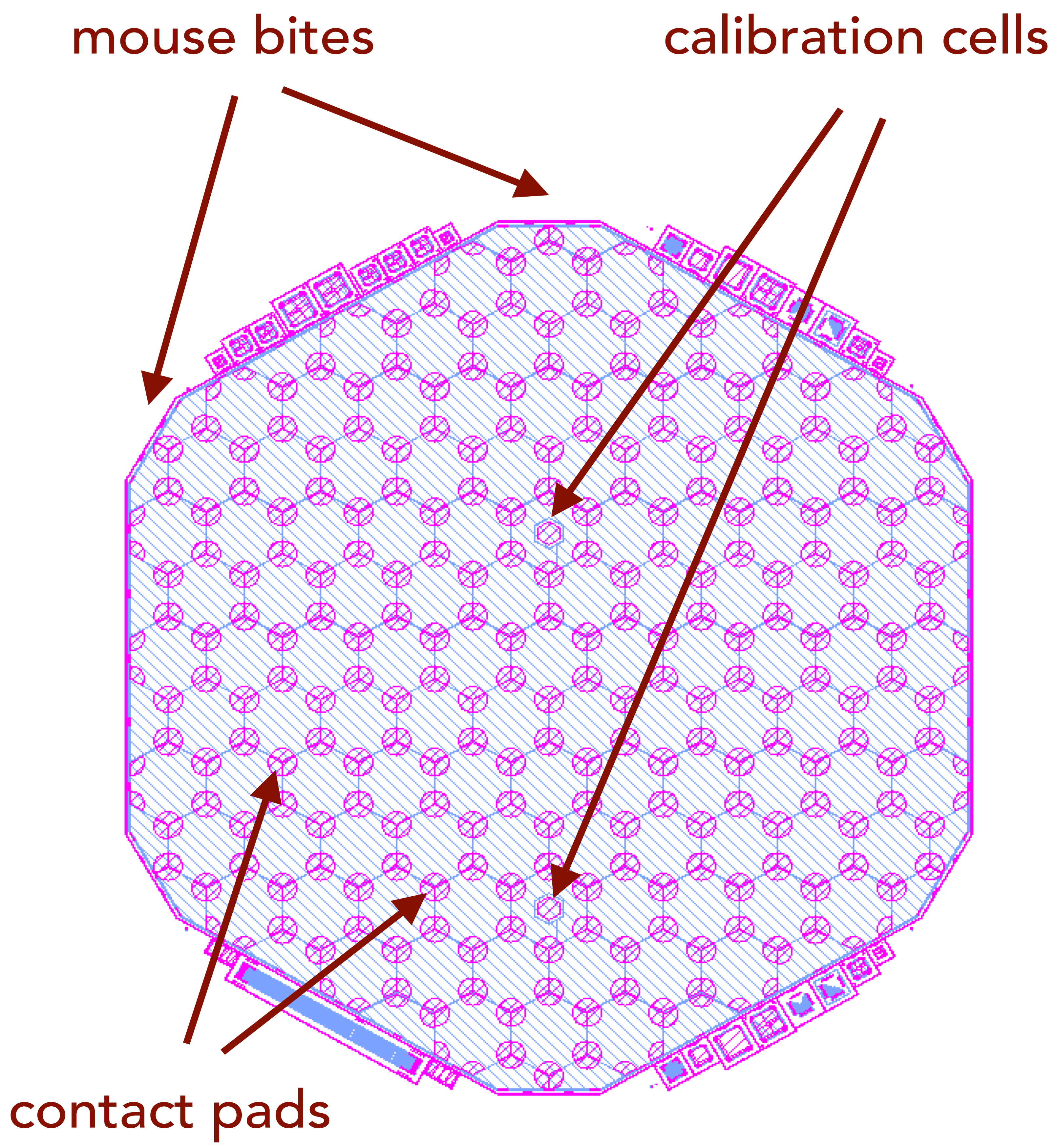
- Firmware simulations of the stage 1 algorithms show perfect agreement with software



HGCAL SI-SENSOR AND WAFERS

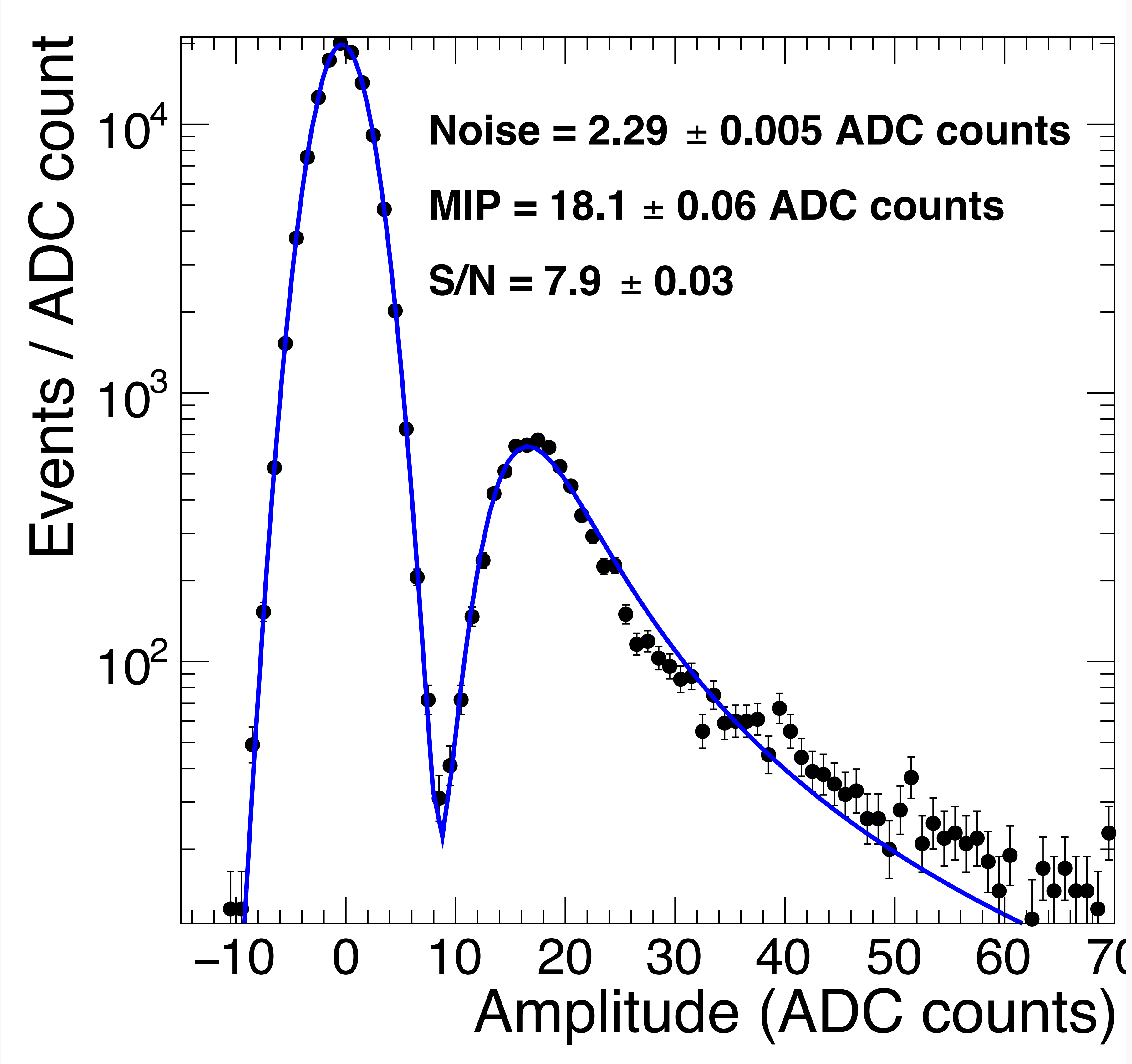
- **Hexagonal geometry** as largest tile-able polygon
  - **6" and 8"** sensors considered
  - Cell sizes of **~0.5 cm^2 and ~1 cm^2**
  - Cell capacitance of **~50 pF**
  - Will most likely need n-on-p for inner layers
- Some design goals
  - **1kV sustainability** to mitigate radiation damage
  - **Four quadrants** to study inter-cell gap distance and its influence on V_{bd}, C_{int} and CCE
- A few more details about those sensors
  - Active thickness by **deep diffusion or thinning**
  - Inner **guard ring is grounded**, outer guard ring is floating
  - Truncated tips, so called **mouse bites,** for module mounting
  - **Calibration cells** of smaller size for single MIP sensitivity at end of life

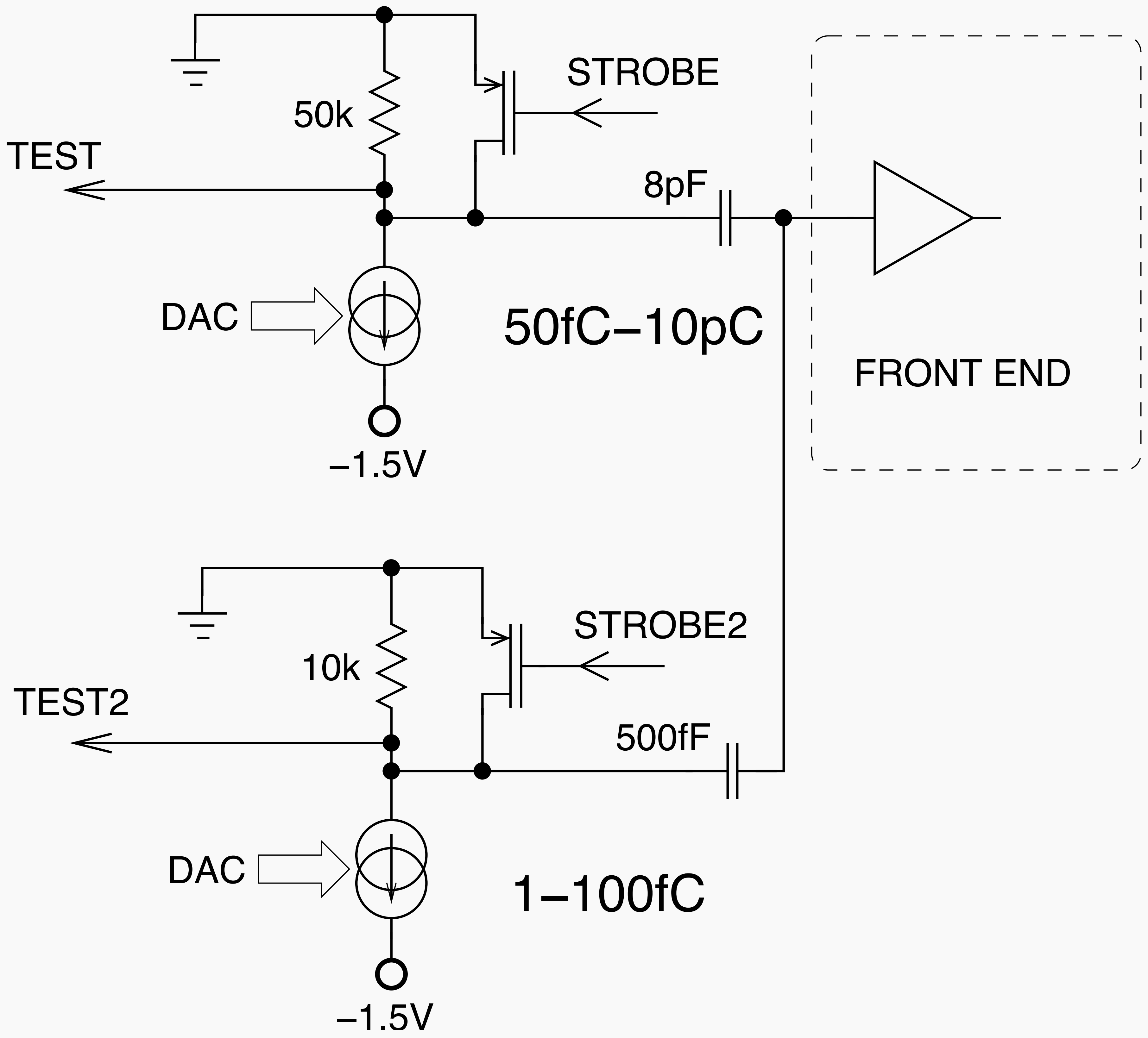
From TIPP-2017



Hamamatsu 6" 128ch design

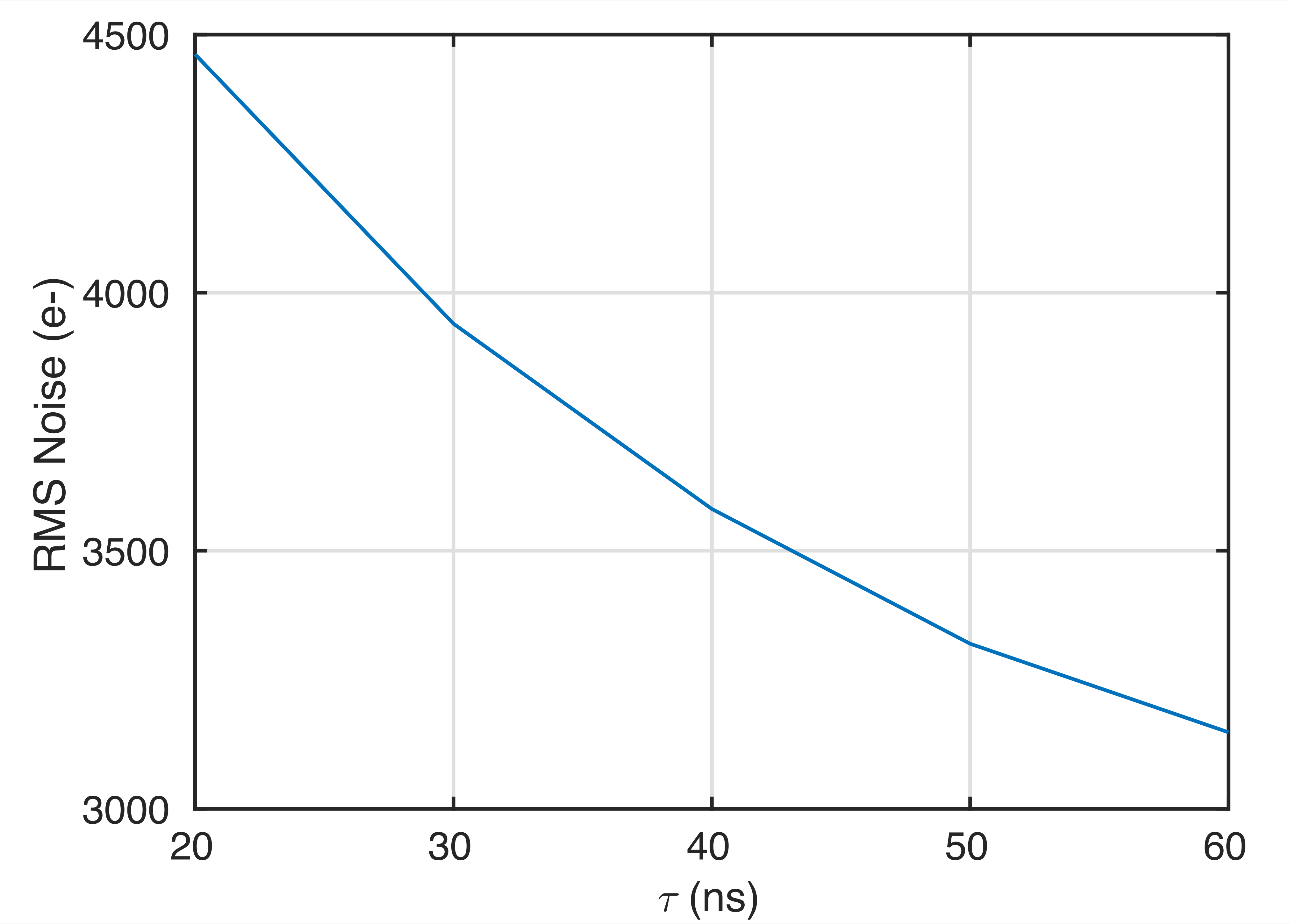
HGCAL CALIBRATION

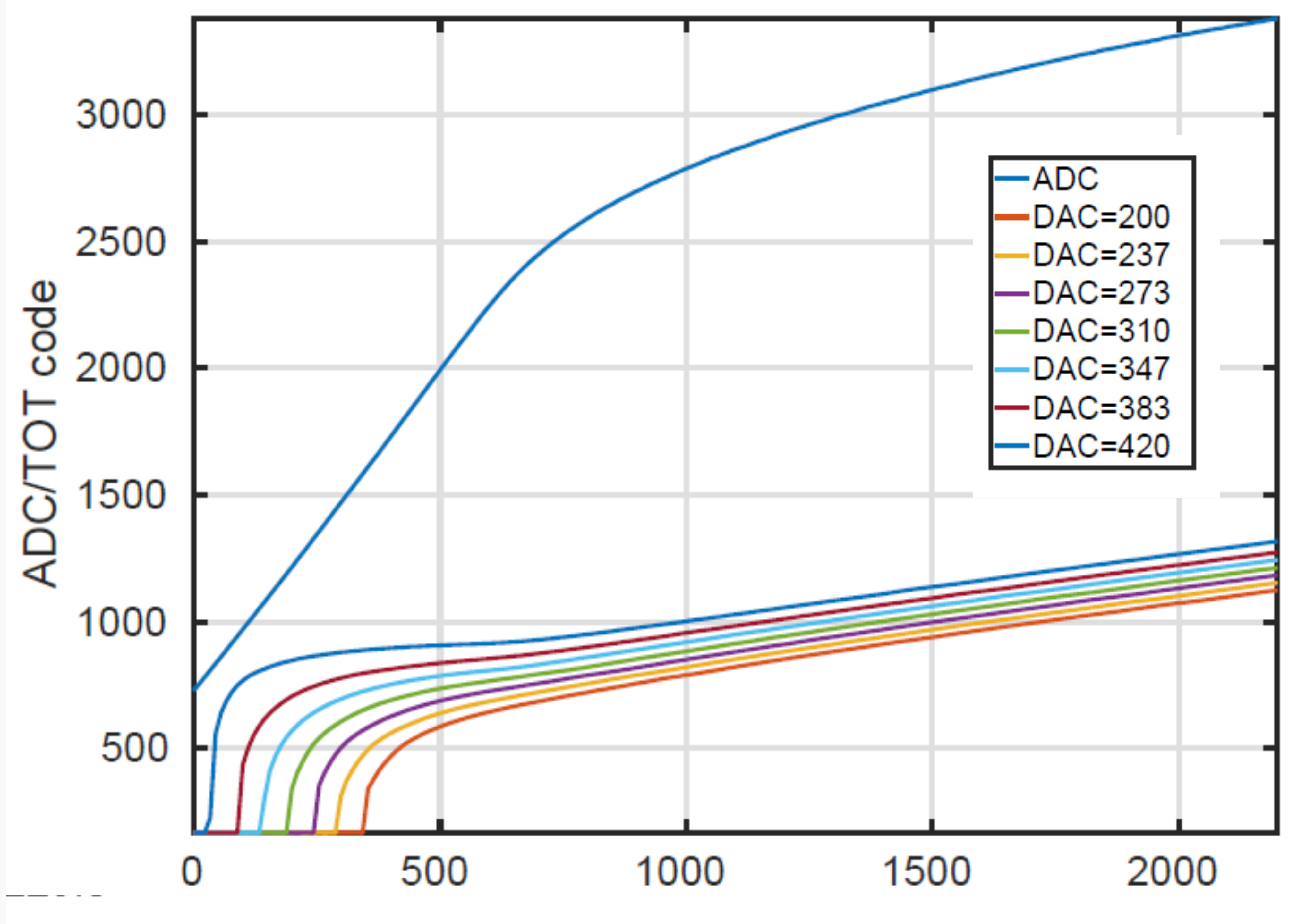




- MIP calibration for the absolute calibration of the ADC
- A charge injection circuit with a large dynamic range will be used for covering both the ADC and TOT ranges

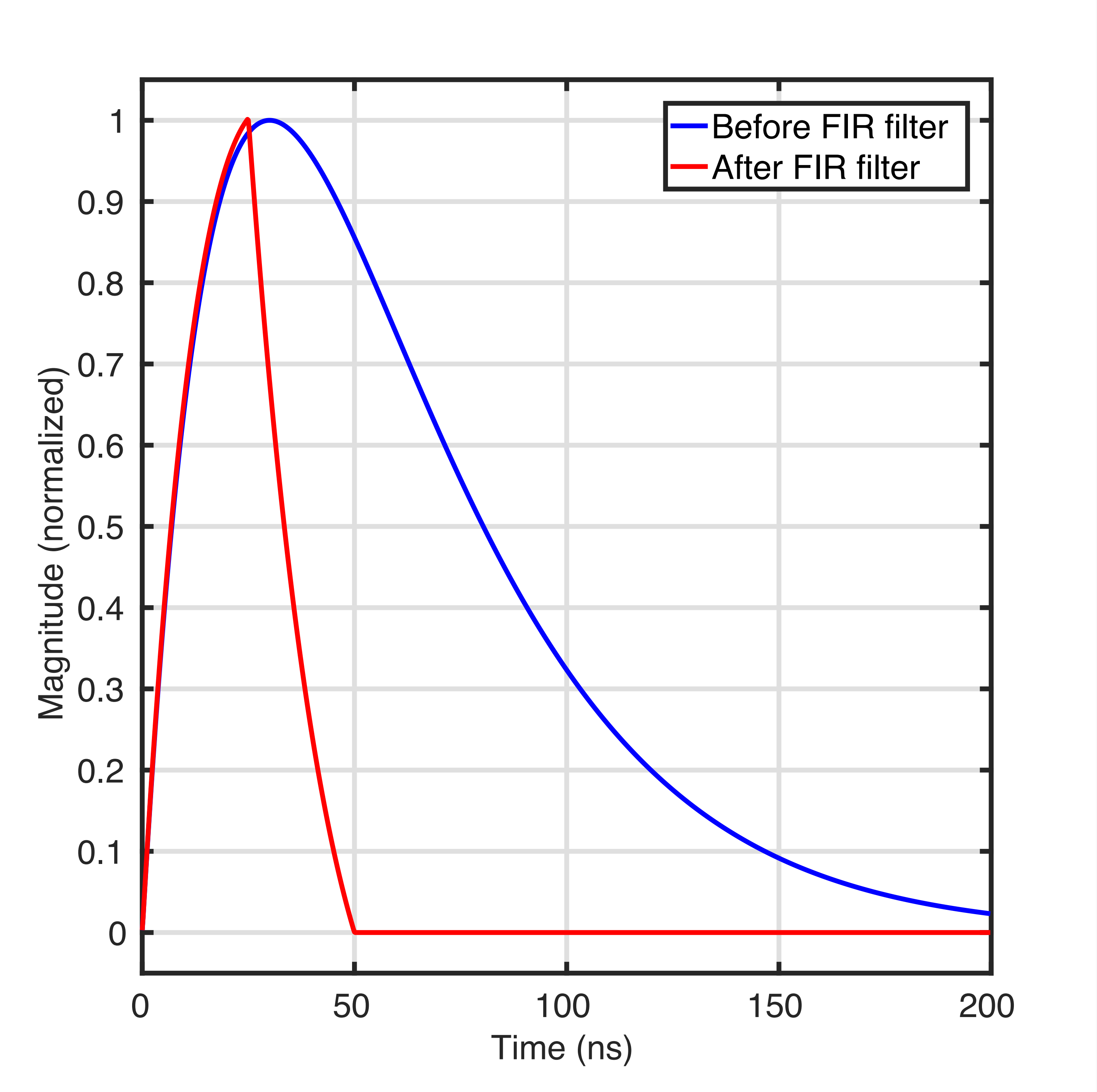
SKIROC2CMS

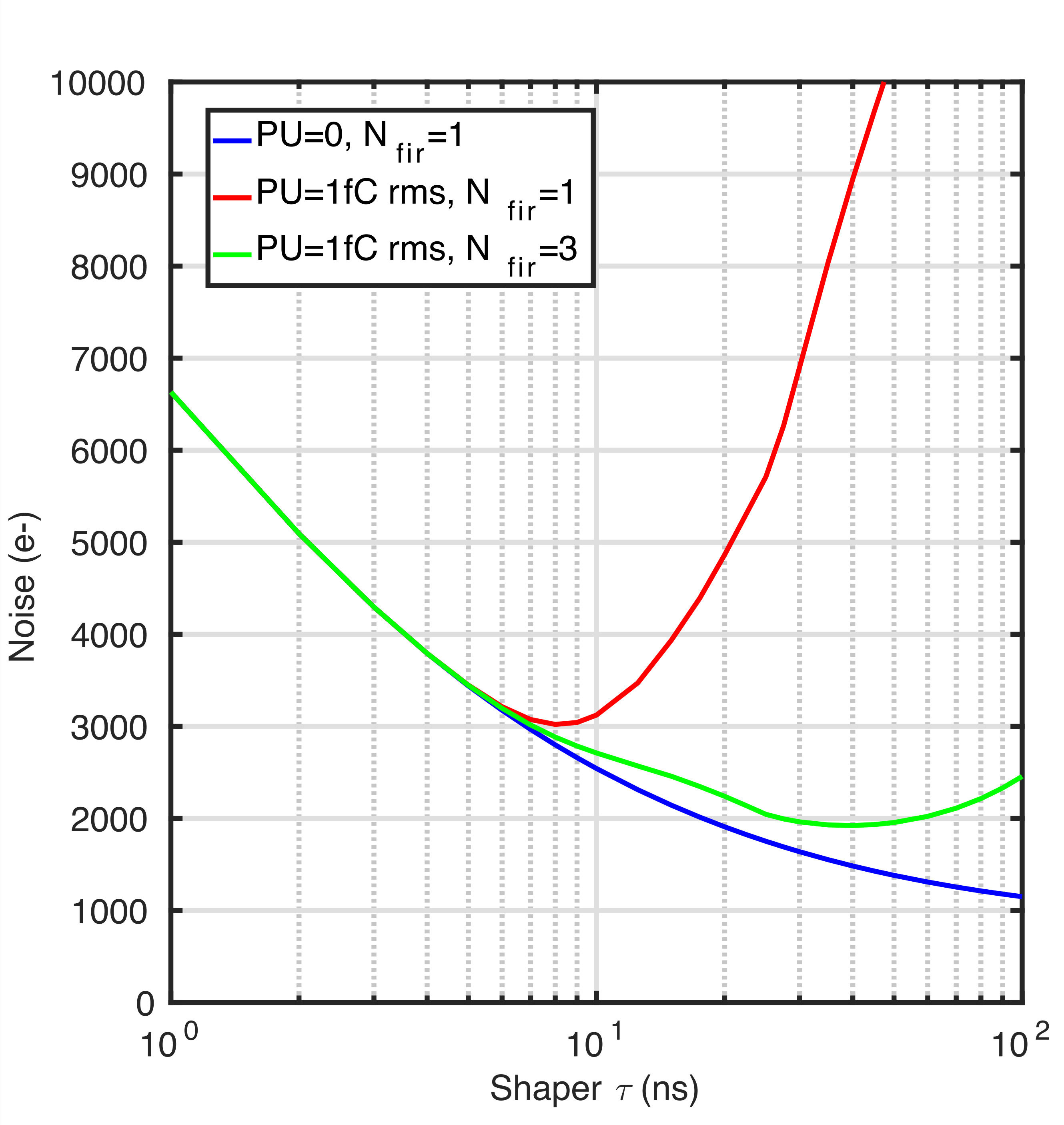




- Measurements from the SKIROC2_CMS currently used for HGCAL testbeams
- Highlights the increasing difficulty of achieving good noise performance at short shaping time

Using FIR filters to manage occupancy





- 3-coefficient analog or digital finite impulse response (FIR) filters can help managing the high occupancy
- Simulated for e_n=0.5 nV/$\sqrt{Hz}$, C_d=80 pF, 10-bit signal to noise ratio after the preamplifier, with and without 1 fC (6250 e-) pileup noise in preceding samples

CONCENTRATOR ASIC

- Basic task: receive, select and transmit trigger and data
  - In two separate chains
- HGCROC trigger output: 4 e-links @ 1.28 Gb/s
- HGCROC data output: 1 e-link @ 1.28 Gb/s
- Trigger logic:
  - Reducing event size
  - Threshold or fixed number of highest trigger cells selection
  - Transmiting selected trigger cells and global sums
- Design and production to be in sync with VFE ASIC