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CSC 142

Homework 6

1.
2.

2-way set associativity
2 blocks per set

index	V	tag		4 words per block		
0000						
0001						
0010						
0011						
0100						
0101						
0110						
0111						
1000						
1001						
1010						
1011						
1100						
1101						
1110						
1111						

0000						
0001						
0010						
0011						
0100						
0101						
0110						
0111						
1000						
1001						
1010						
1011						
1100						
1101						
1110						
1111						

3. index – 16 sets – 4 bits
   word offset – 4 words per block – 2 bits
   byte offset – 1 byte per word – 0 bits

Dec addr	block addr	word offset	hit/miss
2	0000	10	miss
3	0000	11	miss
11	0010	11	miss
16	0100	00	miss
21	0101	01	miss
13	0011	01	miss
64	0000	00	miss
48	1100	00	miss
19	0100	11	miss
11	0010	11	hit
3	0000	11	hit
32	1000	00	miss

2-way set associativity
2 blocks per set

index	V	tag	00	01	10	11
0000			Mem[64]		Mem[2]	Mem[3]
0001			Mem[4]		Mem[6]	
0010						Mem[11]
0011				Mem[13]		
0100			Mem[16]			Mem[19]
0101				Mem[21]	Mem[22]	
0110						Mem[27]
0111						
1000			Mem[32]			
1001						
1010						
1011						
1100			Mem[48]			
1101						
1110						
1111						

0000						
0001						
0010						
0011						
0100						
0101						
0110						
0111						
1000						
1001						
1010						
1011						
1100						
1101						
1110						
1111						

4. One set in a fully-associative cache.
5. One block per set in a direct-mapped cache.
6. 4-way set associative is 4 blocks per set.

7.

5.6.1 P1 – 1 / 0.66*10^-9 = 1.5 GHz
P2 – 1 / 0.9*10^-9 = 1.11 GHz

5.6.2 P1 – 0.66ns + 0.08 * 70ns = 6.26ns
P2 – 0.90ns + 0.06 * 70ns = 5.1 ns

5.6.3