1st Programming Assignment, Intro to Verilog, a Hardware Description Language (HDL)

The four diagrams below depicts different logic circuits that can be simulated with Verilog programs on the gate-logic level.

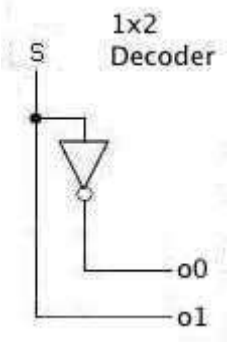
The example programs are for `1x2 decoder` and `2x1 multiplexer`. Program the other two circuits will be for you to work on. Submit your source files: first name them as ***decoder2x4.v*** and ***mux4x1.v*** in your own directory, then submit both program files into the single folder called ***1stPrgAssig*** of the folder of your name (created by the instructor). **Add your full name in the beginning of the program (in a comment section)!**

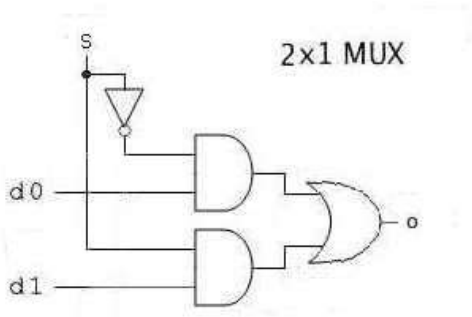
The runtime of your programs should look like these: **Program Output**.

Follow the instruction linked below to access the dropbox host and submit your source files in the correct dropbox folder ***1stPrgAssig*** on host Voyager. Do not submit your runtime executable **a.out** or other files such as the program output.

At the start of each program, put your name in the comments.

To connect to the programming host, launch two **PuTTy** (PC) or **terminals** (Mac) so one for editing programs and the other compiling and running. Connect to the host ***atoz, sp1, sp2, or sp3*** for Verilog use. Via either host ***titan.ecs.csus.edu*** or ***athena.ecs.csus.edu*** and change to atoz, etc., if you are outside of the ECS net (in some other building or at home).

<table>
<tr>
<td> 

Program Listing</td>
<td> 

Program Listing</td>
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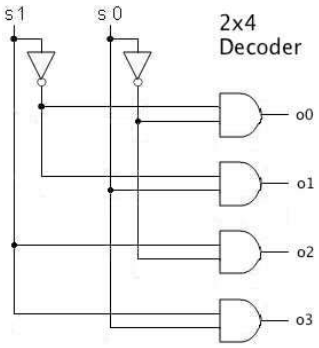
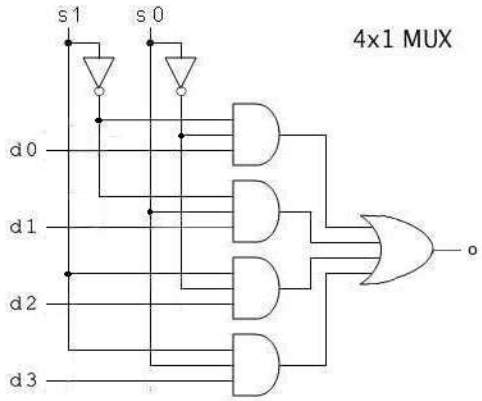
<tr>
<td> 

Program decoder2x4.v and submit it</td>
<td> 

Program mux4x1.v and submit it</td>
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At a Linux shell command prompt, issue shell commands to make subdirectories (subfolders) in order to organize your class work there. Learn to use editor such as vi, etc. will enhance your software development skills. Learning materials are linked in the following.

- Useful Linux and vi Commands