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41 **Chapter 1**

42 **Introduction**

43 Pixel detectors, members of the semiconductor detector family, have significantly been used since
44 () at the first accelerator experiments for energy and position measurement. Because of their
45 dimension (today $\sim 30 \mu m$ or even better) and their spatial resolution ($\sim 5\text{-}10 \mu m$), with the
46 availability of technology in 1980s they proved to be perfectly suitable for vertex detector in the
47 inner layer of the detector.

48 Technological development has been constant from then on and today almost every high energy
49 physics (HEP) experiment employs a pixels detector; hybrid pixel currently constitute the state-
50 of-art for large scale pixel detector but experiments began to look at the more innovative monolithic
51 active pixels (MAPS) as perspective for their future upgrades, as BelleII, or they already have
52 installed them, as ALICE.

53 Requirement imposed by accelerator are stringent and they will be even more with the increase
54 of luminosity/intensity, in terms of radiation hardness, efficiency and occupancy, time resolution,
55 material budget and power consumption.

56 Qual è invece la richiesta per la dosimetria?

57

⁵⁸ **Chapter 2**

⁵⁹ **Pixel detectors**

⁶⁰ **2.1 Signal formation**

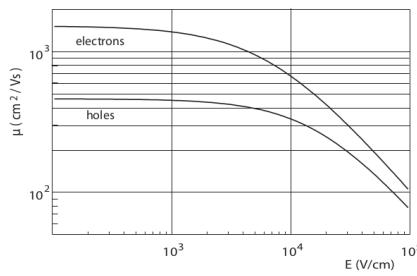
⁶¹ When a charge particle passes through a pixel and loses energy by ionization a part of that
⁶² energy is used to generate electron-hole pairs (another part is used for other processes, as the
⁶³ lattice excitation) which are then separated by the electric field and collected at their respectively
⁶⁴ electrodes (p for holes and n for electrons)¹; by the drift of these charges, a signal i_e is generated
⁶⁵ on the electrode e as stated by the Shockley–Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (2.1)$$

⁶⁶ where $v(t)$ is the instantaneous velocity of the charge q and E_{WF} is the weighting field, that is the
⁶⁷ field obtained biasing the electrode e with 1V and all the others with 0V. The drift velocity of the
⁶⁸ charge depends on the electric field and on the mobility of the particle:

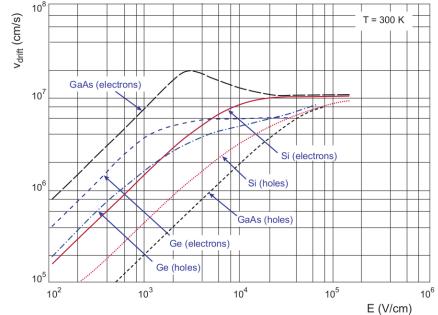
$$v = \mu(E) E \quad (2.2)$$

⁶⁹ where $\mu(E)$ is a function of the electric field and is linear with E only for small E : at higher values
⁷⁰ the probability of interactions with optical phonons increases and the mobility drops and this leads
⁷¹ to an independence of the velocity from the electric field (fig. 2.1b).



(a) Typical values for electrons and holes mobility in

silicon at room temperature are $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$, $\mu_h = 500$



(b) Drift velocity at room temperature in different semiconductors

⁷² The average energy needed to create a pair at 300 K in silicon is $w_i = 3.65 \text{ eV}$, that is more
⁷³ than the mean ionization energy because of the interactions with phonon, since for a minimum
⁷⁴ ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is
⁷⁵ 0.28 keV/ μ , hence the number of e/h pairs is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (2.3)$$

¹Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout

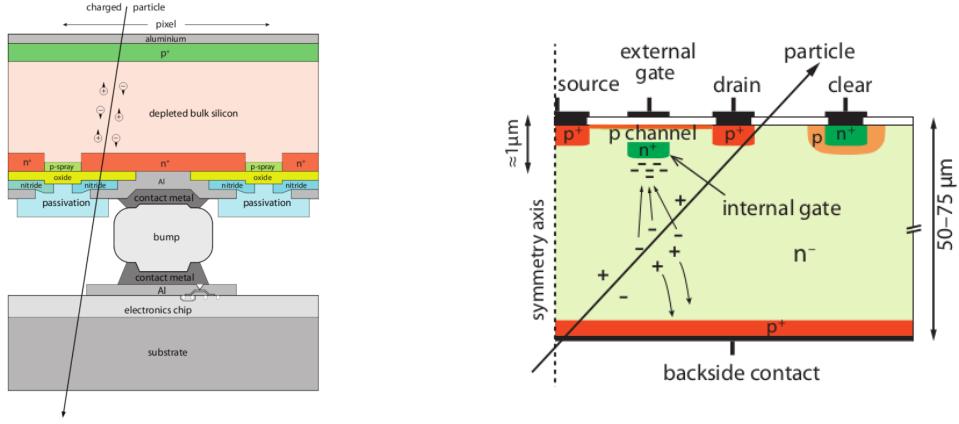


Figure 2.2: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

76 CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALEMTE SI AGGIUNGE IL
 77 FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. IL FATTORE DI FANO È
 78 0.115 NELL SILICIO. ecc It is fundamental that pairs e/h are produced in the depleted region
 79 of the semiconductor where the probability of recombination with charge carriers is low to avoid
 80 loss of signals. Pixel detectors are then commonly reverse biased: a positive bias is given to the
 81 n electrode and a negative to the p to grow the depletion zone in the epitaxial layer below the
 82 electrode. The width of the depletion region is related with the external bias V_{ext} , the resistivity
 83 ρ and also with the dopant:

$$d_n \sim 0.55 \sqrt{\frac{\rho}{\Omega cm} \frac{V_{ext}}{V}} \mu m \quad (2.4) \quad d_p \sim 0.32 \sqrt{\frac{\rho}{\Omega cm} \frac{V_{ext}}{V}} \mu m \quad (2.5)$$

84

85

86

87 For that reason high resistivity wafers ($100 \Omega cm - k\Omega cm$) are typically preferred because they
 88 allow bigger depletion zone with smaller voltage bias.

89 2.2 Hybrid pixels

90 Hybrid pixels are made of two parts (fig. 2.2a), the sensor and the electronics: for each pixel these
 91 two parts are welded together through microconnection (bump bond).

92 They provide a practical system where readout and sensor can be optimized separately, although
 93 the testing is less easy-to-do since the sensor and the R/O must be connected together before.

94 In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-
 95 cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high
 96 levels of radiation, and also expensive.

97 A critical parameter for accelerator experiments is the material budget, which represents the main
 98 limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are
 99 thicker (\sim hundreds of μm) than monolithic ones (even less than $100 \mu m$), using the latter the
 100 material budget can be down by a third: typical value for hybrid pixels is 1.5 % X_0 per layer,
 101 while for monolithic 0.5 % X_0 .

102 Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,
 103 by the way, a bigger cooling system leading in turn to an increase in material too.

104

105 DEPFET are the first attempt towards the integration of the front end (FE) on the sensor bulk:
 106 they are typically mounted on a hybrid structure but they also integrate the first amplification
 107 stage.

108 Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor
 109 (a p-channel in fig. 2.2b): an hole current flows from source to drain which is controlled by the
 110 external gate and the internal gate together. The internal gate is made by a deep $n+$ implant
 111 towards which electrons drift after being created in the depletion region (to know how the signal

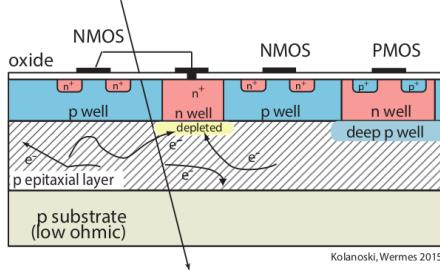


Figure 2.3: Concept cross-section of CMOS MPAS pixel

is created in a pixel detector look at appendix A); the accumulation of electrons in the region underneath the n implant changes the gate potential and controls the transistor current.
DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and the large depletion region. But, since they need to be connected with ASIC the limiting factor still is the material budget.

2.3 CMOS MAPS and DMPAS

Monolithic active pixels accommodate on the same wafer both the sensor and the front end electronics, with the second one implanted on top.
MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the development of the electronic sector which guarantees the decrease in CMOS transistors dimension at least every two years, as stated by the Moore's law².
As a matter of fact the dimension of components, their organization on the pixel area and logic density are important issues for the design and for the layout; typically different decisions are taken for different purposes.

Monolithic active pixel can be distinguished between two main categories: MAPS and depleted MAPS (DMPAS).

MAPS (figure a 2.3) have typically an epitaxial layer in range 1-20 μm and because they are not depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the collection could be partial especially after the irradiation of the detector (look at A for radiation damages), when the trapping probability become higher.
In figure 2.3 is shown as example of CMOS MAPS: the sensor in the scheme implements an n well as collection diode; to avoid the others n wells (which contain PMOS transistor) of the electronic circuit would compete in charge collection and to shield the CMOS circuit from the substrate, additionally underlying deep p well are needed. DMPAS are instead MAPS depleted with d typically in $\sim 25\text{-}150 \mu\text{m}$ (eq. 2.1) which extends from the diode to the deep p-well, and sometimes also to the backside (in this case if one wants to collect the signal also on this electrode, additional process must be done).

2.3.1 DMAPS: large and small fill factor

There are two different sensor-design approaches (figure 2.4) to DMAPS:

- large fill factor: a large collection electrode that is a large deep n-well and that host the embedded electronics
- small fill factor: a small n-well is used as charge collection node

To implement a uniform and stronger electric field, DMAPS often uses large electrode design that requires multiple wells (typically four including deep n and p wells); this layout adds on to the standard terms of the total capacity of the sensor a new term (fig. 2.5), that contributes to the total amplifier input capacity. In addition to the capacity between pixels (C_{pp}) and between the pixel and the backside (C_b), a non-negligible contribution comes from the capacities between wells

²Moore's law states that logic density doubles every two years.

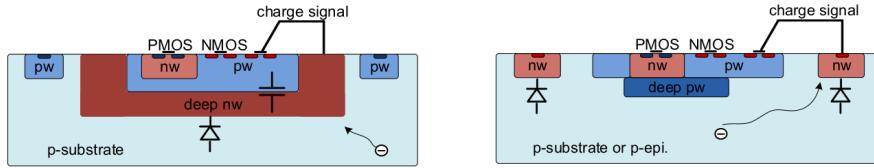


Figure 2.4: Concept cross-section with large and small fill factor

	small fill factor	large fill factor
small sensor C	✓ (< 5 fF)	✗ (~ 100-200 fF)
low noise	✓	✗
low cross talk	✓	✗
velocity performances	✓	✗ (~ 100 ns)
short drift paths	✗	✓
radiation hard	✗	✓

Table 2.1: Small and large fill factor DMAPS characteristics

150 (C_{SW} and C_{WW}) needed to shield the embedded electronics. These capacities affect the thermal
151 and 1/f noise of the charge amplifier and the τ_{CSA} too:

$$ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.6) \quad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.7)$$

153 where g_m is the transconductance, τ_{sh} is the shaping time.

154 Among the disadvantages coming from this large input capacity could be the coupling between
155 the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring
156 electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this problem
is especially connected with the intra wells capacities. So, larger charge collection electrode

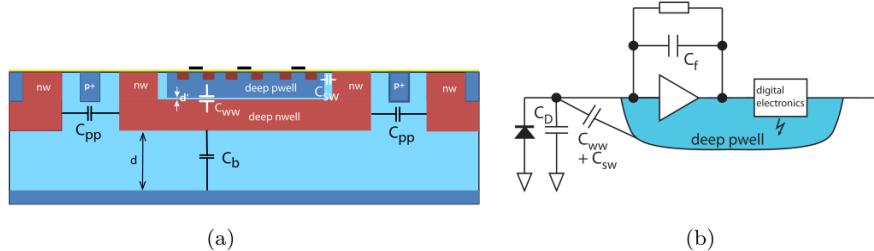


Figure 2.5: C_{pp} , C_b , C_{WW} , C_{SW}

157 sensors provide a uniform electric field in the bulk that results in short drift path and so in good
158 collection properties, especially after irradiation, when trapping probability can become an issue.
159 The drawback of a large fill-factor is the large capacity (~100 fF): this contributes to the noise
160 and to a speed penalty and to a larger possibility of cross talk.

161 The small fill-factor variant, instead, benefits from a small capacity (5-20 fF), but suffers from
162 a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando dei
163 MAPS, devo ripetere qui?**

164 As we'll see these two different types of sensor require different amplifier: the large electrode one is
165 coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.4.1).

167 2.3.2 A modified sensor

168 A process modification developed by CERN in collaboration with the foundries has become the
169 standard solution to combine the characteristics of a small fill factor sensor (small input amplifier
170 capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE

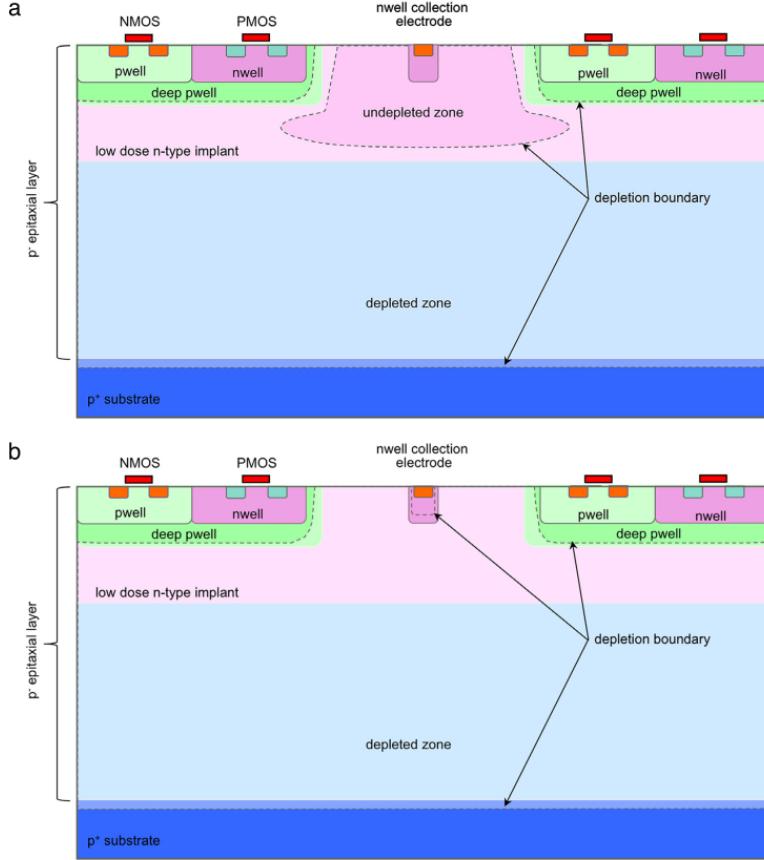


Figure 2.6: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

171 upgrade about ten years [1].

172 A compromise between the two sensors could also be making smaller pixels, but this solution
173 requires reducing the electronic circuit area, so a completely new pixel layout should be though.
174 The modification consists in inserting a low dose implant under the electrode and one its advantage
175 lies in its versatility: both standard and modified sensor are often produced for testing in fact.

176 Before the process modification the depletion region extends below the diode towards the sub-
177 strate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.6).

178 After, two distinct pn junctions are built: one between the deep p well and the n^- layer, and the
179 other between the n^- and the p^- epitaxial layer, extending to the all area of the sensor.

180 Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes
181 can be biased separately³ and this is beneficial to enhance the vertical electric field component.

182 The doping concentration is a trimmer parameter: it must be high enough to be greater than the
183 epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be
184 lower enough to allow the depletion without reaching too high bias.

185 2.4 Analog front end

186 After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.7), ready
187 to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an
188 efficient, high-speed readout architecture, consuming as low power as possible must be provided
189 by the readout integrated electronics (ROIC).

190 Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually
191 often is the only amplification stage) with a reset to the baseline mechanism and a leakage current

³This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

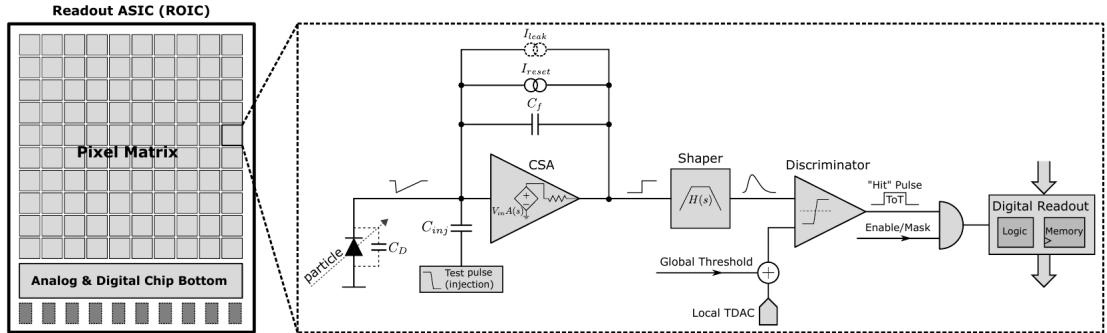


Figure 2.7: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise before the amplification stage in order to not multiply that noise, and chose a reasonable threshold of the discriminator to cut noise-hits much as possible.

2.4.1 Preamplifier

Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled as an operational amplifier (OpAmp) where the gain is determined by the input and feedback impedance (first step in figure 2.7):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.8)$$

Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor MAPS whose signal is already enough high: $v_{in} = Q/C_D \approx 3fC/100 \text{ pF} = 0.03 \text{ mV}$, but it's fine for the small fill factor ones: $v_{in} = Q/C_D \approx 3fC/3 \text{ pF} = 1 \text{ mV}$.

In the case of a resistor feedback, if the signal duration time is longer than the discharge time ($\tau = R_S C_D$) of the detector the system works as current amplifier, as the signal is immediately transmit to the amplifier; in the complementary case (signal duration longer than the discharge time) the system integrates the current on the C_D and operates as a voltage amplifier.

2.5 Readout logic

Readout logic includes the part of the circuit which takes the FE output signal, processes it and then transmit it out of pixel and/or out of chip; depending on the situation of usage different readout characteristics must be provided.

To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is recorded).

A common compromise often made is to save the time over threshold (ToT) of the pulse in clock cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen bits but, being correlated and hopefully being linear with the deposited charge by the impinging particle in the detector, it provides a sufficient information. The ToT digitalization usually takes advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels' matrix. The required timing precision is at least around 25 ns, that corresponds to the period of bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is 40 MHz.

Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they have been read, and then the ToT is obtained from their difference.

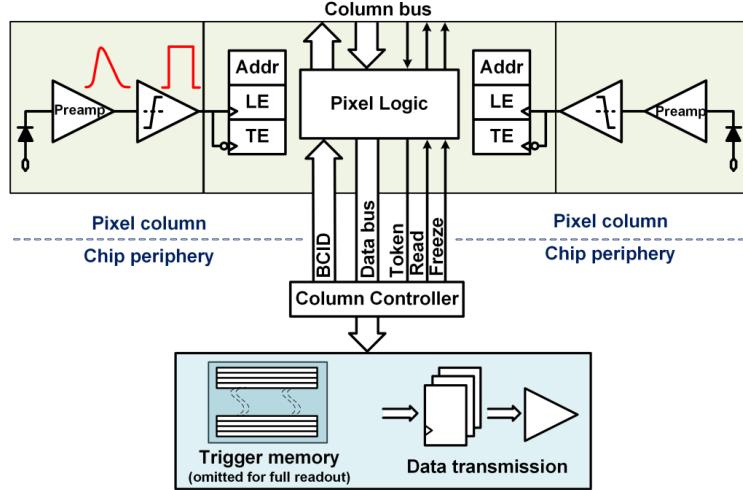


Figure 2.8: Column drain R/O scheme where ToT is saved

Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger system decides if the hit must be stored or not. On one hand the triggered-readout needs buffers and storage memories, on the other the full readout, because there is no need to store hit data on chip, needs an high enough bandwidth.

A triggered readout is fundamental in accelerator experiments where the quantity of data to store is too large to be handled, and some selections have to be applied by the trigger: to give an order of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100 MBit/s [2] (pag. 797).

Typically the trigger signal is processed in a few μs , so the pixel gets it only after a hundred clock cycles from the hit arrival time: the buffer depth must then handle the higher trigger latency.

After having taken out the data from the pixel, it has to be transmitted to the end of column (EoC) where a serializer delivers it out of chip, typically to an FPGA.

There are several ways of transmitting data from pixel to the end of column: one of the most famous is the column-drain read out, developed for CMS and ATLAS experiments [3]. All the pixels in a double-column share a data bus and only one pixel at a time, according to a priority chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored on a RAM until the SR does not allow the access to memory by data bus.

Even if many readout architectures are based on the column-drain one, it doesn't suit for large size matrices. The problem is that increasing the pixels on a column would also raise the number of pixels in the priority chain and that would result in a slowdown of the readout.

If there isn't any storage memory, the double-column behaves as a single server queue and the probability for a pixel of waiting a time T greater than t , with an input hit rate on the column μ and an output bandwidth B_W is [4]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.9)$$

To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time τ due to the AFE), for example imposing $P(T > t) \sim 0.001$, one obtains $(B_W - \mu) t_t \sim 6$, where t_t is the time needed to transfer the hit; since t_t is small, one must have $B_W \gg \mu$, that means a high bandwidth [4].

Actually the previous one is an approximation since each pixel sees a different bandwidth depending on the position on the queue: the first one sees a full bandwidth, but the next sees a smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen by the pixel i is $B_i = B - \sum_j \mu_j$, where μ_j is the hit rate of the j th pixel.

The efficiency requirement on the bandwidth and the hit rate becomes: $B_{W,i} > \mu_i$, where the index i means the constraint is for a single pixel; if all the N pixels on a column have the same rate $\mu = N\mu_i$, the condition reduces to $B_W > \mu$. The bandwidth must be chosen such that the mean time between hits of the last pixel in the readout chain is bigger than that.

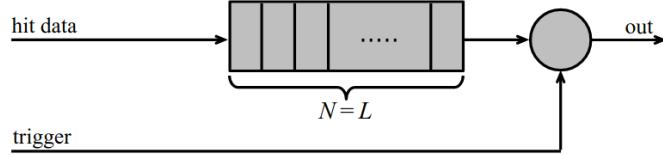


Figure 2.9: Block diagram of a pipeline buffer: N is the dimension of memory buffer and L is the trigger latency expressed in BCID cycles

263 In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed;
264 this means that only information from channels where the signal exceeds the discriminator thresh-
265 old are stored. Qu'è la zero suppression? La metto qui questa affermazione?

266 If instead there is a local storage until a trigger signal arrives, the input rate to column bus
267 μ' is reduced compared to the hit rate μ as: $\mu' = \mu \times r \times t$, where r is the trigger rate and t is
268 the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth,
269 but the limiting factor is the buffer depth: the amount of memory designed depends both on the
270 expected rate μ and on the trigger latency t as $\propto \mu \times t$, that means that the higher the trigger
271 latency and the lower the hit rate to cope with.

272 In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels
273 into regions with shared storage. Let's compare two different situations: in the first one a buffer
274 is located on each pixel area, while in the second one a core of four pixels share a common buffer
275 (this architecture is commonly called FE-I4).

Consider a 50 kHz single pixel hits rate and a trigger latency of 5 μs , the probability of losing

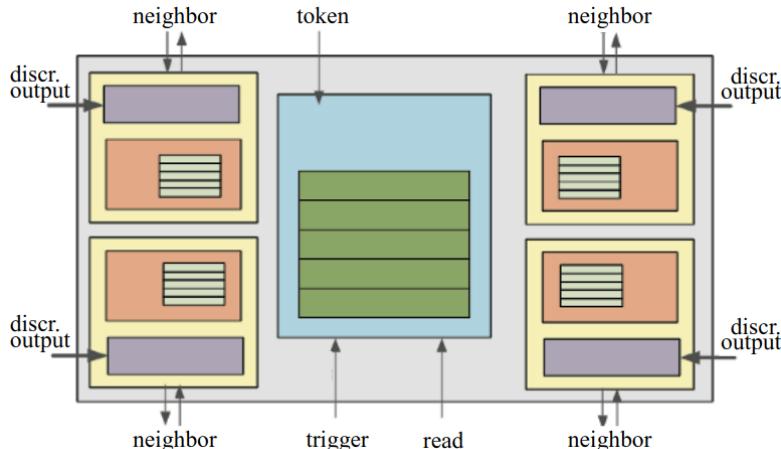


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is high-
lighted in light blue; latency counters and trigger management section are highlighted in green;
hit processing blocks are highlighted in purple; ToT counters and ToT management units are high-
lighted in orange

276 hits is:

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.10)$$

278 where I have assumed a Poissonian distribution with mean $\nu = 0.25$ to describe the counts N.
279 To get an efficiency ϵ greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.11)$$

280 Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four
281 pixels the mean number of hits per trigger latency is $\nu = 0.25 \times 4 = 1$. To get an efficiency of
282 99.9% (eq. 2.11) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

²⁸³ **Chapter 3**

²⁸⁴ **Use of pixel detectors**

²⁸⁵ Pixel detectors have been firstly developed for particle physics in 1980s and during the past 40
²⁸⁶ years have transformed particle tracking in experiments.

²⁸⁷ qualcosa del tipo: I più grandi esperimenti hanno tutti un rivelatore a pixel..

²⁸⁸ During the past 40 years, silicon sensors have transformed particle tracking in high-energy
²⁸⁹ physics experiments

²⁹⁰ Beside tracking, the development of pixel detectors is a very active field with many applications
²⁹¹ in medical imaging and astrophysics.. A noteworthy example of detector originally used in
²⁹² particle physics, and later employed mainly for medical imaging, but also in space and for art
²⁹³ authentication, is Medipix, a hybrid system developed at CERN within the Medipix collaboration.

²⁹⁴ In particolare la tecnologia CMOS, comunissima nell'ambito commerciale, basti pensare alle
²⁹⁵ fotocamere. Originariamente erano CCD poi ora CMOS MAPS. A partire dal 2017, i sensori
²⁹⁶ CMOS rappresentano l'89% delle vendite globali di sensori di immagine. Ma praticamente dal
²⁹⁷ 2010 in poi solo CMOS e non più CCD.

²⁹⁸

²⁹⁹ **3.1 Tracking in HEP**

³⁰⁰ Per gli acceleratori la richieste sono molto stringenti e lo saranno sempre di più con l'aumento dell'
³⁰¹ intensità o della luminosità in termini di radiation hardness (per HL-LHC for example expected
³⁰² in 5 anni 500 Mrad e NIEL di 10 alla 16), efficiency e occupancy (efficienza alta dopo tanta
³⁰³ radiazione e noise occupancy bassa), time resolution (bunch crossing 40 Mhz), material budget e
³⁰⁴ power consumption (material budget below 2 per cento e power consumption 500 mW/cm²)
³⁰⁵ Usati come tracciatori per misure di impulso e per misure di energia (per rigettare) ad esempio
³⁰⁶ dati di fondo (topic fondamentale per BELLE-II).

³⁰⁷ **3.1.1 Hybrid pixels: ATLAS, CMS and LHC-b(?) /Belle-II?**

³⁰⁸ From the middle of 2013 a dedicated collaboration, RD 53 ('Development of pixel readout integrated
³⁰⁹ circuits for extreme rate and radiation'), has been established with the specific goal to find
³¹⁰ a pixel detector suitable for phase II future upgrades of the experiments CMS and ATLAS. Even
³¹¹ if the collaboration is specifically focused on design of hybrid pixel readout chips, also monolithic
³¹² options have been taken in account for ATLAS ITK outer layers. Tra i chip designed for that
³¹³ purpose there are LF an TJ Monopix.

³¹⁴ **ATLAS**

³¹⁵ **CMS**

³¹⁶ **Belle-II**

³¹⁷

³¹⁸ **3.1.2 CMOS MAPS: ALICE and STAR**

³¹⁹ Experiments such as ALICE at LHC and STAR at RHIC have already introduced the CMOS
³²⁰ MAPS technology in their detectors. ALICE Tracking System (ITS2), upgraded during the LHC

321 long shut down in 2019-20, was the first large-area ($\sim 10 \text{ m}^2$) silicon vertex detector based on
322 CMOS MAPS.

323 **ALICE**

324 ALICE (A Large Ion Collider Experiment) is a detector dedicated to heavy-ion physics at the
325 LHC. **Metti una cosa generale su com'è fatto tutto il detector di ALICE: tpc ecc.**

326 The expected dose is smaller by two order than the one at ATLAS and CMS.(cita libro). The rate
327 of interactions is few MHz, but the number of particles produced in each interaction is really high.
328 The pixel system must cope with high densisties as high as $100/\text{cm}^2$, ma ha abbastanza tempo
329 tra un interazione e l'altra. The challenge is recustruct very complicated events and relevant is
330 minimize the amount of material since any kind of secondary interaction will complicate futher the
331 event topology e diminuisce efficenza e risoluzione delle tracce a più basso momento.

332 **ALICE MAPS: MONOPIX1 COM'è fatto il rivelatore a pixel di ALICE** Thanks to the reduction
333 of the material budget, ITS2, which uses the ALPIDE chip developed by ALICE collaboration,
334 obtained an amazing improvement both in the position measurement and in the momentum resolu-
335 tion, improving the efficiency pf track reconstruction for particle with very low transverse momen-
336 tum (by a factor 6 at $pT \sim 0.1 \text{ GeV}/c$). Further advancements in CMOS MAPS technology are
337 being aggressively pursued for the ALICE ITS3 and the Belle II vertex detector upgrades (both
338 foreseen around 2026-27) and other experiments, with the goals of further reducing the sensor
339 thickness and improving the readout speed of the devices, while keeping power consumption at a
340 minimum.

341 **STAR**

342

343

3.2 Application in medical imaging

344

3.2.1 Medipix and Timepix

345

3.2.2 Applicability to FLASH radiotherapy

³⁴⁶ **Chapter 4**

³⁴⁷ **TJ-Monopix1**

³⁴⁸ TJ-Monopix1 is a small electrode DMAPS with fast R/O capability, fabricated by TowerJazz
³⁴⁹ foundry in 180 nm CMOS imaging process. It is part, together with prototypes from other series
³⁵⁰ such as TJ-MALTA, of the ongoing R&D efforts aimed at developing DMAPS in commercial CMOS
³⁵¹ processes, that could cope with the requirements at accelerator experiments. Both TJ-Monopix
³⁵² and TJ-MALTA series [5], produced with the same technology by TowerJazz (the timeline of the
³⁵³ foundry products is shown in figure 4.1), are small electrode demonstrators and principally differ in
³⁵⁴ the readout design: while Monopix implements a column-drain R/O, an asynchronous R/O without
³⁵⁵ any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.



Figure 4.1: Timeline in TowerJazz productions in 180 nm CMOS imaging process

³⁵⁶ Another Monopix series, but in 150 nm CMOS technology, has been produced by LFoundry [6].
³⁵⁷ The main differences between the LF-Monopix1 and the TJ-Monopix1 (summarized in table 4.2),
³⁵⁸ lay in the sensor rather than in the readout architecture, as both chips implements a fast col-
³⁵⁹ umn drain R/O with ToT capability [7][8]. Concerning the sensors, either are based on a p-type
³⁶⁰ substrate, but with slightly different resistivities; in addition LFoundry pixels are larger, thicker
³⁶¹ and have a large fill factor (the very deep n-well covers ~55% of the pixel area). The primary
³⁶² consequence is that LF-Monopix1 pixels have a higher capacity resulting in higher consumption
³⁶³ and noise. As I discussed in section 2.3.1, the fact that LF-Monopix has a large fill factor electrode
³⁶⁴ is expected to improve its radiation hardness. Indeed, a comparison of the performance of the
³⁶⁵ two chips showed that TJ-Monopix suffers a comparatively larger degradation of efficiency after
³⁶⁶ irradiation, due to the low electric field in the pixel corner; on the other hand, a drawback of the
³⁶⁷ large fill factor in LF-Monopix is a significant cross-talk.

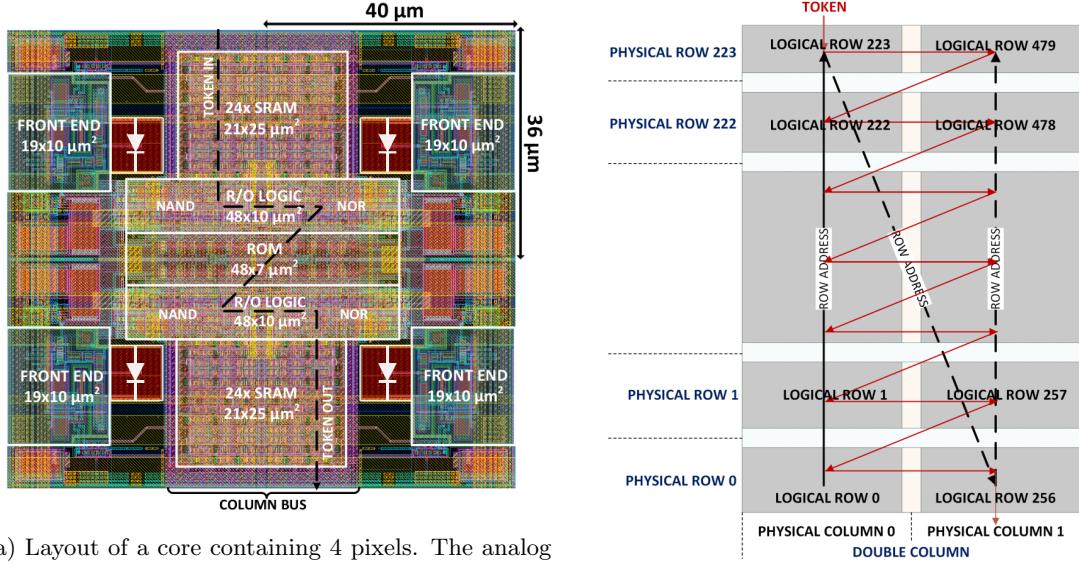
³⁶⁸ The TJ-Monopix1 chip contains, apart from the pixels matrix, all the required support blocks
³⁶⁹ used for configuration and testing:

- ³⁷⁰ the whole matrix contains 224×448 pixels, yielding a total active area approximately equal
³⁷¹ to 145 mm^2 over a total area of $1 \times 2 \text{ cm}^2$;
- ³⁷² at the chip periphery are placed some 7-bit Digital to Analog Converter (DAC), used to
³⁷³ generate the analog bias voltage and current levels and to configure the FE;

	LF-Monopix1	TJ-Monopix1
Resistivity	$>2\text{ k}\Omega\text{cm}$	$>1\text{ k}\Omega\text{cm}$
Pixel size	$50 \times 250\mu\text{m}^2$	$36 \times 40\mu\text{m}^2$
Depth	$100\text{-}750\mu\text{m}$	$25\mu\text{m}$
Capacity	$\sim 400\text{ fF}$	$\sim 3\text{ fF}$
Preamplifier	charge	voltage
Threshold trimming	on pixel (4-bit DAC)	global threshold
ToT	8 bits	6 bits
Consumption	$\sim 300\text{ mW/cm}^2$	$\sim 120\text{ mW/cm}^2$
Threshold	$1500 e^-$	$\sim 270 e^-$
ENC	$100 e^-$	$\sim 30 e^-$

Table 4.1: Main characteristics of Monopix1 produced by TowerJazz and LFoundry [7][8]

- at the EoC is placed a serializer to transferred datas immediately, indeed no trigger memory is implemented in this prototypes;
 - the matrix power pads are distributed at the sides
 - four pixels which have analog output and which can be monitored with an oscilloscope, and therefore used for testing
- Pixels are grouped in 2×2 cores (fig. 4.2a): this layout allows to separate the analog and the digital electronics area in order to reduce the possible interference between the two parts. In addition it simplifies the routing of data as pixels on double column share the same column-bus to EoC. Therefore pixels can be addressed through the physical column/row or through the logical column/row, as shown in fig. 4.2b: in figure is also highlighted the token propagation path, whose I will discuss later.



(a) Layout of a core containing 4 pixels. The analog FE and the digital part are separated in order to reduce cross-talk be

(b)

4.1 The sensor

As already anticipated, TJ-Monopix1 has a p-type epitaxial layer and a n doped small collection electrode ($2\mu\text{m}$ in diameter); to avoid the n-wells housing the PMOS transistors competing for the charge collection, a deep p-well substrate, common to all the pixel FE area, is used. TJ-Monopix1 adopts the modification described in section 2.3.2 that allows to achieve a planar depletion region

Parameter	Value
Matrix size	$1 \times 2 \text{ cm}^2$
Pixel size	$36 \times 40 \mu\text{m}^2$
Depth	$25 \mu\text{m}$
Electrode size	$2 \mu\text{m}$
BCID	40 MHz
ToT-bit	6
Power consumption	$\sim 120 \text{ mW/cm}^2$

Table 4.2

near the electrode applying a relatively small reverse bias voltage. This modification improves the efficiency of the detector, especially after irradiation, however a simulation of the electric field in the sensor, made with the software TCAD (Technology Computer Aided Design), shows that a nonuniform field is still produced in the lateral regions of the pixel compromising the efficiency at the corner. Two variations to the process have been proposed in order to further enhance the transversal component of electric field at the pixel borders: on a sample of chip, which includes the one in Pisa, a portion of low dose implant has been removed, creating a step discontinuity in the deep p-well corner (fig. 4.3); the second solution proposed[MOUSTAKAS THESYS, PAG 58] consists in adding an extra deep p-well near the pixel edge. A side effect of the alteration in the low dose implant is that the separation between the deep p-well and the p-substrate becomes weak to the point that they cannot be biased separately to prevent the punchthrough.

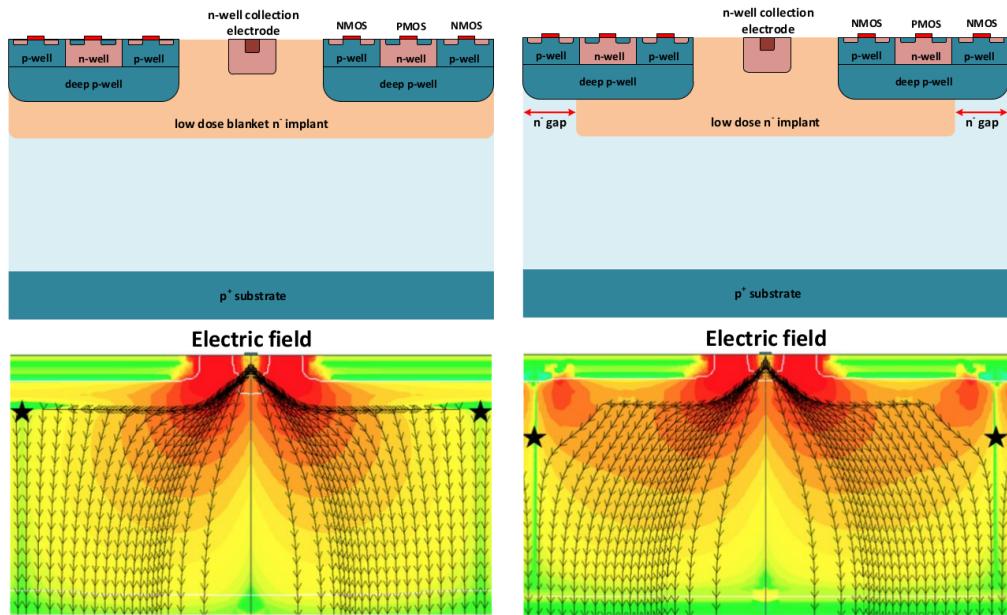


Figure 4.3: (a) The cross-section of a monolithic pixel in the TJ-Monopix with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field. this point in figure is indicated by a star . transversal component of the electric field drops at the pixel corner

Moreover, to investigate the charge collection properties, pixels within the matrix are split between bottom top half and bottom half and feature a variation in the coverage of the deep p-well: the electronics area can be fully covered or not. In particular the pixels belonging to rows from 0 to 111 are fully covered (FDPW) and pixels belonging to rows from 112 to 223 have a reduced p-well (RDPW), resulting in a enhancement of the lateral component of the electric field.

4.2 Front end

The matrix is split in four sections, each one corresponding to a different flavor of the FE. The four variation have been implemented in order to test the data-bus readout circuits and the input reset modes.

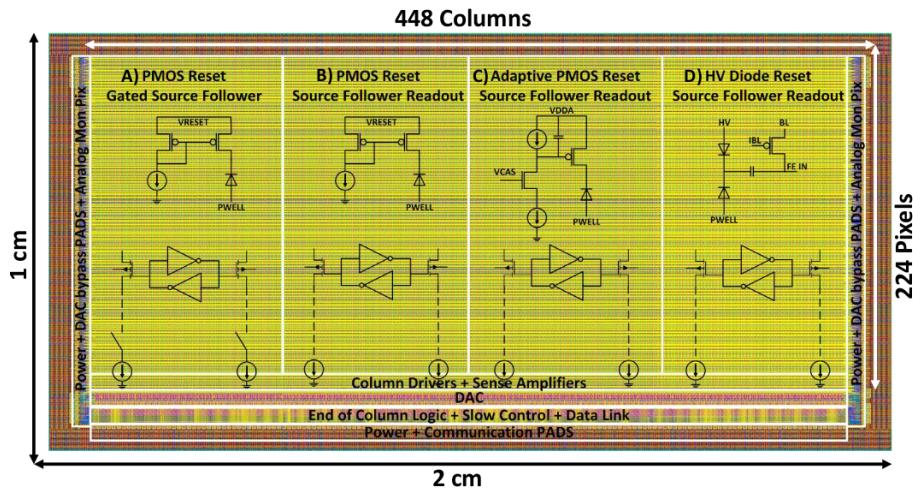


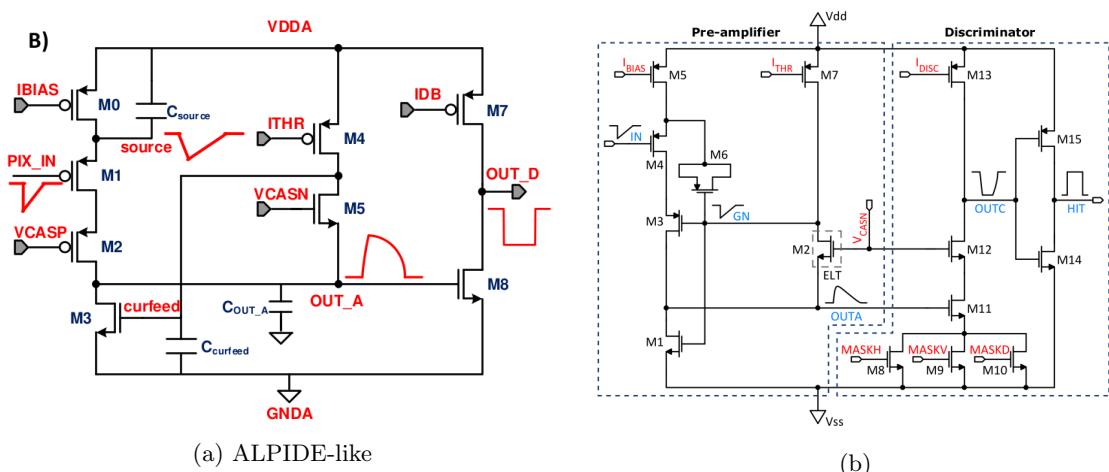
Figure 4.4

All the flavors implement a source-follower double-column bus readout: the standard variation is the flavor B, that features a PMOS input reset (referred as "PMOS reset"). Flavor A is identical to flavor B except for the realization of the source follower (it is a gated one) that aim to reduce the power consumption. cosa significa? C instead implements a novel leakage compensation circuit. Moreover the collection electrode in flavors A, B, C is DC-coupled to the front-end input, while in D is AC-coupled, providing to applu a high bias voltage; for this reason flavor D il called "HV flavor".

R resistenza di reset deve essere abbastanza grande in modo da far si che il ritorno allo zero è abbastanza lento (non devi "interferire" con la tot slope e non devi più corto del tempo del preamplificatore, sennò hai perdita di segnale). Baseline reset: all'input solitamente hai un PMOSS o un diodo; R reset; Voltage amplifier

4.2.1 ALPIDE-like

ALPIDE chips, developed by the ALICE collaboration, implemented a standard FE to the point that many CMOS MAPS detectors used a similar FE and are called "ALIPDE-like". Considering that both TJ-Monopix1 and ARCADIA-MD1 have an ALPIDE-like FE, I am going to explain the broad principles of the early FE stage. The general idea is of the amplification to transfer the



426 charge from a bigger capacity[9], C_{source} , to a smaller one, C_{out} : the input transistor M1 with
 427 current source IBIAS acts as a source follower and this forces the source of M1 to be equal to the
 428 gate input $\Delta V_{PIX_IN} = Q_{IN}/C_{IN}$.

$$Q_{source} = C_{source} \Delta V_{PIX_IN} \quad (4.1)$$

429 The current in M2 and the charge accumulates on C_{out} is fixed by the one on C_{source} :

$$\Delta V_{OUT_A} = \frac{Q_{source}}{C_{OUT_A}} = \frac{C_{source} \Delta V_{PIX_IN}}{C_{OUT_A}} = \frac{C_{source}}{C_{OUT_A}} \frac{Q_{IN}}{C_{IN}} \quad (4.2)$$

430 A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR
 431 set the baseline value of the signal on C_{OUT_A} and the velocity to goes down to the baseline.

IL RUOLO DI CURVFEED NON L'HO CAPITO.

433 Finally IDB defines the charge threshold with which the signal OUT_A must be compared: depending on if the signal is higher than the threshold or not, the OUT_D is high or low respectively.
 434

435 The actual circuit implemented in TJ-Monopix1 is shown in figure 4.5b: the principal difference
 436 lays in the addition of disableing pixels' readout. This possibility is uttermost important in order to
 437 reduce the hit rate and to avoid saturating the bandwidth due to the noisy pixels, which typically
 438 are those with manufacturing defects. In the circuit transistors M8, M9 and M10 have the function
 439 of disabling registers with coordinates MASKH, MASKV and MASKD (respectively vertical, ori-
 440 ginal and diagonal) from readout: if all three transistors-signals are low, the pixel's discriminator
 441 is disabled. Compared with a configurable masking register which would allow disableing pixels
 442 individually, to use a triple redundancy reduces the sensistivity to SEU¹ but also gives amount of
 443 intentionally masked ("ghost") pixels. This approach is suitable only for extremely small number
 444 N of pixel has to be masked: if two coordinate projection scheme had been implemented, the
 445 number of ghost pixels would have scale with N^2 , if instead three coordinates are used, the N's
 exponential is lower than 2 (fig. 4.6)

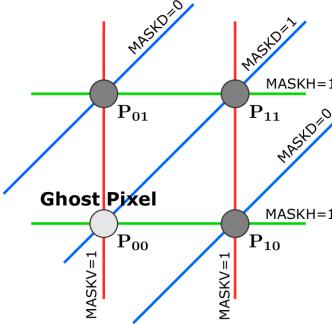


Figure 4.6

446

4.3 Readout logic

448 TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain
 449 architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit
 450 LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address.
 451 Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is
 452 already storing a previous one, the new data get lost. After being read, the data packet is sent to
 453 the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (4.7). There
 454 a FIFO is used to temporarily stored the data, which is transmitted to a computer through an
 455 ethernet cable in a later time.

¹Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché una particella deposita carica nell'elettronica che fa da memoria registro/RAM/.... Questo tipo di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più carica di quanto farebbe una MIP. Questo metodo pur essendo più comodo richiede less amount of area ha però come drawback che il registro può essere soggetto a SEU problema non trascurabile in acceleratori come HL-LHC adronici

Parameter	Meaning	
IBIAS	sets the discriminator threshold	yes
IDB	sets the velocity of the return to the baseline	yes
ITHR	sets the baseline of the signal	yes
ICASN	sets the gain of the preamplifier	yes
VRESET	sets the gain of the preamplifier	yes
IRESET	sets the gain of the preamplifier	no

Table 4.3: FE parameters which must be setted through the DAQ. "Function" means that higher parameter implies higher value

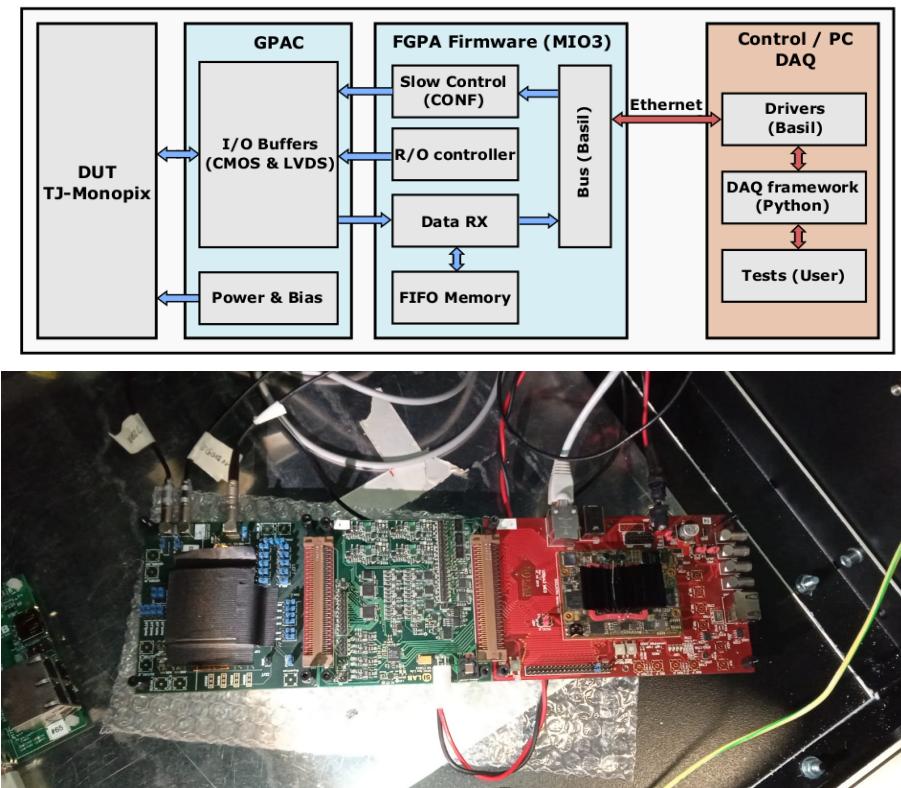
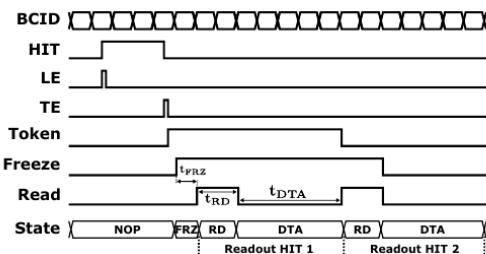


Figure 4.7: Main caption

456 The access to the pixels' memory and the transmission of the data to the EoC, following
 457 a priority chain, is managed by control signals and is based on a Finite State Machine (FSM)
 458 composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and data transfer (DTA).
 459 The readout sequence (??) starts with the TE of a pulse: the pixel immediately tries to grab the
 460 column-bus turning up a hit flag signal called *token*. The token is used to control the priority chain
 461 and propagates across the column indicating what pixel that must be read. To start the readout
 462 and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal is activated, and
 463 then a *read* signal controls the readout and the access to memory. During the freeze, the state of
 464 the token for all pixels on the matrix remains settled: this does not forbid new hits on other pixels
 465 from being recorded, but forbids pixels hit from turning on the token until the freeze is ended. The
 466 freeze stays on until the token covers the whole priority chain and gets the EoC: during that time
 467 new token cannot be turned on, and all hits arrived during a freeze will turn on their token at the
 468 end of the previous freeze. Since the start of the token is used to assign a timestamp to the hit,
 469 the token time has a direct impact on the time resolution measurement; this could be a problem
 coping with high hits rate.



(b) Readout sequence timing diagram. In this example two hits are being processed.

Figure 4.8: Readout timing diagram: in this example two hits are being processed

470 The analog FE circuit and the pixel control logic are connected by an edge detector which is
 471 used to determine the LE and the TE of the hit pulse(fig. 4.9): when the TE is stored in the first
 472 latch the edge detector is disabled and, if the FREEZE signal is not set yet, the readout starts. At
 473 this point the HIT flag is set in a second latch and a token signal is produced and depending on
 474 the value of *Token in* in the pixel can be read or must wait until the *Token in* is off. In figure an OR
 475 is used to manage the token propagation, but since a native OR logic port cannot be implemented
 476 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly
 477 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token
 478 and to speed up the circuit optimized solution are often implemented. When the pixel become the
 479 next to be read in the queue, and at the rising edge of the *READ* signal, the state of the pixel is
 480 stored in a D-latch and the pixel is allowed to use the data bus; the TE and the HIT flag latches
 481 are reset and a *READINT* signal that enable access of the RAM and ROM cells is produced.
 482

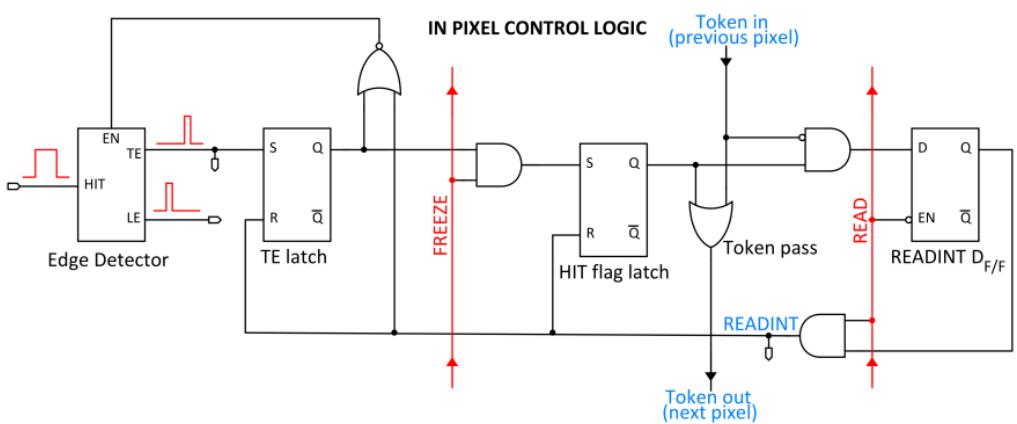


Figure 4.9

484 The final data must provide all the hits' information: the pixel address, the ToT and the
485 timestamp. All those parts are assigned and appended at different time during the R/O chain:

- 486 • **Pixel address:** while the double column address (6-bit) is appended by the EoC circuit,
487 the row address (8-bits for each flavor) and the physical column in the doublet (1-bit) are
488 assigned by the in-pixel logic
- 489 • **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge
490 detector in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is
491 range 0-64 clock cycle which corresponds to 0-1.6 μ s
- 492 • **Timestamp:** The timestamp of the hit correspond to the time when the pixel set up the
493 token; it is assigned by the FPGA, that uses the LE, TE and a 640 MHz clock to derive
494 it. For all those hits which arrived while the matrix is frozen, the timestamp is no more
495 correlated with the time of arrival of the particle

496 When the bits are joined up together the complete hit data packet is 27-bit.

497 4.3.1 Dead time measurements

498 The hit loss is due to analog and digital pile up: the first one occurs when a new hit arrives during
499 the pre-amplifier response, the second instead, which is the more relevant contribution, while the
500 information of the previous hit has not yet been transferred to the periphery. As only one hit at
501 a time can be stored on the pixel's RAM, until the data have completed the path to get out, the
502 pixel is paralyzed and the dead time τ almost corresponds with the time needed to trasmit the
503 data-packets off-chip. Since the exportation of data from pixel to the EoC occurs via a 21-bits
504 data bus, only one clock cycle is need to transfer the data to the end of column and the dead time
505 bottleneck is given by the bandwidth of the serializer at the EoC. In our setup it operates at 40
506 MHz, thus to transmit a data packet (27-bit) at least 675 ns are needed. For what we have said so
507 far, the R/O is completely sequential and therefore is expected a linear dependence of the reading
508 time on the number of pixels to read:

$$\tau = 25 \text{ ns} \times (\alpha N + \beta) \quad (4.3)$$

509 where α and β are parameters dependent on the readout chain setting.

510 To measure and test the linearity of the reading time with the number of pixels firing, I have
511 used the injection mode available on the chip. Indeed, the injection mode allows fixing not only
512 the amplitude of the pulse, which corresponds to the charge in DAC units, but also the period and
513 the width. I have injected a fix number of pulses (100) and looked for the rate when the efficiency
514 decreases. Moreover to test that there is no dependece of the digital readout time from the charge
515 of the pulse, I have try to change the amplitude of the pulse injected, but the parameters found
516 were consistent with the default configuration ones.

517 **Un esempio se leggo un singolo pixel: LA SLOPE CON CUI L'EFFICIENZA SCENDE È
518 ABBSTANZA UNIFORME? perchè satura a 50?**

519 While the single pixel reading time and the dead time do not depend on the position on the
520 pixel matrix and are equal to 106 (46+60) clock counts within 1 clock count, on the other hand the
521 τ depends on the pixel position on the matrix when more than one pixel are firing. In particular
522 the priority chain goes from row 224 to row 0, and from col 0 to 112, that means the last pixels to
523 be read is the one on le bottom right corner of the matrix.

524 In figure 4.11 is reported the reading time versus the number of pixels injected; the R/O
525 parameters that control the reading time and their default values are reported on table ??.

526 The factor α , referring to eq. 4.3 is proportional to the difference (STOP_FREEZE - START_READ),
527 while the offset β lies between 5 and 15 clock counts. Since through the injection a random hit rate
528 on the matrix can't be simulated, as the coordinates of the pixels to inject must be specified, for
529 convenience I used the pixels on the same column/row. No difference in the α and β coefficients
530 has been observed between the two case.

531 **A tutte le hit di una iniezione che arrivano contemporaneamente viene assegnato lo stesso
532 timestamp; Risoluzione temporale??**

Parameter	Value [DAC]	Value [μ s]
START_FREEZE	64	1.6
STOP_FREEZE	100	2.5
START_READ	66	1.65
STOP_READ	68	1.7

Table 4.4: Default configuration of the R/O parameters

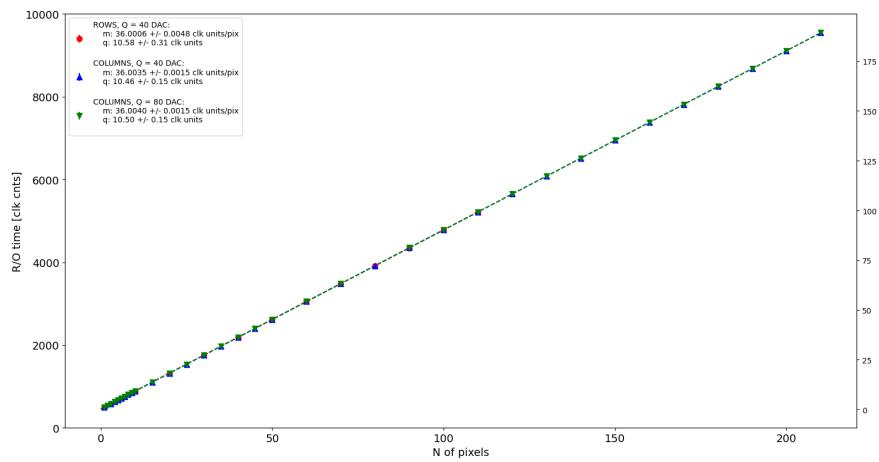


Figure 4.10

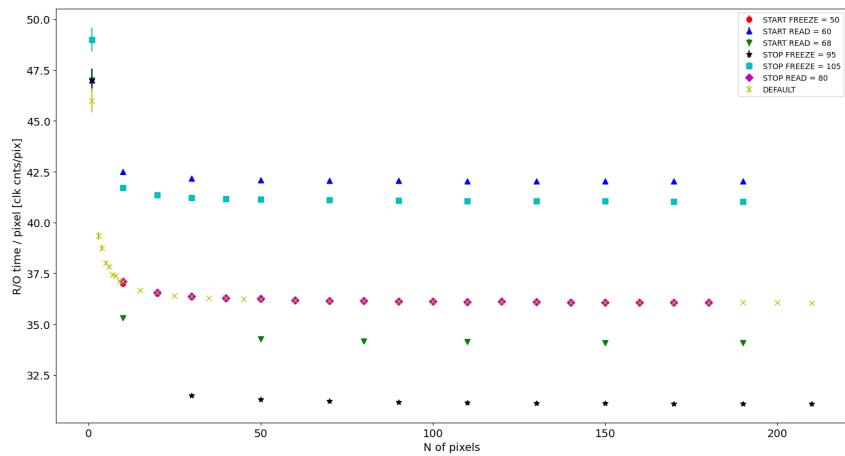


Figure 4.11

533 Chapter 5

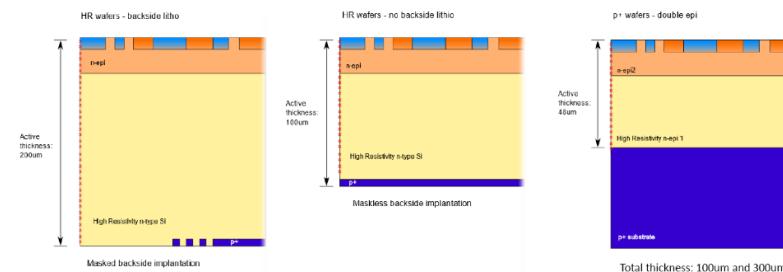
534 Arcadia-MD1

535 [10] [11]

536 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED
537 Matisse a Md1 e Md2

538 5.1 The sensor

539 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node
540 with six metal layer ???. The standard p-type substrate was replaced with an n-type floating zone
541 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).



542 Figure 5.1

543 Wafer thinning and backside litography were necessary to introduce a junction at the bottom
544 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.
545 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthrough
546 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

547 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,
548 COME VENGONO FATTI I MAPS COME FAI LE GIUNZIONI

549 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.
550 It is operated in full depletion with fast charge collection by drift.

551 Prima SEED si occupa di studiare le prestazioni: oncept study with small-scale test struc-
552 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo
553 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il
554 pwell e quanto al diodo. ..

555 5.2 Readout logic and data structure

556 5.2.1 Matrix division and data-packets

557 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided
558 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in

559 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei
 serializzatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

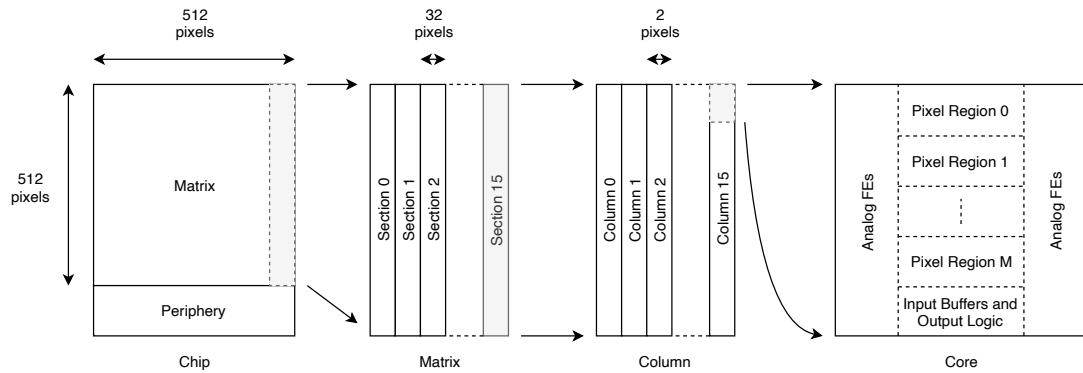


Figure 5.2

560

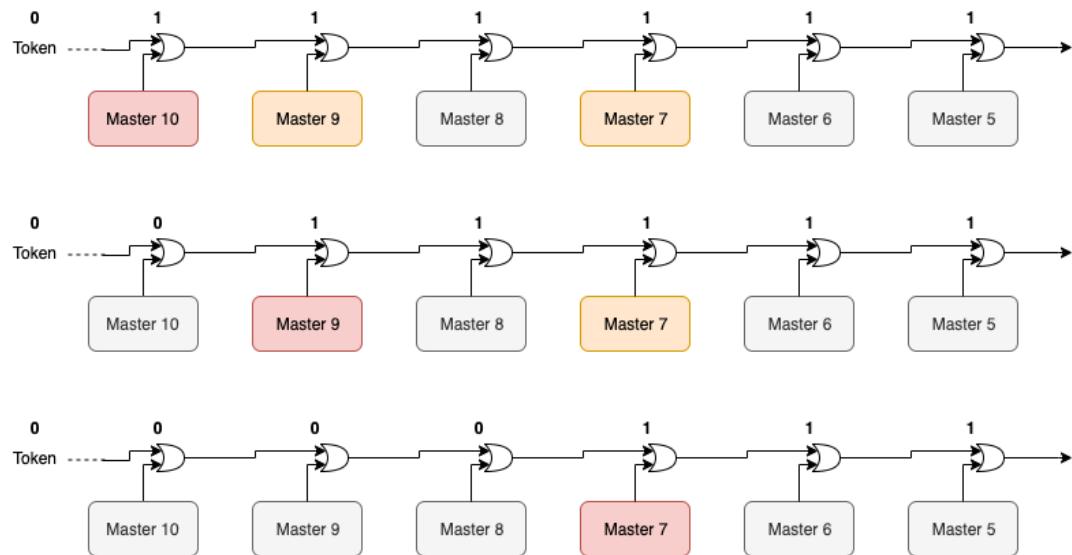


Figure 5.3

561 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le
 562 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,
 563 e devi accennare al timestamp

564 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively
 565 large core allows one to take full advantage of digital synthesis tools to implement complex func-
 566 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della
 567 review.

568

569 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column
 570 (512x2) Core (32x2) Region (4x2)

571 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

572 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for
 573 example 8b10b encoding n =5"

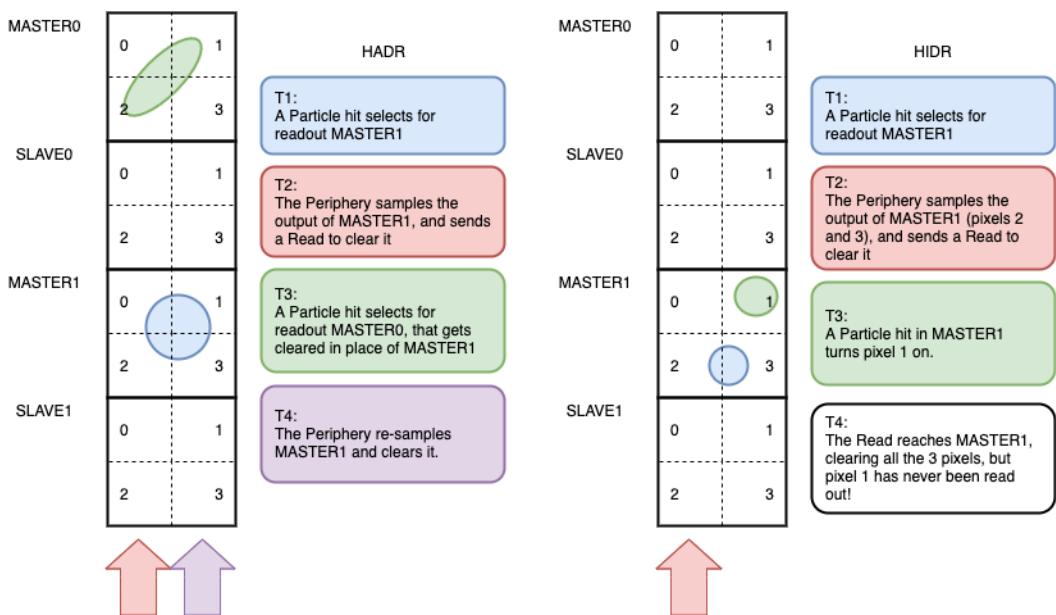


Figure 5.4

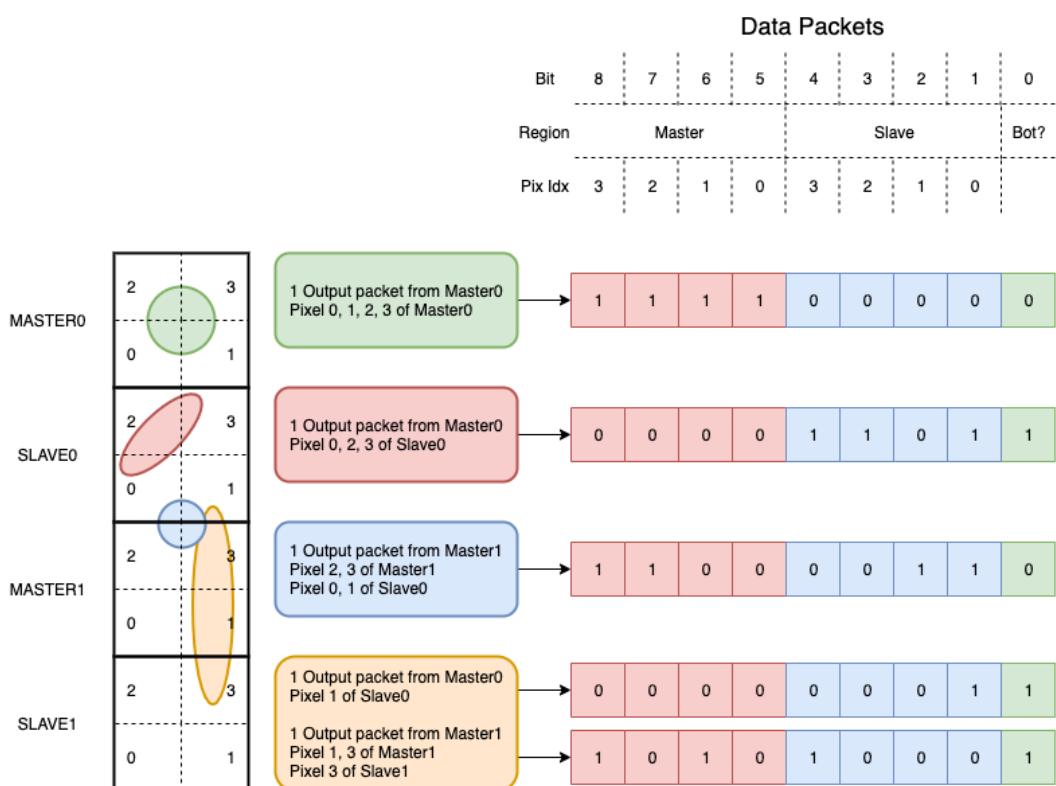


Figure 5.5

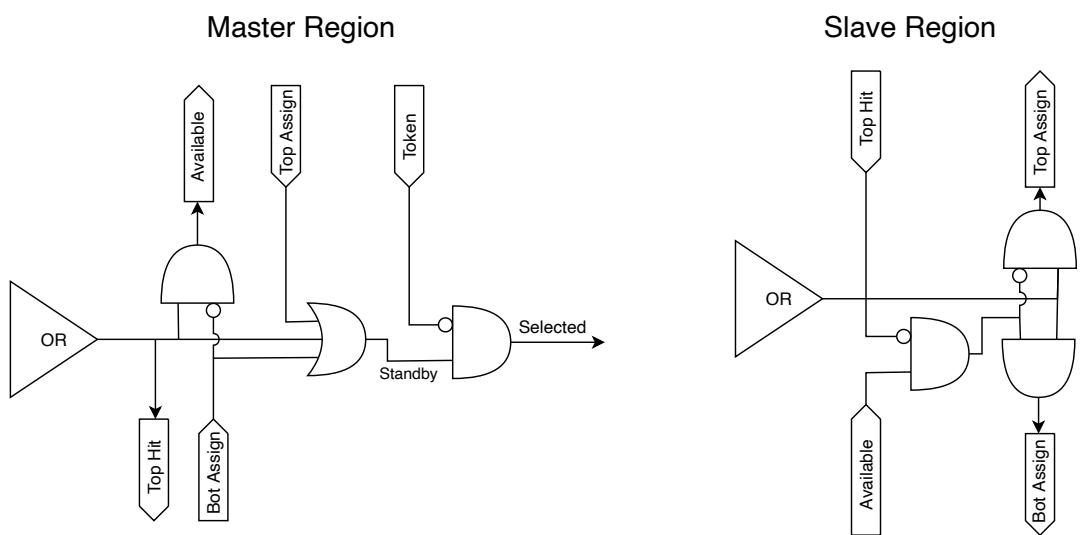


Figure 5.6

574 **Chapter 6**

575 **Threshold and noise
576 characterization**

577 **6.1 Threshold and noise: figure of merit for pixel detectors**

578 The signal to threshold ratio is the figure of merit for pixel detectors.

579
580 la soglia deve essere abb alta da tagliare il rumore ma abb bassa da non perdere efficienza.
581 Invece di prendere il rapporto segnale rumore prendi il rapporto segnale soglia. Perchè? la soglia
582 è collegato al rumore, nel senso che: supponiamo di volere un occupancy di 10-4 allora sceglierò la
583 soglia in base a questo. (plot su quaderno) Da questo conto trovo la minima soglia mettibile
584 In realtà quello che faccio è mettere una soglia un po' più grande perchè il rate di rumore dipende
585 da molti fattori quali la temperatura, l annealing ecc, e non voglio che cambiando leggermente uno
586 di questi parametri vedo alzarsi molto il rate di rumore. In realtà non è solo il rumore sensibile a
587 diversi fattori, ma anche la soglia: ad esempio la cosa classica è la variabilità della soglia da pixel
588 a pixel.

589 In questo modo rumore e soglia diventano parenti.

590 Review pag 26.

591 The noise requirement can be expressed as:

592 Questo implica tra le altre cose che voglio poter assegnare delle soglie diverse a diversi pixel:

593 Drawback è dare spazio per registri e quantaltro.

594 Questo lascia però ancora aperto il problema temporale delle variazioni del rumore: problema per
595 cui diventano necessarie le misure dei sensori dopo l'irraggiamento.

596
597 Per arcadia i registri (c'è un DAC) per la soglia (VCASN) si trovano in periferia. Non fare
598 trimming sulla soglia è uno dei problemi che si sono sempre incontrati: a casusa dei mismatch dei
599 transistor le soglie efficaci pixel per pixel cambiano tanto. La larghezza della s curve è il noise se se
600 assumi che il noise è gaussiano

601 Il trimming della soglia avviene con dei DAC: la dispersione della soglia dopo al tuning e dovuta
602 al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.1)$$

603 dove il numero di bit cambia varia tra 3-7 tipicamente. Monopix è 7 Arcadia 6

604
605 Each ROIC is different in this respect, but in general the minimum stable threshold was around
606 2500 electrons (e) in 1st generation ROICs, whereas it will be around 500 e for the 3rd generation.
607 This reduction has been deliberate: required by decreasing input signal values. Large pixels (2 104
608 um²), thick sensors (maggiore di 200 um), and moderate sensor radiation damage for 1st generation
609 detectors translated into expected signals of order 10 ke, while small pixels (0.25 104 um²), thinner
610 sensors (100 um), and heavier sensor radiation damage will lead to signals as low as 2 ke at the
611 HL-LHC

612 The ENC can be directly calculated by the Cumulative Distribution Function (CDF) (scurve)
613 obtained from the discriminator "hit" pulse response to multiple charge injections

₆₁₄ **6.2 TJ-Monopix1 characterization**

₆₁₅ **6.3 ARCADIA-MD1 characterization**

616 Appendix A

617 Pixels detector: a brief overview

618 A.1 Radiation damages

619 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they
 620 are almost always installed near the interaction point where there is a high energy level of radiation.
 621 At LHC the ϕ_{eq} per year in the innermost pixel detector is $10^{14} n_{eq}/cm^2$; this number reduces by
 622 an order passing to the outer tracker layer [2] pag 341 Wermes. Here the high fluence of particles
 623 can cause a damage both in the substrate of the detector and in the superficial electronics.

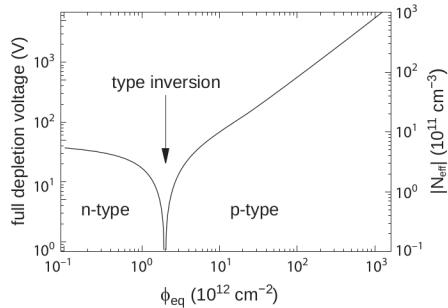
624 The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but
 625 it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the
 626 NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV
 627 neutrons. Differently, surface damages are principally due to ionizing energy loss.

628 **DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide (S_iO_2) can
 629 cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages
 630 are mostly less relevant than the previous one, since with the development of microelectronics and
 631 with the miniaturization of components (in electronic industry 6-7 nm transistors are already used,
 632 while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit
 633 is reduced.

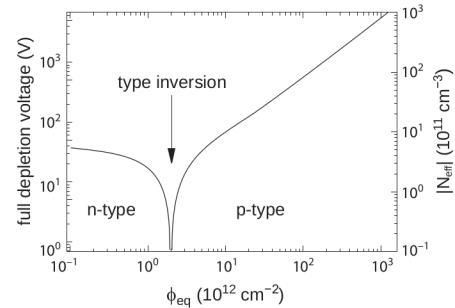
634 Let's spend instead two more other words on the more-relevant substrate damages: the general
 635 result of high radiation level is the creation of new energy levels within the silicon band gap and
 636 depending on their energy-location their effect can be different, as described in the Shockely-Read-
 637 Hall (SRH) statistical model. The three main consequence of radiation damages are the changing
 638 of the effect doping concentration, the leakage current and the increasing of trapping probability.

639 **Changing of the effective doping concentration:** is associated with the creation/removal
 640 of donors and acceptors center which trap respectively electrons/holes from the conduction band
 641 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type¹)
 642 can happen: indeed it is quite common at not too high fluences ($\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$). A changing
 643 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime
 644 (eq.2.1) and sometimes can be difficult keeping to fully deplete the bulk.

¹L'INVERSIONE OPPOSTA NON CE L'HA PERCHÈ?



(a) 1a



(b) 1b

645 **Leakage current:** is associated with the generation-recombination centers. It has a strong
646 dependence with the temperature ($I_{leak} \propto T^2$), whose solution is therefore to operate at lower
647 temperature.

648 **Increase of trapping probability:** since the trapping probability is constant in the depleted
649 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,
650 that is the mean trapping path, decreases after irradiation and typical values are 125-250 μm and
651 must be compared with the thickness of the depleted region which () corresponds to the mean drift
652 path.

653 Different choices for substrate resistivity, for junctions type and for detector design are typically
654 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced
655 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))
656 for example, show a compensation effect for radiation damage; another example is the usage of
657 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage
658 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p
659 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be
660 placed near the diode.

661 Appendix B

662 FLASH radiotherapy

663 La radioterapia si usa nel 60 per cento dei pazienti, sia come cura che come trattamento palliativo.
664 Si associa spesso ad altre cure e si può fare prima/durante/dopo un intervento.

665

666 Si può fare in modi diversi: da dentro (brachytherapy) oppure da fuori (quella standard). Un
667 requisito importante è la delinazione del target (non vuoi rischiare di beccare i tessuti sani), per
668 cui prima tipicamente si fanno esami di imaginig del tumore. Tipicamente anche gli acceleratori
669 stessi per la terapia sono provvisti di radiografia.

670 Un problema dei fotoni ad esempio è che il loro rilascio di dose è lineare, per cui danneggia
671 anche i tessuti sani. Il problema dei protoni invece è che hanno un picco troppo stretto per cui non
672 puoi coprire grosse zone e soprattutto se sbagli rischi davvero di danneggiare molto i tessuti sani.

673

674 B.1 Cell survival curves

675 Curva di efficacia del trattamento in funzione della dose:

$$\frac{S(D)}{S(0)} = e^{-F(D)} \quad (\text{B.1})$$

676 dove $F(D)$

$$F(D) = \alpha D + \beta D^2 \quad (\text{B.2})$$

677 dove α e β rappresentano due tipi di danno diversi: coefficients, experimentally determined, characterizing the radiation response of cells. In particular, alpha represents the rate of cell killing by single ionizing events, while beta indicates the maximal rate of cell killing by double hits observed when the repair mechanisms do not activate during the radiation exposure. Si ottiene una curva di sopravvivenza dove si vede la possibilità delle cellule di autoripararsi. A basse dosi infatti le cellule possono ripararsi.

683

684 Per introdurre l'effetto FLASH introduco prima la therapeutic window.

685

686 TCP è la tumor control Probability che indica la probabilità delle cellule del tumore di essere uccise dopo una certa dose (con in riferimento a dose in acqua)

687 Se una media di $\mu(D)$ di cellule di tumore are killed con una dose D , la probabilità che n cellule sopravvivono è data da $P(n|\mu)$ poisson:

$$P(n|\mu) = \frac{\mu(D)^n e^{-\mu(D)}}{n!} \quad (\text{B.3})$$

$$TCP(D) = P(n=0|\mu(D)) = e^{-\mu(D)} \quad (\text{B.4})$$

690 D'altra parte hai una probabilità di fare danno su normal tissue NTCP Normal Tissue Complication Probability, che rappresenta il problema principale e che limita la massima radiazione erogabile
691 Una scelta bilanciata si applica guardando a questi due fattori; si usa il therapeutic index definito
692 come TCP/NTCP.

694 La cosa ottimale è ampliare la finestra del therapeutic ratio.

695 CONV-RT 0.01-5 Gy/min. A typical RT regime today consists of daily fractions of 1.5 to 3
696 Gy given over several weeks.

698 Nell Intra operative radiation therapy (IORT), where they reach values respectively about 20 and
699 100 times greater than those of conventional radiation therapy.

700 FLASH vuole ultrahigh mean dose-rate (maggione di 40 Gy/s) in modo da ridurere anche il
701 trattamento a meno di un secondo.

703 **B.2 FLASH effect**

704 Ci sono due effetti che affect the flash effect and la sua applicabilità: Dose rate effect e oxygen

706 Cellule che esibiscono hypoxia (cioè cellule che non hanno ossigeno sono radioresistenti); al
707 contrario normoxia e physoxia non lo sono. la presenza di ossigeno rende la curva steeper indicando
708 che lo stesso danno si raggiunge a livelli di dose più bassi rispetto al caso senza ossigeno.

709 FIGURA con una curva a confronto con e senza ossigeno.

710 Typically, the OER is in the order of 2.5–3.5 for most cellular systems

711 Quindi si vogliono sfruttare questi effetti per diminuire la tossicità sui tessuti sani

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