

Summary

2	1 Introduction	3
3	2 Pixel detectors	5
4	2.1 Signal formation	5
5	2.2 CCDs	6
6	2.3 Hybrid pixels	6
7	2.4 CMOS MAPS and DMPAS	7
8	2.4.1 DMAPS: large and small fill factor	8
9	2.4.2 A modified sensor	9
10	2.5 Analog front end	9
11	2.5.1 Preamplifier	9
12	2.6 Readout logic	11
13	3 Use of pixel detectors	14
14	3.1 Tracking in HEP	14
15	3.1.1 Hybrid pixels at LHC: ATLAS, CMS and LHC-b	15
16	3.1.2 A DEPFET example: Belle-II	16
17	3.1.3 CMOS MAPS: ALICE and STAR	16
18	3.2 Applications in imaging	16
19	3.2.1 Applicability to FLASH radiotherapy	17
20	4 TJ-Monopix1	20
21	4.1 The sensor	21
22	4.2 Front end	23
23	4.2.1 ALPIDE-like	23
24	4.3 Readout logic	24
25	4.3.1 Dead time measurements	26
26	4.4 Measurements with radioactive sources	28
27	4.5 Calibration of the ToT signal	28
28	5 Arcadia-MD1	29
29	5.1 The sensor	29
30	5.2 Readout logic and data structure	29
31	5.2.1 Matrix division and data-packets	29
32	6 Threshold and noise characterization	33
33	6.1 Threshold and noise: figure of merit for pixel detectors	33
34	6.2 TJ-Monopix1 characterization	34
35	6.2.1 Threshold and noise dispersion	34
36	6.2.2 Absolute calibration of ToT	34
37	6.3 ARCADIA-MD1 characterization	34
38	7 Test beam measurements	35
39	7.1 Testbeam motivation	35
40	7.2 Apparatus description	35
41	A Pixels detector: a brief overview	37
42	A.1 Radiation damages	37

⁴³ **Bibliography** **39**

⁴⁴ Characterization of monolithic CMOS pixel sensors for charged particle detectors and for high
⁴⁵ intensity dosimetry

⁴⁶ **Chapter 1**

⁴⁷ **Introduction**

⁴⁸ Pixel detectors, members of the semiconductor detector family, have significantly been used at the
⁴⁹ accelerator experiments for energy and position measurement. Because of their dimension (today
⁵⁰ $\sim 30 \mu\text{m}$ or even better) and their spatial resolution ($\sim 5\text{-}10 \mu\text{m}$), with the availability of technology
⁵¹ in 1980s they proved to be perfectly suitable for vertex detector in the inner layer of the detector.

⁵² Despite the monolithic pixels came up with CCDs, invented in 1969 and fastly used in cameras,
⁵³ their usage had to wait for microelectronics developement: in MAPS device the readout electronics
⁵⁴ is build on the pixel's area, then the pixel dimension is limited by the dimension of transistors. This
⁵⁵ constraint favoured the usage in physics experiment of hybrid pixels, which currently constitute
⁵⁶ the state-of-art for large scale pixel detector. These ones are made by two different wafer each one
⁵⁷ containing or the sensor or the ASIC, which are after joined together through microconnection.
⁵⁸ This structure allows a separate optimization for the two components and makes hybrid pixels
⁵⁹ flexible and versatile.

⁶⁰ Requirement imposed by accelerator are stringent and they will be even more with the increase
⁶¹ of luminosity in terms of radiation hardness, efficiency and occupancy, time resolution, material
⁶² budget and power consumption. For this reason experiments (as ATLAS, CMS, BelleII) began to
⁶³ look at the more innovative and well-performing monolithic active pixels (MAPS) as perspective for
⁶⁴ their future upgrades.

⁶⁵ Che condiziona la risoluzione e l'efficienza di ricostruzione della sua traccia, e consumi del
⁶⁶ detector, sono diventati sempre più rilevanti; molti esperimenti (ATLAS, CMS, BelleII,..) stanno
⁶⁷ infatti valutando la possibilità di sostituire gli ibridi con i MAPS, che per i temi precedenti offrono
⁶⁸ prestazioni migliori, a scapito di tempi di lettura mediamente più lunghi, vista anche la positiva
⁶⁹ esperienza di ALICE ad LHC, primo esperimento ad introdurre un detector a pixel monolitico.

⁷⁰ During my thesys I studied and characterised two monolithic active pixel chips, TJ-Monopix1
⁷¹ and MD1; this devices, that are still prototypes, have been conceived and designed for physics
⁷² experiments at colliders, space experiments and also for medical applications.

⁷³ il primo, TJ-Monopix1, è un prototipo di un modello selezionato per l'upgrade di Belle II
⁷⁴ durante il LSD nel 2025 (il chip finale si chiamerà OBELIX e avrà come sensore TJ-Monopix2,
⁷⁵ successore di Monopix1); il secondo chip è stato progettato da ARCADIA che potrà avere, nelle
⁷⁶ versioni future, applicazioni in fisica medica, in esperimenti nello spazio e ai collider.

⁷⁷ Le differenze principali tra i due chip risiedono nel segnale fornito in output (Monopix fornisce il
⁷⁸ tempo sopra soglia dell'impulso triangolare, proporzionale alla carica rilasciata nel sensore, mentre
⁷⁹ arcadia fornisce un segnale puramente digitale), nella sequenza di readout dei pixel (monopix ha
⁸⁰ una lettura puramente sequenziale di tipo "column drain") mentre arcadia ha una lettura più
⁸¹ moderna che consente di poter aggregare dati durante la trasmissione (ad esempio nel caso di
⁸² formazione di cluster e creazione di hti su pixel adiacenti).

⁸³ I performed a threshold and noise characterization ($\sim 400 \text{ e}^-$ and $\sim 15 \text{ e}^-$) of TJ-Monopix1 in
⁸⁴ order

⁸⁵ Tra i test con Monopix1 ho effettuato una caratterizzazione in soglia ($\sim 400 \text{ e}^-$) e rumore (\sim
⁸⁶ 15 e^-) al fine di visualizzare la dispersione di questi valori sulla matrice; per poter minimizzare la
⁸⁷ dispersione sulla matrice e avere una più uniforme selezione della soglia (che è globale su tutta
⁸⁸ la matrice), le versioni successive di TJ-Monopix1 includono e includeranno la possibilità di fare
⁸⁹ piccole correzioni (3 bit per pixel vengono allocati in Monopix2) di quest'ultima pixel per pixel.
⁹⁰ Per poter fornire le misure dei segnale fornito, tempo sopra soglia ToT, in elettroni, che assieme

91 alle lacune vengono create dal passaggio della particella incidente e che quindi sono la quantità
92 fisica "importante" nella misura, è stata necessaria una calibrazione assoluta dell'oggetto. Per
93 quest'ultima e per altri test ?? mi sono servita di sorgenti radiattive come il ferro 55 (emissione di
94 un fotone gamma a 5.9 kev e dello stronzio 90 il cui spettro dell'elettrone emesso ha un end point
95 a x) e dei cosmici. Inoltre ho partecipato ai test di Monopix1 su fascio: abbiamo testato il chip in
96 una modalità diversa da quella per cui è stato progettato (tracking) e più simile al funzionamento
97 delle CCD, in cui non si cerca di distinguere il singolo elettrone incidente ma si integra in un
98 singolo segnale di output la carica rilasciata da più elettroni incidenti. Il fascio utilizzato (elettroni
99 da 7-9 MeV) è un fascio ad altissima intensità e verrà utilizzato per fare ricerca su radioterapia
100 ad alto rate (l'acceleratore è in grado di rilasciare dosi -con riferimento in acqua- fino a 40 Gy/s,
101 corrispondenti ad un numero di particelle di ..). Per quanto riguarda, invece, le misure sul chip
102 MD1, ho partecipato ai test elettrici e sul front end di un prototipo non ancora completamente
103 funzionante. Un nuovo chip dovrebbe arrivare nei prossimi giorni a Pisa.

¹⁰⁴ **Chapter 2**

¹⁰⁵ **Pixel detectors**

¹⁰⁶ I pixel detector fanno parte della famiglia dei detector a semiconduttore e il loro funzionamento si
¹⁰⁷ basa sulla creazione di coppie elettrone lacuna all'interno del bulk. Dalla creazione della particella
¹⁰⁸ incidente di queste coppie e facendole driftare attraverso l'applicazione di un campo elettrico, si
¹⁰⁹ ottiene quindi un segnale all'interno del rivelatore correlabile all'energia della particella incidente.
¹¹⁰ Il campo elettrico applicato, lo spessore della zona di svuotamento, le modalità con cui il
¹¹¹ segnale viene processato e trasmesso all'esterno del rivelatore sono caratteristiche specifiche del
¹¹² tipo di chip. In questo capitolo tratterò dunque i principali tipi di rivelatori a pixel, sofferandomi
¹¹³ in particolare sui pixel monoliti.

¹¹⁴ **2.1 Signal formation**

¹¹⁵ When a charge particle passes through a pixel and loses energy by ionization a part of that
¹¹⁶ energy is used to generate electron-hole pairs (another part is used for other processes, as the
¹¹⁷ lattice excitation) which are then separated by the electric field and collected at their respectively
¹¹⁸ electrodes (*p* for holes and *n* for electrons)¹; by the drift of these charges, a signal i_e is generated
¹¹⁹ on the electrode *e* as stated by the Shockley-Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (2.1)$$

¹²⁰ where $v(t)$ is the instantaneous velocity of the charge q and E_{WF} is the weighting field, that is the
¹²¹ field obtained biasing the electrode *e* with 1V and all the others with 0V. The drift velocity of the
¹²² charge depends on the electric field and on the mobility of the particle:

$$v = \mu(E) E \quad (2.2)$$

¹²³ where $\mu(E)$ is a function of the electric field and is linear with E only for small E : at higher values
¹²⁴ the probability of interactions with optical phonons increases and the mobility drops and this leads
¹²⁵ to an independence of the velocity from the electric field (fig. 2.1b).

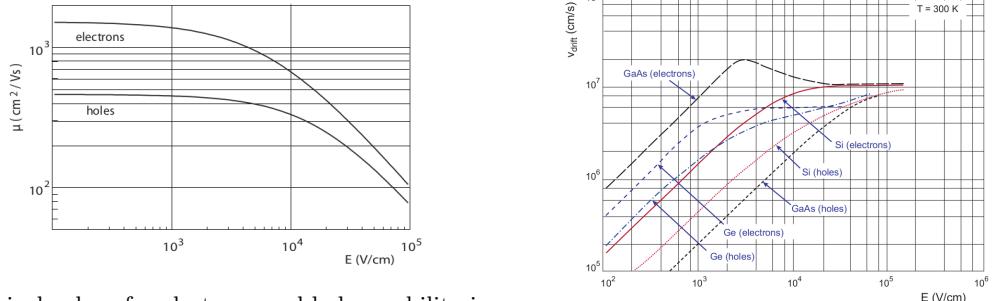
¹²⁶ The average energy needed to create a pair at 300 K in silicon is $w_i = 3.65$ eV, that is more
¹²⁷ than the mean ionization energy because of the interactions with phonon, since for a minimum
¹²⁸ ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is
¹²⁹ 0.28 keV/ μ , hence the number of e/h pairs is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (2.3)$$

¹³⁰ CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALEMTE SI AGGIUNGE IL
¹³¹ FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. IL FATTORE DI FANO È
¹³² 0.115 NEL SILICIO. ecc

¹³³ It is fundamental that pairs e/h are produced in the depleted region of the semiconductor where
¹³⁴ the probability of recombination with charge carriers is low to avoid loss of signals. Pixel detectors

¹Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout



(a) Typical values for electrons and holes mobility in silicon at room temperature are $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$, $\mu_h = 500$
(b) Drift velocity at room temperature in different semiconductors

135 are then commonly reverse biased: a positive bias is given to the n electrode and a negative to the
136 p to grow the depletion zone in the epitaxial layer below the electrode. The width of the depletion
137 region is related with the external bias V_{ext} , the resistivity ρ and also with the dopant:

$$139 d_n \sim 0.55 \sqrt{\frac{\rho}{\Omega cm}} \frac{V_{ext}}{V} \mu m \quad (2.4) \quad d_p \sim 0.32 \sqrt{\frac{\rho}{\Omega cm}} \frac{V_{ext}}{V} \mu m \quad (2.5)$$

138
140

141 For that reason high resistivity wafers ($100 \Omega cm - k\Omega cm$) are typically preferred because they
142 allow bigger depletion zone with smaller voltage bias. **Metto il disegno "standard" di una giunzione**

143 2.2 CCDs

144 **descrivi come sono fatte e come funziona il readout** Tens of ms due to the need to transfer the
145 charge signals pixel by pixel through a single output circuit For photon imaging the need of high
146 assorbtion efficiency, **per cui usi materiali con alto Z**

147 2.3 Hybrid pixels

148 **METTI IN EVIDENZAZ CHE PUOI FARE UN READOUT CON TECNOLOGIA CMOS.** Metti
149 **in evidenza che sono più veloci** Hybrid pixels are made of two parts (fig. 2.2a), the sensor and the
150 electronics: for each pixel these two parts are welded together through microconnection (bump
151 bond).

152 They provide a practical system where readout and sensor can be optimized separately, although
153 the testing is less easy-to-do since the sensor and the R/O must be connected together before.

154 In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-
155 cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high
156 levels of radiation, and also expensive.

157 A critical parameter for accelerator experiments is the material budget, which represents the main
158 limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are
159 thicker (\sim hundreds of μm) than monolithic ones (even less than $100 \mu m$), using the latter the
160 material budget can be down by a third: typical value for hybrid pixels is $1.5 \% X_0$ per layer,
161 while for monolithic $0.5 \% X_0$.

162 Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,
163 by the way, a bigger cooling system leading in turn to an increase in material too.

164 **DEPFET** are the first attempt towards the integration of the front end (FE) on the sensor bulk:
165 they are typically mounted on a hybrid structure but they also integrate the first amplification
166 stage.

168 Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor
169 (a p-channel in fig. 2.2b): an hole current flows from source to drain which is controlled by the
170 external gate and the internal gate together. The internal gate is made by a deep $n+$ implant

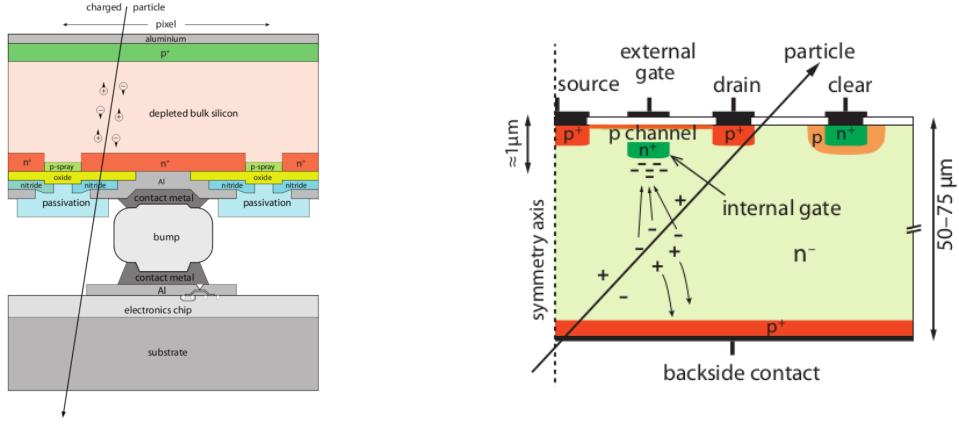


Figure 2.2: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

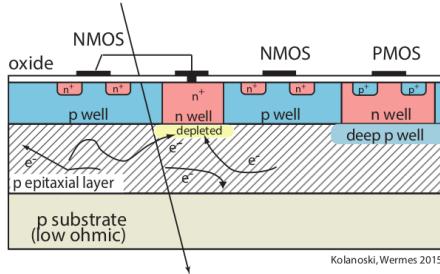


Figure 2.3: Concept cross-section of CMOS MPAS pixel

171 towards which electrons drift after being created in the depletion region (to know how the signal
 172 is created in a pixel detector look at appendix A); the accumulation of electrons in the region
 173 underneath the n implant changes the gate potential and controls the transistor current.
 174 DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and
 175 the large depletion region. But, since they need to be connected with ASIC the limiting factor still
 176 is the material budget.

177 2.4 CMOS MAPS and DMPAS

178 With respect to CCDs, the radiation tolerance could be greatly increased by sensing the signal
 179 charge within its own pixel, instead of transporting it over thousands of pixels. The readout
 180 speed could also be dramatically increased by in-pixel amplitude discrimination, followed by sparse
 181 readout of only the hit pixels Monolithic active pixels accommodate on the same wafer both the
 182 sensor and the front end electronics, with the second one implanted on top within a depth of about
 183 1 μm below the surface.

184 MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the
 185 development of the electronic sector which guarantees the decrease in CMOS transistors dimension
 186 at least every two years, as stated by the Moore's law².

187 As a matter of fact the dimension of components, their organization on the pixel area and logic
 188 density are important issues for the design and for the layout; typically different decisions are taken
 189 for different purposes.

190 Monolithic active pixel can be distinguished between two main categories: MAPS and depleted
 191 MAPS (DMAPS).

192 MAPS (figure a 2.3) have typically an epitaxial layer in range 1-20 μm and because they are not
 193 depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of
 194 charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the
 195 collection could be partial especially after the irradiation of the detector (look at A for radiation
 196 damages), when the trapping probability become higher.

²Moore's law states that logic density doubles every two years.

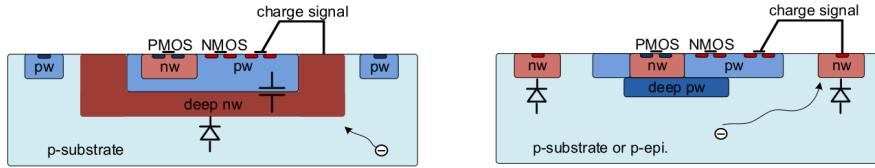


Figure 2.4: Concept cross-section with large and small fill factor

197 In figure 2.3 is shown as example of CMOS MAPS: the sensor in the scheme implements an
 198 n well as collection diode; to avoid the others n wells (which contain PMOS transistor) of the
 199 electronic circuit would compete in charge collection and to shield the CMOS circuit from the
 200 substrate, additionally underlying deep p well are needed. DMAPS are instead MAPS depleted
 201 with d typically in $\sim 25\text{-}150 \mu\text{m}$ (eq. 2.1) which extends from the diode to the deep p-well, and
 202 sometimes also to the backside (in this case if one wants to collect the signal also on this electrode,
 203 additional process must be done).

204 2.4.1 DMAPS: large and small fill factor

205 There are two different sensor-design approaches (figure 2.4) to DMAPS:

- 206 • large fill factor: a large collection electrode that is a large deep n-well and that host the
 207 embedded electronics
- 208 • small fill factor: a small n-well is used as charge collection node

209 To implement a uniform and stronger electric field, DMAPS often uses large electrode design that
 210 requires multiple wells (typically four including deep n and p wells); this layout adds on to the
 211 standard terms of the total capacity of the sensor a new term (fig. 2.5), that contributes to the
 212 total amplifier input capacity. In addition to the capacity between pixels (C_{pp}) and between the
 213 pixel and the backside (C_b), a non-negligible contribution comes from the capacities between wells
 214 (C_{WW} and C_{SW}) needed to shield the embedded electronics. These capacities affect the thermal
 215 and 1/f noise of the charge amplifier and the τ_{CSA} too:

$$216 \quad ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.6) \qquad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.7)$$

217 where g_m is the transconductance, τ_{sh} is the shaping time.
 218 Among the disadvantages coming from this large input capacity could be the coupling between
 219 the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring
 220 electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this prob-
 lem is especially connected with the intra wells capacities. So, larger charge collection electrode

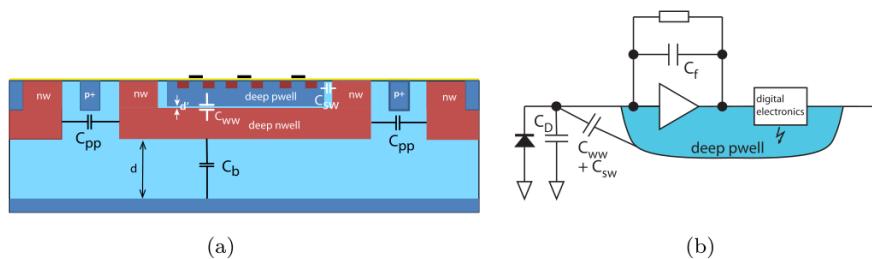


Figure 2.5: C_{pp} , C_b , C_{WW} , C_{SW}

221 sensors provide a uniform electric field in the bulk that results in short drift path and so in good
 222 collection properties, especially after irradiation, when trapping probability can become an issue.
 223 The drawback of a large fill-factor is the large capacity ($\sim 100 \text{ fF}$): this contributes to the noise
 224 and to a speed penalty and to a larger possibility of cross talk.

	small fill factor	large fill factor
small sensor C	✓ (< 5 fF)	✗ (~ 100-200 fF)
low noise	✓	✗
low cross talk	✓	✗
velocity performances	✓	✗ (~ 100 ns)
short drift paths	✗	✓
radiation hard	✗	✓

Table 2.1: Small and large fill factor DMAPS characteristics

226 The small fill-factor variant, instead, benefits from a small capacity (5-20 fF), but suffers from
 227 a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando dei
 228 MAPS, devo ripetere qui?**

229 As we'll see these two different types of sensor require different amplifier: the large electrode one is
 230 coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.5.1).

231 2.4.2 A modified sensor

232 A process modification developed by CERN in collaboration with the foundries has become the
 233 standard solution to combine the characteristics of a small fill factor sensor (small input amplifier
 234 capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE
 235 upgrade about ten years [1].

236 A compromise between the two sensors could also be making smaller pixels, but this solution
 237 requires reducing the electronic circuit area, so a completely new pixel layout should be though.
 238 The modification consists in inserting a low dose implant under the electrode and one its advantage
 239 lies in its versatility: both standard and modified sensor are often produced for testing in fact.

240 Before the process modification the depletion region extends below the diode towards the sub-
 241 strate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.6).
 242 After, two distinct pn junctions are built: one between the deep p well and the n^- layer, and the
 243 other between the n^- and the p^- epitaxial layer, extending to the all area of the sensor.

244 Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes
 245 can be biased separately³ and this is beneficial to enhance the vertical electric field component.

246 The doping concentration is a trimmer parameter: it must be high enough to be greater than the
 247 epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be
 248 lower enough to allow the depletion without reaching too high bias.

249 2.5 Analog front end

250 After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.7), ready
 251 to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an
 252 efficient, high-speed readout architecture, consuming as low power as possible must be provided
 253 by the readout integrated electronics (ROIC).

254 Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually
 255 often is the only amplification stage) with a reset to the baseline mechanism and a leakage current
 256 compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be
 257 optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise
 258 before the amplification stage in order to not multiply that noise, and chose a reasonable threshold
 259 of the discriminator to cut noise-hits much as possible.

260 2.5.1 Preamplifier

261 Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled
 262 as an operational amplifier (OpAmp) where the gain is determined by the input and feedback

³This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

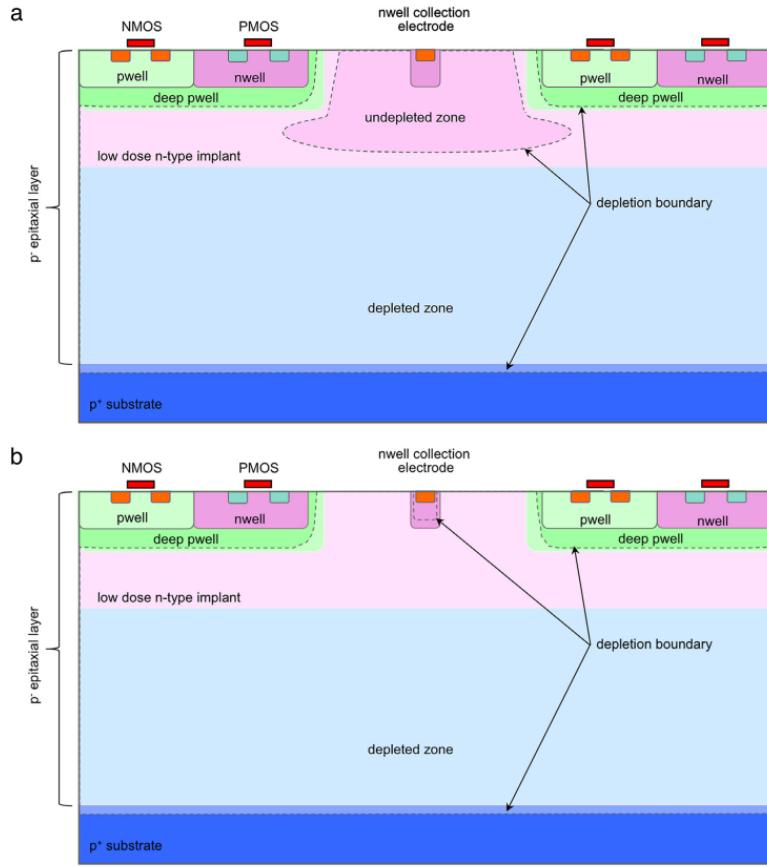


Figure 2.6: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

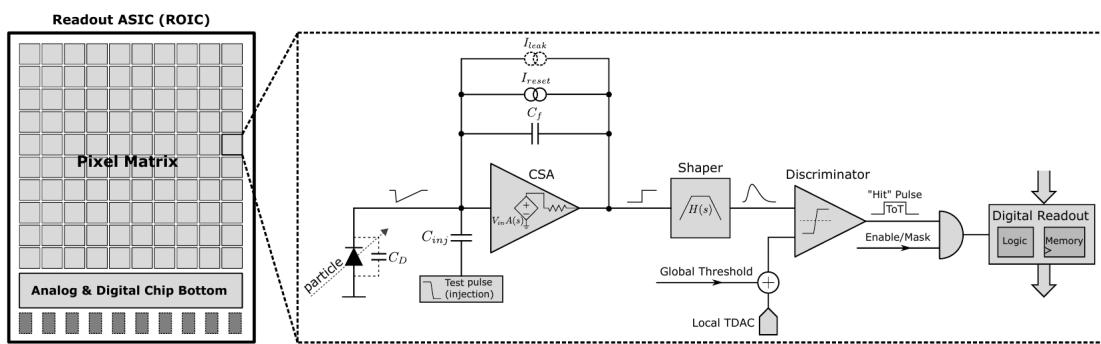


Figure 2.7: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

263 impedance (first step in figure 2.7):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.8)$$

264 Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a
 265 voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the
 266 voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor
 267 MAPS whose signal is already enough high: $v_{in} = Q/C_D \approx 3\text{fC}/100\text{ pF} = 0.03\text{ mV}$, but it's fine
 268 for the small fill factor ones: $v_{in} = Q/C_D \approx 3\text{fC}/3\text{ pF} = 1\text{ mV}$.

269 In the case of a resistor feedback, if the signal duration time is longer than the discharge time
 270 ($\tau = R_S C_D$) of the detector the system works as current amplifier, as the signal is immediately
 271 trasmit to the amplifier; in the complementary case (signal duration longer than the discharge
 272 time) the system integrates the current on the C_D and operates as a voltage amplifier.

273 2.6 Readout logic

274 Readout logic includes the part of the circuit which takes the FE output signal, processes it and
 275 then transmit it out of pixel and/or out of chip; depending on the situation of usage different
 276 readout characteristics must be provided.

277 To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers
 278 and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really
 279 high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is
 280 recorded).

281 A common compromise often made is to save the time over threshold (ToT) of the pulse in clock
 282 cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen
 283 bits but, being correlated and hopefully being linear with the deposited charge by the impinging
 284 particle in the detector, it provides a sufficient information. The ToT digitalization usually takes
 285 advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels'
 286 matrix. The required timing precision is at least around 25 ns, that corresponds to the period of
 287 bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is
 288 40 MHz.

289 Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they
 have been read, and then the ToT is obtained from their difference.

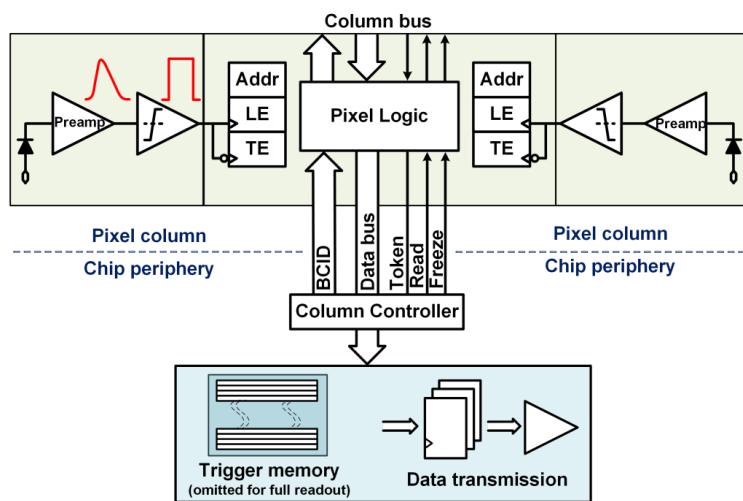


Figure 2.8: Column drain R/O scheme where ToT is saved

290 Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger
 291 system decides if the hit must be store or not. On one hand the triggered-readout needs buffers
 292 and storage memories, on the other the full readout, because there is no need to store hit data on
 293 chip, needs an high enough bandwidth.

294 A triggered readout is fundamental in accelerator experiments where the quantity of data to store
 295 is too large to be handled, and some selections have to be applied by the trigger: to give an order

297 of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100
 298 MBit/s [2] (pag. 797).

299 Typically the trigger signal is processed in a few μs , so the pixel gets it only after a hundred clock
 300 cycles from the hit arrival time: the buffer depth must then handle the higher trigger latency.

301 After having taken out the data from the pixel, it has to be transmitted to the end of column
 302 (EoC) where a serializer deliver it out of chip, typically to an FPGA.

303 There are several ways of transmitting data from pixel to the end of column: one of the most
 304 famous is the column-drain read out, developed for CMS and ATLAS experiments [3]. All the
 305 pixels in a double-column share a data bus and only one pixel at a time, according to a priority
 306 chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit
 307 arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored
 308 on a RAM until the SH does not allow the access to memory by data bus.

309 Even if many readout architectures are based the column-drain one, it doesn't suit for large size
 310 matrices. The problem is that increasing the pixels on a column would also raise the number of
 311 pixels in the priority chain and that would result in a slowdown of the readout.

312 If there isn't any storage memory, the double-column behaves as a single server queue and the
 313 probability for a pixel of waiting a time T greater than t , with an input hit rate on the column μ
 314 and an output bandwidth B_W is [4]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.9)$$

315 To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time τ due to the
 316 AFE), for example imposing $P(T > t) \sim 0.001$, one obtains $(B_W - \mu) t_t \sim 6$, where t_t is the time
 317 needed to transfer the hit; since t_t is small, one must have $B_W \gg \mu$, that means a high bandwidth
 [4].

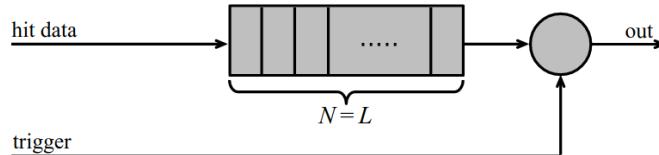


Figure 2.9: Block diagram of a pipeline buffer: N is the dimension of memory buffer and L is the trigger latency expressed in BCID cycles

318 Actually the previous one is an approximation since each pixel sees a different bandwidth de-
 319 pending on the position on the queue: the first one sees a full bandwidth, but the next sees a
 320 smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen
 321 by the pixel i is $B_i = B - \sum_j \mu_j$, where μ_j is the hit rate of the j th pixel.

322 The efficiency requirement on the bandwidth and the hit rate becomes: $B_{W,i} > \mu_i$, where the
 323 index i means the constraint is for a single pixel; if all the N pixels on a column have the same
 324 rate $\mu = N\mu_i$, the condition reduces to $B_W > \mu$. The bandwidth must be chosen such that the
 325 mean time between hits of the last pixel in the readout chain is bigger than that.

326 In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed;
 327 this means that only information from channels where the signal exceeds the discriminator thresh-
 328 old are stored. Qualcosa sulla zero suppression? La metto qui questa affermazione?

329 If instead there is a local storage until a trigger signal arrives, the input rate to column bus
 330 μ' is reduced compared to the hit rate μ as: $\mu' = \mu \times r \times t$, where r is the trigger rate and t is
 331 the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth,
 332 but the limiting factor is the buffer depth: the amount of memory designed depends both on the
 333 expected rate μ and on the trigger latency t as $\propto \mu \times t$, that means that the higher the trigger
 334 latency and the lower the hit rate to cope with.

335 In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels
 336 into regions with shared storage. Let's compare two different situations: in the first one a buffer
 337 is located on each pixel area, while in the second one a core of four pixels share a common buffer
 338 (this architecture is commonly called FE-I4).

339 Consider a 50 kHz single pixel hits rate and a trigger latency of 5 μs , the probability of losing

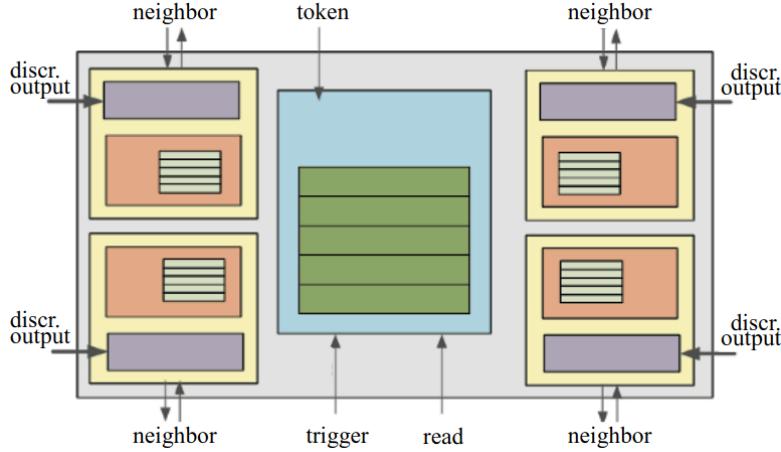


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is highlighted in light blue; latency counters and trigger management section are highlighted in green; hit processing blocks are highlighted in purple; ToT counters and ToT management units are highlighted in orange

³⁴¹ hits is:

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.10)$$

³⁴² where I have assumed a Poissonian distribution with mean $\nu = 0.25$ to describe the counts N.

³⁴³ To get an efficiency ϵ greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.11)$$

³⁴⁴ Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four
³⁴⁵ pixels the mean number of hits per trigger latency is $\nu = 0.25 \times 4 = 1$. To get an efficiency of
³⁴⁶ 99.9% (eq. 2.11) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

³⁴⁷ Chapter 3

³⁴⁸ Use of pixel detectors

³⁴⁹ There always was a tight relation between the development of cameras and pixel detectors since
³⁵⁰ 1969, when the idea of CCDs, thanks to whom Boyle and Smith were awarded the Nobel Prize in
³⁵¹ Physics in 2009, revolutionized photography allowing light to be captured electronically instead of
³⁵² on film. Even though the CMOS technology was already known when CCDs spread, the costs of
³⁵³ productions were too high to allow the diffusion of these sensors for which needed to wait until
³⁵⁴ 1990s. From that period on, the fast diffusion of CMOS was mainly due to the less cost than
³⁵⁵ CCD, and the less power required for supply. Nowadays CCDs are still preferred over MAPS in
³⁵⁶ astronomy, where the astronomical sources' rate are low enough to cope with tens of ms for the
³⁵⁷ readout.

³⁵⁸ The principal use cases of pixel detectors are particle tracking and imaging: in the former case
³⁵⁹ individual charged particles have to be identified, in the latter instead an image is obtained by
³⁶⁰ the usually un-triggered accumulation of the impinging radiation. Also the demands on detectors
³⁶¹ performance depends on their usage, in particular tracking requires high spatial resolution, fast
³⁶² readout and radiation hardness.

³⁶³ 3.1 Tracking in HEP

³⁶⁴ At first the physics world overlooked the CCDs, and all pixel in general, as against the gaseous
³⁶⁵ detector for tracking: there was no need to replace these ones which had a sufficient good resolution
³⁶⁶ ($100\text{ }\mu\text{m}$). Since 1974, with the measurement of the invariant mass of the **j psi** and the affirmation
³⁶⁷ of the quark model, all experiments start to look for better spatial resolutions in order to achieve
³⁶⁸ the possibility of reconstructing short lived particle.

³⁶⁹ Historically, the first pixel detector employed in particle physics was a CCD: it was installed in
³⁷⁰ the spectrometer at the CERN's Super Proton Synchrotron (SPS) by the ACCMOR Collaboration
³⁷¹ (Amsterdam, CERN, Cracow, Munich, Oxford, RAL) at mid 1980s, with the purpose of studying
³⁷² the recently-discovered charm particles. The second famous usage of CCDs took place at SLAC
³⁷³ in the Large Detector (SLD) during the two years 1996-98. **Cosa vedono di così importante da**
³⁷⁴ **dire che servono i pixel detector?** From that period on particle tracking in experiments have been
³⁷⁵ transformed radically: it was mandatory for HEP experiments to build an inner vertex detector.
³⁷⁶ In 1991, the more demanding environments led to the development of hybrid pixel detectors:
³⁷⁷ a dedicated collaboration, RD19, was established at CERN with the specific goal to define a
³⁷⁸ semiconductor micropattern detector with an incorporated signal processing at a microscopic level.
³⁷⁹ In those years a wide set of prototypes of hybrid pixel has been manufactured; among the greatest
³⁸⁰ productions a mention goes to the huge ATLAS and CMS vertex detectors. From the middle of
³⁸¹ 2013 a second collaboration, RD 53, has been established with the new goal to find a pixel detector
³⁸² suitable for phase II future upgrades of those experiments. Even if the collaboration is specifically
³⁸³ focused on design of hybrid pixel readout chips (aiming to 65 nm technique so that the electronics
³⁸⁴ fits within the pixel area), also other options have been taken in account and many test have been
³⁸⁵ done on MAPS for example. Requirements imposed by HL-LHC will become tighter in time: for
³⁸⁶ example, a dose and radiation of 5 Mrad and 1016 NIEL are expected after 5 years of operation.
³⁸⁷ Time resolution, material budget and power consumption are also issues for the upgrade: a time
³⁸⁸ resolution better than 25 ns for a bunch crossing frequency of 40 MHz, a material budget lower
³⁸⁹ than 2% and a power consumption lower than 500 mW/cm^2 are required.

390 Amidst the solutions proposed 3D silicon detector, invented by Sherwood Parker in 1995, and
391 MAPS are the most promising. In 3D sensors the electrode is a narrow column of n-type implanted
392 vertically across the bulk instead of being implanted on the wafer's surface. The charge produced
393 by the impinging particle is then drifted transversally within the pixel, and, as the mean path
394 between two electrode can be sufficient low, the trap probability is not an issue. 3D pixels have
395 been already proved in ATLAS tracker [quando?](#). Even if 3D detector are adequately radiation hard,
396 MAPS architecture looked very promising from the beginning: they overcome both the CCDs long
397 reading time and the hybrid problems (I have already explained in section ?? the benefits of
398 MAPS). Experiments such as ALICE at LHC and STAR at RHIC have already introduced the
399 CMOS MAPS technology in their detectors. ALICE Tracking System (ITS2), upgraded during the
400 LHC long shut down in 2019-20, was the first large-area ($\sim 10 \text{ m}^2$ covered by 2.5 Gpixels) silicon
401 vertex detector based on CMOS MAPS.

402 3.1.1 Hybrid pixels at LHC: ATLAS, CMS and LHC-b

403 ATLAS

404 With CMS, ATLAS is one of two general-purpose detectors at the LHC and has the largest volume
405 detector ever constructed for a particle collider (46 m long and 25 m in diameter). The Inner
406 Detector consists of three different systems all immersed in a magnetic field parallel to the beam
407 axis whose main components are: the pixel, the micro-strips and transition radiation trackers.
408 Concerning the pixel detector, 92 million pixels are divided in 4 barrel layers and 3 disks in each
409 end-cap region, covering a total area of 1.9 m^2 and having a 15 kW of power consumption.

410 As stated by the ATLAS collaboration the pixel detector is exposed by an extreme particle
411 flux: "By the end of Run 3¹, the number of particles that will have hit the innermost pixel layers
412 will be comparable to the number it would receive if it were placed only a few kilometres from
413 the Sun during a solar flare". Considering that the particle density will increase even more with
414 HL-LHC, radiation hardness is definitively target to achieve.

415 The most ambitious goal is employ a MAPS-based detector for the inner-layer barrels, and for
416 this reason the RD53 collaboration is performing many test on MAPS prototypes, as Monopix of
417 which I will talk about in section ??.

418 Up to now this possibility will be eventually implemented during the second phase of the HL-
419 LHC era, as at the start of high-luminosity operation the selected option is the hybrid one. The
420 sensor will be bonded with ITkPix, the first full-scale 65 nm hybrid pixel-readout chip developed
421 by the RD53 collaboration. Regarding the sensor, a valuable option is using 3D pixels, which
422 have already proved themselves in ATLAS, for the insertable B layer (IBL).[qualcosa in più sui 3d.](#)
423 The number of pixels will be increased of a factor about 7, passing from 92 millions to 6 billion.

424 CMS

425 LHCb

426 LHCb is a dedicated heavy-flavour physics experiment that exploits pp interactions at 14 TeV at
427 LHC. It was the last experiment to upgrade the vertex detector, the Vertex Locator (VELO),
428 replacing the silicon-strip with pixels in May 2022. As the instantaneous luminosity in Run3 is
429 increased by a factor $\lesssim 10$, much of the readout electronics and of the trigger system have been
430 developed in order to cope with the large interaction rate. To place the detector as close as possible
431 to the beampipe and reach a better track reconstruction resolution, the VELO has a surprising
432 feature: it can be moved. During the injection of LHC protons it is parked at 3 cm from the beams
433 and only when the stability is reached it is brought at ~ 5 mm. Radiation hardness as well as readout
434 speed are then a priority for the detectors: that's why the collaboration opted for a hybrid system.
435 The Velopix is made bonding sensors, each measuring 55×55 micrometers, 200 μm -thick to a
436 200 μm -thick ASIC specially developed for LHCb and coming from the Medipix family (sec. ??),
437 which can handle hit rates up to 900 MHz per chip. Since the detector is operated under vacuum
438 near the beam pipe, the heat removal is particularly difficult and evaporative CO₂ microchannel
439 cooling are used.

¹Run 3 start in June 2022

440 **3.1.2 A DEPFET example: Belle-II**

441 **da scrivere, Depleted P-channel FET (DEPFET)**

442 Per l'upgrade LSH2 nel 2026-7 sostituzione di VXD con VTX. VXD è costituito attualmente
443 da PXD e dalle microtips, si sostituiranno le microstrip con un rivelatore a pixel monolitico.
444 Grande vantaggio introdotto sarà una diminuzione dell'occupancy, molto importante se si vuole
445 raggiungere alte luminosità. Consentirà inoltre una **più grande** reiezione del fondo; inoltre verrà
446 introdotto nel flow del trigger l'informazione del pixel detector, cosa che non è vera adesso. Con la
447 diminuzione del material budget si avrà un miglioramento sulla ricostruzione dei vertici che è un
448 aspetto importante soprattutto nel caso in cui si voglia studiare decadimenti di particelle a vita
449 media breve. The OBELIX chip, selezionato per l'upgrade, is currently under design e sarà basato
450 su TJ-Monopix2, successore di monopix1 se non he conterrà ina memoria.

451 **3.1.3 CMOS MAPS: ALICE and STAR**

452 **ALICE**

453 ALICE (A Large Ion Collider Experiment) is a detector dedicated to heavy-ion physics and to the
454 study of the condensed phase of the chromodynamics at the LHC. The tracking detector consists of
455 the Inner Tracking System (ITS), the gaseous Time Projection Chamber (TPC) and the Transition
456 Radiation Detector (TRD), and all those are embedded in a magnetic field of 0.5 T. The ITS is
457 made by six layers of detectors, two for each type, from the interaction point outwards: Silicon
458 Pixel Detector (SPD), Silicon Drift Detector (SDD) and Silicon Strip Detector (SSD). Contrary
459 to the others LHC experiments, ALICE tracker in placed in a quite different environments: the
460 expected dose is smaller by two order of magnitude and the rate of interactions is few MHz instead
461 of 40 MHz, but the number of particles comes out of each interaction is higher (the SPS is invested
462 by a density of particles of $\sim 100 \text{ cm}^{-2}$). The reconstruction of very complicated events whit a
463 large number of particle is a challenge, hence to segment and to minimize the amount of material,
464 which may cause secondary interaction complicating futher the event topology, is considered a
465 viable strategy. Thanks to the reduction of the material budget, ITS2, which uses the ALPIDE
466 chip developed by ALICE collaboration, obtained an amazing improvement both in the position
467 measurement and in the momentum resolution, improving the efficiency of track reconstruction
468 for particle with very low transverse momentum (by a factor 6 at $pT \sim 0.1 \text{ GeV}/c$). Further
469 advancements in CMOS MAPS technology are being aggressively pursued for the ALICE ITS3
470 vertex detector upgrades (foreseen around 2026-27), with the goals of further reducing the sensor
471 thickness and improving the readout speed of the devices, while keeping power consumption at a
472 minimum.

473

474 **STAR**

475 MIMOSA-28 devices for the first MAPS-based vertex detector: a 356 Mpixel two-layer barrel
476 system for the STAR experiment at Brookhaven's Relativistic Heavy Ion Collide **da scrivere**

477 **3.2 Applications in imaging**

478 Historically for imaging pourpose the CCDs were the favoured device: they can be used as single
479 photon counter or integrating and collecting the charge released by more impinging particles. The
480 utilisation in the first case is similar to the tracking one, except that the requirements are less
481 tight, so much that two noteworthy of microchips originally meant for detectors in particle physics
482 at the LHC, and later employed in other fields are Medipix and Timepix. They are read-out chips
483 developed by the Medipix Collaborations since early 1990s. For two decades, different Medipix
484 generations have been produced, having a rough correlation with the feature size used: Medipix2
485 (1999) used 250 nm feature size CMOS while Medipix3 (2005) 130 nm. The aim of the fourth col-
486 laboration (2016), instead, is designing pixel read-out chips that prepared for **TSV processing and**
487 **may be tiled on all four sides. DOVREI METTERE DUE RIGHE SU TSV OPPURE TAGLIARE.**

488 For photons imaging other materials with higher atomic charge than silicon could be prefered,
489 as a high photon absorption efficiency is needed: it was for this reason that Medipix2 was bump
490 bonded to identically segmented sensors of both silicon and GaAs.

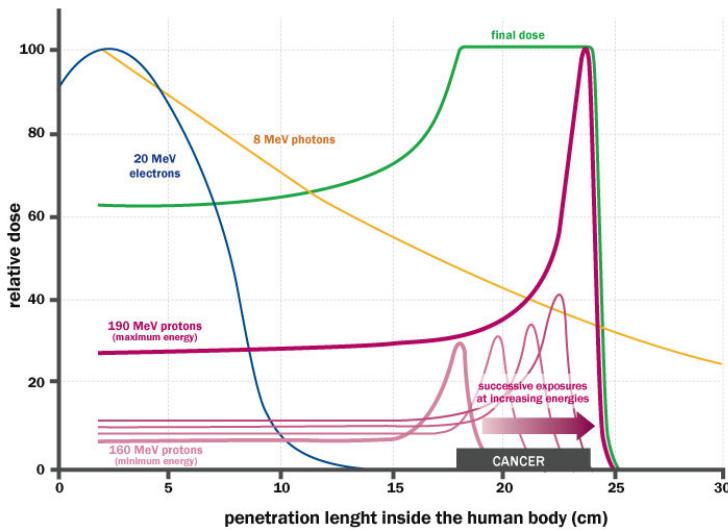


Figure 3.1: The Spread Out Bragg Peak (SOBP) curve (green), which is a constant dose distribution, is obtained from the superposition of many Bragg peak of hadrons with different energy.

491 The applications in scientific imaging vary from astrophysics and medical imaging to more exotic
 492 domains as studies of protein dynamics, art authentication and dosimetry. The most important
 493 employment of Medipix is as X-ray single photon counting in industrial and medical radiography
 494 and in 3D computed tomography. Thanks to a New-Zealand company, the MARS Bioimaging
 495 detector has been fabricated, which is capable of resolving the photons energy and produce 3D
 496 coloured images. Besides tracking in HEP (I have already cited the use of Timepix3 is in the beam
 497 telescope of the LHCb VELO), an important use of Timepix is in dosimetry [Timepix Detector](#)
 498 [for Imaging in Ion Beam Radiotherapy- aggiungi qualche info](#) A small-Timepix detector with the
 499 dimension of a USB can also be found at the International Space Station, where it is exploited for
 500 radiation, principally made of heavy-ion, monitoring.

501 3.2.1 Applicability to FLASH radiotherapy

502 The radiological treatment is a common method used in 60% of tumors both as palliative care
 503 and as treatment. It can be given before, after or during a surgery, (Intra operative radiation
 504 therapy-IORT) and many different types of radiations (photons, electrons, protons and ions, which
 505 mainly are hydrogen and carbon) can be used to irradiate the affected tissues. Exploiting the
 506 ionizing energy loss a biological damage can be delivered to the tissue. [nomina il LET](#). If x-ray
 507 photons, with energy in \sim 4-25MeV, are used, the ionization is caused by the Compton electrons
 508 and is more in the superficial layers of the tissue due to the exponential attenuation of the beam.
 509 The hadrons energy loss, instead, is strongly localized in the last region of the track, that is the
 510 Bragg peak. Ion beam enables better focusing of the radiation thereby improves the sparing of the
 511 surrounding healthy tissues; on the other hand the delivered dose distribution depends more on
 512 the patient's density tissues (e.g. bones, swelling, fat).

513 Recently² a promising method for RT at ultra high dose rate (at least 40 Gy/s) and for this
 514 reason called FLASH-RT, instead of CONV-RT (0.03 Gy/s), came out. This treatment takes
 515 advantages of biological differences between tumors and healthy tissues: it is characterized by
 516 reducing normal tissue toxicity and maintaining equivalent tumor damage. The response to dose
 517 can be described by the survival fraction probability, describing the fraction of surviving cell as a
 518 function of the dose:

²The first evidences has been observed on a mice experiments in 1966 and in 2014 by the group of Favaudon and Vozenin. After this, many test on cats and pigs have been performed, and also there has been a clinical trial on a cutaneous tumor-patient

	CONV-RT	FLASH-RT
Dose rate	0.03 Gy/s	40 Gy/s
Intra pulse dose rate	100 Gy/s	106 Gy/s
Treatment duration	~minutes	$\lesssim 500 \text{ ms}$
DDP		1.5 Gy
N of pulses		10

Table 3.1: Esempi di valori tipici di dose in un trattamento

$$S(D) = S(0) e^{-F(D)} \quad (3.1)$$

$$F(D) = \alpha D + \beta D^2 \quad (3.2)$$

519

521

522 dove $F(D)$ è una funzione che rappresenta il danno alle cellule ed α and β are respectively
 523 Hence, at high doses the density of damages increases and the cells repair becomes more difficult.
 524 Even if the FLASH effect is not yet completely understood, it looks like there are two different
 525 recipes which are involved:

- 526 • the dose rate: come mostrato in figura ad alti dose rate il danno è maggiore. However at lower
 527 dose rates and therefore longer irradiation time, other effects such as redistribution of cells
 528 through the cell cycle and cell repopulation can also modify the sparing effect.
- 529 • oxygen effect: The presence or absence of molecular oxygen O₂ within a cell influences the
 530 biological effect of ionizing radiation: hypoxic cells are very resistant to radiation, whereas
 531 normal oxygenated cells are highly radiosensitive. Cellule che esibiscono hypoxia (cioè cellule
 532 che non hanno ossigeno sono radioresistenti); al contrario normoxia e physoxia non lo sono.
 533 la presenza di ossigeno rende la curva steeper indicando che lo stesso danno si raggiunge a
 534 livelli di dose più bassi rispetto al caso senza ossigeno. Dovuto al fatto che sotto la radice le
 535 molecole si rompono e se c'è ossigeno (molto elettronegativo) si possono formare dei radicali
 536 dannosi.

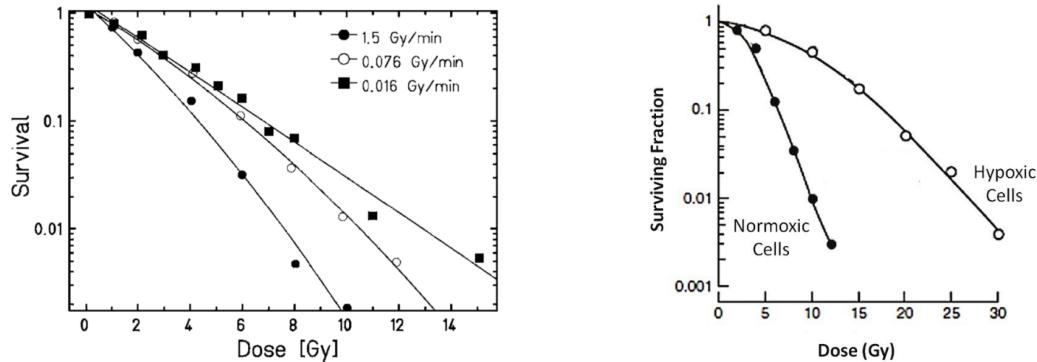


Figure 3.2: (a) Survival curve . (b)

537 The Tumor Control Probability (TCP) and the Normal Tissue Complication (NTC) functions
 538 parametrize respectively the efficiency of damaging on the tumor after having released a certain
 539 dose and the probability of not affecting the healthy tissues. The intermediate zone between the
 540 increase of the TC and of the NTC is called therapeutic window, and the wider it is and the more
 541 effective the treatment is.

542 Dosimetric problems

543 Finding equipment suitable for dosimetry at ultra high dose rate is an issue: FLASH-RT cause
 544 a radical change in the beam characteristics, in the delivery time structure and, above all, in the
 545 average and instantaneous dose-rate, which points-out the limits of the current available dosime-
 546 ters. In fact, the active dosimeters for online monitoring of the beam that are used in daily clinical

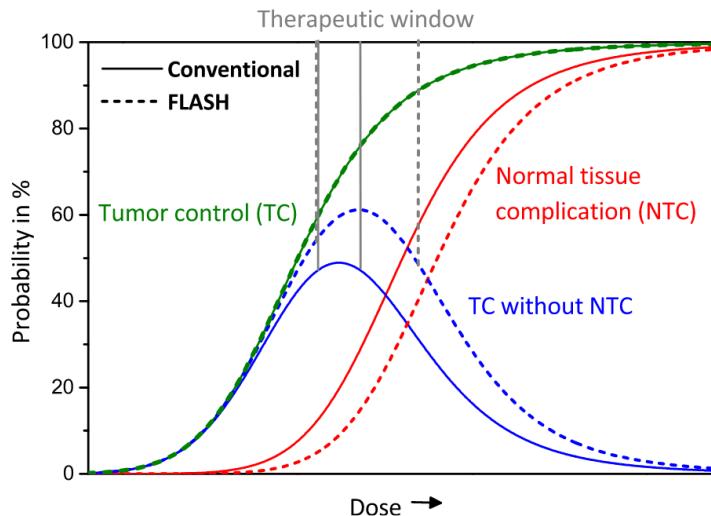


Figure 3.3: Illustration of dependence of TCP, NTCP and therapeutic window on dose, for CONV-RT ad FLASH-RT.

practice show saturation problem: crucial both for radiobiological studies and for a safe clinical translation. On the other hand passive dosimeters could provide dosimetric data, showing dose-rate independence up to 10 alla nove Gy/s for radiochromic films. Cosa sono i radiochromic films and they do not have the same accuracy of other detectors.

For online measurements, the available detector are ionization chamber, semiconductors and scintillators, but nevertheless they start to exhibit saturation when the dose-rate/DPP is increased beyond what is used in clinical routine. Le camere a ionizzazione hanno già un po' di problemi a DPP di due ordini di grandezza sotto la DDP della flash (quindi quelle tipiche della iort.) Doppi problemi sia di saturazione sia di scariche: questo doppio effetto è dato dal fatto che, creandosi tante cariche nella camera, che va ad annullare il campo elettrico di drift. Questo ovviamente paralizza le cariche che non driftano più, ma che anzi si ricombinano ed inoltre facilita la formazione di scariche. Scintillators have reusable, non-exhaustible scintillation centers. However, the system has a total deadtime given by both the crystal scintillation time and the electronics read-out deadtime.

Semiconductors show a nonreversible saturation beyond a threshold around 15 cGy/p. The scintillator used, shows a negligible saturation up to 1 Gy/p, but it increases significantly up to at least 11 Gy/p, and it reaches a cutoff value between 11 and 36 Gy/p.

Scintillator dosimeters are widely used in radiotherapy. They are usually operating in counting-mode where each detected signal is processed by read-out electronics. When a scintillator dosimeter is used in integrator-mode the signal is integrated over the entire irradiation time. A deadtime, due to the decay time of the scintillating material, is considered on average every N recorded pulses, where N is the number of scintillation centres in the dosimeter.

Besides saturation i problemi sono anche altri: The most important dosimetric aspects needed for an active detector are dose rate independence and high temporal resolution.

Concerning spatial resolution: Un altro grande limite delle camere a ionizzazione è la risoluzione spaziale dato ch non posson essere fatte più piccole di circa un centimetro. Questo limite è principalmente dovuto a problemi meccanici per cui non si può fare una camera con P bassa e con materiali sottili, perchè le pareti si incurvano.

Monitorare la posizione e direzionalità del fascio, anche per la VHEE quindi detto in altre parole un beam monitor. Questo detector deve essere abbastanza veloce da poter fornire una risposta in real time e avere anche una buona risoluzione temporale.

⁵⁷⁸ **Chapter 4**

⁵⁷⁹ **TJ-Monopix1**

⁵⁸⁰ TJ-Monopix1 is a small electrode DMAPS with fast R/O capability, fabricated by TowerJazz
⁵⁸¹ foundry in 180 nm CMOS imaging process. It is part, together with prototypes from other series
⁵⁸² such as TJ-MALTA, of the ongoing R&D efforts aimed at developing DMAPS in commercial CMOS
⁵⁸³ processes, that could cope with the requirements at accelerator experiments. Both TJ-Monopix
⁵⁸⁴ and TJ-MALTA series [5], produced with the same technology by TowerJazz (the timeline of the
⁵⁸⁵ foundry products is shown in figure 4.1), are small electrode demonstrators and principally differ in
⁵⁸⁶ the readout design: while Monopix implements a column-drain R/O, an asynchronous R/O without
⁵⁸⁷ any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.



Figure 4.1: Timeline in TowerJazz productions in 180 nm CMOS imaging process

⁵⁸⁸ Another Monopix series, but in 150 nm CMOS technology, has been produced by LFoundry [6].
⁵⁸⁹ The main differences between the LF-Monopix1 and the TJ-Monopix1 (summarized in table 4.2),
⁵⁹⁰ lay in the sensor rather than in the readout architecture, as both chips implements a fast col-
⁵⁹¹ umn drain R/O with ToT capability [7][8]. Concerning the sensors, either are based on a p-type
⁵⁹² substrate, but with slightly different resistivities; in addition LFoundry pixels are larger, thicker
⁵⁹³ and have a large fill factor (the very deep n-well covers ~55% of the pixel area). The primary
⁵⁹⁴ consequence is that LF-Monopix1 pixels have a higher capacity resulting in higher consumption
⁵⁹⁵ and noise. As I discussed in section 2.4.1, the fact that LF-Monopix has a large fill factor electrode
⁵⁹⁶ is expected to improve its radiation hardness. Indeed, a comparison of the performance of the
⁵⁹⁷ two chips showed that TJ-Monopix suffers a comparatively larger degradation of efficiency after
⁵⁹⁸ irradiation, due to the low electric field in the pixel corner; on the other hand, a drawback of the
⁵⁹⁹ large fill factor in LF-Monopix is a significant cross-talk.

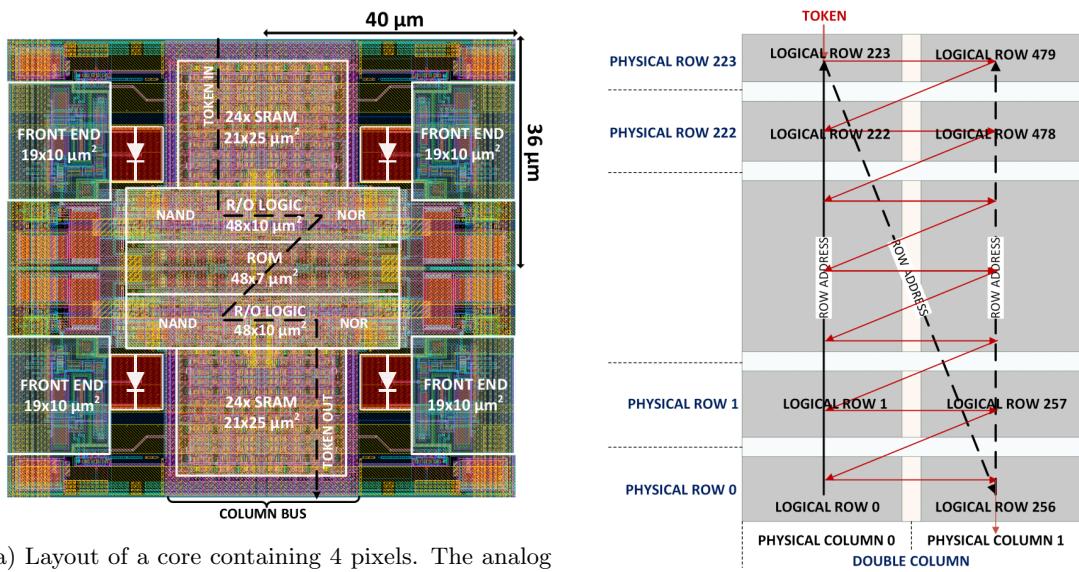
⁶⁰⁰ The TJ-Monopix1 chip contains, apart from the pixels matrix, all the required support blocks
⁶⁰¹ used for configuration and testing:

- ⁶⁰² the whole matrix contains 224×448 pixels, yielding a total active area approximately equal
⁶⁰³ to 145 mm^2 over a total area of $1 \times 2 \text{ cm}^2$;
- ⁶⁰⁴ at the chip periphery are placed some 7-bit Digital to Analog Converter (DAC), used to
⁶⁰⁵ generate the analog bias voltage and current levels and to configure the FE;

	LF-Monopix1	TJ-Monopix1
Resistivity	$>2\text{ k}\Omega\text{cm}$	$>1\text{ k}\Omega\text{cm}$
Pixel size	$50 \times 250\mu\text{m}^2$	$36 \times 40\mu\text{m}^2$
Depth	$100\text{-}750\mu\text{m}$	$25\mu\text{m}$
Capacity	$\sim 400\text{ fF}$	$\sim 3\text{ fF}$
Preamplifier	charge	voltage
Threshold trimming	on pixel (4-bit DAC)	global threshold
ToT	8 bits	6 bits
Consumption	$\sim 300\text{ mW/cm}^2$	$\sim 120\text{ mW/cm}^2$
Threshold	$1500 e^-$	$\sim 270 e^-$
ENC	$100 e^-$	$\sim 30 e^-$

Table 4.1: Main characteristics of Monopix1 produced by TowerJazz and LFoundry [7][8]

- at the EoC is placed a serializer to transferred datas immediately, indeed no trigger memory is implemented in this prototypes;
 - the matrix power pads are distributed at the sides
 - four pixels which have analog output and which can be monitored with an oscilloscope, and therefore used for testing
- Pixels are grouped in 2×2 cores (fig. 4.2a): this layout allows to separate the analog and the digital electronics area in order to reduce the possible interference between the two parts. In addition it simplifies the routing of data as pixels on double column share the same column-bus to EoC. Therefore pixels can be addressed through the physical column/row or through the logical column/row, as shown in fig. 4.2b: in figure is also highlighted the token propagation path, whose I will discuss later.



(a) Layout of a core containing 4 pixels. The analog FE and the digital part are separated in order to reduce cross-talk be

(b)

4.1 The sensor

As already anticipated, TJ-Monopix1 has a p-type epitaxial layer and a n doped small collection electrode ($2\mu\text{m}$ in diameter); to avoid the n-wells housing the PMOS transistors competing for the charge collection, a deep p-well substrate, common to all the pixel FE area, is used. TJ-Monopix1 adopts the modification described in section 2.4.2 that allows to achieve a planar depletion region

Parameter	Value
Matrix size	$1 \times 2 \text{ cm}^2$
Pixel size	$36 \times 40 \mu\text{m}^2$
Depth	$25 \mu\text{m}$
Electrode size	$2 \mu\text{m}$
BCID	40 MHz
ToT-bit	6
Power consumption	$\sim 120 \text{ mW/cm}^2$

Table 4.2

near the electrode applying a relatively small reverse bias voltage. This modification improves the efficiency of the detector, especially after irradiation, however a simulation of the electric field in the sensor, made with the software TCAD (Technology Computer Aided Design), shows that a nonuniform field is still produced in the lateral regions of the pixel compromising the efficiency at the corner. Two variations to the process have been proposed in order to further enhance the transversal component of electric field at the pixel borders: on a sample of chip, which includes the one in Pisa, a portion of low dose implant has been removed, creating a step discontinuity in the deep p-well corner (fig. 4.3); the second solution proposed[MOUSTAKAS THESYS, PAG 58] consists in adding an extra deep p-well near the pixel edge. A side effect of the alteration in the low dose implant is that the separation between the deep p-well and the p-substrate becomes weak to the point that they cannot be biased separately to prevent the punchthrough.

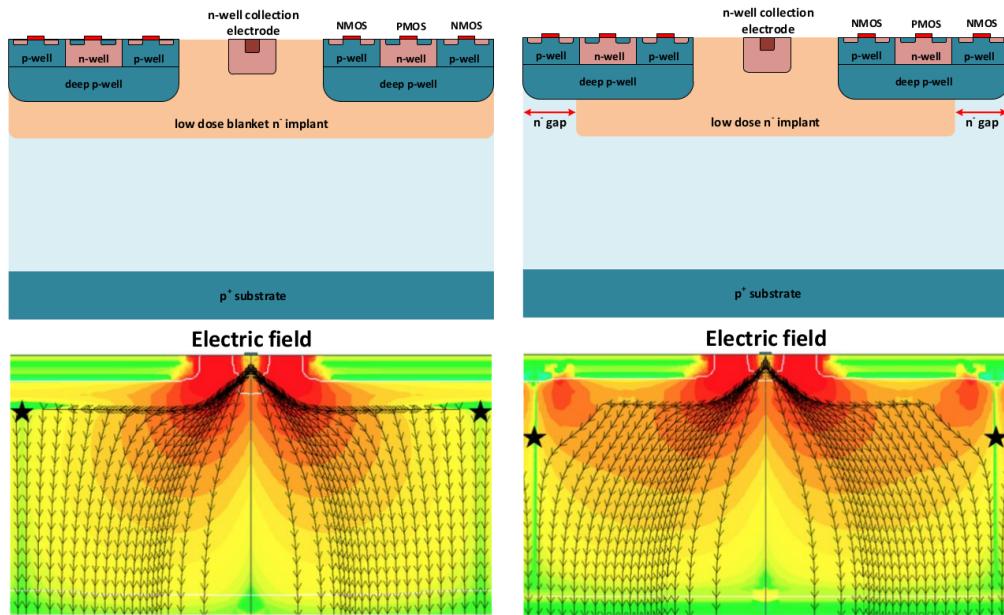


Figure 4.3: (a) The cross-section of a monolithic pixel in the TJ-Monopix with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field. this point in figure is indicated by a star . transversal component of the electric field drops at the pixel corner

Moreover, to investigate the charge collection properties, pixels within the matrix are split between bottom top half and bottom half and feature a variation in the coverage of the deep p-well: the electronics area can be fully covered or not. In particular the pixels belonging to rows from 0 to 111 are fully covered (FDPW) and pixels belonging to rows from 112 to 223 have a reduced p-well (RDPW), resulting in a enhancement of the lateral component of the electric field.

4.2 Front end

639 The matrix is split in four sections, each one corresponding to a different flavor of the FE. The
640 four variation have been implemented in order to test the data-bus readout circuits and the input
reset modes.

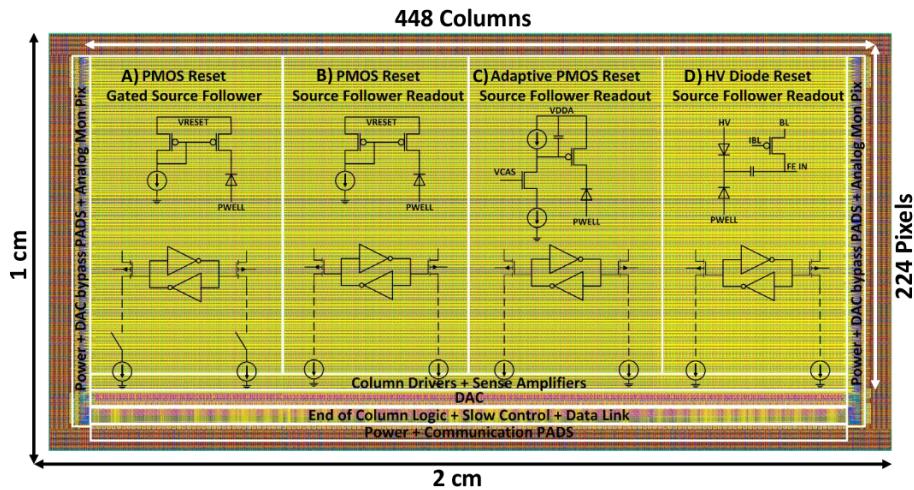


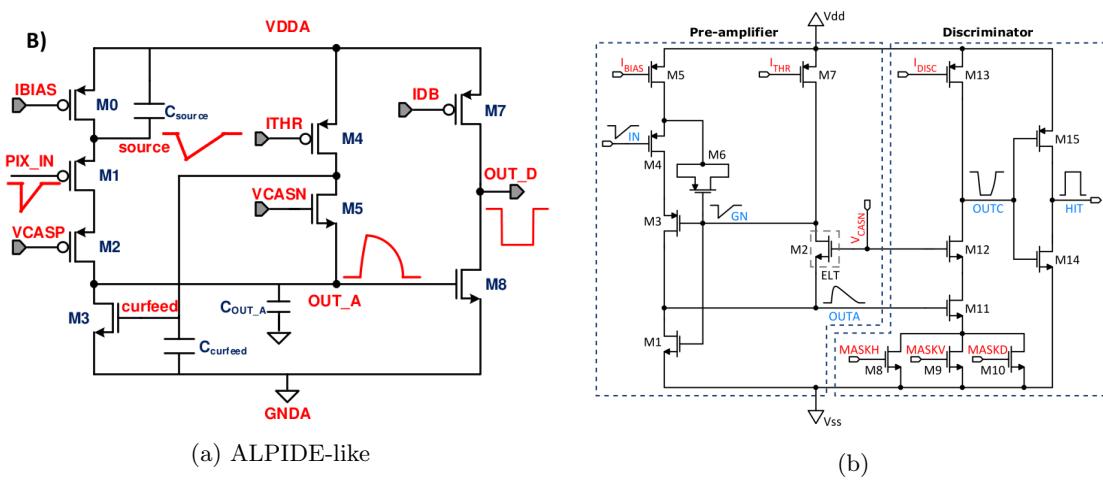
Figure 4.4

All the flavors implement a source-follower double-column bus readout: the standard variation is the flavor B, that features a PMOS input reset (referred as "PMOS reset"). Flavor A is identical to flavor B except for the realization of the source follower (it is a gated one) that aim to reduce the power consumption.**cosa significa?** C instead implements a novel leakage compensation circuit. Moreover the collection electrode in flavors A, B, C is DC-coupled to the front-end input, while in D is AC-coupled, providing to applu a high bias voltage; for this reason flavor D il called "HV flavor".

Principio generale: R resistenza di reset deve essere abbastanza grande in modo da far sì che il ritorno allo zero è abbastanza lento (non devi "interferire" con la tot slope e non deve essere più corto del tempo del preamplificatore, sennò hai perdita di segnale). Baseline reset: all'input solitamente hai un PMOSS o un diodo; R reset

4.2.1 ALPIDE-like

654 ALPIDE chips, developed by the ALICE collaboration, implemented a standard FE to the point
655 that many CMOS MAPS detectors used a similar FE and are called "ALIPDE-like". Considering
656 that both TJ-Monopix1 and ARCADIA-MD1 have an ALPIDE-like FE, I am going to explain the
broad principles of the early FE stage. The general idea is of the amplification to transfer the



Parameter	Meaning	
IBIAS	mainly controls the rise time	yes? check
IDB	sets the discriminator threshold	yes
ITHR	sets the velocity of the return to the baseline	yes
ICASN	sets the baseline of the signal	yes
VRESET	sets the gain of the preamplifier	yes
IRESET	sets the gain of the preamplifier	no

Table 4.3: FE parameters which must be setted through the DAQ. "Function" means that higher parameter implies higher value

658 charge from a bigger capacity[9], C_{source} , to a smaller one, C_{out} : the input transistor M1 with
 659 current source IBIAS acts as a source follower and this forces the source of M1 to be equal to the
 660 gate input $\Delta V_{PIX_IN} = Q_{IN}/C_{IN}$.

$$Q_{source} = C_{source} \Delta V_{PIX_IN} \quad (4.1)$$

661 The current in M2 and the charge accumulates on C_{out} is fixed by the one on C_{source} :

$$\Delta V_{OUT_A} = \frac{Q_{source}}{C_{OUT_A}} = \frac{C_{source} \Delta V_{PIX_IN}}{C_{OUT_A}} = \frac{C_{Source}}{C_{OUT_A}} \frac{Q_{IN}}{C_{IN}} \quad (4.2)$$

662 A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR
 663 set the baseline value of the signal on C_{OUT_A} and the velocity to goes down to the baseline.

IL RUOLO DI CURVFEED NON L'HO CAPITO.

664 Finally IDB defines the charge threshold with which the signal OUT_A must be compared: de-
 665 pending on if the signal is higher than the threshold or not, the OUT_D is high or low respectively.

666 The actual circuit implemented in TJ-Monopix1 is shown in figure 4.5b: the principal difference
 667 lays in the addition of disableing pixels' readout. This possibility is uttermost important in order to
 668 reduce the hit rate and to avoid saturating the bandwidth due to the noisy pixels, which typically
 669 are those with manufacturing defects. In the circuit transistors M8, M9 and M10 have the function
 670 of disabling registers with coordinates MASKH, MASKV and MASKD (respectively vertical, ori-
 671 ginal and diagonal) from readout: if all three transistors-signals are low, the pixel's discriminator
 672 is disabled. Compared with a configurable masking register which would allow disableing pixels
 673 individually, to use a triple redundancy reduces the sensistivity to SEU but also gives amount of
 674 intentionally masked ("ghost") pixels. This approach is suitable only for extremely small number
 675 N of pixel has to be masked: if two coordinate projection scheme had been implemented, the
 676 number of ghost pixels would have scale with N^2 , if instead three coordinates are used, the N's
 677 exponential is lower than 2 (fig. 4.6)

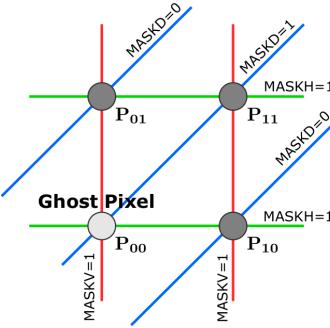


Figure 4.6

678

4.3 Readout logic

680 TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain
 681 architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit

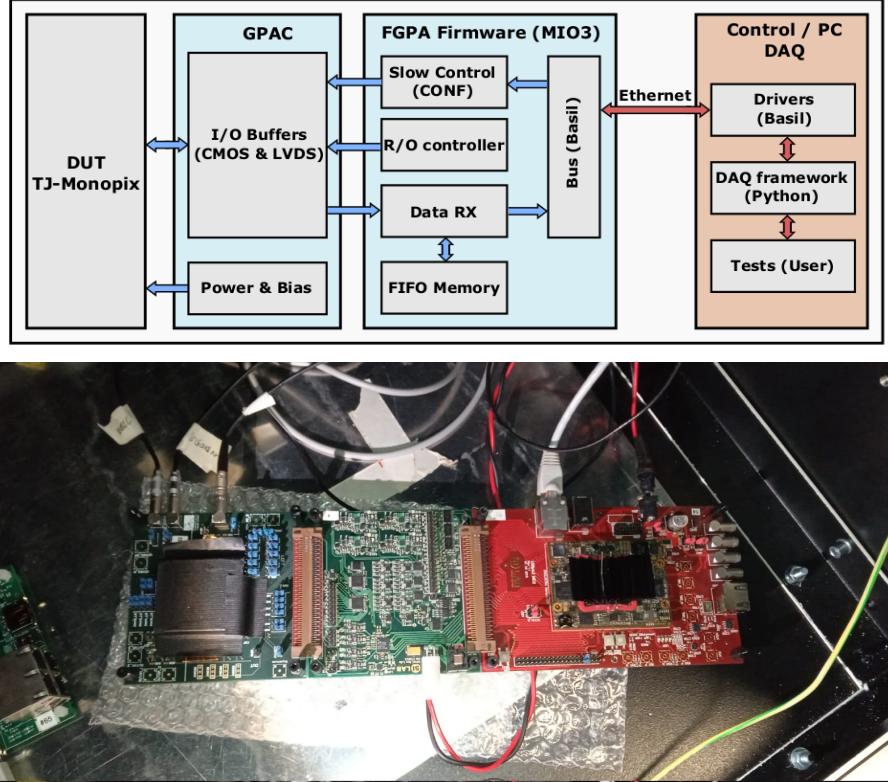
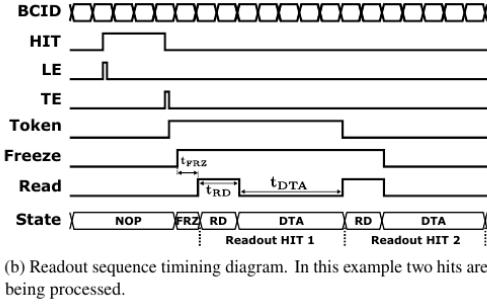


Figure 4.7: Main caption

682 LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address.
 683 Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is
 684 already storing a previous one, the new data get lost. After being read, the data packet is sent to
 685 the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (4.7). There
 686 a FIFO is used to temporarily stored the data, which is transmitted to a computer through an
 687 ethernet cable in a later time.

688 The access to the pixels' memory and the transmission of the data to the EoC, following
 689 a priority chain, is managed by control signals and is based on a Finite State Machine (FSM)
 690 composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and data transfer (DTA).
 691 The readout sequence (??) starts with the TE of a pulse: the pixel immediately tries to grab the
 692 column-bus turning up a hit flag signal called *token*. The token is used to control the priority chain
 693 and propagates across the column indicating what pixel that must be read. To start the readout
 694 and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal is activated, and
 695 then a *read* signal controls the readout and the access to memory. During the freeze, the state of
 696 the token for all pixels on the matrix remains settled: this does not forbid new hits on other pixels
 697 from being recorded, but forbids pixels hit from turning on the token until the freeze is ended. The
 698 freeze stays on until the token covers the whole priority chain and gets the EoC: during that time
 699 new token cannot be turned on, and all hits arrived during a freeze will turn on their token at the
 700 end of the previous freeze. Since the start of the token is used to assign a timestamp to the hit,
 701 the token time has a direct impact on the time resolution measurement; this could be a problem
 702 coping with high hits rate.

703 The analog FE circuit and the pixel control logic are connected by an edge detector which is
 704 used to determine the LE and the TE of the hit pulse(fig. 4.9): when the TE is stored in the first
 705 latch the edge detector is disabled and, if the **FREEZE** signal is not set yet, the readout starts. At
 706 this point the HIT flag is set in a second latch and a token signal is produced and depending on
 707 the value of **Token in** the pixel can be read or must wait until the **Token in** is off. In figure an OR
 708 is used to manage the token propagation, but since a native OR logic port cannot be implemented
 709 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly
 710 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token



(b) Readout sequence timing diagram. In this example two hits are being processed.

Figure 4.8: Readout timing diagram: in this example two hits are being processed

711 and to speed up the circuit optimized solution are often implemented. When the pixel become the
 712 next to be read in the queue, and at the rising edge of the **READ** signal, the state of the pixel is
 713 stored in a D-latch and the pixel is allowed to use the data bus; the TE and the HIT flag latches
 714 are reset and a **READINT** signal that enable access of the RAM and ROM cells is produced.

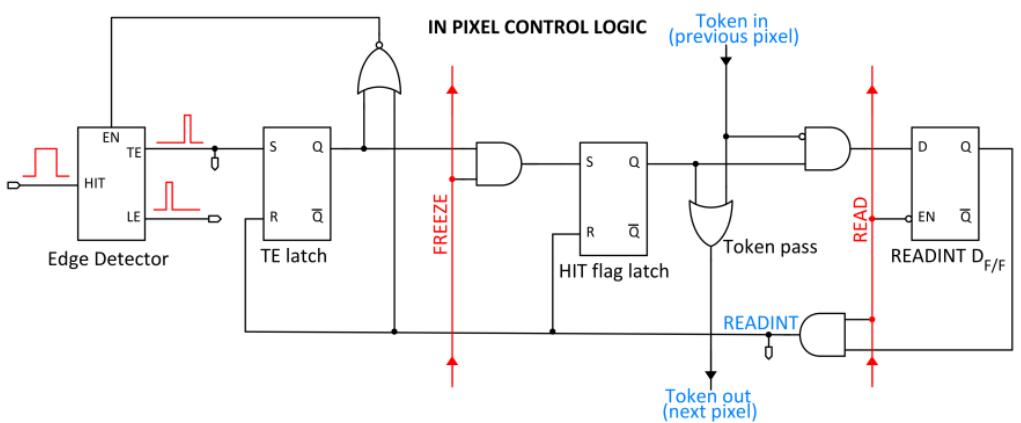


Figure 4.9

715
 716 The final data must provide all the hits' information: the pixel address, the ToT and the
 717 timestamp. All those parts are assigned and appended at different time during the R/O chain:

- 718 • **Pixel address:** while the double column address (6-bit) is appended by the EoC circuit,
 719 the row address (8-bits for each flavor) and the physical column in the doublet (1-bit) are
 720 assigned by the in-pixel logic
- 721 • **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge
 722 detector in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is
 723 range 0-64 clock cycle which corresponds to 0-1.6 μ s
- 724 • **Timestamp:** The timestamp of the hit correspond to the time when the pixel set up the
 725 token; it is assigned by the FPGA, that uses the LE, TE and a 640 MHz clock to derive
 726 it. For all those hits which arrived while the matrix is frozen, the timestamp is no more
 727 correlated with the time of arrival of the particle

728 When the bits are joined up together the complete hit data packet is 27-bit.

729 4.3.1 Dead time measurements

730 The hit loss is due to analog and digital pile up: the first one occurs when a new hit arrives during
 731 the pre-amplifier response, the second instead, which is the more relevant contribution with high
 732 rate, while the information of the previous hit has not yet been transferred to the periphery. As
 733 only one hit at a time can be stored on the pixel's RAM, until the data have completed the path
 734 to get out, the pixel is paralyzed and the dead time τ almost corresponds with the time needed

Parameter	Value [DAC]	Value [μs]
START_FREEZE	64	1.6
STOP_FREEZE	100	2.5
START_READ	66	1.65
STOP_READ	68	1.7

Table 4.4: Default configuration of the R/O parameters

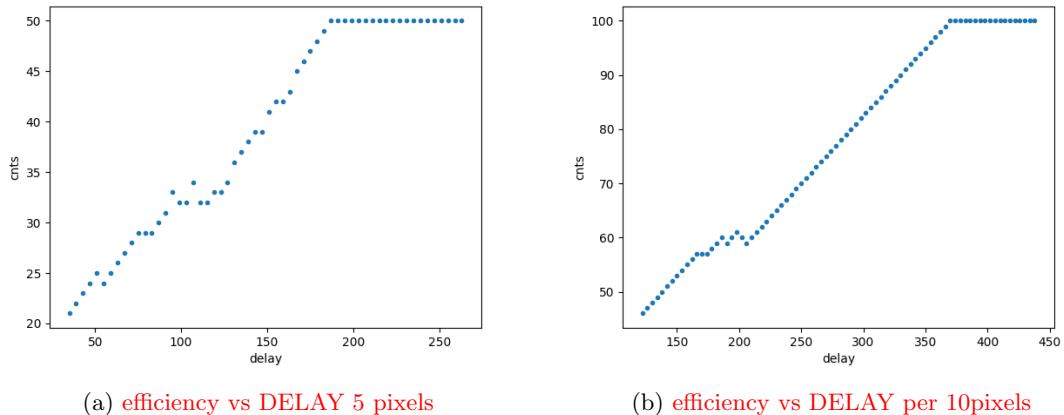
735 to trasmit the data-packets off-chip. Since the exportation of data from pixel to the EoC occurs
 736 via a 21-bits data bus, only one clock cycle is need to transfer the data to the end of column and
 737 the dead time bottleneck is given by the bandwidth of the serializer at the EoC. In our setup the
 738 serializer operates at 40 MHz, thus to transmit a data packet (27-bit considering the addition at
 739 the EoC) at least 675 ns are needed. For what we have said so far, the R/O is completely sequential
 740 and therefore is expected a linear dependence of the reading time on the number of pixels to read:

$$\tau = 25 \text{ ns} \times (\alpha N + \beta) \quad (4.3)$$

741 where α and β are parameters dependent on the readout chain setting.

742 To measure and test the linearity of the reading time with the number of pixels firing, I have
 743 used the injection mode available on the chip. Indeed, the injection mode allows fixing not only
 744 the amplitude of the pulse, which corresponds to the charge in DAC units, but also the period and
 745 the width. I have injected a fix number of pulses (100) and looked for the rate when the efficiency
 746 decreases. Moreover to test that there is no dependece of the digital readout time from the charge
 747 of the pulse, I have try to change the amplitude of the pulse injected, but the parameters found
 748 were consistent with the default configuration ones.

749 Al posto degli esempi con 5 e 10 pixels metterei un esempio dell'efficienza vs il periodo quando
 750 leggo un singolo pixel. Una cosa che volevo fare era anche provare a fissare la slope con cui
 l'efficienza scende: se la slope è uguale per tutti il readout diventa completamente predittivo.



(a) efficiency vs DELAY 5 pixels

(b) efficiency vs DELAY per 10pixels

751 While the single pixel reading time and the dead time do not depend on the position on the
 752 pixel matrix and are equal to 106 (46+60) clock counts within 1 clock count, on the other hand the
 753 τ depends on the pixel position on the matrix when more than one pixel are firing. In particular
 754 the priority chain goes from row 224 to row 0, and from col 0 to 112, that means the last pixels to
 755 be read is the one on the bottom right corner of the matrix.

756 In figure 4.12 is reported the reading time versus the number of pixels injected; the R/O
 757 parameters that control the reading time and their default values are reported on table ??.

758 The factor α , referring to eq. 4.3 is proportional to the difference (STOP_FREEZE - START_READ),
 759 while the offset β lies between 5 and 15 clock counts. Since through the injection a random hit rate
 760 on the matrix can't be simulated, as the coordinates of the pixels to inject must be specified, for
 761 convenience I used the pixels on the same column/row. No difference in the α and β coefficients
 762 has been observed between the two case.

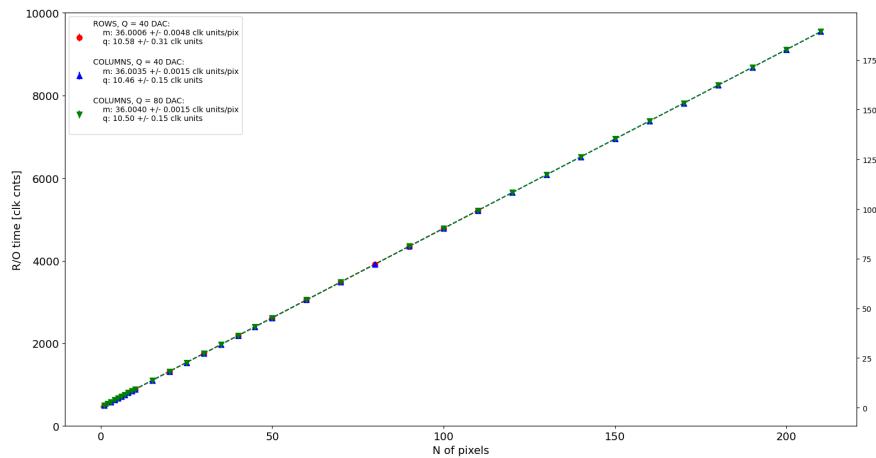


Figure 4.11

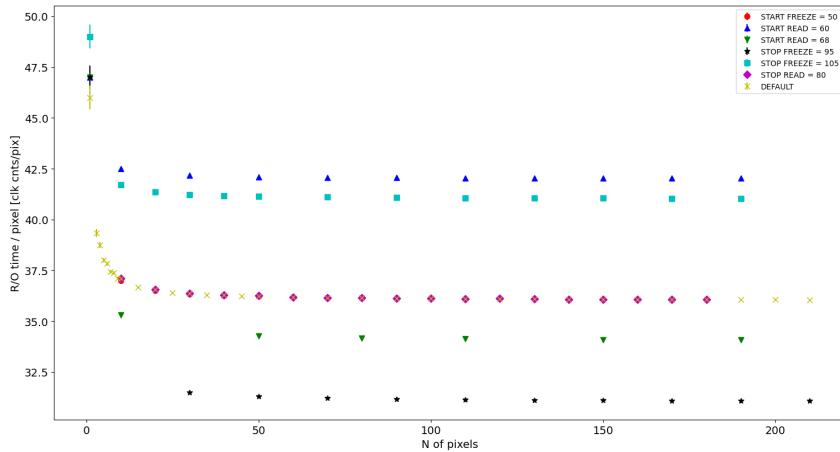


Figure 4.12

764 Ci sarebbe da spiegare perchè i parametri che usiamo noi come default non sono quelli che
 765 minimizzano il tempo di lettura. La spiegazione è che "Abbiamo copiato i valori dal repository
 766 di quelli di Bonn". Un'altra domanda potrebbe essere: come mai non ho esplorato una zona più
 767 vasta per i parametri del R/O. Cambiando molto i parametri del R/O la lettura non funziona
 768 per niente: ad esempio CONF_STOP_FREEZE non può essere impostato né sopra 105 né sotto 95

769 4.4 Measurements with radioactive sources

770 CI metterei i plot con ferro, stronzio e cosmici Istogrammi, cluster distribution e definizione di
 771 cluster, coincidenze casuali con rumore.

772 4.5 Calibration of the ToT signal

773 calibrazione con il ferro Ci metterei un'istogramma del

774 Chapter 5

775 Arcadia-MD1

776 [10] [11]

777 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED
778 Matisse a Md1 e Md2

779 5.1 The sensor

780 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node
781 with six metal layer ???. The standard p-type substrate was replaced with an n-type floating zone
782 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).

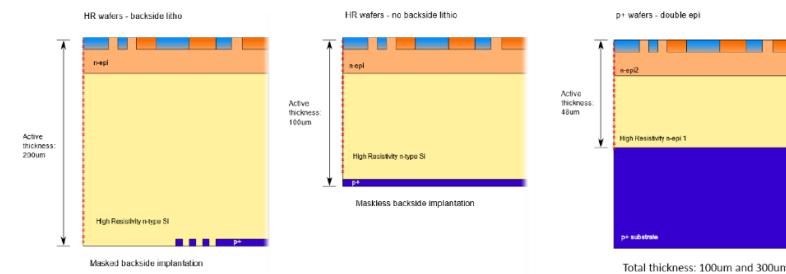


Figure 5.1

783
784 Wafer thinning and backside litography were necessary to introduce a junction at the bottom
785 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.
786 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthought
787 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

788 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,
789 COME VENGONO FATTI I MAPS COME FAI LE GIUNZIONI

790 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.
791 It is operated in full depletion with fast charge collection by drift.

792 Prima SEED si occupa di studiare le prestazioni: oncept study with small-scale test struc-
793 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo
794 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il
795 pwell e quanto al diodo. ..

796 5.2 Readout logic and data structure

797 5.2.1 Matrix division and data-packets

798 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided
799 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in

800 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei serializzatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

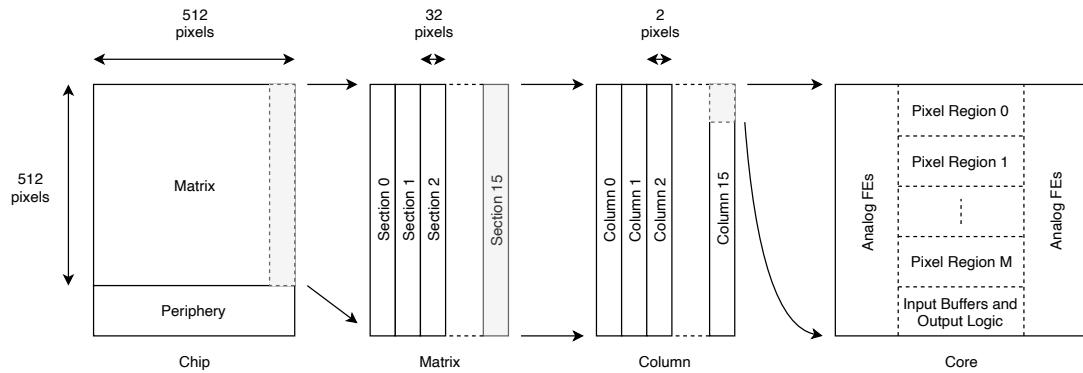


Figure 5.2

801

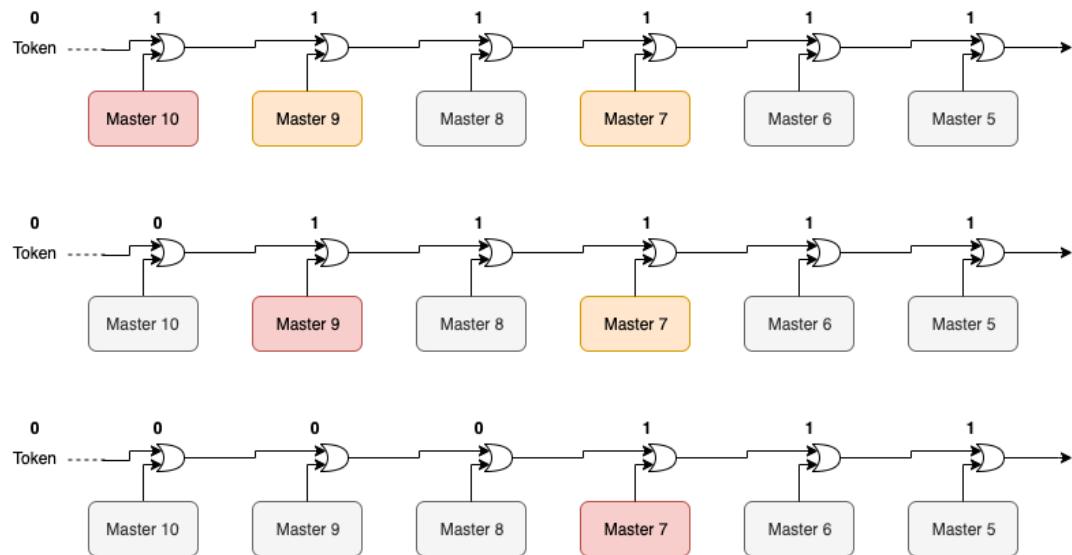


Figure 5.3

802 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le
803 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,
804 e devi accennare al timestamp

805 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively
806 large core allows one to take full advantage of digital synthesis tools to implement complex func-
807 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della
808 review.

809

810 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column
811 (512x2) Core (32x2) Region (4x2)

812 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

813 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for
814 example 8b10b encoding n =5"

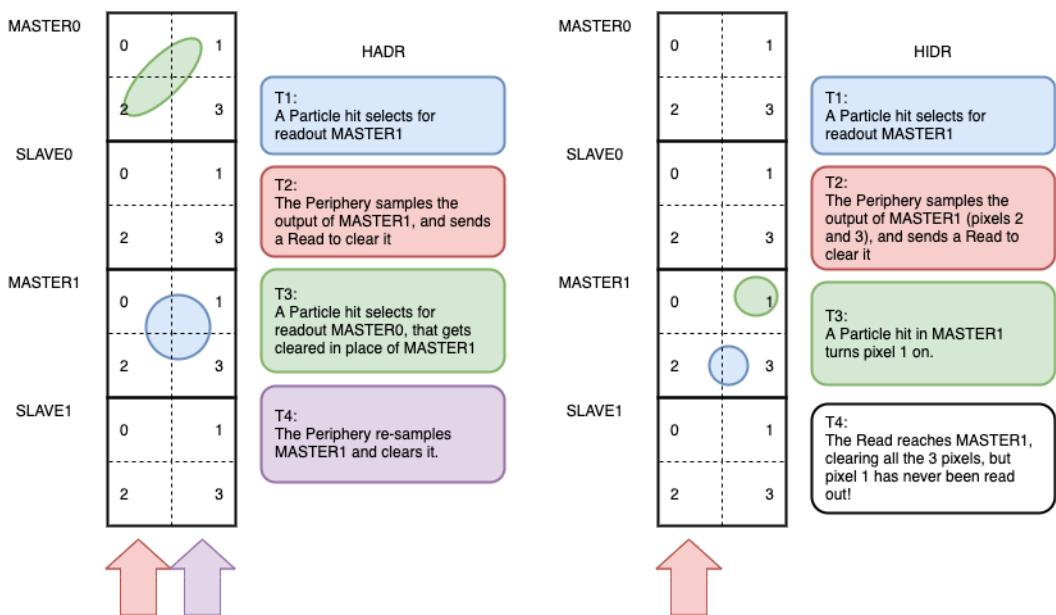


Figure 5.4

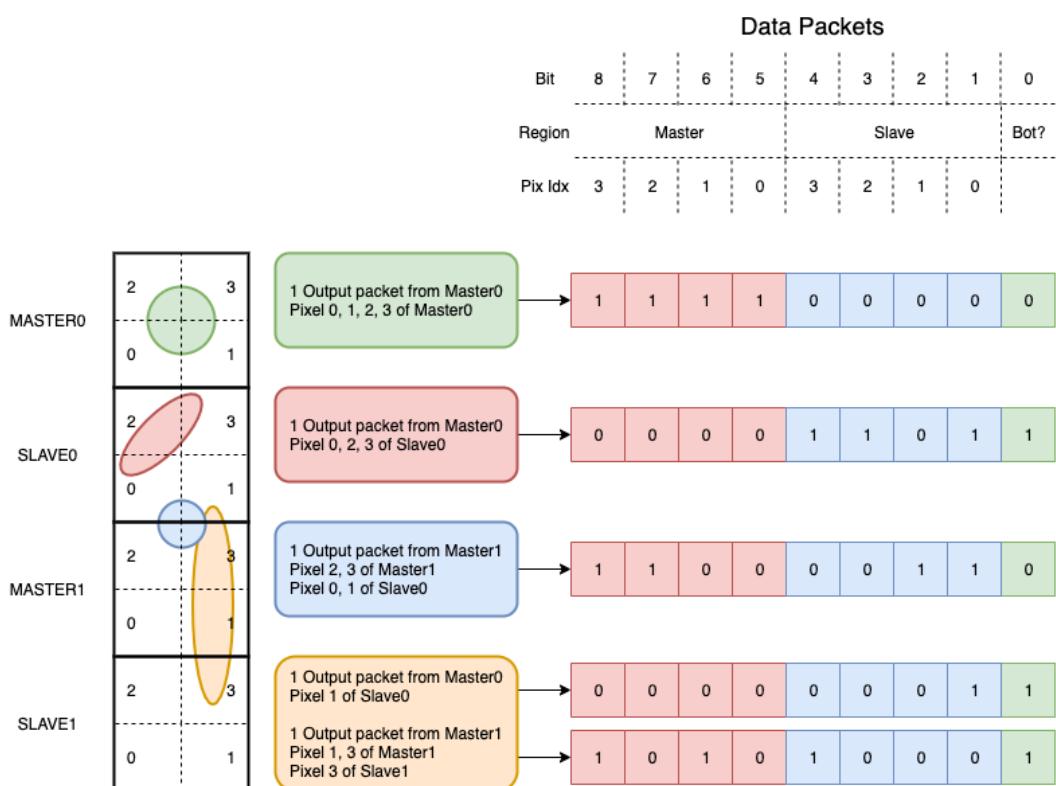


Figure 5.5

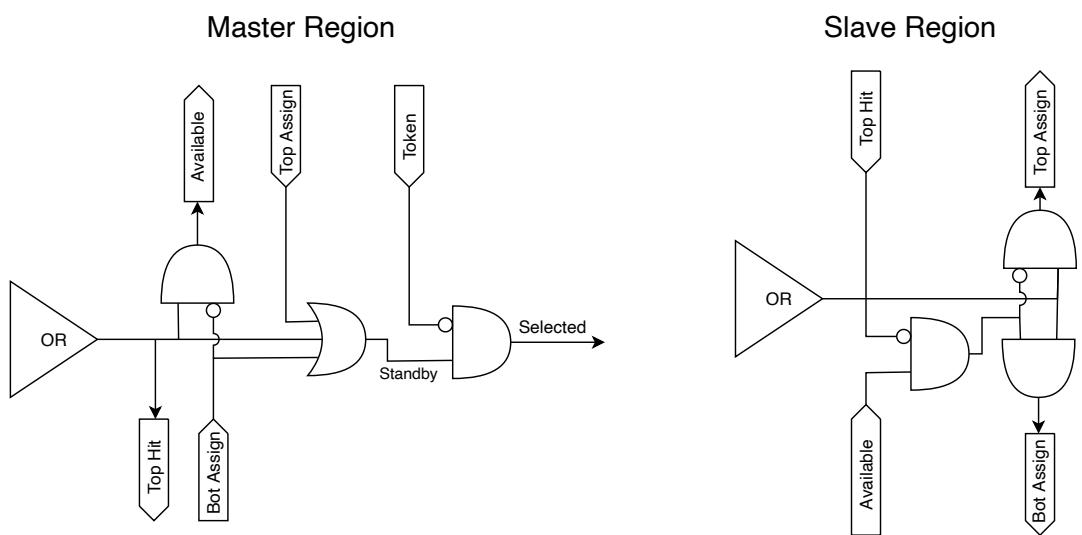


Figure 5.6

815 **Chapter 6**

816 **Threshold and noise
817 characterization**

818 **6.1 Threshold and noise: figure of merit for pixel detectors**

819 IN QUESTO CAPITOLO HO MESSO SOLO APPUNTI SPARSI DA RIORGANIZZARE, E
820 DEVO AGGIUNGERE POI I PLOT DI MONOPIX1

821 The signal to threshold ratio is the figure of merit for pixel detectors.

822 la soglia deve essere abb alta da tagliare il rumore ma abb bassa da non perdere efficienza.
823 Invece di prendere il rapporto segnale rumore prendi il rapporto segnale soglia. Perchè? la soglia
824 è collegato al rumore, nel senso che: supponiamo di volere un occupancy di 10-4 allora sceglierò la
825 soglia in base a questo. (plot su quaderno) Da questo conto trovo la minima soglia mettibile
826 In realtà quello che faccio è mettere una soglia un po' più grande perchè il rate di rumore dipende
827 da molti fattori quali la temperatura, l annealing ecc, e non voglio che cambiando leggermente uno
828 di questi parametri vedo alzarsi molto il rate di rumore. In realtà non è solo il rumore sensibile a
829 diversi fattori, ma anche la soglia: ad esempio la cosa classica è la variabilità della soglia da pixel
830 a pixel.

831 In questo modo rumore e soglia diventano parenti.

832 Review pag 26.

833 Questo implica tra le altre cose che voglio poter assegnare delle soglie diverse a diversi pixel:

834 Drawback è dare spazio per registri e quantaltro.

835 Questo lascia però ancora aperto il problema temporale delle variazioni del rumore: problema per
836 cui diventano necessarie le misure dei sensori dopo l'irraggiamento.

837 Non fare trimming sulla soglia è uno dei problemi che si sono sempre incontrati: a casusa dei
838 mismatch dei transistor le soglie efficaci pixel per pixel cambiano tanto. La larghezza della s curve
839 è il noise se assumi che il noise è gaussiano

840 Il trimming della soglia avviene con dei DAC: la dispersione della soglia dopo al tuning e dovuta
841 al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.1)$$

842 dove il numero di bit cambia varia tra 3-7 tipicamente. Monopix è 7 Arcadia 6

843 Each ROIC is different in this respect, but in general the minimum stable threshold was around
844 2500 electrons (e) in 1st generation ROICs, whereas it will be around 500 e for the 3rd generation.
845 This reduction has been deliberate: required by decreasing input signal values. Large pixels (2 104
846 um²), thick sensors (maggiore di 200 um), and moderate sensor radiation damage for 1st generation
847 detectors translated into expected signals of order 10 ke, while small pixels (0.25 104 um²), thinner
848 sensors (100 um), and heavier sensor radiation damage will lead to signals as low as 2 ke at the
849 HL-LHC

850 The ENC can be directly calculated by the Cumulative Distribution Function (CDF) (scurve)
851 obtained from the discriminator "hit" pulse response to multiple charge injections

855 **6.2 TJ-Monopix1 characterization**

856 **6.2.1 Threshold and noise dispersion**

857 Un plot con s curve e residui (perchè dovrebbe essere migliore il modello con doppia retta? sul
858 RD53 c'era scritto, trovalo e leggilo) Istogrammi e colormap

859

860 **6.2.2 Absolute calibration of ToT**

861 Misure con il ferro. Metti un plot di singolo pixel dello spettro del ferro fittato con CB. Perchè
862 CB? rimuovere i cluster comunque lasciava una coda abbastanza grande a sx e fittare con una
863 gaussiana comunque non dava risultati migliori.

864 **6.3 ARCADIA-MD1 characterization**

865 **Chapter 7**

866 **Test beam measurements**

867 **7.1 Testbeam motivation**

868 Possibilità di integrare carica sul pixel: due elettroni consecutivi su un pixel ogni quanto arrivano?

869 Vogliamo sfruttare l'analog pile up, per fare questo dobbiamo fare attenzione a non finire nel
870 digital pile up Devi avere che il tot dell'elettrone (cioè MIP) è maggiore del deltat medio; in questo
871 caso potresti riuscire ad integrare carica.

872 **7.2 Apparatus description**

873 L'acceleratore utilizzato è un acceleratore per ricerca sulla flash di fisica medica. È l'unico al mondo
874 che permette di raggiungere alti dosaggi mantenendo l'indipendenza dei parametri del fascio. La
875 struttura del fascio e le varie quantità che si usano per descriverlo sono riportate in figure 7.1.

876 The medium is ordinarily water, since dosimetric protocols are based on measurements in
877 water as reference

$$R[Hz/cm^2] = \frac{DPP[Gy]}{1.6 \cdot 10^{10} S[g/cm^2]} \quad (7.1)$$

878 where S is the stopping power in water, 2.17 g/cm^2

Table 1. Terminology used throughout the text.

Term	Symbol	Description
intra-pulse dose-rate	—	The duration of a single pulse. ^a
	\bar{D}	Mean dose-rate for a multi-pulse delivery.
pulse repetition frequency	\dot{D}_p	Dose-rate in a single pulse. ^a
	DPP	Dose in a single pulse. ^a
	PRF	Number of pulses delivered per unit time. ^a
	t_i	Total irradiation time from the beginning of the first delivered pulse to the end of the last delivered pulse.
ultrahigh dose-rate	—	Radiation delivered with mean dose-rate of $> \sim 40 \text{ Gy s}^{-1}$.
	—	Ultrahigh dose-rate RT that presents decreased damage to normal tissues compared to RT delivered with conventional dose-rate of $\sim 0.04 \text{ Gy s}^{-1}$.

^aPulses are considered to be macro-pulses unless otherwise stated (see also figure 1).

^bIn literature sometimes referred to as the instantaneous dose-rate.

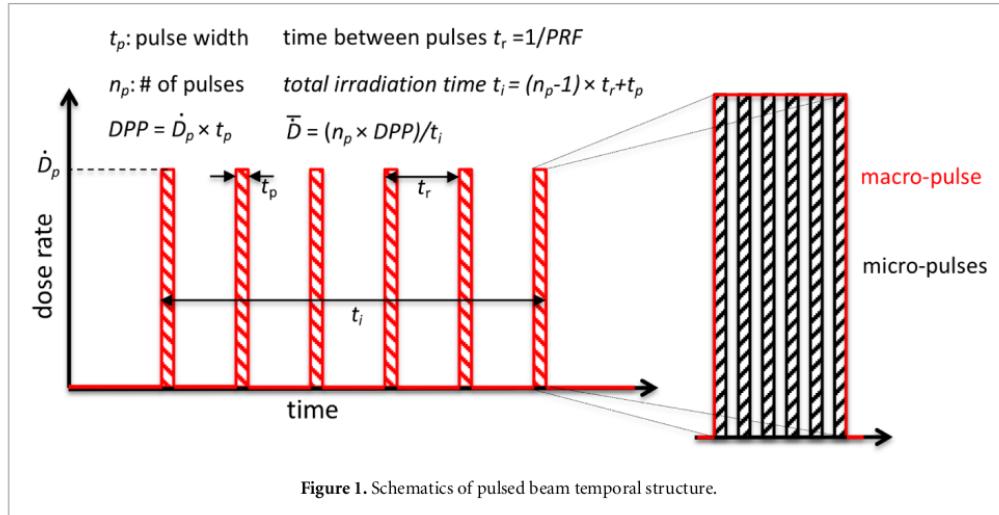


Figure 7.1

879 Appendix A

880 Pixels detector: a brief overview

881 A.1 Radiation damages

882 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they
 883 are almost always installed near the interaction point where there is a high energy level of radiation.
 884 At LHC the ϕ_{eq} per year in the innermost pixel detector is $10^{14} n_{eq}/cm^2$; this number reduces by
 885 an order passing to the outer tracker layer [2] pag 341 Wermes. Here the high fluence of particles
 886 can cause a damage both in the substrate of the detector and in the superficial electronics.

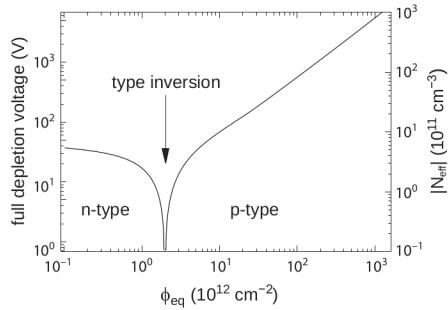
887 The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but
 888 it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the
 889 NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV
 890 neutrons. Differently, surface damages are principally due to ionizing energy loss.

891 **DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide (S_iO_2) can
 892 cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages
 893 are mostly less relevant than the previous one, since with the development of microelectronics and
 894 with the miniaturization of components (in electronic industry 6-7 nm transistors are already used,
 895 while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit
 896 is reduced.

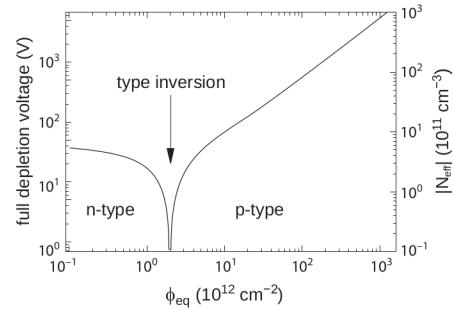
897 Let's spend instead two more other words on the more-relevant substrate damages: the general
 898 result of high radiation level is the creation of new energy levels within the silicon band gap and
 899 depending on their energy-location their effect can be different, as described in the Shockely-Read-
 900 Hall (SRH) statistical model. The three main consequence of radiation damages are the changing
 901 of the effect doping concentration, the leakage current and the increasing of trapping probability.

902 **Changing of the effective doping concentration:** is associated with the creation/removal
 903 of donors and acceptors center which trap respectively electrons/holes from the conduction band
 904 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type¹)
 905 can happen: indeed it is quite common at not too high fluences ($\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$). A changing
 906 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime
 907 (eq.2.1) and sometimes can be difficult keeping to fully deplete the bulk.

¹L'INVERSIONE OPPOSTA NON CE L'HA PERCHÈ?



(a) 1a



(b) 1b

908 **Leakage current:** is associated with the generation-recombination centers. It has a strong
909 dependence with the temperature ($I_{leak} \propto T^2$), whose solution is therefore to operate at lower
910 temperature.

911 **Increase of trapping probability:** since the trapping probability is constant in the depleted
912 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,
913 that is the mean trapping path, decreases after irradiation and typical values are 125-250 μm and
914 must be compared with the thickness of the depleted region which () corresponds to the mean drift
915 path.

916 Different choices for substrate resistivity, for junctions type and for detector design are typically
917 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced
918 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))
919 for example, show a compensation effect for radiation damage; another example is the usage of
920 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage
921 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p
922 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be
923 placed near the diode.

924 Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché
925 una particella deposita carica nell'elettronica che fa da memoria registro/RAM/.... Questo tipo
926 di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti
927 tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip
928 in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più
929 carica di quanto farebbe una MIP. Questo metodo pur essendo più comodo richiede less amount of
930 area ha però come drawback che il registro può essere soggetto a SEU problema non trascurabile
931 in acceleratori come HL-LHC adronici

932 Bibliography

- 933 [1] W. Snoeys et al. “A process modification for CMOS monolithic active pixel sensors for
934 enhanced depletion, timing performance and radiation tolerance”. In: (2017). DOI: <https://doi.org/10.1016/j.nima.2017.07.046>.
- 935 [2] H. Kolanoski and N. Wermes. *Particle Detectors: Fundamentals and Applications*. OXFORD
936 University Press, 2020. ISBN: 9780198520115.
- 937 [3] E. Mandelli. “Digital Column Readout Architecture for the ATLAS Pixel 0.25 um Front End
938 IC”. In: (2002).
- 939 [4] M. Garcia-Sciveres and N. Wermes. “A review of advances in pixel detectors for experiments
940 with high rate and radiation”. In: (2018). DOI: <https://doi.org/10.1088/1361-6633/aab064>.
- 941 [5] M. Dyndal et al. “Mini-MALTA: Radiation hard pixel designs for small-electrode monolithic
942 CMOS sensors for the High Luminosity LHC”. In: (2019). DOI: <https://doi.org/10.1088/1748-0221/15/02/p02005>.
- 943 [6] M. Barbero. “Radiation hard DMAPS pixel sensors in 150 nm CMOS technology for opera-
944 tion at LHC”. In: (2020). DOI: <https://doi.org/10.1088/1748-0221/15/05/p05013>.
- 945 [7] K. Moustakas et al. “CMOS Monolithic Pixel Sensors based on the Column-Drain Architec-
946 ture for the HL-LHC Upgrade”. In: (2018). DOI: <https://doi.org/10.1016/j.nima.2018.09.100>.
- 947 [8] I. Caicedo et al. “The Monopix chips: depleted monolithic active pixel sensors with a column-
948 drain read-out architecture for the ATLAS Inner Tracker upgrade”. In: (2019). DOI: <https://doi.org/10.1088/1748-0221/14/06/C06006>.
- 949 [9] D. Kim et al. “Front end optimization for the monolithic active pixel sensor of the ALICE
950 Inner Tracking System upgrade”. In: *JINST* (2016). DOI: doi:10.1088/1748-0221/11/02/
951 C02042.
- 952 [10] L. Pancheri et al. “A 110 nm CMOS process for fully-depleted pixel sensors”. In: (2019). DOI:
953 <https://doi.org/10.1088/1748-0221/14/06/c06016>.
- 954 [11] L. Pancheri et al. “Fully Depleted MAPS in 110-nm CMOS Process With 100–300-um Active
955 Substrate”. In: (2020). DOI: 10.1109/TED.2020.2985639.
- 956