

Summary

2	1	Introduction	2
3	2	Pixel detectors	3
4	2.1	Signal formation	3
5	2.2	Hybrid pixels	4
6	2.3	CMOS MAPS and DMPAS	5
7	2.3.1	DMAPS: large and small fill factor	5
8	2.3.2	A modified sensor	6
9	2.4	Analog front end	7
10	2.4.1	Preamplifier	8
11	2.5	Readout logic	8
12	3	Use of pixels detector	11
13	3.1	Tracking in HEP	11
14	3.1.1	Hybrid pixels: ATLAS, CMS and LHC-b	11
15	3.1.2	CMOS MAPS: ALICE and STAR	11
16	3.2	Application in medical imaging	11
17	3.2.1	Medipix and Timepix	11
18	3.2.2	Applicability to FLASH radiotherapy	11
19	4	TJ-Monopix1	12
20	4.1	The sensor	13
21	4.2	Front end	14
22	4.2.1	Four flavors	14
23	4.2.2	ALPIDE-like front end	15
24	4.2.3	Front end parameters	16
25	4.3	Readout logic	16
26	4.3.1	Dead time measurement	18
27	5	Arcadia-MD1	20
28	5.1	The sensor	20
29	5.2	Readout logic and data structure	20
30	5.2.1	Matrix division and data-packets	20
31	6	Threshold and noise characterization	24
32	6.1	Threshold and noise: figure of merit for pixel detectors	24
33	6.2	TJ-Monopix1 characterization	25
34	6.3	ARCADIA-MD1 characterization	25
35	A	Pixels detector: a brief overview	26
36	A.1	Radiation damages	26
37	B	FLASH radiotherapy	28
38	B.1	Cell survival curves	28
39	B.2	FLASH effect	29

⁴⁰	Bibliography	30
⁴¹	Characterization of monolithic CMOS pixel sensors for charged particle detectors and for high	
⁴²	intensity dosimetry	

⁴³ **Chapter 1**

⁴⁴ **Introduction**

⁴⁵ Pixel detectors, members of the semiconductor detector family, have significantly been used since
⁴⁶ () at the first accelerator experiments for energy and position measurement. Because of their
⁴⁷ dimension (today $\sim 30 \mu m$ or even better) and their spatial resolution ($\sim 5\text{-}10 \mu m$), with the
⁴⁸ availability of technology in 1980s they proved to be perfectly suitable for vertex detector in the
⁴⁹ inner layer of the detector.

⁵⁰ Technological development has been costant from then on and today almost every high energy
⁵¹ physics (HEP) experiment employs a pixels detector; hybrid pixel currently constitute the state-
⁵² of-art for large scale pixel detector but experiments began to look at the more innovative monolithic
⁵³ active pixels (MAPS) as perspective for their future upgrades, as BelleII, or they already have
⁵⁴ installed them, as ALICE.

⁵⁵ Requirement imposed by accelerator are stringent and they will be even more with the increase
⁵⁶ of luminosity/intensity, in terms of radiation hardness, efficiency and occupancy, time resolution,
⁵⁷ material budget and power consumption.

⁵⁸ Qual è invece la richiesta per la dosimetria?

⁵⁹

⁶⁰ **Chapter 2**

⁶¹ **Pixel detectors**

⁶² **2.1 Signal formation**

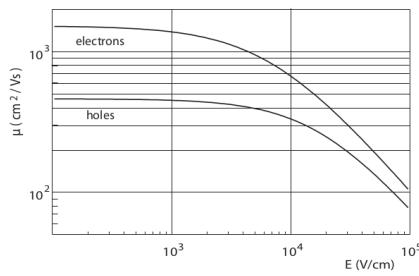
⁶³ When a charge particle passes through a pixel and loses energy by ionization a part of that
⁶⁴ energy is used to generate electron-hole pairs (another part is used for other processes, as the
⁶⁵ lattice excitation) which are then separated by the electric field and collected at their respectively
⁶⁶ electrodes (p for holes and n for electrons)¹; by the drift of these charges, a signal i_e is generated
⁶⁷ on the electrode e as stated by the Shockley–Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (2.1)$$

⁶⁸ where $v(t)$ is the instantaneous velocity of the charge q and E_{WF} is the weighting field, that is the
⁶⁹ field obtained biasing the electrode e with 1V and all the others with 0V. The drift velocity of the
⁷⁰ charge depends on the electric field and on the mobility of the particle:

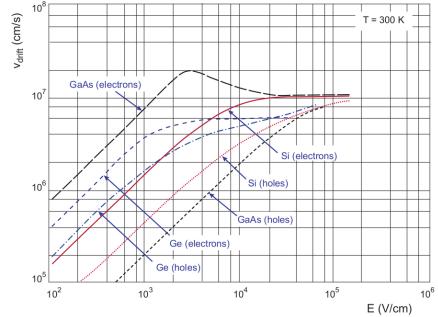
$$v = \mu(E) E \quad (2.2)$$

⁷¹ where $\mu(E)$ is a function of the electric field and is linear with E only for small E : at higher values
⁷² the probability of interactions with optical phonons increases and the mobility drops and this leads
⁷³ to an independence of the velocity from the electric field (fig. 2.1b).



(a) Typical values for electrons and holes mobility in

silicon at room temperature are $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$, $\mu_h = 500$



(b) Drift velocity at room temperature in different semiconductors

⁷⁴ The average energy needed to create a pair at 300 K in silicon is $w_i = 3.65 \text{ eV}$, that is more
⁷⁵ than the mean ionization energy because of the interactions with phonon, since for a minimum
⁷⁶ ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is
⁷⁷ 0.28 keV/ μ , hence the number of e/h pairs is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (2.3)$$

¹Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout

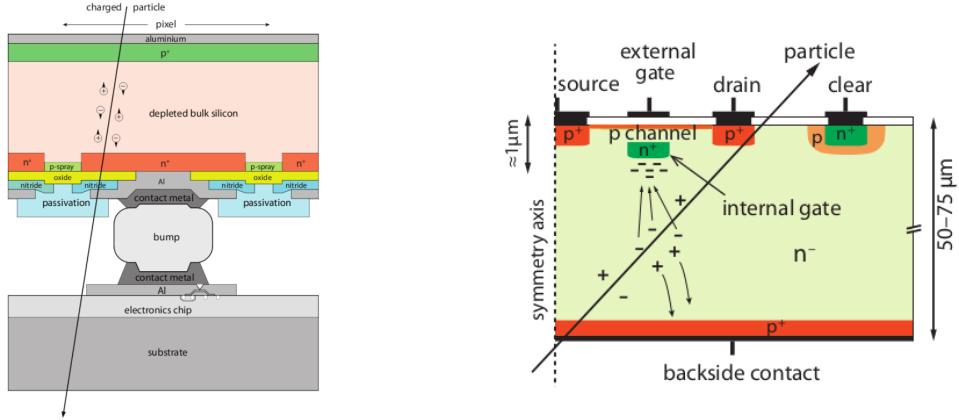


Figure 2.2: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

78 CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALEMTE SI AGGIUNGE IL
 79 FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. IL FATTORE DI FANO È
 80 0.115 NELL SILICIO. ecc It is fundamental that pairs e/h are produced in the depleted region
 81 of the semiconductor where the probability of recombination with charge carriers is low to avoid
 82 loss of signals. Pixel detectors are then commonly reverse biased: a positive bias is given to the
 83 n electrode and a negative to the p to grow the depletion zone in the epitaxial layer below the
 84 electrode. The width of the depletion region is related with the external bias V_{ext} , the resistivity
 85 ρ and also with the dopant:

$$d_n \sim 0.55 \sqrt{\frac{\rho}{\Omega cm} \frac{V_{ext}}{V}} \mu m \quad (2.4) \quad d_p \sim 0.32 \sqrt{\frac{\rho}{\Omega cm} \frac{V_{ext}}{V}} \mu m \quad (2.5)$$

86

87

88

89 For that reason high resistivity wafers ($100 \Omega cm - k\Omega cm$) are typically preferred because they
 90 allow bigger depletion zone with smaller voltage bias.

91 2.2 Hybrid pixels

92 Hybrid pixels are made of two parts (fig. 2.2a), the sensor and the electronics: for each pixel these
 93 two parts are welded together through microconnection (bump bond).

94 They provide a practical system where readout and sensor can be optimized separately, although
 95 the testing is less easy-to-do since the sensor and the R/O must be connected together before.

96 In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-
 97 cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high
 98 levels of radiation, and also expensive.

99 A critical parameter for accelerator experiments is the material budget, which represents the main
 100 limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are
 101 thicker (\sim hundreds of μm) than monolithic ones (even less than $100 \mu m$), using the latter the
 102 material budget can be down by a third: typical value for hybrid pixels is 1.5 % X_0 per layer,
 103 while for monolithic 0.5 % X_0 .

104 Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,
 105 by the way, a bigger cooling system leading in turn to an increase in material too.

106

107 DEPFET are the first attempt towards the integration of the front end (FE) on the sensor bulk:
 108 they are typically mounted on a hybrid structure but they also integrate the first amplification
 109 stage.

110 Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor
 111 (a p-channel in fig. 2.2b): an hole current flows from source to drain which is controlled by the
 112 external gate and the internal gate together. The internal gate is made by a deep n+ implant
 113 towards which electrons drift after being created in the depletion region (to know how the signal

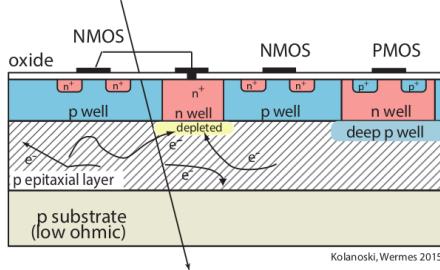


Figure 2.3: Concept cross-section of CMOS MPAS pixel

is created in a pixel detector look at appendix A); the accumulation of electrons in the region underneath the n implant changes the gate potential and controls the transistor current.
DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and the large depletion region. But, since they need to be connected with ASIC the limiting factor still is the material budget.

2.3 CMOS MAPS and DMPAS

Monolithic active pixels accommodate on the same wafer both the sensor and the front end electronics, with the second one implanted on top.

MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the development of the electronic sector which guarantees the decrease in CMOS transistors dimension at least every two years, as stated by the Moore's law².

As a matter of fact the dimension of components, their organization on the pixel area and logic density are important issues for the design and for the layout; typically different decisions are taken for different purposes.

Monolithic active pixel can be distinguished between two main categories: MAPS and depleted MAPS (DMPAS).

MAPS (figure a 2.3) have typically an epitaxial layer in range 1-20 μm and because they are not depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the collection could be partial especially after the irradiation of the detector (look at A for radiation damages), when the trapping probability become higher.

In figure 2.3 is shown as example of CMOS MAPS: the sensor in the scheme implements an n well as collection diode; to avoid the others n wells (which contain PMOS transistor) of the electronic circuit would compete in charge collection and to shield the CMOS circuit from the substrate, additionally underlying deep p well are needed. DMPAS are instead MAPS depleted with d typically in $\sim 25\text{-}150 \mu\text{m}$ (eq. 2.1) which extends from the diode to the deep p-well, and sometimes also to the backside (in this case if one wants to collect the signal also on this electrode, additional process must be done).

2.3.1 DMAPS: large and small fill factor

There are two different sensor-design approaches (figure 2.4) to DMAPS:

- large fill factor: a large collection electrode that is a large deep n-well and that host the embedded electronics
- small fill factor: a small n-well is used as charge collection node

To implement a uniform and stronger electric field, DMAPS often uses large electrode design that requires multiple wells (typically four including deep n and p wells); this layout adds on to the standard terms of the total capacity of the sensor a new term (fig. 2.5), that contributes to the total amplifier input capacity. In addition to the capacity between pixels (C_{pp}) and between the pixel and the backside (C_b), a non-negligible contribution comes from the capacities between wells

²Moore's law states that logic density doubles every two years.

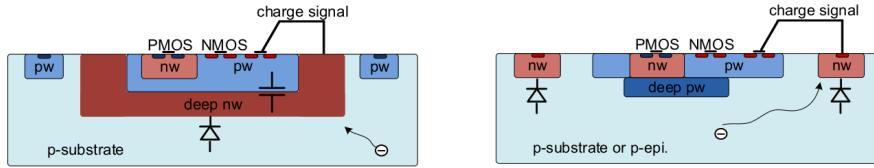


Figure 2.4: Concept cross-section with large and small fill factor

	small fill factor	large fill factor
small sensor C	✓ (< 5 fF)	✗ (~ 100-200 fF)
low noise	✓	✗
low cross talk	✓	✗
velocity performances	✓	✗ (~ 100 ns)
short drift paths	✗	✓
radiation hard	✗	✓

Table 2.1: Small and large fill factor DMAPS characteristics

152 (C_{SW} and C_{WW}) needed to shield the embedded electronics. These capacities affect the thermal
153 and 1/f noise of the charge amplifier and the τ_{CSA} too:

$$ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.6) \quad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.7)$$

155 where g_m is the transconductance, τ_{sh} is the shaping time.
156 Among the disadvantages coming from this large input capacity could be the coupling between
157 the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring
158 electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this problem
is especially connected with the intra wells capacities. So, larger charge collection electrode

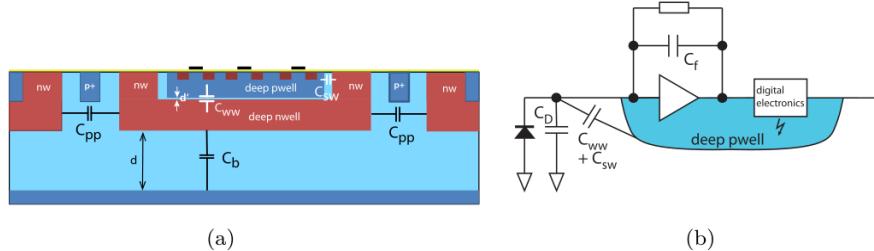


Figure 2.5: C_{pp} , C_b , C_{WW} , C_{SW}

159 sensors provide a uniform electric field in the bulk that results in short drift path and so in good
160 collection properties, especially after irradiation, when trapping probability can become an issue.
161 The drawback of a large fill-factor is the large capacity (~100 fF): this contributes to the noise
162 and to a speed penalty and to a larger possibility of cross talk.

163 The small fill-factor variant, instead, benefits from a small capacity (5-20 fF), but suffers from
164 a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando dei
165 MAPS, devo ripetere qui?**

166 As we'll see these two different types of sensor require different amplifier: the large electrode one is
167 coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.4.1).

169 2.3.2 A modified sensor

170 ?? A process modification developed by CERN in collaboration with the foundries has become the
171 standard solution to combine the characteristics of a small fill factor sensor (small input amplifier
172 capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE

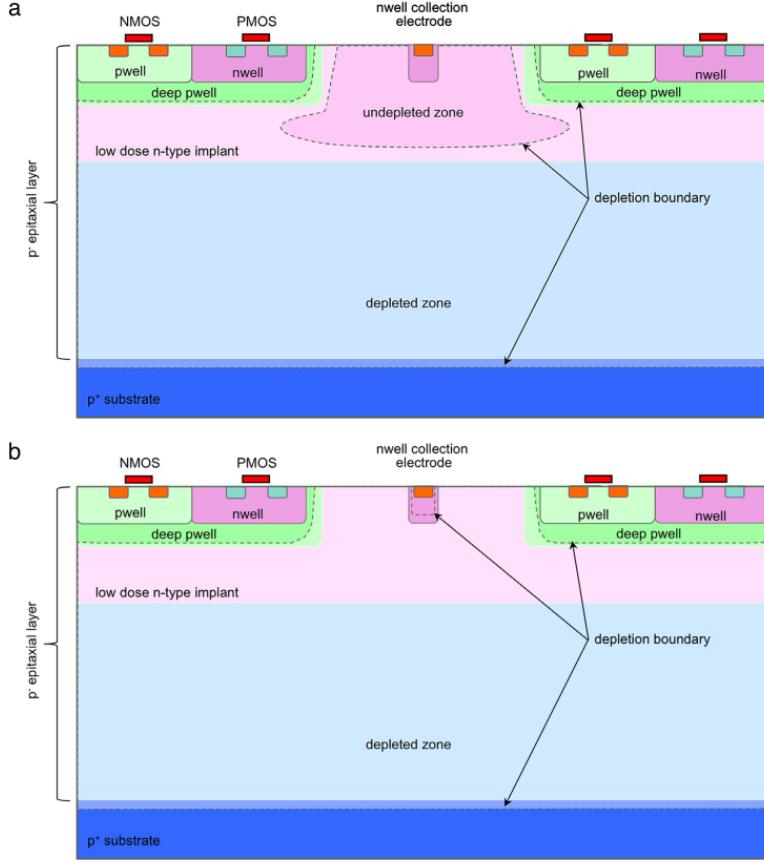


Figure 2.6: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

173 upgrade about ten years [1].

174 A compromise between the two sensors could also be making smaller pixels, but this solution
175 requires reducing the electronic circuit area, so a completely new pixel layout should be though.
176 The modification consists in inserting a low dose implant under the electrode and one its advantage
177 lies in its versatility: both standard and modified sensor are often produced for testing in fact.

178 Before the process modification the depletion region extends below the diode towards the sub-
179 strate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.6).
180 After, two distinct pn junctions are built: one between the deep p well and the n^- layer, and the
181 other between the n^- and the p^- epitaxial layer, extending to the all area of the sensor.
182 Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes
183 can be biased separately³ and this is beneficial to enhance the vertical electric field component.
184 The doping concentration is a trimmer parameter: it must be high enough to be greater than the
185 epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be
186 lower enough to allow the depletion without reaching too high bias.

187 2.4 Analog front end

188 After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.7), ready
189 to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an
190 efficient, high-speed readout architecture, consuming as low power as possible must be provided
191 by the readout integrated electronics (ROIC).

192 Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually
193 often is the only amplification stage) with a reset to the baseline mechanism and a leakage current

³This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

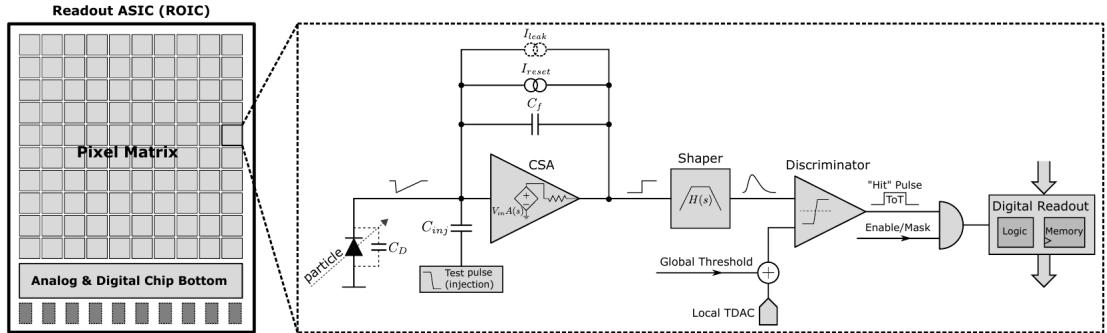


Figure 2.7: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

194 compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be
 195 optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise
 196 before the amplification stage in order to not multiply that noise, and chose a reasonable threshold
 197 of the discriminator to cut noise-hits much as possible.

198 2.4.1 Preamplifier

199 Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled
 200 as an operational amplifier (OpAmp) where the gain is determined by the input and feedback
 201 impedance (first step in figure 2.7):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.8)$$

202 Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a
 203 voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the
 204 voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor
 205 MAPS whose signal is already enough high: $v_{in} = Q/C_D \approx 3fC/100 \text{ pF} = 0.03 \text{ mV}$, but it's fine
 206 for the small fill factor ones: $v_{in} = Q/C_D \approx 3fC/3 \text{ pF} = 1 \text{ mV}$.

207 In the case of a resistor feedback, if the signal duration time is longer than the discharge time
 208 ($\tau = R_S C_D$) of the detector the system works as current amplifier, as the signal is immediately
 209 transmit to the amplifier; in the complementary case (signal duration longer than the discharge
 210 time) the system integrates the current on the C_D and operates as a voltage amplifier.

211 2.5 Readout logic

212 Readout logic includes the part of the circuit which takes the FE output signal, processes it and
 213 then transmit it out of pixel and/or out of chip; depending on the situation of usage different
 214 readout characteristics must be provided.

215 To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers
 216 and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really
 217 high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is
 218 recorded).

219 A common compromise often made is to save the time over threshold (ToT) of the pulse in clock
 220 cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen
 221 bits but, being correlated and hopefully being linear with the deposited charge by the impinging
 222 particle in the detector, it provides a sufficient information. The ToT digitalization usually takes
 223 advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels'
 224 matrix. The required timing precision is at least around 25 ns, that corresponds to the period of
 225 bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is
 226 40 MHz.

227 Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they
 228 have been read, and then the ToT is obtained from their difference.

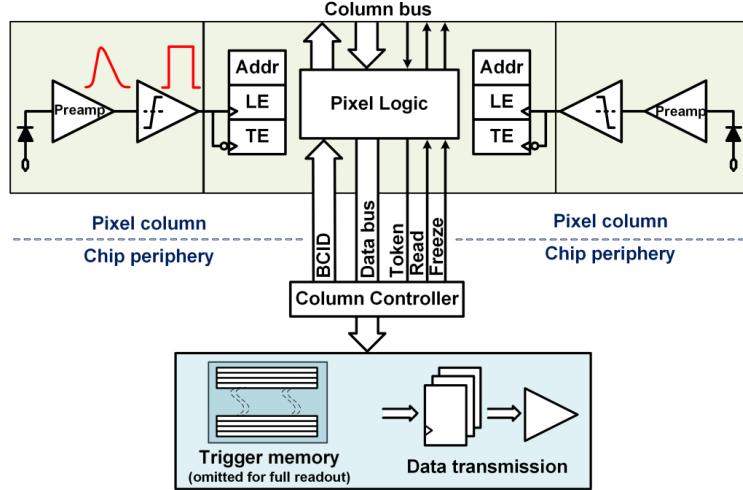


Figure 2.8: Column drain R/O scheme where ToT is saved

Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger system decides if the hit must be stored or not. On one hand the triggered-readout needs buffers and storage memories, on the other the full readout, because there is no need to store hit data on chip, needs an high enough bandwidth.

A triggered readout is fundamental in accelerator experiments where the quantity of data to store is too large to be handled, and some selections have to be applied by the trigger: to give an order of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100 MBit/s [2] (pag. 797).

Typically the trigger signal is processed in a few μs , so the pixel gets it only after a hundred clock cycles from the hit arrival time: the buffer depth must then handle the higher trigger latency.

After having taken out the data from the pixel, it has to be transmitted to the end of column (EoC) where a serializer delivers it out of chip, typically to an FPGA.

There are several ways of transmitting data from pixel to the end of column: one of the most famous is the column-drain read out, developed for CMS and ATLAS experiments [3]. All the pixels in a double-column share a data bus and only one pixel at a time, according to a priority chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored on a RAM until the SR does not allow the access to memory by data bus.

Even if many readout architectures are based on the column-drain one, it doesn't suit for large size matrices. The problem is that increasing the pixels on a column would also raise the number of pixels in the priority chain and that would result in a slowdown of the readout.

If there isn't any storage memory, the double-column behaves as a single server queue and the probability for a pixel of waiting a time T greater than t , with an input hit rate on the column μ and an output bandwidth B_W is [4]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.9)$$

To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time τ due to the AFE), for example imposing $P(T > t) \sim 0.001$, one obtains $(B_W - \mu) t_t \sim 6$, where t_t is the time needed to transfer the hit; since t_t is small, one must have $B_W \gg \mu$, that means a high bandwidth [4].

Actually the previous one is an approximation since each pixel sees a different bandwidth depending on the position on the queue: the first one sees a full bandwidth, but the next sees a smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen by the pixel i is $B_i = B - \sum_j \mu_j$, where μ_j is the hit rate of the j th pixel.

The efficiency requirement on the bandwidth and the hit rate becomes: $B_{W,i} > \mu_i$, where the index i means the constraint is for a single pixel; if all the N pixels on a column have the same rate $\mu = N\mu_i$, the condition reduces to $B_W > \mu$. The bandwidth must be chosen such that the mean time between hits of the last pixel in the readout chain is bigger than that.

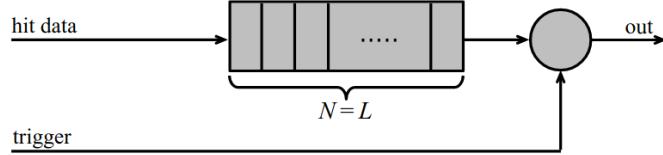


Figure 2.9: Block diagram of a pipeline buffer: N is the dimension of memory buffer and L is the trigger latency expressed in BCID cycles

265 In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed;
 266 this means that only information from channels where the signal exceeds the discriminator thresh-
 267 old are stored. Qu'è succiso con la zero suppression? La metto qui questa affermazione?

268 If instead there is a local storage until a trigger signal arrives, the input rate to column bus
 269 μ' is reduced compared to the hit rate μ as: $\mu' = \mu \times r \times t$, where r is the trigger rate and t is
 270 the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth,
 271 but the limiting factor is the buffer depth: the amount of memory designed depends both on the
 272 expected rate μ and on the trigger latency t as $\propto \mu \times t$, that means that the higher the trigger
 273 latency and the lower the hit rate to cope with.

274 In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels
 275 into regions with shared storage. Let's compare two different situations: in the first one a buffer
 276 is located on each pixel area, while in the second one a core of four pixels share a common buffer
 277 (this architecture is commonly called FE-I4).

Consider a 50 kHz single pixel hits rate and a trigger latency of 5 μs , the probability of losing

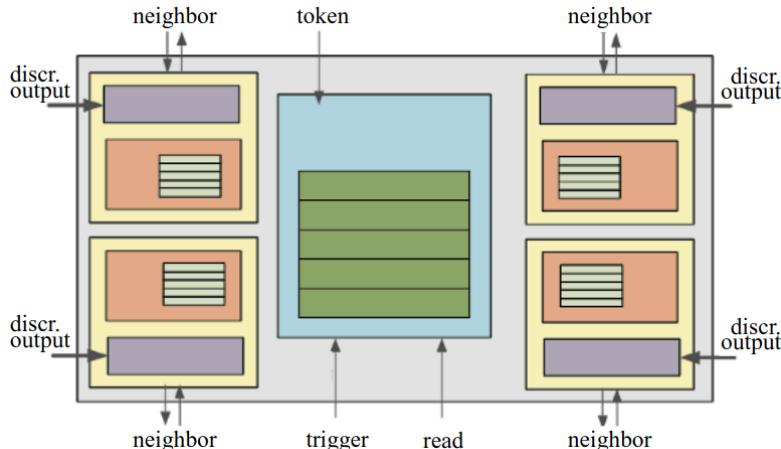


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is highlighted in light blue; latency counters and trigger management section are highlighted in green; hit processing blocks are highlighted in purple; ToT counters and ToT management units are highlighted in orange

278 hits is:
 279

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.10)$$

280 where I have assumed a Poissonian distribution with mean $\nu = 0.25$ to describe the counts N.
 281 To get an efficiency ϵ greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.11)$$

282 Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four
 283 pixels the mean number of hits per trigger latency is $\nu = 0.25 \times 4 = 1$. To get an efficiency of
 284 99.9% (eq. 2.11) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

²⁸⁵ **Chapter 3**

²⁸⁶ **Use of pixels detector**

²⁸⁷ A partire dal 2017, i sensori CMOS rappresentano l'89% delle vendite globali di sensori di immagine.
²⁸⁸ Ma praticamente dal 2010 in poi solo CMOS e non più CCD.

²⁸⁹

²⁹⁰ **3.1 Tracking in HEP**

²⁹¹ Per gli acceleratori la richieste sono molto stringenti e lo saranno sempre di più con l'aumento dell'
²⁹² intensità o della luminosità in termini di radiation hardness (per HL-LHC for example expected
²⁹³ in 5 anni 500 Mrad e NIEL di 10 alla 16), efficiency e occupancy (efficienza alta dopo tanta
²⁹⁴ radiazione e noise occupancy bassa), time resolution (bunch crossing 40 Mhz), material budget e
²⁹⁵ power consumption (material budget below 2 per cento e power consumption 500 mW/cm²)
²⁹⁶ Usati come tracciatori per misure di impulso e per misure di energia (per rigettare) ad esempio
²⁹⁷ dati di fondo (topic fondamentale per BELLE-II).

²⁹⁸ **Resolution**

²⁹⁹ Depending on the type of signal reading the spatial resolution is $\sigma_x = \frac{p}{\sqrt{12}}$ where p is the pitch
³⁰⁰ between pixels, or even better if other analogica information, as the charge, are read and capacitive
³⁰¹ charge division method is applied.

³⁰² **3.1.1 Hybrid pixels: ATLAS, CMS and LHC-b**

³⁰³ **3.1.2 CMOS MAPS: ALICE and STAR**

³⁰⁴ For years ALICE have been pioneering MAPS detectors and its sensors are currently state-of-the
³⁰⁵ art in this sector, to the point that most of today's CMOS MAPS chips implement the same FE
³⁰⁶ of ALICE Pixel Detector, and in fact they are commonly called "ALPIDE-like" sensors¹.

³⁰⁷ **3.2 Application in medical imaging**

³⁰⁸ **3.2.1 Medipix and Timepix**

³⁰⁹ **3.2.2 Applicability to FLASH radiotherapy**

¹As we'll see TJ-Monopix1 and ARCADIA have an ALPIDE-like front end.

³¹⁰ **Chapter 4**

³¹¹ **TJ-Monopix1**

³¹²

- ³¹³ • scrivere la differenza tra i FE
- ³¹⁴ • fare disegno uguale a quello del mascheramento però con solo due coordinate (oggi?)
- ³¹⁵ • scrivere delle misure cambiando i parametri del FE, e rifare le misure del FE con oscilloscopio
- ³¹⁶ e qualche plot
- ³¹⁷ • scrivere misure del tempo morto (oggi)

³¹⁸ The TJ-Monopix1 is one of the chips fabricated by TowerJazz with 180 CMOS imaging process.
³¹⁹ From the middle of 2013 a dedicated collaboration, RD 53 ('Development of pixel readout integrated
³²⁰ circuits for extreme rate and radiation'), has been established with the specific goal to find
³²¹ a sensor suitable as vertex detector for future upgrade of CMS and ATLAS experiments. Among
³²² the main objects of study of the collaboration there are both hybrid pixels and monolithic options
³²³ as CMOS MAPS: fig 4.1 shows the intermediate MAPS-prototypes made by TowerJazz.

Besides the TowerJazz series, also LFoundry fabricated other similar sensors with 150 CMOS



Figure 4.1: Timeline in TowerJazz productions. In addition to Monopix series also the small electrode demonstrator TJ-Malta and mini-Malta have been produced and tested[6]. The Malta prototypes differ from TJ-Monopix in the readout: while Monopix implements a column-drain R/O, an asynchronous R/O without any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.

³²⁴

³²⁵ technology [7][8]: LF-Monopix.

³²⁶ The main differences between the LFoundry and TowerJazz's products (tab. 4.2), are in the sensor
³²⁷ structure rather than in the readout architecture, based on a column drain R/O with ToT capability
³²⁸ (LF-Monopix has 8 bits dedicated and TJ-Monopix 6 bits). Concerning the sensor, LFoundry
³²⁹ pixels are bigger and have a large fill factor, while TJ-Monopix ones have a small fill-factor elec-
³³⁰ trode.

³³¹ The performances of both the detectors have been tested before and after irradiation (\sim
³³² $10^{10} n_{eq}/cm^2$) and the result is, as expected since LF-Monopix is a large fill factor electrode (chap.
³³³ ??), that LF-Monopix is more radiation hard than TJ-Monopix whereas the main degradation of

Parameter	Value
Matrix size	
Pixel size	$26 \times 40 \mu\text{m}^2$
Depth	$25 \mu\text{m}$
BCID	40 MHz
ToT-bit	6
Power consumption	$\sim 120 \text{ mW/cm}^2$

Table 4.1

	LF-Monopix1	TJ-Monopix1
Bulk Resistivity	p-type substrate <i>maggior</i> $2 \text{k}\Omega\text{cm}$	p-epi. on a low ρ substrate <i>maggior</i> $1 \text{k}\Omega\text{cm}$
Pixel size	$50 \times 250 \mu\text{m}^2$	$26 \times 40 \mu\text{m}^2$
Depth	$100-750 \mu\text{m}$	$25 \mu\text{m}$
Capacity	$\sim 400 \text{ fF}$	$\sim 3 \text{ fF}$
Preamplifier	CSA	Voltage
Threshold trimming	on pixel (4-bit DAC)	global threshold
Readout mode	Fast column drain	Fast column drain
Consumption	$\sim 300 \text{ mW/cm}^2$	$\sim 120 \text{ mW/cm}^2$
Threshold	$1500 e^-$	$\sim 270 e^-$
ENC	$100 e^-$	$\sim 30 e^-$

Table 4.2: Main characteristics of TJ-Monopix and LF-Monopix [8]TRASFORMALA IN TESTO

efficiency in TJ-Monopix chips is due to the low electric field in the pixel corner. On the other hand one more accidental consequence of the large fill factor size in LF-Monopix (the deep p-well covers $\sim 55 \%$ of the pixel area) is a significant cross-talk problem.

4.1 The sensor

TJ-Monopix1 adopts the modification described in ?? that allows to achieve a planar depletion region near the electrode applying a relatively small reverse bias voltage: a low dose n implant is build on a high resistivity ($\geq 1 \text{ k}\Omega \text{ cm}$), p-type epitaxial layer.

This modification improves the efficiency of the detector, especially after irradiation[]; however a Technology Computer Aided Design (TCAD) simulation has shown that a nonuniform electric field is still produced in the lateral regions after the modification; since the transversal component of the electric field drops at the pixel corner (this point in figure 4.2 is indicated by a star) the efficiency at the side is reduced.

On a sample of chip, the one I've tested in Pisa belongs to these, a second optimization have been made to enhance the lateral component of electric field and improve the efficiency and velocity in charge collection near the corners of the sensor: a portion of low dose implant has been removed, creating a step discontinuity in the pixel corner. A side effect is the weaker separation between the deep p-well and the p-substrate, that cannot be biased separately anymore to prevent the punchthrough.

Moreover, to investigate the charge collection properties, as the threshold, the noise and the efficiency, pixels within the matrix feature a difference in the doping structure of the deep p-well: rows from 0 to 111 are fully covered by deep p-well (FDPW) under p-well near the sensor, while rows from 112 till the last 223 have a portion of deep p-well removed (RDPW). **a pagina 69 della tesi spiega come fa a non creare danno la rimozione del deep pwell**

The removing enhance the lateral electric field component then resulting in a higher efficiency, as we'll see later.

The collection electrode size is $2 \mu\text{m}$ in diameter and its spacing from the electronics area is equal to $3 \mu\text{m}$; In order to reduce possible crosstalk, the digital and analog areas are physically separated

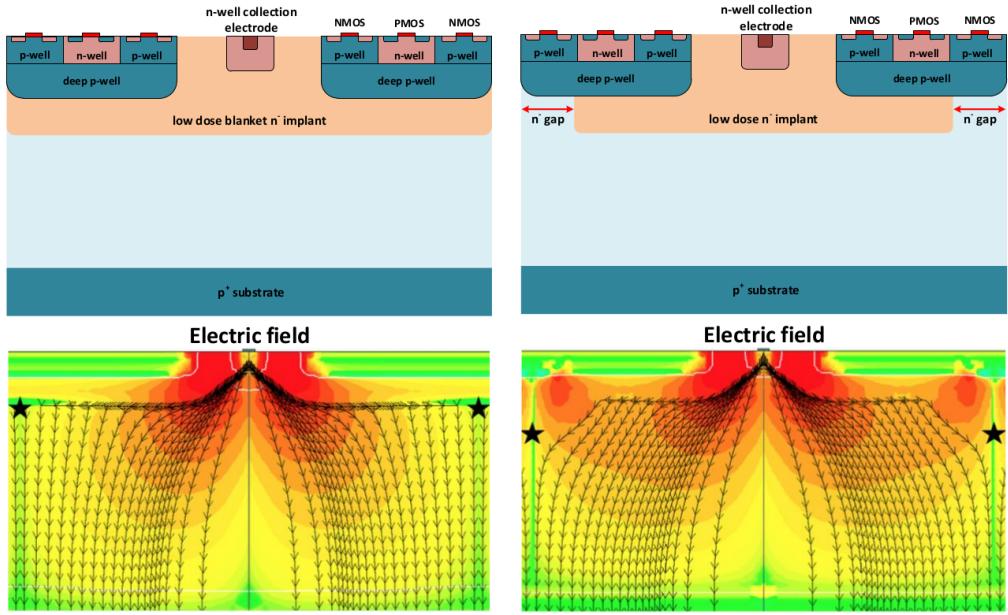


Figure 4.2: (a) The cross-section of a monolithic pixel in the TJ-Monopix 180 nm with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field

4.2 Front end

The whole matrix contains 224×448 pixels, with size $36 \times 40 \mu\text{m}^2$ yielding a total active area approximately equal to 145 mm^2 over a total area of $1 \times 2 \text{ cm}^2$. The chip periphery includes all the required support blocks to bias, configure, test and readout the pixel matrix. A 7-bit Digital to Analog Converter (DAC) is used to generate the analog bias voltage and current levels. No trigger memory is implemented in this prototype, hence the readout is full (continuous). Pixel data is transferred to the End of Column (EoC) logic, serialized and then immediately transmitted. Digital Input/Output (I/O) CMOS transceivers, operating at 40 MBps, are used for communication and data transmission to the external DAQ testing system. Matrix power pads are distributed at the sides

4.2.1 Four flavors

Four different flavors have been implemented in order to explore different variations of the data-bus readout circuitry and of the reset: each flavor corresponds to a different sector on the matrix (fig. 4.3) and thus having a separate readout and data transmission. Flavors B, C and D feature a source-follower column-bus readout derived from the LF-Monopix1 chip, that aims to reduce the crosstalk. However, it leads in a significant amount of static power being drawn at the EoC periphery. To eliminate static power consumption a modified gated source follower readout has been included in a flavor A, which is otherwise identical to flavor B. Flavor B, referred to as the "PMOS reset", is the standard (reference) variation and features a DC-coupled PMOS input reset. Flavor C incorporates a novel leakage compensation circuit and flavor D, also called the "HV" flavor, explores the possibility of applying a high front-side bias voltage to the collection electrode which in this case is AC-coupled to the front-end input. R resistenza di reset deve essere abbastanza grande in modo da far sì che il ritorno allo zero è abbastanza lento (non devi "interferire" con la tot slope e non devi più corto del tempo del preamplificatore, sennò hai perdita di segnale). Baseline reset: all'input solitamente hai un PMOSS o un diodo; R reset; Voltage amplifier The FE circuit 4.4b is ALPIDE-like, so it is similar to the one described in ??; a quanto già detto voglio però aggiungere due parole: come viene implementato il mascheramento dei pixels e il reset.

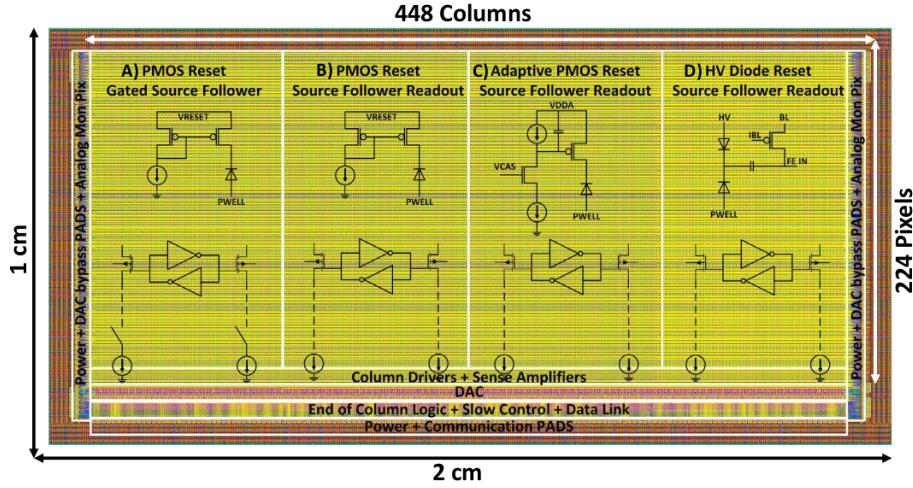
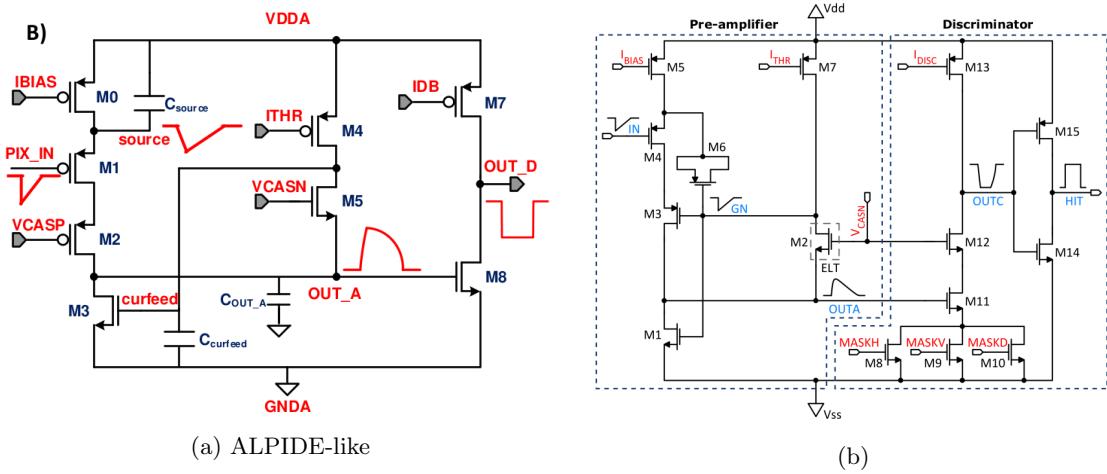


Figure 4.3

4.2.2 ALPIDE-like front end

As I already mentioned, ALICE Pixel Detector (ALPIDE) is the current state-of-art and most of the following chips' FE are inspired by that, making it a standard in the FE design. The idea of the



amplification stage is to transfer the charge from a bigger capacity[5], C_{source} , to a smaller one, C_{out} : the input transistor M1 with current source IBIAS acts as a source follower and this forces the source of M1 to be equal to the gate input $\Delta V_{PIX_IN} = Q_{IN}/C_{IN}$.

$$Q_{source} = C_{source} \Delta V_{PIX_IN} \quad (4.1)$$

The current in M2 and the charge accumulates on C_{out} is fixed by the one on C_{source} :

$$\Delta V_{OUT_A} = \frac{Q_{source}}{C_{OUT_A}} = \frac{C_{source} \Delta V_{PIX_IN}}{C_{OUT_A}} = \frac{C_{source}}{C_{OUT_A}} \frac{Q_{IN}}{C_{IN}} \quad (4.2)$$

A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR set the baseline value of the signal on C_{OUT_A} and the velocity to goes down to the baseline.

IL RUOLO DI CURVFEED NON L'HO CAPITO.

Finally IDB defines the charge threshold with which the signal OUT_A must be compared: depending on if the signal is higher than the threshold or not, the OUT_D is high or low respectively. I've already mentioned ALICE pixel detector talking about the new process modification, now the ALICE name comes up again talking about FE: this is because ALPIDE (ALice PIxel DEtector) is one of the first MAPS detector (TowerJazz 180 nm CMOS) installed ¹, therefore it is the current

¹It was installed in the Inner Tracking System during the second long shut down of the LHC in 2019

Parameter	Meaning
IBIAS	
IDB	
ITHR	
VCASN	
VREF	
IREF	

Table 4.3

404 state-of-art and most of the following chips' FE are inspired by that, making it a standard in the
405 FE design.

406 In order to reduce the hit rate and to avoid saturating the bandwidth, is uttermost important
407 to include in the FE a way to mask noisy pixels, which typically are those with manufacturing
408 defects. In the circuit in fig. 4.4b transistors M8, M9 and M10 have the function of disabling
409 registers with coordinates MASKH, MASKV and MASKD (respectively vertical, orizontal and
410 diagonal) from readout: if all three transistors-signals are low, the pixel's discriminator is disabled.
411 Compared with a configurable masking register which would allow disableing pixels individually,
412 to use a triple redundancy reduces the sensistivity to SEU² but also gives amount of intentionally
413 masked ("ghost") pixels. This approach is suitable only for extremely small number N of pixel has
414 to be masked: if two coordinate projection scheme had been implemented, the number of ghost
415 pixels would have scale with N^2 , if instead three coordinates are used, the N's exponential is lower
than 2 (fig. 4.5)

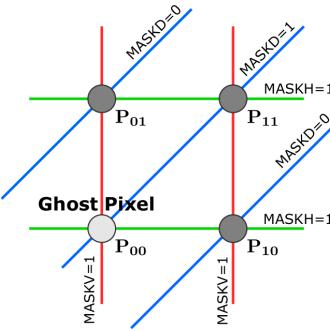


Figure 4.5

416

4.2.3 Front end parameters

417 Descrivo un po' le misure fatte sul fe e sul significato dei vari parametri.
418 it allows injecting pixels with a known charge in DAC units. the front-end analog output of
419 four special pixels at each side, placed next to the matrix, is buffered and can be monitored for
420 characterization and debugging purposes.

4.3 Readout logic

423 The BCID timestamp, data lines and read/freeze control signals use differential signaling in order
424 to reduce electromagnetic interference, reject common mode noise and effectively double the signal
425 to noise ratio. As a result, the BCID timing uncertainty (jitter) is reduced and the data-bus speed

²Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché una particella deposita carica nell'elettronica che fa da memoria registro/RAM/.... Questo tipo di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più carica di quanto farebbe una MIP. Questo metodo pur essendo più comodo richiede less amount of area ha però come drawback che il registro può essere soggetto a SEU problema non trascurabile in acceleratori come HL-LHC adronici

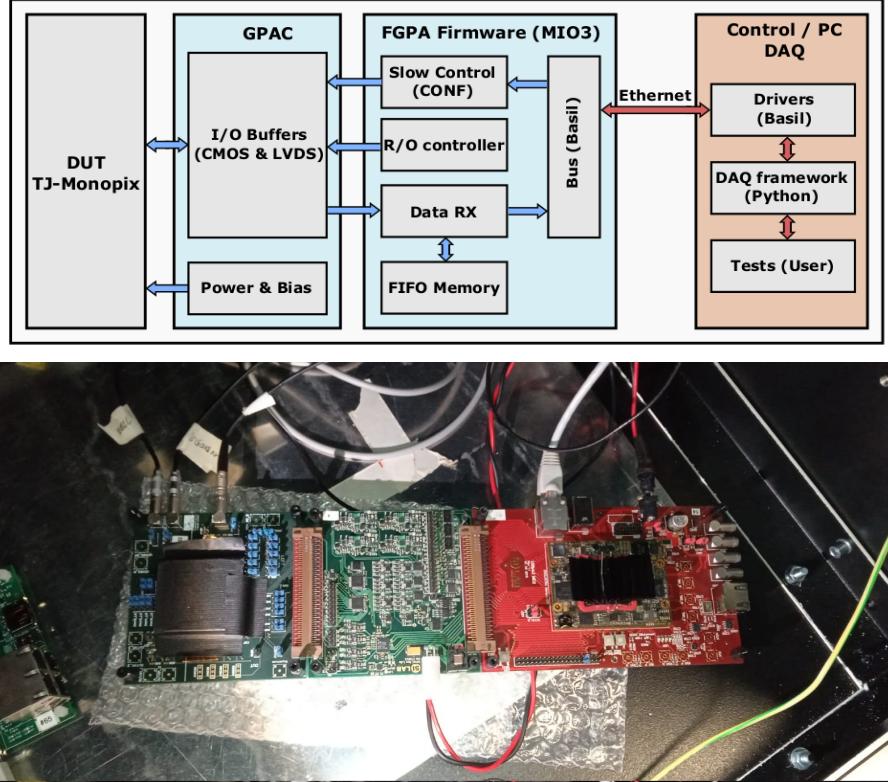
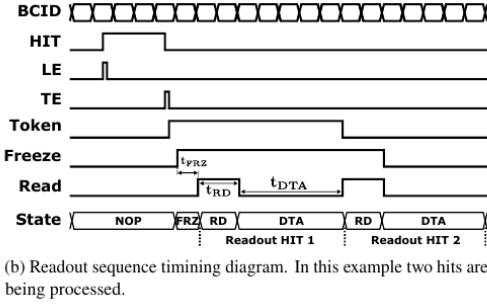


Figure 4.6: Main caption

(column bandwidth) is increased. The drawback of differential signaling is the higher routing complexity that requires double the amount of metal wires and can impact the pixel size. TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address. Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is already storing a previous one, the new data get lost. After being read, the data packet is sent to the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (4.6). There a FIFO is used to temporarily stored the data, which is transmitted to a computer through an ethernet cable in a later time.

The access to the pixels' memory and the transmission of the data to the EoC is based on a Finite State Machine (FSM) composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and data transfer (DTA). The readout sequence (??) starts with the TE of a pulse: the pixel immediately tries to grab the column-bus turning up a hit flag signal called *token*. The token is used to control the priority chain and propagates across the column indicating what pixel that must be read. To start the readout and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal is activated, and then a *read* signal controls the readout and the access to memory. During the freeze, the state of the token for all pixels on the matrix remains settled: this does not forbid new hits on other pixels from being recorded, but forbids pixels hit from turning on the token until the freeze is ended. The freeze stays on until the token covers the whole priority chain and gets the EoC: during that time new token cannot be turned on, and all hits arrived during a freeze will turn on their token at the end of the previous freeze. Since the start of the token is used to assign a timestamp to the hit, the token time has a direct impact on the time resolution measurement; this could be a problem coping with high hits rate.

The analog FE circuit and the pixel control logic are connected by an edge detector which is used to determine the LE and the TE of the hit pulse(fig. 4.8): when the TE is stored in the first latch the edge detector is disabled and, if the **FREEZE** signal is not set yet, the readout starts. At this point the HIT flag is set in a second latch and a token signal is produced and depending on the value of **Token in** the pixel can be read or must wait until the **Token in** is off. In figure an OR



(b) Readout sequence timing diagram. In this example two hits are being processed.

Figure 4.7: Readout timing diagram: in this example two hits are being processed

455 is used to manage the token propagation, but since a native OR logic port cannot be implemented
 456 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly
 457 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token
 458 and to speed up the circuit optimized solution are often implemented. When the pixel become the
 459 next to be read in the queue, and at the rising edge of the **READ** signal, the state of the pixel is
 460 stored in a D-latch and the pixel is allowed to use the data bus; the **TE** and the **HIT** flag latches
 461 are reset and a **READINT** signal that enable access of the RAM and ROM cells is produced.

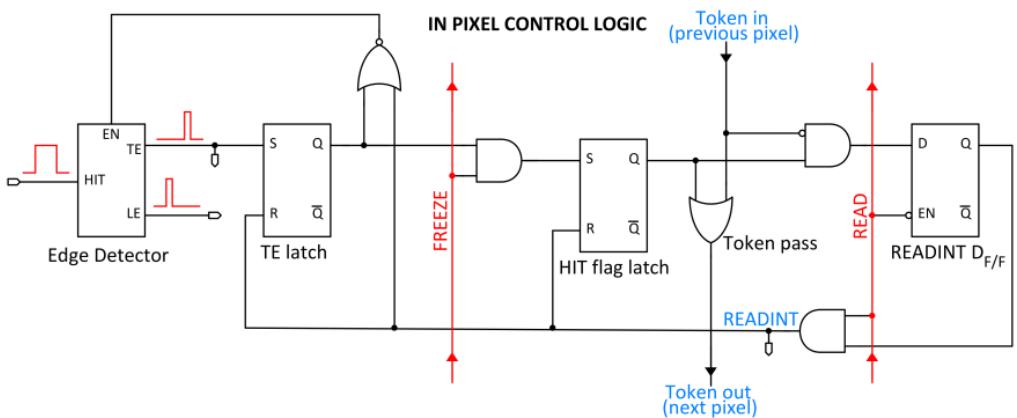


Figure 4.8

462
 463 The final data must provide all the hits' information: the pixel address, the ToT and the
 464 timestamp. All those parts are assigned and appended at different time during the R/O chain:

- 465 • **Pixel address:** while the double column address (6-bit) is appended by the EoC circuit,
 466 the row address (8-bits for each flavor) and the physical column in the doublet (1-bit) are
 467 assigned by the in-pixel logic
- 468 • **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge
 469 detector in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is
 470 range 0-64 clock cycle which corresponds to 0-1.6 μ s
- 471 • **Timestamp:** The timestamp of the hit correspond to the time when the pixel set up the
 472 token; it is assigned by the FPGA, that uses the LE, TE and a 640 MHz clock to derive
 473 it. For all those hits which arrived while the matrix is frozen, the timestamp is no more
 474 correlated with the time of arrival of the particle

475 When the bits are joined up together the complete hit data packet is 27-bit.

476 4.3.1 Dead time measurement

477 The hit loss can be due to both analog and digital pile up: the first one occurs when a new hit
 478 arrives during the pre-amplifier response, the second instead occurs when a new hit arrives while

479 the information of the previous hit has not yet been transferred to the periphery. The digital
 480 pile-up contribution is the more relevant and the dead time is almost entirely determined by that;
 481 as only one hit at a time can be stored on the pixel's RAM, until the data have completed the path
 482 to get out, the pixel readout is paralyzed and the τ corresponds with the time needed to export
 483 the data-packets. Since the transmission of data from pixel to the EoC occurs via a ?-bits data
 484 bus (this means that only one clock cycle is need to transfer the data to the end of column), the
 485 dead time bottleneck is given by the bandwidth of the serializer at the EoC: typically it operates
 486 at 40 MHz, and to transmit a data packet (27-bit) at least 675 ns are needed. For what we have
 487 said so far, the R/O is completely sequential and therefore is expected a linear dependence of τ on
 488 the number of pixels to read:

$$\tau = 25 \text{ ns} \times (\alpha N + \beta) \quad (4.3)$$

489 where α and β are parameters dependent on the readout chain. In particular, looking at fig. 4.7, α
 490 is the time with α (CONF STOP FREEZE-CONF START READ), and β ToT + CONF START
 491 FREEZE.

492 To measure and to test the linearity of the dead time with the number of pixels firing, I have
 493 used the injection mode available on the chip, that allows fixing not only the amplitude of the pulse
 494 (charge in DAC, as already seen in the previous section) but also the period and width. I have
 495 injected one hundred of pulses Reducing each time the distance between two consecutive pulses, I
 496 have injected until the number of hits counted were less than the injected ones.

497 Per definire meglio il τ faccio riferimento alla fig ??: se una hit arriva su un pixel mentre ha
 498 il token alto allora la hit viene persa. Se una hit arriva su un pixel che non ha il token alto
 499 ma ha il freeze alto, allora non viene persa ma le viene assegnato un timestamp errato. PARLO
 ANCHE DELLA "RISOLUZIONE TEMPORALE?" A tutte le hit di una iniezione che arrivano

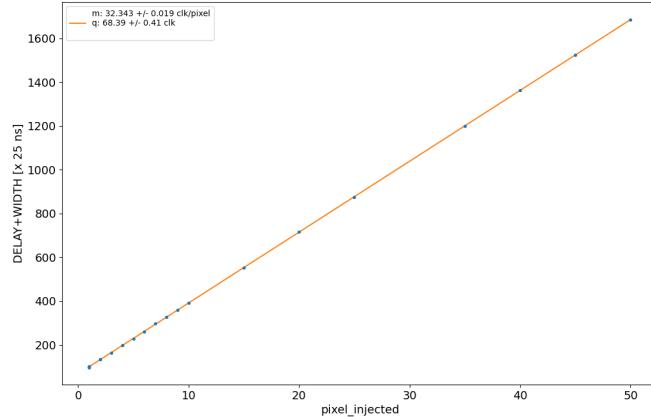


Figure 4.9

500 contemporaneamente viene assegnato lo stesso timestamp; quando le hit iniziano ad essere meno
 501 di quelle che mi aspetti. Mappa in funzione delle iniezioni di quali pixel hai letto.

503 Chapter 5

504 Arcadia-MD1

505 [9] [10]

506 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED
507 Matisse a Md1 e Md2

508 5.1 The sensor

509 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node
510 with six metal layer ???. The standard p-type substrate was replaced with an n-type floating zone
511 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).

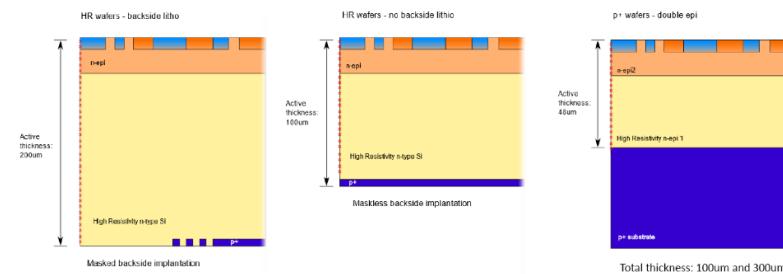


Figure 5.1

512
513 Wafer thinning and backside litography were necessary to introduce a junction at the bottom
514 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.
515 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthought
516 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

517 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,
518 COME VENGONO FATTI I MAPS COME FAI LE GIUNZIONI

519 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.
520 It is operated in full depletion with fast charge collection by drift.

521 Prima SEED si occupa di studiare le prestazioni: oncept study with small-scale test struc-
522 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo
523 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il
524 pwell e quanto al diodo. ..

525 5.2 Readout logic and data structure

526 5.2.1 Matrix division and data-packets

527 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided
528 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in

529 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei
 serializzatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

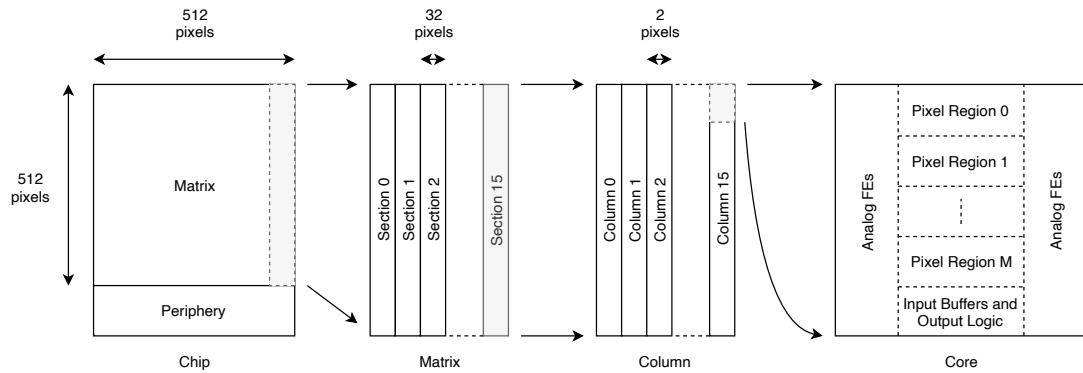


Figure 5.2

530

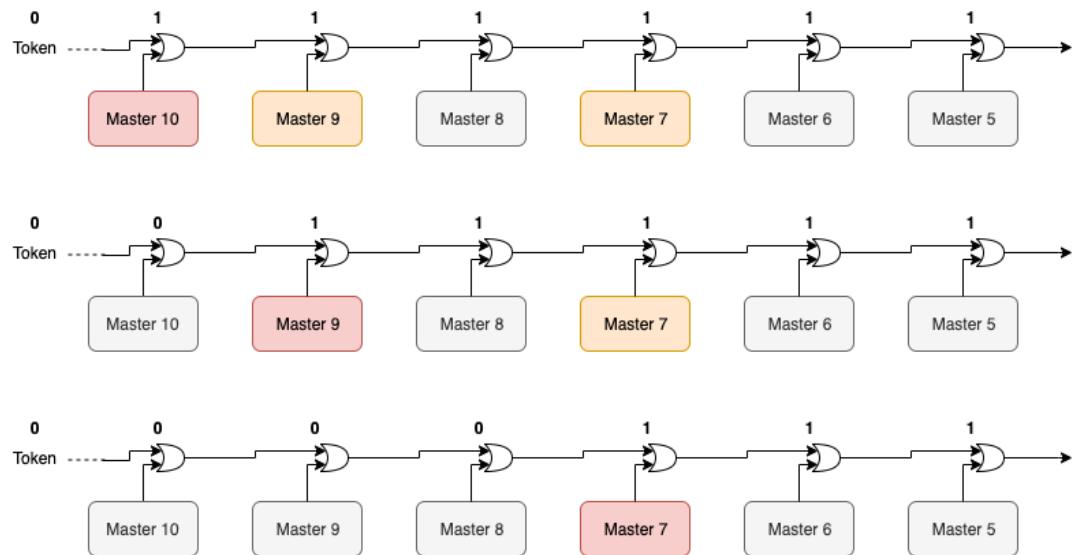


Figure 5.3

531 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le
 532 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,
 533 e devi accennare al timestamp

534 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively
 535 large core allows one to take full advantage of digital synthesis tools to implement complex func-
 536 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della
 537 review.

538

539 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column
 540 (512x2) Core (32x2) Region (4x2)

541 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

542 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for
 543 example 8b10b encoding n =5"

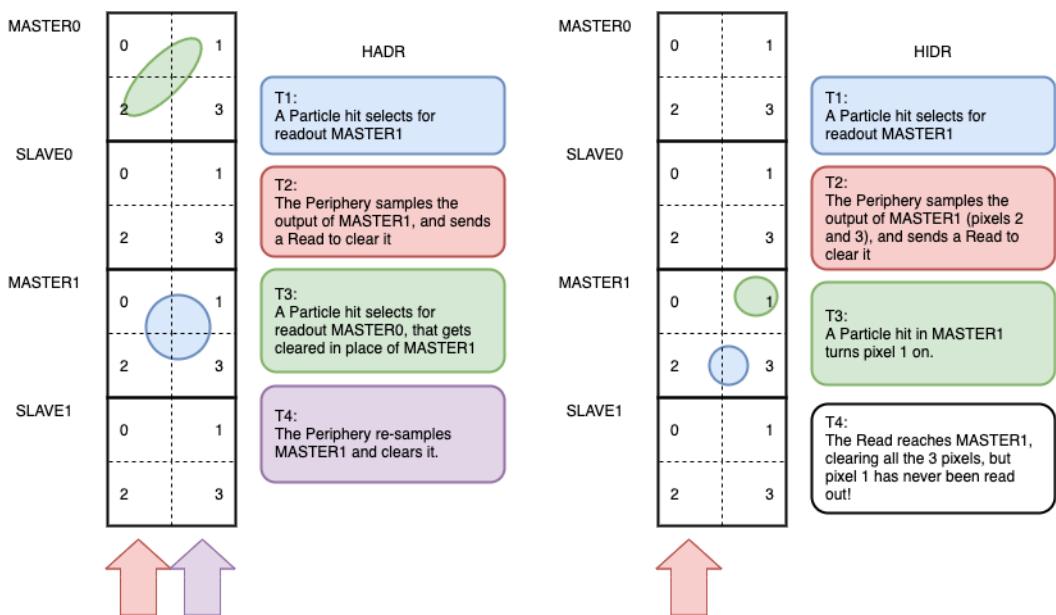


Figure 5.4

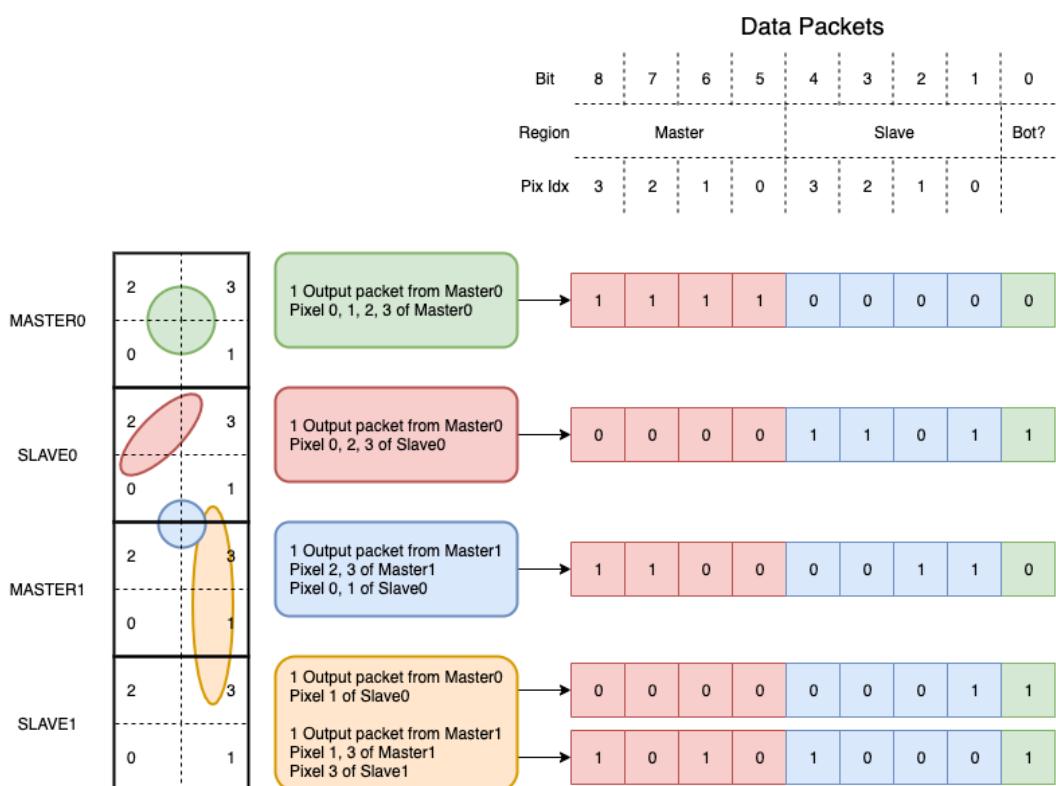


Figure 5.5

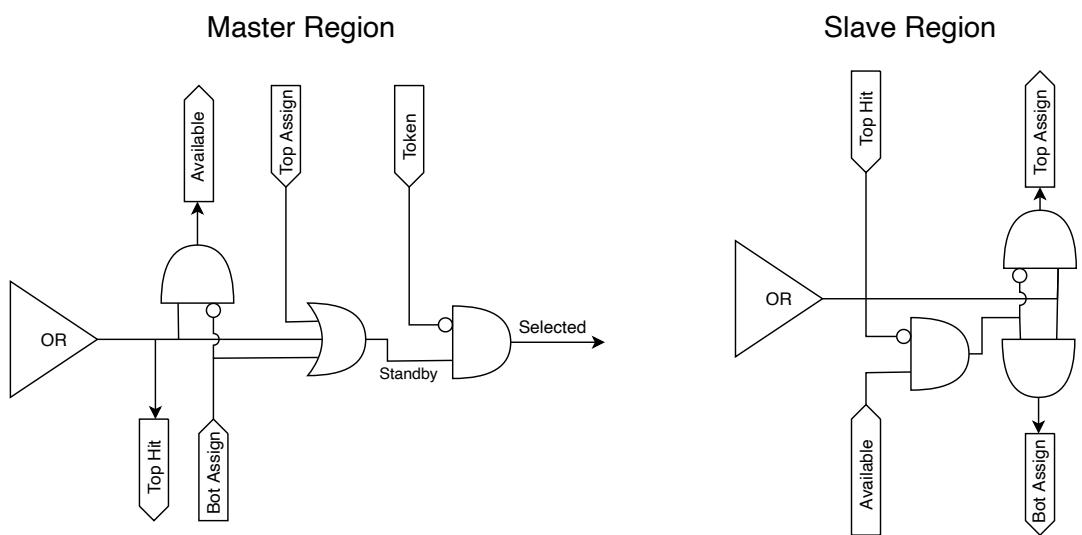


Figure 5.6

544 **Chapter 6**

545 **Threshold and noise
546 characterization**

547 **6.1 Threshold and noise: figure of merit for pixel detectors**

548 The signal to threshold ratio is the figure of merit for pixel detectors.

549
550 la soglia deve essere abb alta da tagliare il rumore ma abb bassa da non perdere efficienza.
551 Invece di prendere il rapporto segnale rumore prendi il rapporto segnale soglia. Perchè? la soglia
552 è collegato al rumore, nel senso che: supponiamo di volere un occupancy di 10-4 allora sceglierò la
553 soglia in base a questo. (plot su quaderno) Da questo conto trovo la minima soglia mettibile
554 In realtà quello che faccio è mettere una soglia un po' più grande perchè il rate di rumore dipende
555 da molti fattori quali la temperatura, l annealing ecc, e non voglio che cambiando leggermente uno
556 di questi parametri vedo alzarsi molto il rate di rumore. In realtà non è solo il rumore sensibile a
557 diversi fattori, ma anche la soglia: ad esempio la cosa classica è la variabilità della soglia da pixel
558 a pixel.

559 In questo modo rumore e soglia diventano parenti.

560 Review pag 26.

561 The noise requirement can be expressed as:

562 Questo implica tra le altre cose che voglio poter assegnare delle soglie diverse a diversi pixel:
563 Drawback è dare spazio per registri e quantaltro.
564 Questo lascia però ancora aperto il problema temporale delle variazioni del rumore: problema per
565 cui diventano necessarie le misure dei sensori dopo l'irraggiamento.

566
567 Per arcadia i registri (c'è un DAC) per la soglia (VCASN) si trovano in periferia. Non fare
568 trimming sulla soglia è uno dei problemi che si sono sempre incontrati: a casusa dei mismatch dei
569 transistor le soglie efficaci pixel per pixel cambiano tanto. La larghezza della s curve è il noise se se
570 assumi che il noise è gaussiano

571 Il trimming della soglia avviene con dei DAC: la dispersione della soglia dopo al tuning e dovuta
572 al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.1)$$

573 dove il numero di bit cambia varia tra 3-7 tipicamente. Monopix è 7 Arcadia 6

574
575 Each ROIC is different in this respect, but in general the minimum stable threshold was around
576 2500 electrons (e) in 1st generation ROICs, whereas it will be around 500 e for the 3rd generation.
577 This reduction has been deliberate: required by decreasing input signal values. Large pixels (2 104
578 um²), thick sensors (maggiore di 200 um), and moderate sensor radiation damage for 1st generation
579 detectors translated into expected signals of order 10 ke, while small pixels (0.25 104 um²), thinner
580 sensors (100 um), and heavier sensor radiation damage will lead to signals as low as 2 ke at the
581 HL-LHC

582 The ENC can be directly calculated by the Cumulative Distribution Function (CDF) (scurve)
583 obtained from the discriminator "hit" pulse response to multiple charge injections

⁵⁸⁴ **6.2 TJ-Monopix1 characterization**

⁵⁸⁵ **6.3 ARCADIA-MD1 characterization**

586 Appendix A

587 Pixels detector: a brief overview

588 A.1 Radiation damages

589 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they
 590 are almost always installed near the interaction point where there is a high energy level of radiation.
 591 At LHC the ϕ_{eq} per year in the innermost pixel detector is $10^{14} n_{eq}/cm^2$; this number reduces by
 592 an order passing to the outer tracker layer [2] pag 341 Wermes. Here the high fluence of particles
 593 can cause a damage both in the substrate of the detector and in the superficial electronics.

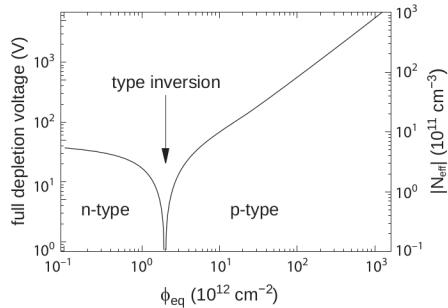
594 The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but
 595 it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the
 596 NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV
 597 neutrons. Differently, surface damages are principally due to ionizing energy loss.

598 **DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide (S_iO_2) can
 599 cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages
 600 are mostly less relevant than the previous one, since with the development of microelectronics and
 601 with the miniaturization of components (in electronic industry 6-7 nm transistors are already used,
 602 while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit
 603 is reduced.

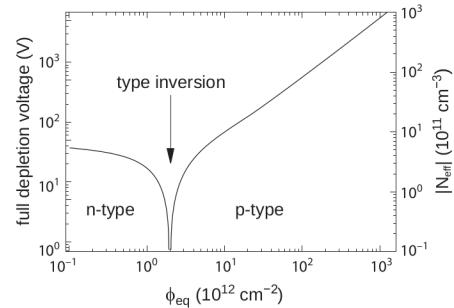
604 Let's spend instead two more other words on the more-relevant substrate damages: the general
 605 result of high radiation level is the creation of new energy levels within the silicon band gap and
 606 depending on their energy-location their effect can be different, as described in the Shockely-Read-
 607 Hall (SRH) statistical model. The three main consequence of radiation damages are the changing
 608 of the effect doping concentration, the leakage current and the increasing of trapping probability.

609 **Changing of the effective doping concentration:** is associated with the creation/removal
 610 of donors and acceptors center which trap respectively electrons/holes from the conduction band
 611 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type¹)
 612 can happen: indeed it is quite common at not too high fluences ($\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$). A changing
 613 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime
 614 (eq.2.1) and sometimes can be difficult keeping to fully deplete the bulk.

¹L'INVERSIONE OPPOSTA NON CE L'HA PERCHÈ?



(a) 1a



(b) 1b

615 **Leakage current:** is associated with the generation-recombination centers. It has a strong
616 dependence with the temperature ($I_{leak} \propto T^2$), whose solution is therefore to operate at lower
617 temperature.

618 **Increase of trapping probability:** since the trapping probability is constant in the depleted
619 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,
620 that is the mean trapping path, decreases after irradiation and typical values are 125-250 μm and
621 must be compared with the thickness of the depleted region which () corresponds to the mean drift
622 path.

623 Different choices for substrate resistivity, for junctions type and for detector design are typically
624 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced
625 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))
626 for example, show a compensation effect for radiation damage; another example is the usage of
627 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage
628 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p
629 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be
630 placed near the diode.

631 Appendix B

632 FLASH radiotherapy

633 La radioterapia si usa nel 60 per cento dei pazienti, sia come cura che come trattamento palliativo.
634 Si associa spesso ad altre cure e si può fare prima/durante/dopo un intervento.

635

636 Si può fare in modi diversi: da dentro (brachytherapy) oppure da fuori (quella standard). Un
637 requisito importante è la delinazione del target (non vuoi rischiare di beccare i tessuti sani), per
638 cui prima tipicamente si fanno esami di imaginig del tumore. Tipicamente anche gli acceleratori
639 stessi per la terapia sono provvisti di radiografia.

640 Un problema dei fotoni ad esempio è che il loro rilascio di dose è lineare, per cui danneggia
641 anche i tessuti sani. Il problema dei protoni invece è che hanno un picco troppo stretto per cui non
642 puoi coprire grosse zone e soprattutto se sbagli rischi davvero di danneggiare molto i tessuti sani.

643

644 B.1 Cell survival curves

645 Curva di efficacia del trattamento in funzione della dose:

$$\frac{S(D)}{S(0)} = e^{-F(D)} \quad (\text{B.1})$$

646 dove $F(D)$

$$F(D) = \alpha D + \beta D^2 \quad (\text{B.2})$$

647 dove α e β rappresentano due tipi di danno diversi: coefficients, experimentally determined, characterizing the radiation response of cells. In particular, alpha represents the rate of cell killing by single ionizing events, while beta indicates the maximal rate of cell killing by double hits observed when the repair mechanisms do not activate during the radiation exposure. Si ottiene una curva di sopravvivenza dove si vede la possibilità delle cellule di autoripararsi. A basse dosi infatti le cellule possono ripararsi.

653

654 Per introdurre l'effetto FLASH introduco prima la therapeutic window.

655

656 TCP è la tumor control Probability che indica la probabilità delle cellule del tumore di essere uccise dopo una certa dose (con in riferimento a dose in acqua)

657 Se una media di $\mu(D)$ di cellule di tumore are killed con una dose D , la probabilità che n cellule sopravvivono è data da $P(n|\mu)$ poisson:

$$P(n|\mu) = \frac{\mu(D)^n e^{-\mu(D)}}{n!} \quad (\text{B.3})$$

$$TCP(D) = P(n=0|\mu(D)) = e^{-\mu(D)} \quad (\text{B.4})$$

660 D'altra parte hai una probabilità di fare danno su normal tissue NTCP Normal Tissue Complication Probability, che rappresenta il problema principale e che limita la massima radiazione erogabile
661 Una scelta bilanciata si applica guardando a questi due fattori; si usa il therapeutic index definito
662 come TCP/NTCP.

664 La cosa ottimale è ampliare la finestra del therapeutic ratio.

665
666 CONV-RT 0.01-5 Gy/min. A typical RT regime today consists of daily fractions of 1.5 to 3
667 Gy given over several weeks.

668 Nell Intra operative radiation therapy (IORT), where they reach values respectively about 20 and
669 100 times greater than those of conventional radiation therapy.

670 FLASH vuole ultrahigh mean dose-rate (maggione di 40 Gy/s) in modo da ridurere anche il
671 trattamento a meno di un secondo.

672

673 **B.2 FLASH effect**

674 Ci sono due effetti che affect the flsh effect and la sua applicabilità: Dose rate effect e oxygen

675

676 Cellule che esibiscono hypoxia (cioè cellule che non hanno ossigeno sono radioresistenti); al
677 contrario normoxia e physoxia non lo sono. la presenza di ossigeno rende la curva steeper indicando
678 che lo stesso danno si raggiunge a livelli di dose più bassi rispetto al caso senza ossigeno.

679 FIGURA con una curva a confronto con e senza ossigeno.

680 Typically, the OER is in the order of 2.5–3.5 for most cellular systems

681 Quindi si vogliono sfruttare questi effetti per diminuire la tossicità sui tessuti sani

682

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