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⁴⁰ **Chapter 1**

⁴¹ **Introduction**

⁴² Pixel detectors, members of the semiconductor detector family, have significantly been used since
⁴³ () at the first accelerator experiments for energy and position measurement. Because of their
⁴⁴ dimension (today $\sim 30 \mu\text{m}$ or even better) and their spatial resolution ($\sim 5\text{-}10 \mu\text{m}$), with the
⁴⁵ availability of technology in 1980s they proved to be perfectly suitable for vertex detector in the
⁴⁶ inner layer of the detector.

⁴⁷ Technological development has been constant from then on and today almost every high energy
⁴⁸ physics (HEP) experiment employs a pixels detector; hybrid pixel currently constitute the state-
⁴⁹ of-art for large scale pixel detector but experiments began to look at the more innovative monolithic
⁵⁰ active pixels (MAPS) as perspective for their future upgrades, as BelleII, or they already have
⁵¹ installed them, as ALICE.

⁵² Requirement imposed by accelerator are stringent and they will be even more with the increase
⁵³ of luminosity/intensity, in terms of radiation hardness, efficiency and occupancy, time resolution,
⁵⁴ material budget and power consumption.

⁵⁵ Qual è invece la richiesta per la dosimetria?

⁵⁶ While CCDs pioneered the use of silicon pixels for precision tracking,

⁵⁸ **Chapter 2**

⁵⁹ **Pixel detectors**

⁶⁰ **2.1 Signal formation**

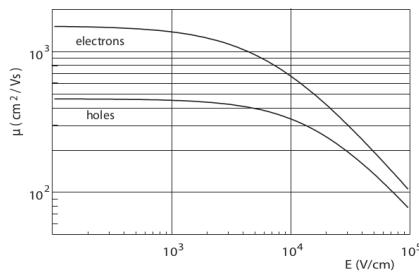
⁶¹ When a charge particle passes through a pixel and loses energy by ionization a part of that
⁶² energy is used to generate electron-hole pairs (another part is used for other processes, as the
⁶³ lattice excitation) which are then separated by the electric field and collected at their respectively
⁶⁴ electrodes (p for holes and n for electrons)¹; by the drift of these charges, a signal i_e is generated
⁶⁵ on the electrode e as stated by the Shockley–Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (2.1)$$

⁶⁶ where $v(t)$ is the instantaneous velocity of the charge q and E_{WF} is the weighting field, that is the
⁶⁷ field obtained biasing the electrode e with 1V and all the others with 0V. The drift velocity of the
⁶⁸ charge depends on the electric field and on the mobility of the particle:

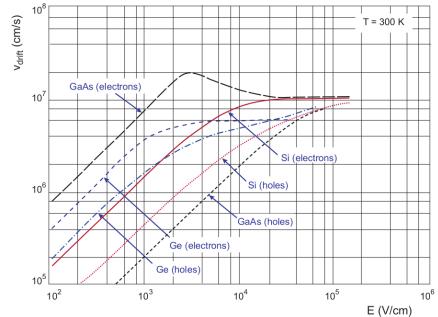
$$v = \mu(E) E \quad (2.2)$$

⁶⁹ where $\mu(E)$ is a function of the electric field and is linear with E only for small E : at higher values
⁷⁰ the probability of interactions with optical phonons increases and the mobility drops and this leads
⁷¹ to an independence of the velocity from the electric field (fig. 2.1b).



(a) Typical values for electrons and holes mobility in

silicon at room temperature are $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$, $\mu_h = 500$



(b) Drift velocity at room temperature in different semiconductors

⁷² The average energy needed to create a pair at 300 K in silicon is $w_i = 3.65 \text{ eV}$, that is more
⁷³ than the mean ionization energy because of the interactions with phonon, since for a minimum
⁷⁴ ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is
⁷⁵ 0.28 keV/ μ , hence the number of e/h pairs is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (2.3)$$

¹Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout

76 CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALEMTE SI AGGIUNGE IL
77 FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. IL FATTORE DI FANO È
78 0.115 NEL SILICIO. ecc

79 It is fundamental that pairs e/h are produced in the depleted region of the semiconductor where
80 the probability of recombination with charge carriers is low to avoid loss of signals. Pixel detectors
81 are then commonly reverse biased: a positive bias is given to the n electrode and a negative to the
82 p to grow the depletion zone in the epitaxial layer below the electrode. The width of the depletion
83 region is related with the external bias V_{ext} , the resistivity ρ and also with the dopant:

$$d_n \sim 0.55 \sqrt{\frac{\rho}{\Omega cm} \frac{V_{ext}}{V}} \mu m \quad 85 \quad (2.4)$$
$$d_p \sim 0.32 \sqrt{\frac{\rho}{\Omega cm} \frac{V_{ext}}{V}} \mu m \quad 86 \quad (2.5)$$

87 For that reason high resistivity wafers ($100 \Omega cm - k\Omega cm$) are typically preferred because they
88 allow bigger depletion zone with smaller voltage bias. Metto il disegno "standard" di una giunzione

89 2.2 CCDs

90 descrivi come sono fatte e come funziona il readout Tens of ms due to the need to transfer the
91 charge signals pixel by pixel through a single output circuit For photon imaging the need of high
92 assorbtion efficiency, per cui usi materiali con alto Z

93 2.3 Hybrid pixels

94 METTI IN EVIDENZAZ CHE PUOI FARE UN READOUT CON TECNOLOGIA CMOS. Metti
95 in evidenza che sono più veloci Hybrid pixels are made of two parts (fig. 2.2a), the sensor and the
96 electronics: for each pixel these two parts are welded together through microconnection (bump
97 bond).

98 They provide a practical system where readout and sensor can be optimized separately, although
99 the testing is less easy-to-do since the sensor and the R/O must be connected together before.

100 In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-
101 cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high
102 levels of radiation, and also expensive.

103 A critical parameter for accelerator experiments is the material budget, which represents the main
104 limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are
105 thicker (\sim hundreds of μm) than monolithic ones (even less than $100 \mu m$), using the latter the
106 material budget can be down by a third: typical value for hybrid pixels is 1.5 % X_0 per layer,
107 while for monolithic 0.5 % X_0 .

108 Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,
109 by the way, a bigger cooling system leading in turn to an increase in material too.

110 DEPFET are the first attempt towards the integration of the front end (FE) on the sensor bulk:
111 they are typically mounted on a hybrid structure but they also integrate the first amplification
112 stage.

113 Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor
114 (a p-channel in fig. 2.2b): an hole current flows from source to drain which is controlled by the
115 external gate and the internal gate together. The internal gate is made by a deep n+ implant
116 towards which electrons drift after being created in the depletion region (to know how the signal
117 is created in a pixel detector look at appendix A); the accumulation of electrons in the region
118 underneath the n implant changes the gate potential and controls the transistor current.

119 DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and
120 the large depletion region. But, since they need to be connected with ASIC the limiting factor still
121 is the material budget.

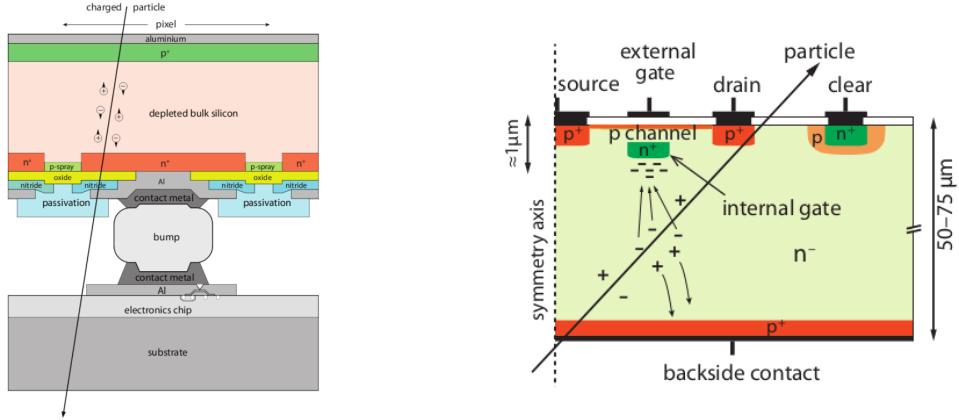


Figure 2.2: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

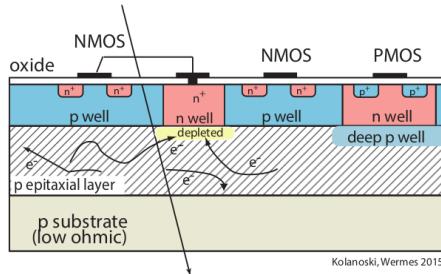


Figure 2.3: Concept cross-section of CMOS MPAS pixel

2.4 CMOS MAPS and DMPAS

With respect to CCDs, the radiation tolerance could be greatly increased by sensing the signal charge within its own pixel, instead of transporting it over thousands of pixels. The readout speed could also be dramatically increased by in-pixel amplitude discrimination, followed by sparse readout of only the hit pixels. Monolithic active pixels accommodate on the same wafer both the sensor and the front end electronics, with the second one implanted on top within a depth of about 1 μm below the surface.

MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the development of the electronic sector which guarantees the decrease in CMOS transistors dimension at least every two years, as stated by the Moore's law².

As a matter of fact the dimension of components, their organization on the pixel area and logic density are important issues for the design and for the layout; typically different decisions are taken for different purposes.

Monolithic active pixel can be distinguished between two main categories: MAPS and depleted MAPS (DMPAS).

MAPS (figure a 2.3) have typically an epitaxial layer in range 1-20 μm and because they are not depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the collection could be partial especially after the irradiation of the detector (look at A for radiation damages), when the trapping probability become higher.

In figure 2.3 is shown as example of CMOS MAPS: the sensor in the scheme implements an n well as collection diode; to avoid the others n wells (which contain PMOS transistors) of the electronic circuit would compete in charge collection and to shield the CMOS circuit from the substrate, additionally underlying deep p well are needed. DMPAS are instead MAPS depleted with d typically in $\sim 25\text{-}150 \mu\text{m}$ (eq. 2.1) which extends from the diode to the deep p-well, and sometimes also to the backside (in this case if one wants to collect the signal also on this electrode, additional process must be done).

²Moore's law states that logic density doubles every two years.

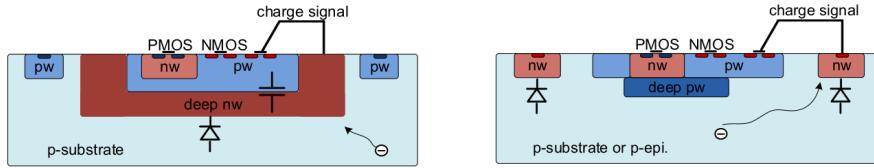


Figure 2.4: Concept cross-section with large and small fill factor

150 2.4.1 DMAPS: large and small fill factor

151 There are two different sensor-design approaches (figure 2.4) to DMAPS:

- 152 • large fill factor: a large collection electrode that is a large deep n-well and that host the
153 embedded electronics
- 154 • small fill factor: a small n-well is used as charge collection node

155 To implement a uniform and stronger electric field, DMAPS often uses large electrode design that
156 requires multiple wells (typically four including deep n and p wells); this layout adds on to the
157 standard terms of the total capacity of the sensor a new term (fig. 2.5), that contributes to the
158 total amplifier input capacity. In addition to the capacity between pixels (C_{pp}) and between the
159 pixel and the backside (C_b), a non-negligible contribution comes from the capacities between wells
160 (C_{WW} and C_{SW}) needed to shield the embedded electronics. These capacities affect the thermal
161 and 1/f noise of the charge amplifier and the τ_{CSA} too:

$$ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.6) \quad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.7)$$

163 where g_m is the transconductance, τ_{sh} is the shaping time.

164 Among the disadvantages coming from this large input capacity could be the coupling between
165 the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring
166 electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this problem
is especially connected with the intra wells capacities. So, larger charge collection electrode

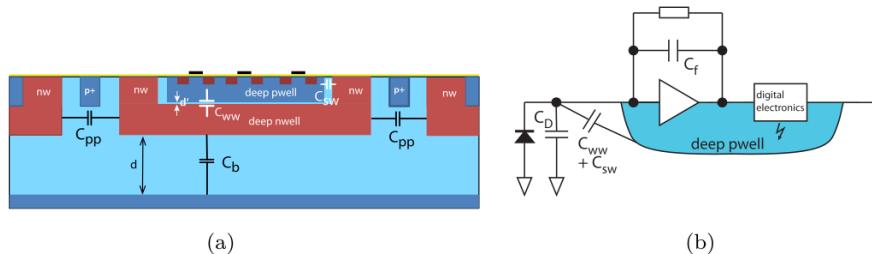


Figure 2.5: C_{pp} , C_b , C_{WW} , C_{SW}

167 sensors provide a uniform electric field in the bulk that results in short drift path and so in good
168 collection properties, especially after irradiation, when trapping probability can become an issue.
169 The drawback of a large fill-factor is the large capacity (~ 100 fF): this contributes to the noise
170 and to a speed penalty and to a larger possibility of cross talk.

172 The small fill-factor variant, instead, benefits from a small capacity (5-20 fF), but suffers from
173 a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando dei
174 MAPS, devo ripetere qui?**

175 As we'll see these two different types of sensor require different amplifier: the large electrode one is
176 coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.5.1).

177 2.4.2 A modified sensor

178 A process modification developed by CERN in collaboration with the foundries has become the
179 standard solution to combine the characteristics of a small fill factor sensor (small input amplifier

	small fill factor	large fill factor
small sensor C	✓ (< 5 fF)	✗ (~ 100-200 fF)
low noise	✓	✗
low cross talk	✓	✗
velocity performances	✓	✗ (~ 100 ns)
short drift paths	✗	✓
radiation hard	✗	✓

Table 2.1: Small and large fill factor DMAPS characteristics

capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE upgrade about ten years [1].

A compromise between the two sensors could also be making smaller pixels, but this solution requires reducing the electronic circuit area, so a completely new pixel layout should be though. The modification consists in inserting a low dose implant under the electrode and one its advantage lies in its versatility: both standard and modified sensor are often produced for testing in fact.

Before the process modification the depletion region extends below the diode towards the substrate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.6). After, two distinct pn junctions are built: one between the deep p well and the n^- layer, and the other between the n^- and the p^- epitaxial layer, extending to the all area of the sensor. Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes can be biased separately³ and this is beneficial to enhance the vertical electric field component. The doping concentration is a trimmer parameter: it must be high enough to be greater than the epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be lower enough to allow the depletion without reaching too high bias.

2.5 Analog front end

After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.7), ready to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an efficient, high-speed readout architecture, consuming as low power as possible must be provided by the readout integrated electronics (ROIC).

Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually often is the only amplification stage) with a reset to the baseline mechanism and a leakage current compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise before the amplification stage in order to not multiply that noise, and chose a reasonable threshold of the discriminator to cut noise-hits much as possible.

2.5.1 Preamplifier

Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled as an operational amplifier (OpAmp) where the gain is determined by the input and feedback impedance (first step in figure 2.7):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.8)$$

Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor MAPS whose signal is already enough high: $v_{in} = Q/C_D \approx 3fC/100 \text{ pF} = 0.03 \text{ mV}$, but it's fine for the small fill factor ones: $v_{in} = Q/C_D \approx 3fC/3 \text{ pF} = 1 \text{ mV}$.

In the case of a resistor feedback, if the signal duration time is longer than the discharge time ($\tau = R_S C_D$) of the detector the system works as current amplifier, as the signal is immediately

³This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

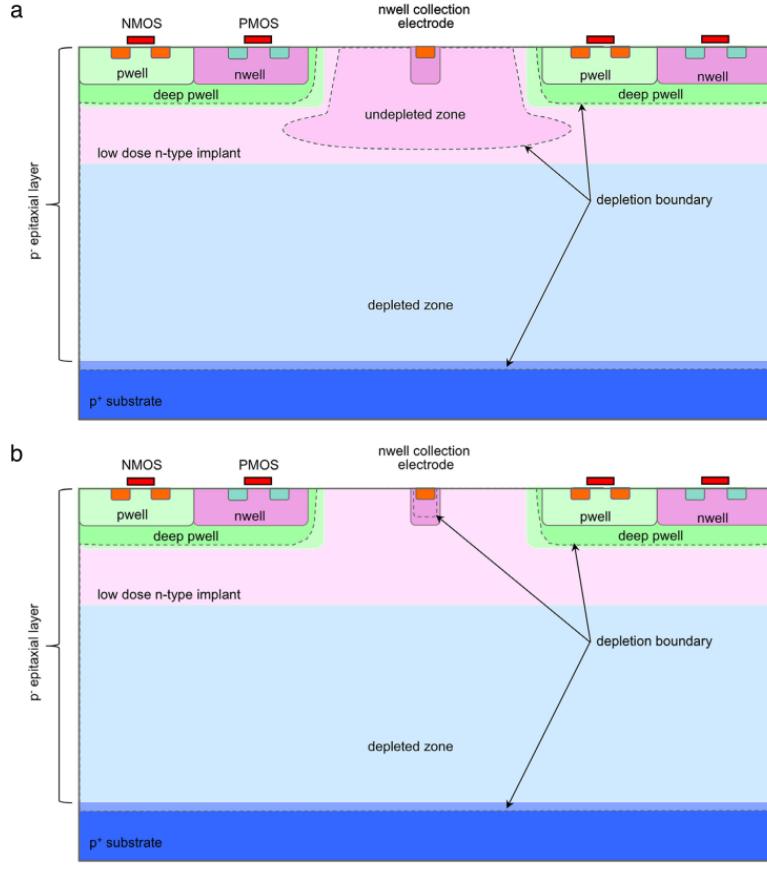


Figure 2.6: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

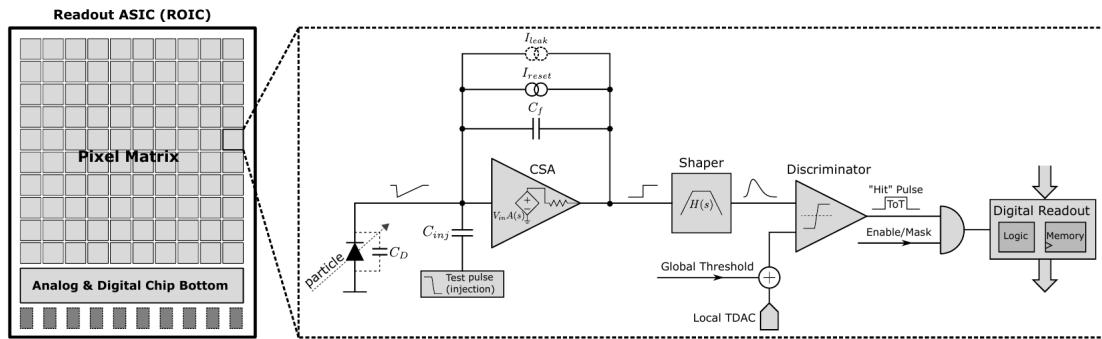


Figure 2.7: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

217 trasmit to the amplifier; in the complementary case (signal duration longer than the discharge
 218 time) the system integrates the current on the C_D and operates as a voltage amplifier.

219 2.6 Readout logic

220 Readout logic includes the part of the circuit which takes the FE output signal, processes it and
 221 then transmit it out of pixel and/or out of chip; depending on the situation of usage different
 222 readout characteristics must be provided.

223 To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers
 224 and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really
 225 high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is
 226 recorded).

227 A common compromise often made is to save the time over threshold (ToT) of the pulse in clock
 228 cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen
 229 bits but, being correlated and hopefully being linear with the deposited charge by the impinging
 230 particle in the detector, it provides a sufficient information. The ToT digitalization usually takes
 231 advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels' matrix.
 232 The required timing precision is at least around 25 ns, that corresponds to the period of
 233 bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is
 234 40 MHz.

235 Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they
 have been read, and then the ToT is obtained from their difference.

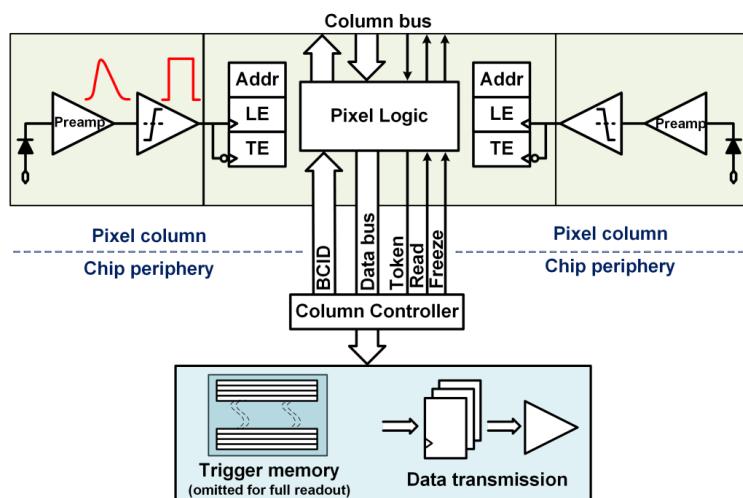


Figure 2.8: Column drain R/O scheme where ToT is saved

236 Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger
 237 system decides if the hit must be stored or not. On one hand the triggered-readout needs buffers
 238 and storage memories, on the other the full readout, because there is no need to store hit data on
 239 chip, needs an high enough bandwidth.

240 A triggered readout is fundamental in accelerator experiments where the quantity of data to store
 241 is too large to be handled, and some selections have to be applied by the trigger: to give an order
 242 of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100
 243 MBit/s [2] (pag. 797).

244 Typically the trigger signal is processed in a few μs , so the pixel gets it only after a hundred clock
 245 cycles from the hit arrival time: the buffer depth must then handle the higher trigger latency.

246 After having taken out the data from the pixel, it has to be transmitted to the end of column
 247 (EoC) where a serializer delivers it out of chip, typically to an FPGA.

248 There are several ways of transmitting data from pixel to the end of column: one of the most
 249 famous is the column-drain read out, developed for CMS and ATLAS experiments [3]. All the
 250 pixels in a double-column share a data bus and only one pixel at a time, according to a priority
 251 chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit

arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored on a RAM until the SH does not allow the access to memory by data bus.
Even if many readout architectures are based the column-drain one, it doesn't suit for large size matrices. The problem is that increasing the pixels on a column would also raise the number of pixels in the priority chain and that would result in a slowdown of the readout.

If there isn't any storage memory, the double-column behaves as a single server queue and the probability for a pixel of waiting a time T greater than t , with an input hit rate on the column μ and an output bandwidth B_W is [4]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.9)$$

To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time τ due to the AFE), for example imposing $P(T > t) \sim 0.001$, one obtains $(B_W - \mu) t_t \sim 6$, where t_t is the time needed to transfer the hit; since t_t is small, one must have $B_W \gg \mu$, that means a high bandwidth [4].

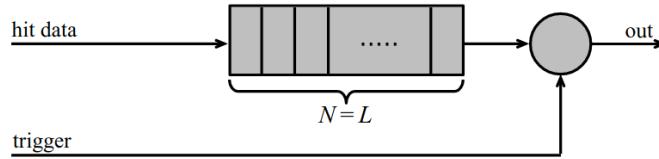


Figure 2.9: Block diagram of a pipeline buffer: N is the dimension of memory buffer and L is the trigger latency expressed in BCID cycles

Actually the previous one is an approximation since each pixel sees a different bandwidth depending on the position on the queue: the first one sees a full bandwidth, but the next sees a smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen by the pixel i is $B_i = B - \sum_j \mu_j$, where μ_j is the hit rate of the j th pixel.
The efficiency requirement on the bandwidth and the hit rate becomes: $B_{W,i} > \mu_i$, where the index i means the constraint is for a single pixel; if all the N pixels on a column have the same rate $\mu = N\mu_i$, the condition reduces to $B_W > \mu$. The bandwidth must be chosen such that the mean time between hits of the last pixel in the readout chain is bigger than that.

In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed; this means that only information from channels where the signal exceeds the discriminator threshold are stored. Qualcosa sulla zero suppression? La metto qui questa affermazione?

If instead there is a local storage until a trigger signal arrives, the input rate to column bus μ' is reduced compared to the hit rate μ as: $\mu' = \mu \times r \times t$, where r is the trigger rate and t is the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth, but the limiting factor is the buffer depth: the amount of memory designed depends both on the expected rate μ and on the trigger latency t as $\propto \mu \times t$, that means that the higher the trigger latency and the lower the hit rate to cope with.

In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels into regions with shared storage. Let's compare two different situations: in the first one a buffer is located on each pixel area, while in the second one a core of four pixels share a common buffer (this architecture is commonly called FE-I4).

Consider a 50 kHz single pixel hits rate and a trigger latency of 5 μs , the probability of losing hits is:

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.10)$$

where I have assumed a Poissonian distribution with mean $\nu = 0.25$ to describe the counts N.

To get an efficiency ϵ greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.11)$$

Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four pixels the mean number of hits per trigger latency is $\nu = 0.25 \times 4 = 1$. To get an efficiency of 99.9% (eq. 2.11) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

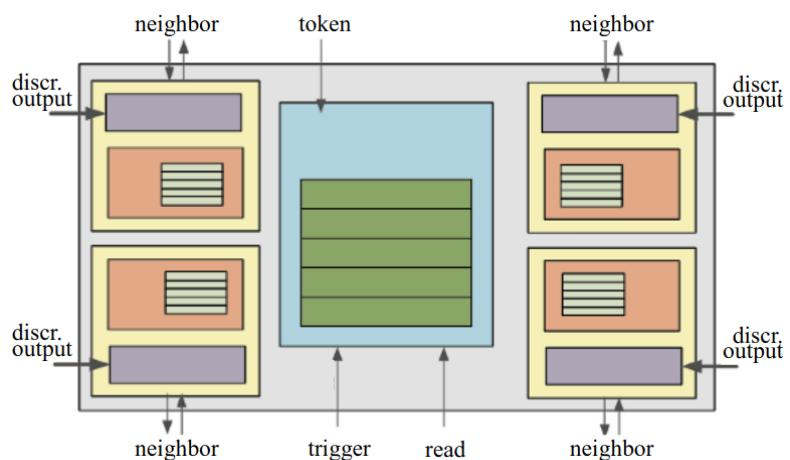


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is highlighted in light blue; latency counters and trigger management section are highlighted in green; hit processing blocks are highlighted in purple; ToT counters and ToT management units are highlighted in orange

293 **Chapter 3**

294 **Use of pixel detectors**

295 There always was a tight relation between the development of cameras and pixel detectors since
296 1969, when the idea of CCDs, thanks to whom Boyle and Smith were awarded the Nobel Prize in
297 Physics in 2009, revolutionized photography allowing light to be captured electronically instead of
298 on film. Even though the CMOS technology was already known when CCDs spread, the costs of
299 productions were too high to allow the diffusion of these sensors for which needed to wait until
300 1990s. From that period on, the fast diffusion of CMOS was mainly due to the less cost than CCD,
301 and the less power required for supply.

302 The principal use cases of pixel detectors are particle tracking and imaging: in the former case
303 individual charged particles have to be identified, in the latter instead an image is obtained by
304 the usually un-triggered accumulation of the impinging radiation. Also the demands on detectors
305 performance depends on their usage, in particular tracking requires high spatial resolution, fast
306 readout and radiation hardness.

307 **3.1 Tracking in HEP**

308 Historically, the first pixel detector employed in particle physics was a CCD: it was installed in
309 the spectrometer at the CERN's Super Proton Synchrotron (SPS) by the ACCMOR Collaboration
310 (Amsterdam, CERN, Cracow, Munich, Oxford, RAL) at mid 1980s, with the purpose of studying
311 the recently-discovered charm particles. The second famous usage of CCDs took place at SLAC
312 in the Large Detector (SLD) during the two years 1996-98. From that period on particle tracking
313 in experiments have been transformed radically: it was mandatory for HEP experiments to build
314 an inner vertex detector. In 1991, the more demanding environments led to the development of hy-
315 brid pixel detectors: a dedicated collaboration, RD19, was established at CERN with the specific
316 goal to define a semiconductor micropattern detector with an incorporated signal processing at a
317 microscopic level. In those years a wide set of prototypes of hybrid pixel has been manufactured;
318 among the greatest productions a mention goes to the huge ATLAS and CMS vertex detectors.
319 From the middle of 2013 a second collaboration, RD 53, has been established with the new goal
320 to find a pixel detector suitable for phase II future upgrades of those experiments. Even if the col-
321 laboration is specifically focused on design of hybrid pixel readout chips (aiming to 65 nm technique
322 so that the electronics fits within the pixel area), also other options have been taken in account
323 and many test have been done on MAPS for example. Requirements imposed by HL-LHC will
324 become higher in time: for example, a dose and radiation of 5 Mrad and 1016NIEL are expected
325 after 5 years of operation. Time resolution, material budget and power consumption are also issues
326 for the upgrade: a time resolution better than 25 ns for a bunch crossing frequency of 40 MHz, a
327 material budget lower than 2% and a power consumption lower than 500 mW/cm² are required.

328 Amidst the solutions proposed 3D silicon detector, invented by Sherwood Parker in 1995, and
329 MAPS are the most promising. In 3D sensors the electrode is a narrow column of n-type implanted
330 vertically across the bulk instead of being implanted on the wafer's surface. The charge produced
331 by the impinging particle is then drifted transversally within the pixel, and, as the mean path
332 between two electrode can be sufficient low, the trap probability is not an issue. 3D pixels have
333 been already proved in ATLAS tracker [quando?](#). Even if 3D detector are adequately radiation hard,
334 MAPS architecture looked very promising from the beginning: they overcome both the CCDs long
335 reading time and the hybrid problems (I have already explained in section ?? the benefits of

336 MAPS). Experiments such as ALICE at LHC and STAR at RHIC have already introduced the
337 CMOS MAPS technology in their detectors. ALICE Tracking System (ITS2), upgraded during the
338 LHC long shut down in 2019-20, was the first large-area ($\sim 10 \text{ m}^2$ covered by 2.5 Gpixels) silicon
339 vertex detector based on CMOS MAPS.

340 3.1.1 Hybrid pixels at LHC: ATLAS, CMS and LHC-b

341 **ATLAS**

342 With CMS, ATLAS is one of two general-purpose detectors at the LHC and has the largest volume
343 detector ever constructed for a particle collider (46 m long and 25 m in diameter). The Inner
344 Detector consists of three different systems all immersed in a magnetic field parallel to the beam
345 axis whose main components are: the pixel, the micro-strips and transition radiation trackers.
346 Concerning the pixel detector, 92 million pixels are divided in 4 barrel layers and 3 disks in each
347 end-cap region, covering a total area of 1.9 m^2 and having a 15 kW of power consumption.

348 As stated by the ATLAS collaboration the pixel detector is exposed by an extreme particle
349 flux: "By the end of Run 3¹, the number of particles that will have hit the innermost pixel layers
350 will be comparable to the number it would receive if it were placed only a few kilometres from
351 the Sun during a solar flare". Considering that the particle density will increase even more with
352 HL-LHC, radiation hardness is definitively target to achieve.

353 The most ambitious goal is employ a MAPS-based detector for the inner-layer barrels, and for
354 this reason the RD53 collaboration is performing many test on MAPS prototypes, as Monopix of
355 which I will talk about in section ??.

356 Up to now this possibility will be eventually implemented during the second phase of the HL-
357 LHC era, as at the start of high-luminosity operation the selected option is the hybrid one. The
358 sensor will be bonded with ITkPix, the first full-scale 65 nm hybrid pixel-readout chip developed
359 by the RD53 collaboration. Regarding the sensor, a valuable option is using 3D pixels, which
360 have already proved themselves in ATLAS, for the insertable B layer (IBL).qualcosa in più sui 3d.
361 The number of pixels will be increased of a factor about 7, passing from 92 millions to 6 billion.

362 **CMS**

363 **Da scrivere LHCb**

364 LHCb is a dedicated heavy-flavour physics experiment that exploits pp interactions at 14 TeV at
365 LHC. It was the last experiment to upgrade the vertex detector, the Vertex Locator (VELO),
366 replacing the silicon-strip with pixels in May 2022. As the instantaneous luminosity in Run3 is
367 increased by a factor $\lesssim 10$, much of the readout electronics and of the trigger system have been
368 developed in order to cope with the large interaction rate. To place the detector as close as possible
369 to the beampipe and reach a better track reconstruction resolution, the VELO has a surprising
370 feature: it can be moved. During the injection of LHC protons it is parket at 3 cm from the beams
371 and only when the stability is reach it is brought at ~ 5 mm. Radiation hardness as well as readout
372 speed are then a priority for the detectors: that's why the collaboration opted for a hybrid system.
373 The Velopix is made bonding sensors, each measuring 55×55 micrometers, $200 \mu\text{m}$ -thick to a
374 $200 \mu\text{m}$ -thick ASIC specially developed for LHCb and coming from the Medipix family (sec. ??),
375 which can handle hit rates up to 900 MHz per chip. Since the detector is operated under vacuum
376 near the beam pipe, the heat removal is particularly difficult and evaporative CO₂ microchannel
377 cooling are used.

378 3.1.2 A DEPFET example: Belle-II

379 **da scrivere**

380 3.1.3 CMOS MAPS: ALICE and STAR

381 **ALICE**

382 ALICE (A Large Ion Collider Experiment) is a detector dedicated to heavy-ion physics and to the
383 study of the condensed phase of the chromodynamics at the LHC. The tracking detector consists of
384 the Inner Tracking System (ITS), the gaseous Time Projection Chamber (TPC) and the Transition

¹Run 3 start in June 2022

385 Radiation Detector (TRD), and all those are embedded in a magnetic field of 0.5 T. The ITS is
386 made by six layers of detectors, two for each type, from the interaction point outwards: Silicon
387 Pixel Detector (SPD), Silicon Drift Detector (SDD) and Silicon Strip Detector (SSD). Contrary
388 to the others LHC experiments, ALICE tracker in placed in a quite different environments: the
389 expected dose is smaller by two order of magnitude and the rate of interactions is few MHz instead
390 of 40 MHz, but the number of particles comes out of each interaction is higher (the SPS is invested
391 by a density of particles of $\sim 100 \text{ cm}^{-2}$). The reconstruction of very complicated events whit a
392 large number of particle is a challenge, hence to segment and to minimize the amount of material,
393 which may cause secondary interaction complicating futher the event topology, is considered a
394 viable strategy. Thanks to the reduction of the material budget, ITS2, which uses the ALPIDE
395 chip developed by ALICE collaboration, obtained an amazing improvement both in the position
396 measurement and in the momentum resolution, improving the efficiency of track reconstruction
397 for particle with very low transverse momentum (by a factor 6 at $pT \sim 0.1 \text{ GeV}/c$). Further
398 advancements in CMOS MAPS technology are being aggressively pursued for the ALICE ITS3
399 vertex detector upgrades (foreseen around 2026-27), with the goals of further reducing the sensor
400 thickness and improving the readout speed of the devices, while keeping power consumption at a
401 minimum.

402 STAR

403 MIMOSA-28 devices for the first MAPS-based vertex detector: a 356 Mpixel two-layer barrel
404 system for the STAR experiment at Brookhaven's Relativistic Heavy Ion Collide **da scrivere**

405 3.2 Applications in imaging

406 frase introduttiva (?). Magari qualcosa tipo: Per l'imaging si possono usare o come integratori di
407 carica (ad esempio si integra la carica rilasciata da più fotoni) oppure come contatori. In questo
408 secondo caso l'utilizzo e l'elettronica utilizzata per leggerli assomiglia all'utilizzo agli acceleratori,
409 anche se i requirements sono molto meno stringenti. Dato che l'utilizzo per l'imaging e per i trac-
410 ciatori può non essere molto diverso, two noteworthy of microchips originally meant for detectors
411 in particle physics at the LHC, and later employed in other fields are Medipix and Timepix. They
412 are read-out chips developed by the Medipix Collaborations since early 1990s. For two decades,
413 different Medipix generations have been produced, having a rough correlation with the feature
414 size used: Medipix2 (1999) used 250 nm feature size CMOS while Medipix3 (2005) 130 nm. The
415 aim of the fourth collaboration (2016), instead, is designing pixel read-out chips that prepared
416 for **TSV processing and may be tiled on all four sides. DOVREI METTERE DUE RIGHE SU**
417 **TSV OPPURE TAGLIARE.** For photons imaging other materials with higher atomic charge than
418 silicon could be prefered, as a high photon absorption efficiency is needed: it was for this reason
419 that Medipix2 was bump bonded to identically segmented sensors of both silicon and GaAs.

420 The applications in scientific imaging vary from astrophysics and medical imaging to more exotic
421 domains as studies of protein dynamics, art authentication and dosimetry. The most important
422 employment of Medipix is as X-ray single photon counting in industrial and medical radiography
423 and in 3D computed tomography. Thanks to a New-Zealand company, the MARS Bioimaging
424 detector has been fabricated, which is capable of resolving the photons energy and produce 3D
425 coloured images. Besides tracking in HEP (I have already cited the use of Timepix3 is in the
426 beam telescope of the LHCb VELO), a important use of Timepix is in dosimetry **Timepix Detector**
427 **for Imaging in Ion Beam Radiotherapy- aggiungi qualche info** A small-Timepix detector with the
428 dimension of a USB can also be found at the International Space Station, where it is exploited for
429 radiation, principally made of heavy-ion, monitoring.

430 3.2.1 Applicability to FLASH radiotherapy

431 **DA QUI IN POI IN QUESTO CAPITOLO CI SONO APPUNTI A CASO, DA RIORDINARE E**
432 **TRADURRE**

433 The radiological treatment is a common method used in 60% of tumors both as palliative
434 care and as treatment. It can be given before, after or during a surgery, **per cosa sta iort** IORT.
435 Moreover many different types of radiations can be used to irradiate the affected tissues; high
436 energy photons

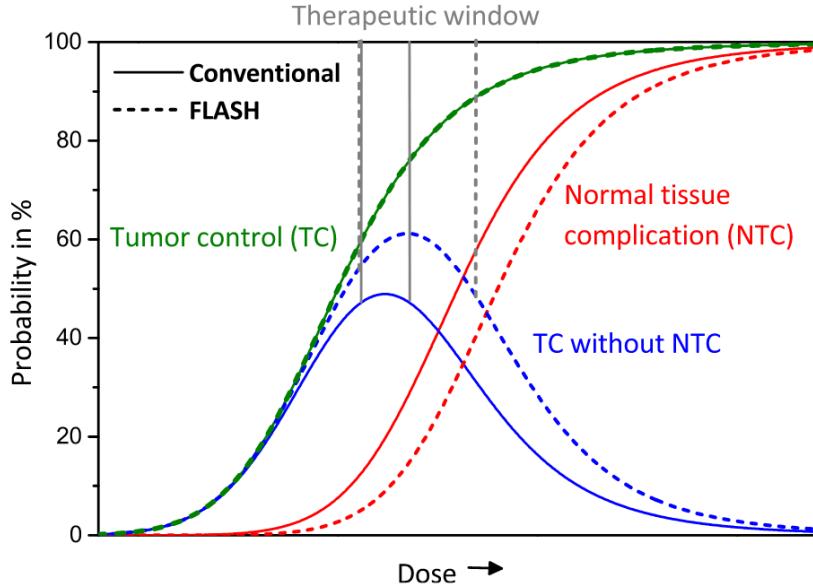


Figure 3.1

437 Un problema dei fotoni ad esempio è che il loro rilascio di dose è lineare, per cui danneggi
 438 anche i tessuti sani. Il problema dei protoni invece è che hanno un picco troppo stretto per cui non
 439 puoi coprire grosse zone e soprattutto se sbagli rischi davvero di danneggiare molto i tessuti sani.

440
 441 Curva di efficacia del trattamento in funzione della dose: The surviving fraction probability is
 442 de

$$\frac{S(D)}{S(0)} = e^{-F(D)} \quad (3.1)$$

443 dove $F(D)$

$$F(D) = \alpha D + \beta D^2 \quad (3.2)$$

444 dove α e β rappresentano due tipi di danno diversi: coefficients, experimentally determined, char-
 445 acterizing the radiation response of cells. In particular, alpha represents the rate of cell killing by
 446 single ionizing events, while beta indicates the maximal rate of cell killing by double hits observed
 447 when the repair mechanisms do not activate during the radiation exposure. Si ottiene una curva
 448 di sopravvivenza dove si vede la possibilità delle cellule di autoripararsi. A basse dosi infatti le
 449 cellule possono ripararsi.

450
 451 Per introdurre l'effetto FLASH instroduco prima la therapeutic window.

452
 453 TCP è la tumor control Probability che indica la probabilità delle cellule del tumore di essere
 454 uccise dopo una certa dose (con riferimento a dose in acqua)

455 Se una media di $\mu(D)$ di cellule di tumore sono uccise con una dose D , la probabilità che n cellule
 456 sopravvivono è data da $P(n|\mu)$ poisson:

$$P(n|\mu) = \frac{\mu(D)^n e^{-\mu(D)}}{n!} \quad (3.3)$$

$$TPC(D) = P(n=0|\mu(D)) = e^{-\mu(D)} \quad (3.4)$$

457 D'altra parte hai una probabilità di fare danno su normal tissue NTCP Normal Tissue Compli-
 458 cation Probability, che rappresenta il problema principale e che limita la massima radiazione erogabile
 459 Una scelta bilanciata si applica guardando a questi due fattori; si usa il therapeutic index definito
 460 come $TCP/NTCP$.

461 La cosa ottimale è ampliare la finestra del therapeutic ratio.

462

463 CONV-RT 0.01-5 Gy/min. A typical RT regime today consists of daily fractions of 1.5 to 3
464 Gy given over several weeks.

465 Nell Intra operative radiation therapy (IORT), where they reach values respectively about 20 and
466 100 times greater than those of conventional radiation therapy.

467 FLASH vuole ultrahigh mean dose-rate (maggione di 40 Gy/s) in modo da ridurre anche il
468 trattamento a meno di un secondo.

469

470 Ci sono due effetti che affect the fish effect and la sua applicabilità: Dose rate effect e oxygen

471

- 472 • dose rate effect

- 473 • oxygen effect

474 Cellule che esibiscono hypoxia (cioè cellule che non hanno ossigeno sono radioresistenti); al
475 contrario normoxia e physoxia non lo sono. la presenza di ossigeno rende la curva steeper indicando
476 che lo stesso danno si raggiunge a livelli di dose più bassi rispetto al caso senza ossigeno.

477 FIGURA con una curva a confronto con e senza ossigeno.

478 Typically, the OER is in the order of 2.5-3.5 for most cellular systems

479 Quindi si vogliono sfruttare questi effetti per diminuire la tossicità sui tessuti sani

480

⁴⁸¹ **Chapter 4**

⁴⁸² **TJ-Monopix1**

⁴⁸³ TJ-Monopix1 is a small electrode DMAPS with fast R/O capability, fabricated by TowerJazz
⁴⁸⁴ foundry in 180 nm CMOS imaging process. It is part, together with prototypes from other series
⁴⁸⁵ such as TJ-MALTA, of the ongoing R&D efforts aimed at developing DMAPS in commercial CMOS
⁴⁸⁶ processes, that could cope with the requirements at accelerator experiments. Both TJ-Monopix
⁴⁸⁷ and TJ-MALTA series [5], produced with the same technology by TowerJazz (the timeline of the
⁴⁸⁸ foundry products is shown in figure 4.1), are small electrode demonstrators and principally differ in
⁴⁸⁹ the readout design: while Monopix implements a column-drain R/O, an asynchronous R/O without
⁴⁹⁰ any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.



Figure 4.1: Timeline in TowerJazz productions in 180 nm CMOS imaging process

⁴⁹¹ Another Monopix series, but in 150 nm CMOS technology, has been produced by LFoundry [6].
⁴⁹² The main differences between the LF-Monopix1 and the TJ-Monopix1 (summarized in table 4.2),
⁴⁹³ lay in the sensor rather than in the readout architecture, as both chips implements a fast col-
⁴⁹⁴ umn drain R/O with ToT capability [7][8]. Concerning the sensors, either are based on a p-type
⁴⁹⁵ substrate, but with slightly different resistivities; in addition LFoundry pixels are larger, thicker
⁴⁹⁶ and have a large fill factor (the very deep n-well covers ~55% of the pixel area). The primary
⁴⁹⁷ consequence is that LF-Monopix1 pixels have a higher capacity resulting in higher consumption
⁴⁹⁸ and noise. As I discussed in section 2.4.1, the fact that LF-Monopix has a large fill factor electrode
⁴⁹⁹ is expected to improve its radiation hardness. Indeed, a comparison of the performance of the
⁵⁰⁰ two chips showed that TJ-Monopix suffers a comparatively larger degradation of efficiency after
⁵⁰¹ irradiation, due to the low electric field in the pixel corner; on the other hand, a drawback of the
⁵⁰² large fill factor in LF-Monopix is a significant cross-talk.

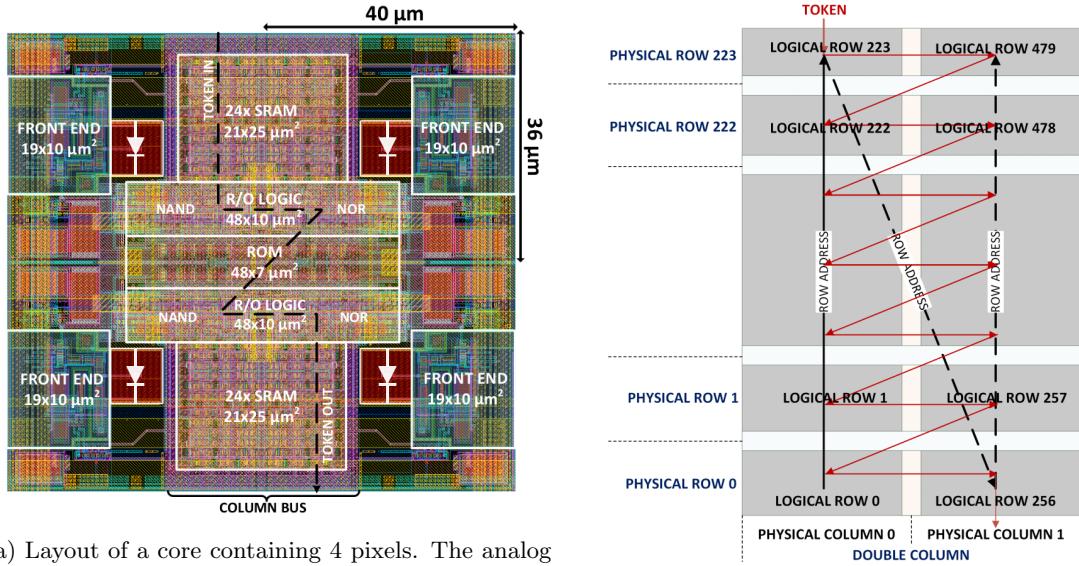
⁵⁰³ The TJ-Monopix1 chip contains, apart from the pixels matrix, all the required support blocks
⁵⁰⁴ used for configuration and testing:

- ⁵⁰⁵ the whole matrix contains 224×448 pixels, yielding a total active area approximately equal
⁵⁰⁶ to 145 mm^2 over a total area of $1 \times 2 \text{ cm}^2$;
- ⁵⁰⁷ at the chip periphery are placed some 7-bit Digital to Analog Converter (DAC), used to
⁵⁰⁸ generate the analog bias voltage and current levels and to configure the FE;

	LF-Monopix1	TJ-Monopix1
Resistivity	$>2\text{ k}\Omega\text{cm}$	$>1\text{ k}\Omega\text{cm}$
Pixel size	$50 \times 250\mu\text{m}^2$	$36 \times 40\mu\text{m}^2$
Depth	$100\text{-}750\mu\text{m}$	$25\mu\text{m}$
Capacity	$\sim 400\text{ fF}$	$\sim 3\text{ fF}$
Preamplifier	charge	voltage
Threshold trimming	on pixel (4-bit DAC)	global threshold
ToT	8 bits	6 bits
Consumption	$\sim 300\text{ mW/cm}^2$	$\sim 120\text{ mW/cm}^2$
Threshold	$1500 e^-$	$\sim 270 e^-$
ENC	$100 e^-$	$\sim 30 e^-$

Table 4.1: Main characteristics of Monopix1 produced by TowerJazz and LFoundry [7][8]

- 509 • at the EoC is placed a serializer to transferred datas immediately, indeed no trigger memory
 510 is implemented in this prototypes;
- 511 • the matrix power pads are distributed at the sides
- 512 • four pixels which have analog output and which can be monitored with an oscilloscope, and
 513 therefore used for testing
- 514 Pixels are grouped in 2×2 cores (fig. 4.2a): this layout allows to separate the analog and the
 515 digital electronics area in order to reduce the possible interference between the two parts. In
 516 addition it simplifies the routing of data as pixels on double column share the same column-bus to
 517 EoC. Therefore pixels can be addressed through the physical column/row or through the logical
 518 column/row, as shown in fig. 4.2b: in figure is also highlighted the token propagation path, whose
 519 I will discuss later.



(a) Layout of a core containing 4 pixels. The analog FE and the digital part are separated in order to reduce cross-talk be

(b)

520 4.1 The sensor

521 As already anticipated, TJ-Monopix1 has a p-type epitaxial layer and a n doped small collection
 522 electrode ($2\mu\text{m}$ in diameter); to avoid the n-wells housing the PMOS transistors competing for the
 523 charge collection, a deep p-well substrate, common to all the pixel FE area, is used. TJ-Monopix1
 524 adopts the modification described in section 2.4.2 that allows to achieve a planar depletion region

Parameter	Value
Matrix size	$1 \times 2 \text{ cm}^2$
Pixel size	$36 \times 40 \mu\text{m}^2$
Depth	$25 \mu\text{m}$
Electrode size	$2 \mu\text{m}$
BCID	40 MHz
ToT-bit	6
Power consumption	$\sim 120 \text{ mW/cm}^2$

Table 4.2

525 near the electrode applying a relatively small reverse bias voltage. This modification improves the
 526 efficiency of the detector, especially after irradiation, however a simulation of the electric field in
 527 the sensor, made with the software TCAD (Technology Computer Aided Design), shows that a
 528 nonuniform field is still produced in the lateral regions of the pixel compromising the efficiency
 529 at the corner. Two variations to the process have been proposed in order to further enhance the
 530 transversal component of electric field at the pixel borders: on a sample of chip, which includes the
 531 one in Pisa, a portion of low dose implant has been removed, creating a step discontinuity in the
 532 deep p-well corner (fig. 4.3); the second solution proposed[MOUSTAKAS THESYS, PAG 58]
 533 consists in adding an extra deep p-well near the pixel edge. A side effect of the alteration in the
 534 low dose implant is that the separation between the deep p-well and the p-substrate becomes weak
 535 to the point that they cannot be biased separately to prevent the punchthrough.

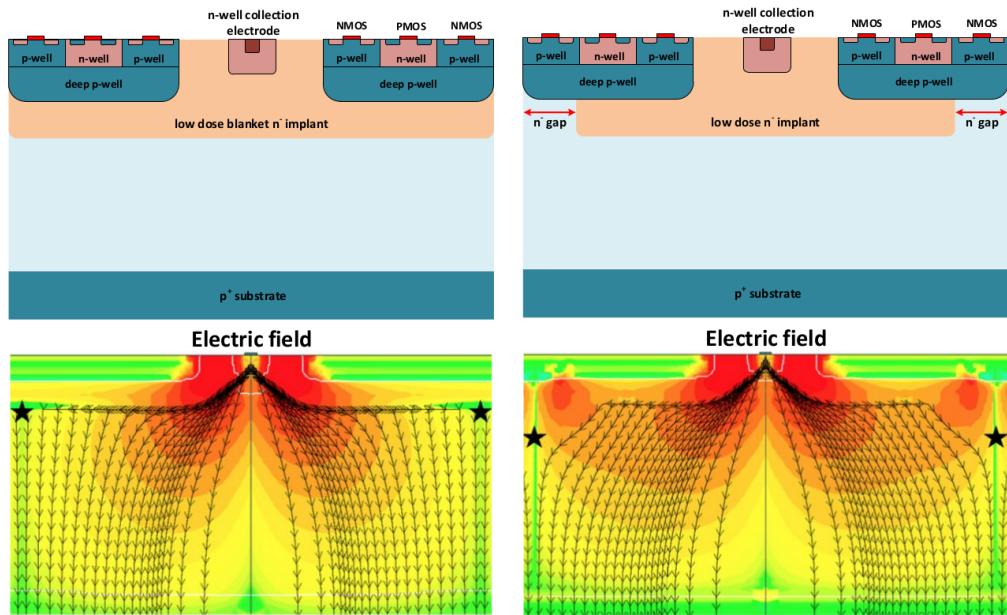


Figure 4.3: (a) The cross-section of a monolithic pixel in the TJ-Monopix with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field. this point in figure is indicated by a star . transversal component of the electric field drops at the pixel corner

536 Moreover, to investigate the charge collection properties, pixels within the matrix are split
 537 between bottom top half and bottom half and feature a variation in the coverage of the deep
 538 p-well: the electronics area can be fully covered or not. In particular the pixels belonging to rows
 539 from 0 to 111 are fully covered (FDPW) and pixels belonging to rows from 112 to 223 have a
 540 reduced p-well (RDPW), resulting in a enhancement of the lateral component of the electric field.

4.2 Front end

The matrix is split in four sections, each one corresponding to a different flavor of the FE. The four variation have been implemented in order to test the data-bus readout circuits and the input reset modes.

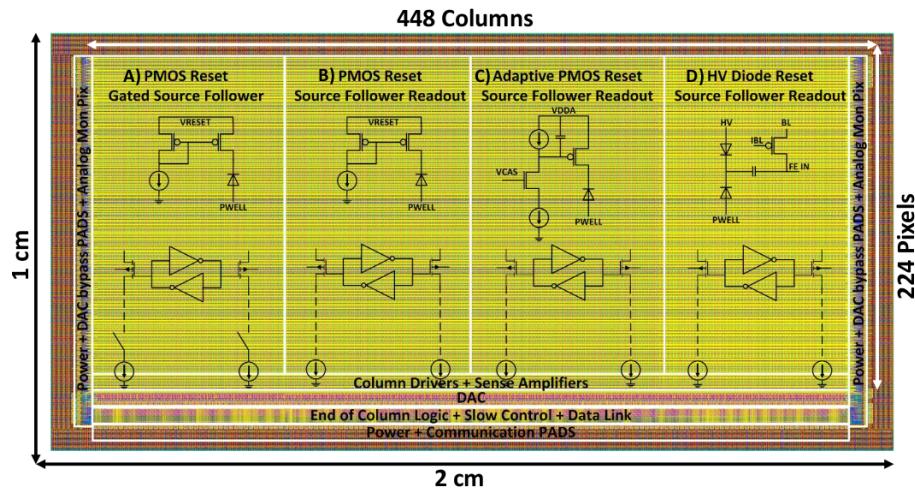


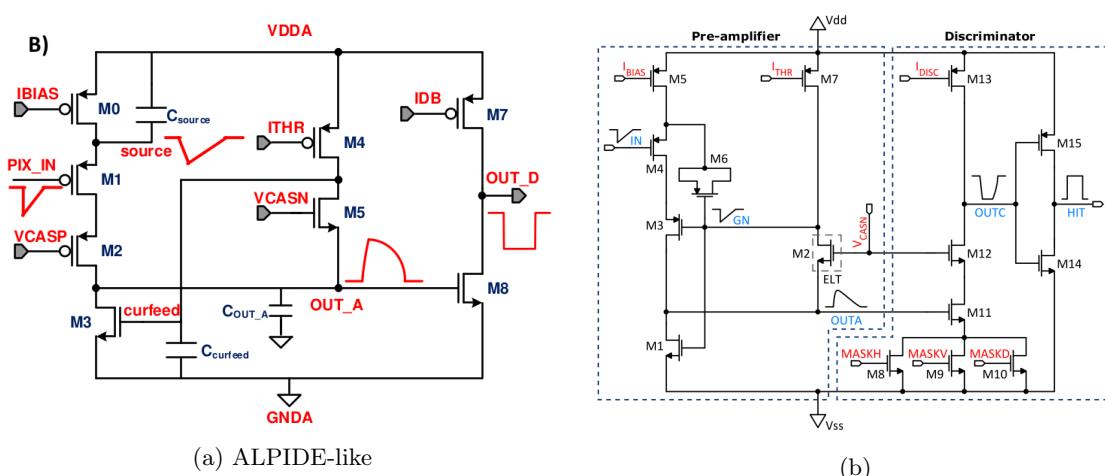
Figure 4.4

All the flavors implement a source-follower double-column bus readout: the standard variation is the flavor B, that features a PMOS input reset (referred as "PMOS reset"). Flavor A is identical to flavor B except for the realization of the source follower (it is a gated one) that aim to reduce the power consumption. cosa significa? C instead implements a novel leakage compensation circuit. Moreover the collection electrode in flavors A, B, C is DC-coupled to the front-end input, while in D is AC-coupled, providing to apply a high bias voltage; for this reason flavor D is called "HV flavor".

Principio generale: R resistenza di reset deve essere abbastanza grande in modo da far sì che il ritorno allo zero è abbastanza lento (non devi "interferire" con la tot slope e non deve essere più corto del tempo del preamplificatore, sennò hai perdita di segnale). Baseline reset: all'input solitamente hai un PMOSS o un diodo; R reset

4.2.1 ALPIDE-like

ALPIDE chips, developed by the ALICE collaboration, implemented a standard FE to the point that many CMOS MAPS detectors used a similar FE and are called "ALPIDE-like". Considering that both TJ-Monopix1 and ARCADIA-MD1 have an ALPIDE-like FE, I am going to explain the broad principles of the early FE stage. The general idea is of the amplification to transfer the



Parameter	Meaning	
IBIAS	mainly controls the rise time	yes? check
IDB	sets the discriminator threshold	yes
ITHR	sets the velocity of the return to the baseline	yes
ICASN	sets the baseline of the signal	yes
VRESET	sets the gain of the preamplifier	yes
IRESET	sets the gain of the preamplifier	no

Table 4.3: FE parameters which must be setted through the DAQ. "Function" means that higher parameter implies higher value

charge from a bigger capacity[9], C_{source} , to a smaller one, C_{out} : the input transistor M1 with current source IBIAS acts as a source follower and this forces the source of M1 to be equal to the gate input $\Delta V_{PIX_IN} = Q_{IN}/C_{IN}$.

$$Q_{source} = C_{source} \Delta V_{PIX_IN} \quad (4.1)$$

The current in M2 and the charge accumulates on C_{out} is fixed by the one on C_{source} :

$$\Delta V_{OUT_A} = \frac{Q_{source}}{C_{OUT_A}} = \frac{C_{source} \Delta V_{PIX_IN}}{C_{OUT_A}} = \frac{C_{Source}}{C_{OUT_A}} \frac{Q_{IN}}{C_{IN}} \quad (4.2)$$

A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR set the baseline value of the signal on C_{OUT_A} and the velocity to goes down to the baseline.

IL RUOLO DI CURVFEED NON L'HO CAPITO.

Finally IDB defines the charge threshold with which the signal OUT_A must be compared: depending on if the signal is higher than the threshold or not, the OUT_D is high or low respectively.

The actual circuit implemented in TJ-Monopix1 is shown in figure 4.5b: the principal difference lays in the addition of disableing pixels' readout. This possibility is uttermost important in order to reduce the hit rate and to avoid saturating the bandwidth due to the noisy pixels, which typically are those with manufacturing defects. In the circuit transistors M8, M9 and M10 have the function of disabling registers with coordinates MASKH, MASKV and MASKD (respectively vertical, horizontal and diagonal) from readout: if all three transistors-signals are low, the pixel's discriminator is disabled. Compared with a configurable masking register which would allow disableing pixels individually, to use a triple redundancy reduces the sensistivity to SEU but also gives amount of intentionally masked ("ghost") pixels. This approach is suitable only for extremely small number N of pixel has to be masked: if two coordinate projection scheme had been implemented, the N's number of ghost pixels would have scale with N^2 , if instead three coordinates are used, the N's exponential is lower than 2 (fig. 4.6)

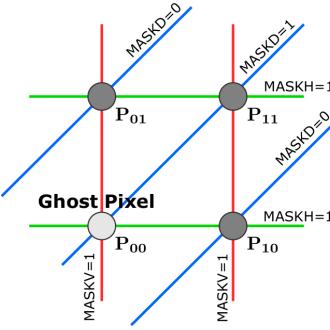


Figure 4.6

581

4.3 Readout logic

TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit

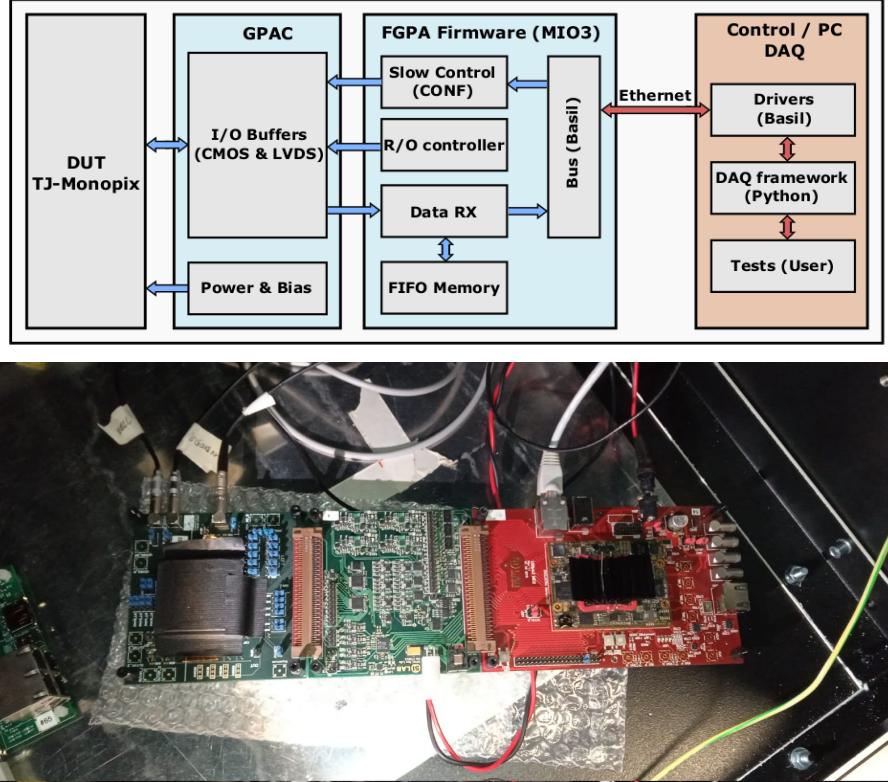
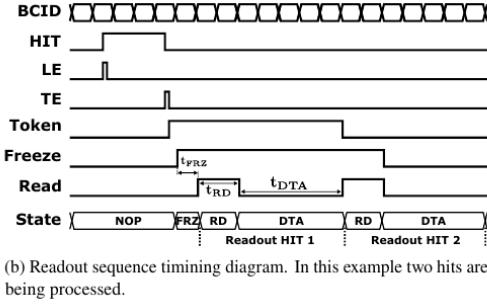


Figure 4.7: Main caption

585 LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address.
 586 Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is
 587 already storing a previous one, the new data get lost. After being read, the data packet is sent to
 588 the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (4.7). There
 589 a FIFO is used to temporarily stored the data, which is transmitted to a computer through an
 590 ethernet cable in a later time.

591 The access to the pixels' memory and the transmission of the data to the EoC, following
 592 a priority chain, is managed by control signals and is based on a Finite State Machine (FSM)
 593 composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and data transfer (DTA).
 594 The readout sequence (??) starts with the TE of a pulse: the pixel immediately tries to grab the
 595 column-bus turning up a hit flag signal called *token*. The token is used to control the priority chain
 596 and propagates across the column indicating what pixel that must be read. To start the readout
 597 and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal is activated, and
 598 then a *read* signal controls the readout and the access to memory. During the freeze, the state of
 599 the token for all pixels on the matrix remains settled: this does not forbid new hits on other pixels
 600 from being recorded, but forbids pixels hit from turning on the token until the freeze is ended. The
 601 freeze stays on until the token covers the whole priority chain and gets the EoC: during that time
 602 new token cannot be turned on, and all hits arrived during a freeze will turn on their token at the
 603 end of the previous freeze. Since the start of the token is used to assign a timestamp to the hit,
 604 the token time has a direct impact on the time resolution measurement; this could be a problem
 605 coping with high hits rate.

606 The analog FE circuit and the pixel control logic are connected by an edge detector which is
 607 used to determine the LE and the TE of the hit pulse(fig. 4.9): when the TE is stored in the first
 608 latch the edge detector is disabled and, if the **FREEZE** signal is not set yet, the readout starts. At
 609 this point the HIT flag is set in a second latch and a token signal is produced and depending on
 610 the value of **Token in** the pixel can be read or must wait until the **Token in** is off. In figure an OR
 611 is used to manage the token propagation, but since a native OR logic port cannot be implemented
 612 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly
 613 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token



(b) Readout sequence timing diagram. In this example two hits are being processed.

Figure 4.8: Readout timing diagram: in this example two hits are being processed

and to speed up the circuit optimized solution are often implemented. When the pixel become the next to be read in the queue, and at the rising edge of the **READ** signal, the state of the pixel is stored in a D-latch and the pixel is allowed to use the data bus; the TE and the HIT flag latches are reset and a **READINT** signal that enable access of the RAM and ROM cells is produced.

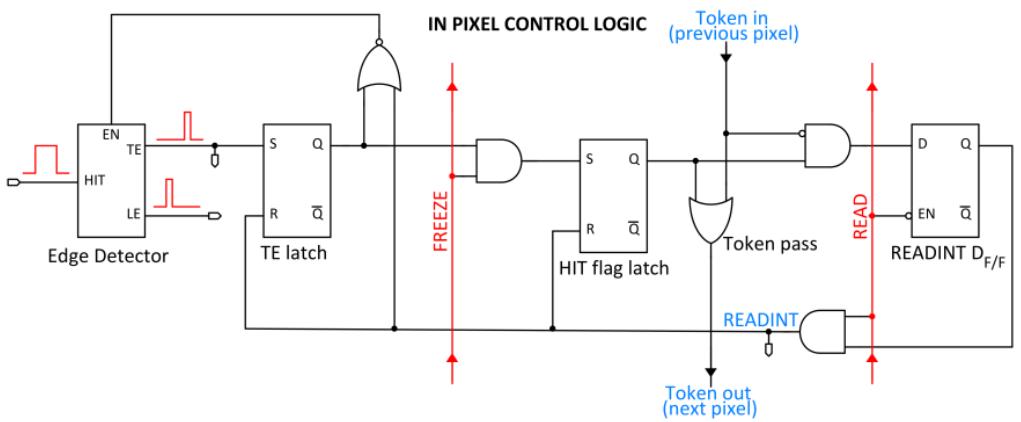


Figure 4.9

The final data must provide all the hits' information: the pixel address, the ToT and the timestamp. All those parts are assigned and appended at different time during the R/O chain:

- **Pixel address:** while the double column address (6-bit) is appended by the EoC circuit, the row address (8-bits for each flavor) and the physical column in the doublet (1-bit) are assigned by the in-pixel logic
- **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge detector in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is range 0-64 clock cycle which corresponds to 0-1.6 μ s
- **Timestamp:** The timestamp of the hit correspond to the time when the pixel set up the token; it is assigned by the FPGA, that uses the LE, TE and a 640 MHz clock to derive it. For all those hits which arrived while the matrix is frozen, the timestamp is no more correlated with the time of arrival of the particle

When the bits are joined up together the complete hit data packet is 27-bit.

4.3.1 Dead time measurements

The hit loss is due to analog and digital pile up: the first one occurs when a new hit arrives during the pre-amplifier response, the second instead, which is the more relevant contribution with high rate, while the information of the previous hit has not yet been transferred to the periphery. As only one hit at a time can be stored on the pixel's RAM, until the data have completed the path to get out, the pixel is paralyzed and the dead time τ almost corresponds with the time needed

Parameter	Value [DAC]	Value [μs]
START_FREEZE	64	1.6
STOP_FREEZE	100	2.5
START_READ	66	1.65
STOP_READ	68	1.7

Table 4.4: Default configuration of the R/O parameters

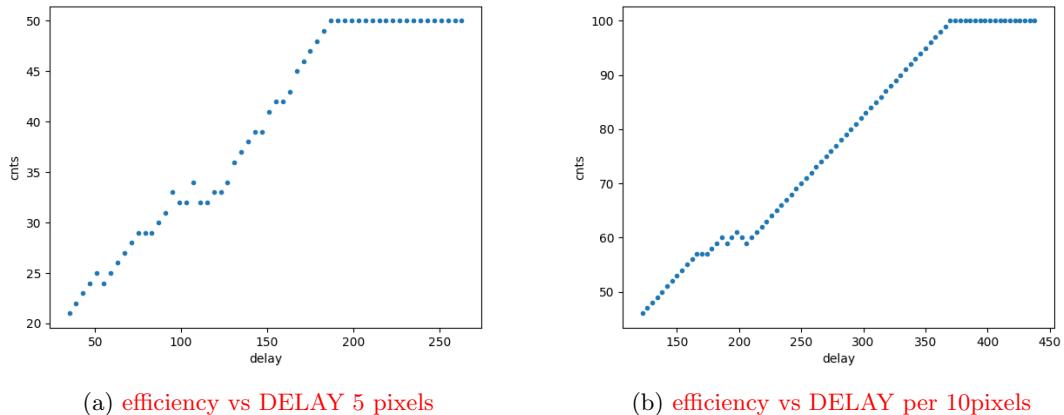
638 to trasmit the data-packets off-chip. Since the exportation of data from pixel to the EoC occurs
 639 via a 21-bits data bus, only one clock cycle is need to transfer the data to the end of column and
 640 the dead time bottleneck is given by the bandwidth of the serializer at the EoC. In our setup the
 641 serializer operates at 40 MHz, thus to transmit a data packet (27-bit considering the addition at
 642 the EoC) at least 675 ns are needed. For what we have said so far, the R/O is completely sequential
 643 and therefore is expected a linear dependence of the reading time on the number of pixels to read:

$$\tau = 25 \text{ ns} \times (\alpha N + \beta) \quad (4.3)$$

644 where α and β are parameters dependent on the readout chain setting.

645 To measure and test the linearity of the reading time with the number of pixels firing, I have
 646 used the injection mode available on the chip. Indeed, the injection mode allows fixing not only
 647 the amplitude of the pulse, which corresponds to the charge in DAC units, but also the period and
 648 the width. I have injected a fix number of pulses (100) and looked for the rate when the efficiency
 649 decreases. Moreover to test that there is no dependece of the digital readout time from the charge
 650 of the pulse, I have try to change the amplitude of the pulse injected, but the parameters found
 651 were consistent with the default configuration ones.

652 Al posto degli esempi con 5 e 10 pixels metterei un esempio dell'efficienza vs il periodo quando
 653 leggo un singolo pixel. Una cosa che volevo fare era anche provare a fissare la slope con cui
 l'efficienza scende: se la slope è uguale per tutti il readout diventa completamente predittivo.



(a) efficiency vs DELAY 5 pixels

(b) efficiency vs DELAY per 10pixels

654 While the single pixel reading time and the dead time do not depend on the position on the
 655 pixel matrix and are equal to 106 (46+60) clock counts within 1 clock count, on the other hand the
 656 τ depends on the pixel position on the matrix when more than one pixel are firing. In particular
 657 the priority chain goes from row 224 to row 0, and from col 0 to 112, that means the last pixels to
 658 be read is the one on the bottom right corner of the matrix.

659 In figure 4.12 is reported the reading time versus the number of pixels injected; the R/O
 660 parameters that control the reading time and their default values are reported on table ??.

661 The factor α , referring to eq. 4.3 is proportional to the difference (STOP_FREEZE - START_READ),
 662 while the offset β lies between 5 and 15 clock counts. Since through the injection a random hit rate
 663 on the matrix can't be simulated, as the coordinates of the pixels to inject must be specified, for
 664 convenience I used the pixels on the same column/row. No difference in the α and β coefficients
 665 has been observed between the two case.

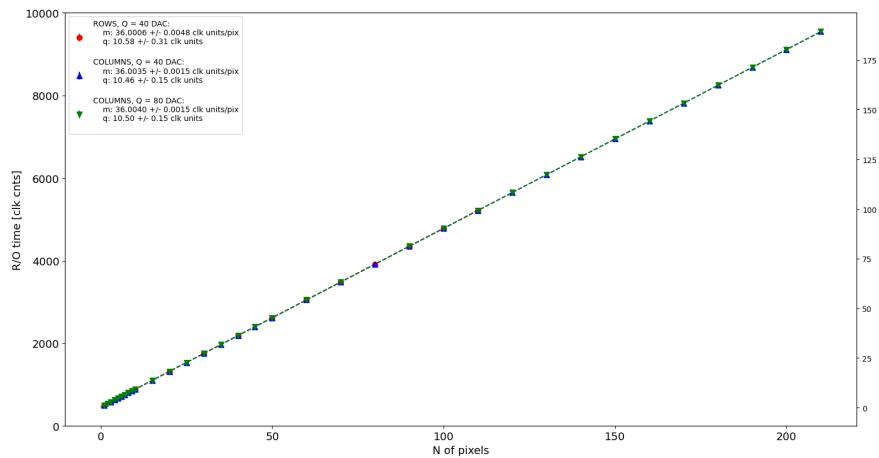


Figure 4.11

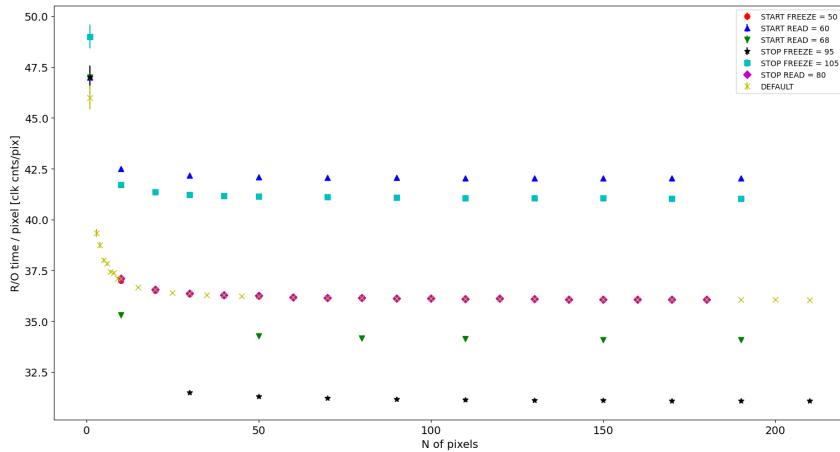


Figure 4.12

667 Ci sarebbe da spiegare perchè i parametri che usiamo noi come default non sono quelli che
 668 minimizzano il tempo di lettura. La spiegazione è che "Abbiamo copiato i valori dal repository
 669 di quelli di Bonn". Un'altra domanda potrebbe essere: come mai non ho esplorato una zona più
 670 vasta per i parametri del R/O. Cambiando molto i parametri del R/O la lettura non funzionava
 671 per niente: ad esempio CONF_STOP_FREEZE non può essere impostato né sopra 105 né sotto 95

672 Chapter 5

673 Arcadia-MD1

674 [10] [11]

675 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED
676 Matisse a Md1 e Md2

677 5.1 The sensor

678 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node
679 with six metal layer ???. The standard p-type substrate was replaced with an n-type floating zone
680 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).

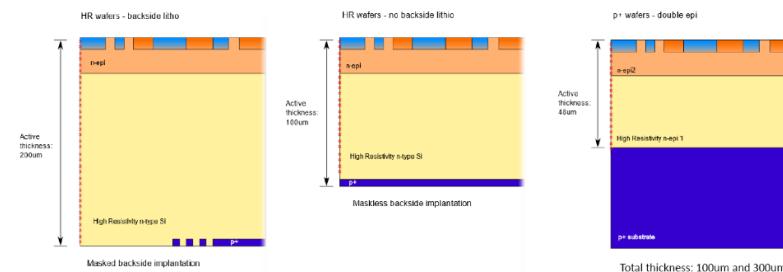


Figure 5.1

681
682 Wafer thinning and backside litography were necessary to introduce a junction at the bottom
683 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.
684 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthought
685 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

686 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,
687 COME VENGONO FATTI I MAPS COME FAI LE GIUNZIONI

688 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.
689 It is operated in full depletion with fast charge collection by drift.

690 Prima SEED si occupa di studiare le prestazioni: oncept study with small-scale test struc-
691 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo
692 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il
693 pwell e quanto al diodo. ..

694 5.2 Readout logic and data structure

695 5.2.1 Matrix division and data-packets

696 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided
697 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in

698 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei serializzatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

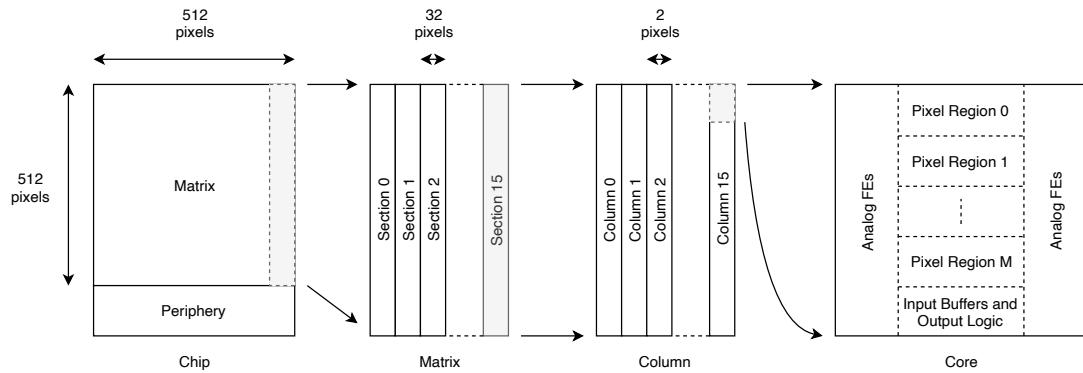


Figure 5.2

699

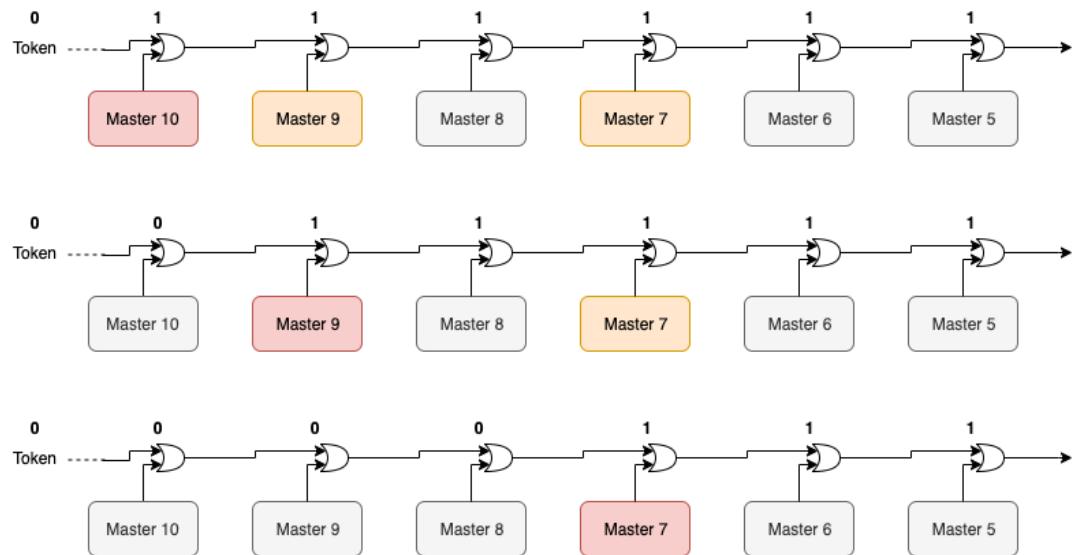


Figure 5.3

700 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le
701 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,
702 e devi accennare al timestamp

703 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively
704 large core allows one to take full advantage of digital synthesis tools to implement complex func-
705 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della
706 review.

707

708 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column
709 (512x2) Core (32x2) Region (4x2)

710 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

711 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for
712 example 8b10b encoding n =5"

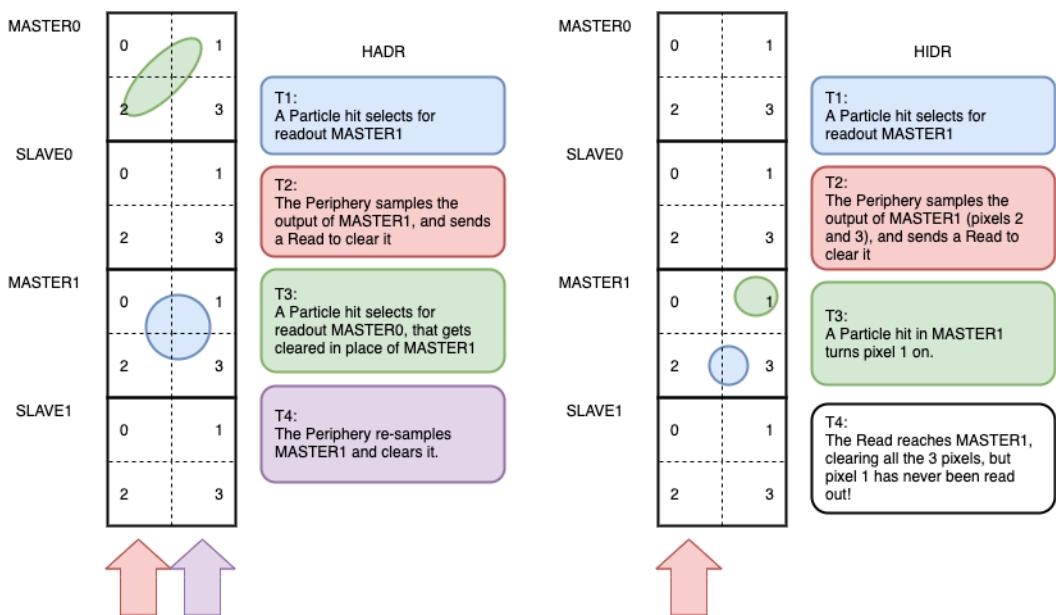


Figure 5.4

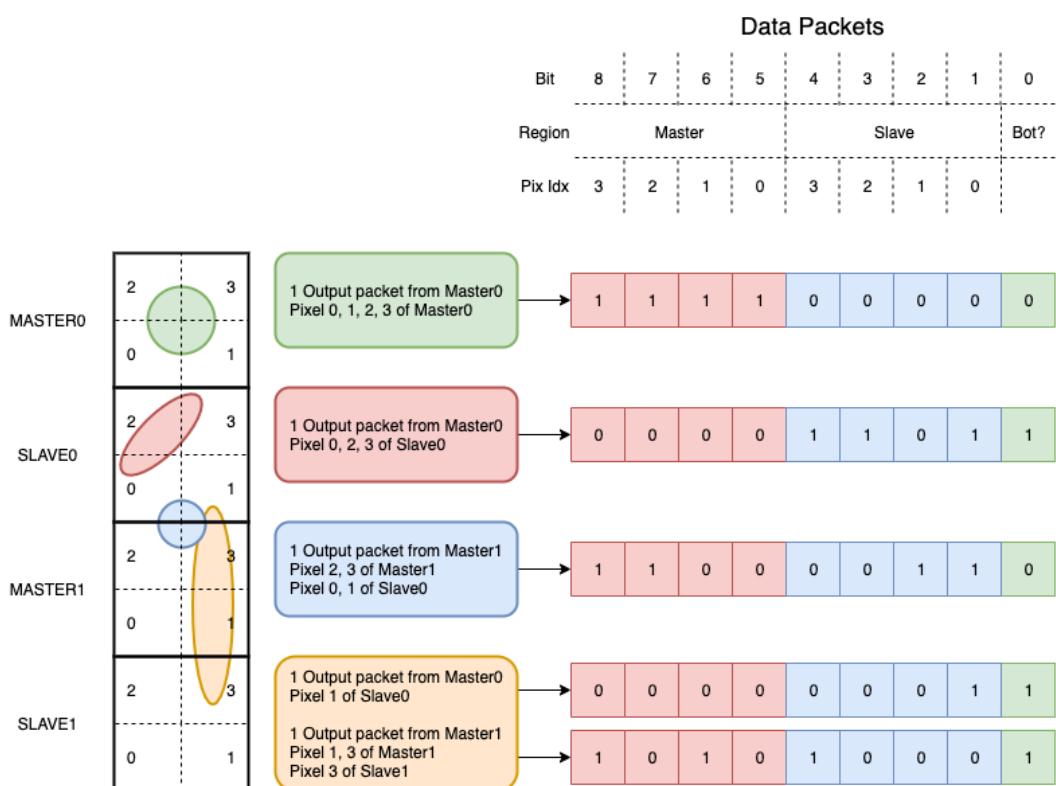


Figure 5.5

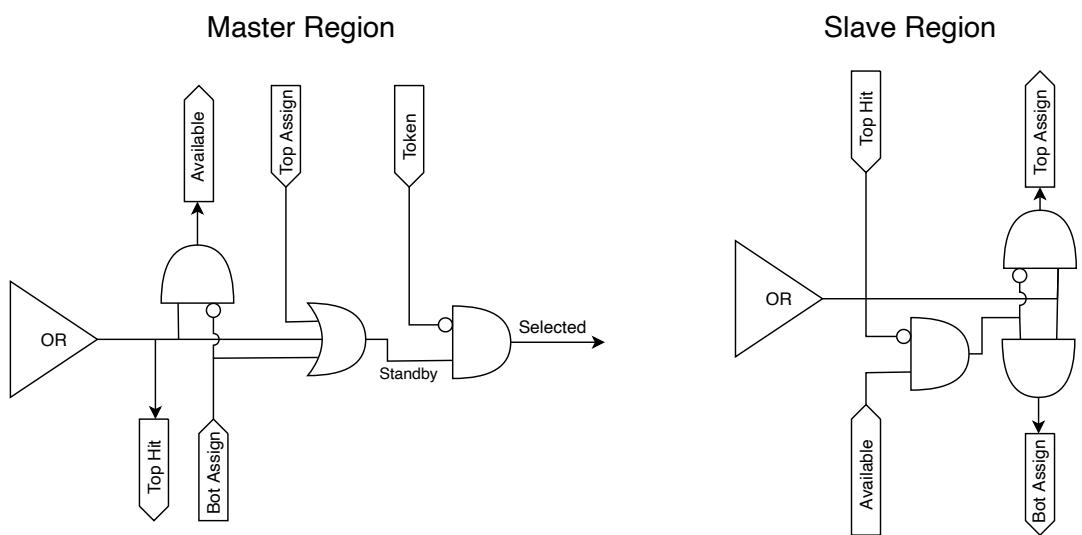


Figure 5.6

713 **Chapter 6**

714 **Threshold and noise
characterization**

716 **6.1 Threshold and noise: figure of merit for pixel detectors**

717 IN QUESTO CAPITOLO HO MESSO SOLO APPUNTI SPARSI DA RIORGANIZZARE, E
718 DEVO AGGIUNGERE POI I PLOT DI MONOPIX1

719 The signal to threshold ratio is the figure of merit for pixel detectors.

720
721 la soglia deve essere abb alta da tagliare il rumore ma abb bassa da non perdere efficienza.
722 Invece di prendere il rapporto segnale rumore prendi il rapporto segnale soglia. Perchè? la soglia
723 è collegato al rumore, nel senso che: supponiamo di volere un occupancy di 10-4 allora sceglierò la
724 soglia in base a questo. (plot su quaderno) Da questo conto trovo la minima soglia mettibile
725 In realtà quello che faccio è mettere una soglia un po' più grande perchè il rate di rumore dipende
726 da molti fattori quali la temperatura, l annealing ecc, e non voglio che cambiando leggermente uno
727 di questi parametri vedo alzarsi molto il rate di rumore. In realtà non è solo il rumore sensibile a
728 diversi fattori, ma anche la soglia: ad esempio la cosa classica è la variabilità della soglia da pixel
729 a pixel.

730 In questo modo rumore e soglia diventano parenti.

731 Review pag 26.

732 Questo implica tra le altre cose che voglio poter assegnare delle soglie diverse a diversi pixel:
733 Drawback è dare spazio per registri e quantaltro.
734 Questo lascia però ancora aperto il problema temporale delle variazioni del rumore: problema per
735 cui diventano necessarie le misure dei sensori dopo l'irraggiamento.

736
737 Non fare trimming sulla soglia è uno dei problemi che si sono sempre incontrati: a casusa dei
738 mismatch dei transistor le soglie efficaci pixel per pixel cambiano tanto. La larghezza della s curve
739 è il noise se assumi che il noise è gaussiano

740 Il trimming della soglia avviene con dei DAC: la dispersione della soglia dopo al tuning e dovuta
741 al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.1)$$

742 dove il numero di bit cambia varia tra 3-7 tipicamente. Monopix è 7 Arcadia 6

743
744 Each ROIC is different in this respect, but in general the minimum stable threshold was around
745 2500 electrons (e) in 1st generation ROICs, whereas it will be around 500 e for the 3rd generation.
746 This reduction has been deliberate: required by decreasing input signal values. Large pixels (2 104
747 um²), thick sensors (maggiore di 200 um), and moderate sensor radiation damage for 1st generation
748 detectors translated into expected signals of order 10 ke, while small pixels (0.25 104 um²), thinner
749 sensors (100 um), and heavier sensor radiation damage will lead to signals as low as 2 ke at the
750 HL-LHC

751 The ENC can be directly calculated by the Cumulative Distribution Function (CDF) (scurve)
752 obtained from the discriminator "hit" pulse response to multiple charge injections

₇₅₃ **6.2 TJ-Monopix1 characterization**

₇₅₄ **6.3 ARCADIA-MD1 characterization**

755 **Chapter 7**

756 **Test beam measurements**

757 L'acceleratore utilizzato è un acceleratore per ricerca sulla flash di fisica medica. È l'unico al mondo
758 che permette di raggiungere alti dosaggi mantenendo l'indipendenza dei parametri del fascio. La
759 struttura del fascio e le varie quantità che si usano per descriverlo sono riportate in figure 7.1.

$$R[Hz/cm^2] = \frac{DPP[Gy]}{1.6 \cdot 10^{10} S[g/cm^2]} \quad (7.1)$$

760 where S is the stopping power in water, $2.17 g/cm^2$

761 Possibilità di integrare carica sul pixel: due elettroni consecutivi su un pixel ogni quanto ar-
762 rivano?

763 Vogliamo sfruttare l'analog pile up, per fare questo dobbiamo fare attenzione a non finire nel
764 digital pile up Devi avere che il tot dell'elettrone (cioè MIP) è maggiore del deltat medio; in questo
765 caso potresti riuscire ad integrare carica.

Table 1. Terminology used throughout the text.

Term	Symbol	Description
intra-pulse dose-rate	—	The duration of a single pulse. ^a
	\bar{D}	Mean dose-rate for a multi-pulse delivery.
pulse repetition frequency	\dot{D}_p	Dose-rate in a single pulse. ^a
	DPP	Dose in a single pulse. ^a
	PRF	Number of pulses delivered per unit time. ^a
	t_i	Total irradiation time from the beginning of the first delivered pulse to the end of the last delivered pulse.
ultrahigh dose-rate	—	Radiation delivered with mean dose-rate of $> \sim 40 \text{ Gy s}^{-1}$.
	—	Ultrahigh dose-rate RT that presents decreased damage to normal tissues compared to RT delivered with conventional dose-rate of $\sim 0.04 \text{ Gy s}^{-1}$.

^aPulses are considered to be macro-pulses unless otherwise stated (see also figure 1).

^bIn literature sometimes referred to as the instantaneous dose-rate.

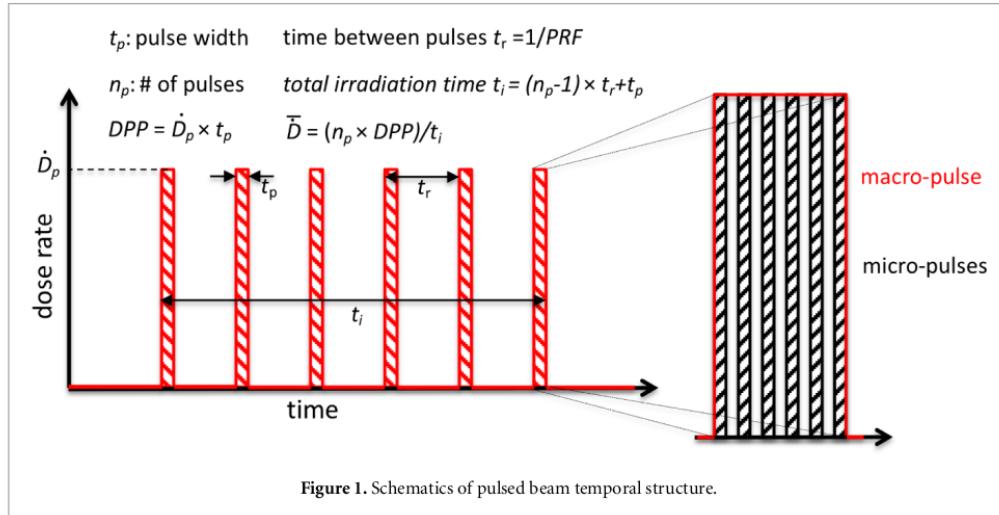


Figure 7.1

766 Appendix A

767 Pixels detector: a brief overview

768 A.1 Radiation damages

769 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they
 770 are almost always installed near the interaction point where there is a high energy level of radiation.
 771 At LHC the ϕ_{eq} per year in the innermost pixel detector is $10^{14} n_{eq}/cm^2$; this number reduces by
 772 an order passing to the outer tracker layer [2] pag 341 Wermes. Here the high fluence of particles
 773 can cause a damage both in the substrate of the detector and in the superficial electronics.

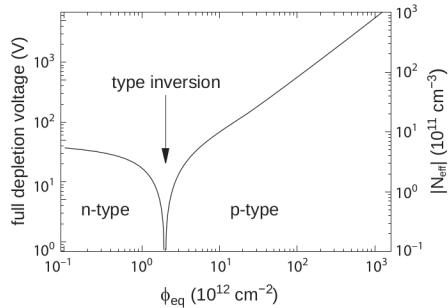
774 The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but
 775 it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the
 776 NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV
 777 neutrons. Differently, surface damages are principally due to ionizing energy loss.

778 **DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide (SiO_2) can
 779 cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages
 780 are mostly less relevant than the previous one, since with the development of microelectronics and
 781 with the miniaturization of components (in electronic industry 6-7 nm transistors are already used,
 782 while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit
 783 is reduced.

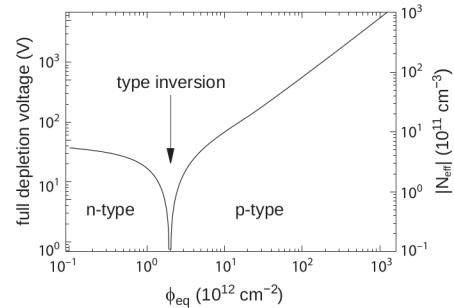
784 Let's spend instead two more other words on the more-relevant substrate damages: the general
 785 result of high radiation level is the creation of new energy levels within the silicon band gap and
 786 depending on their energy-location their effect can be different, as described in the Shockley-Read-
 787 Hall (SRH) statistical model. The three main consequence of radiation damages are the changing
 788 of the effect doping concentration, the leakage current and the increasing of trapping probability.

789 **Changing of the effective doping concentration:** is associated with the creation/removal
 790 of donors and acceptors center which trap respectively electrons/holes from the conduction band
 791 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type¹)
 792 can happen: indeed it is quite common at not too high fluences ($\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$). A changing
 793 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime
 794 (eq.2.1) and sometimes can be difficult keeping to fully deplete the bulk.

¹L'INVERSIONE OPPOSTA NON CE L'HA PERCHÈ?



(a) 1a



(b) 1b

795 **Leakage current:** is associated with the generation-recombination centers. It has a strong
796 dependence with the temperature ($I_{leak} \propto T^2$), whose solution is therefore to operate at lower
797 temperature.

798 **Increase of trapping probability:** since the trapping probability is constant in the depleted
799 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,
800 that is the mean trapping path, decreases after irradiation and typical values are 125-250 μm and
801 must be compared with the thickness of the depleted region which () corresponds to the mean drift
802 path.

803 Different choices for substrate resistivity, for junctions type and for detector design are typically
804 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced
805 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))
806 for example, show a compensation effect for radiation damage; another example is the usage of
807 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage
808 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p
809 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be
810 placed near the diode.

811 Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché
812 una particella deposita carica nell'elettronica che fa da memoria registro/RAM/.... Questo tipo
813 di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti
814 tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip
815 in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più
816 carica di quanto farebbe una MIP. Questo metodo pur essendo più comodo richiede less amount of
817 area ha però come drawback che il registro può essere soggetto a SEU problema non trascurabile
818 in acceleratori come HL-LHC adronici

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