

# Summary

2	<b>1</b>	<b>Introduction</b>	<b>2</b>
3	<b>2</b>	<b>Pixel detectors</b>	<b>3</b>
4	2.1	Hybrid pixels . . . . .	3
5	2.2	CMOS MAPS and DMPAS . . . . .	4
6	2.2.1	DMAPS: large and small fill factor . . . . .	4
7	2.2.2	A modified sensor . . . . .	5
8	2.3	Analog front end . . . . .	6
9	2.3.1	Preamplifier . . . . .	7
10	2.3.2	ALPIDE-like front end . . . . .	7
11	2.4	Readout logic . . . . .	8
12	<b>3</b>	<b>Use of pixels detector</b>	<b>11</b>
13	3.1	Tracking in HEP . . . . .	11
14	3.1.1	Two HEP experiments who chose CMOS-DMAPS . . . . .	11
15	3.2	Dosimetry . . . . .	11
16	3.2.1	Applicability to FLASH radiotherapy . . . . .	11
17	<b>4</b>	<b>TJ-Monopix1</b>	<b>12</b>
18	4.1	The sensor . . . . .	12
19	4.2	FE flavors . . . . .	14
20	4.2.1	FE parameters . . . . .	15
21	4.3	Readout logic . . . . .	16
22	4.3.1	Dead time measurement . . . . .	17
23	<b>5</b>	<b>Arcadia-MD1</b>	<b>18</b>
24	5.1	The sensor . . . . .	18
25	5.2	Readout logic and data structure . . . . .	18
26	5.2.1	Matrix division and data-packets . . . . .	18
27	<b>6</b>	<b>Threshold and noise characterization</b>	<b>22</b>
28	6.1	Threshold and noise: figure of merit for pixel detectors . . . . .	22
29	6.2	TJ-Monopix1 characterization . . . . .	23
30	6.3	ARCADIA-MD1 characterization . . . . .	23
31	<b>A</b>	<b>Pixels detector: a brief overview</b>	<b>24</b>
32	A.1	Signal formation . . . . .	24
33	A.2	Radiation damages . . . . .	25
34	<b>B</b>	<b>FLASH radiotherapy</b>	<b>27</b>
35	B.1	Cell survival curves . . . . .	27
36	B.2	FLASH effect . . . . .	28
37	<b>Bibliography</b>		<b>29</b>
38		Characterization of monolithic CMOS pixel sensors for charged particle detectors and for high intensity dosimetry	

40 **Chapter 1**

41 **Introduction**

42 Pixel detectors, members of the semiconductor detector family, have significantly been used since  
43 () at the first accelerator experiments for energy and position measurement. Because of their  
44 dimension (today  $\sim 30 \mu m$  or even better) and their spatial resolution ( $\sim 5\text{-}10 \mu m$ ), with the  
45 availability of technology in 1980s they proved to be perfectly suitable for vertex detector in the  
46 inner layer of the detector.

47 Technological development has been costant from then on and today almost every high energy  
48 physics (HEP) experiment employs a pixels detector; hybrid pixel currently constitute the state-  
49 of-art for large scale pixel detector but experiments began to look at the more innovative monolithic  
50 active pixels (MAPS) as perspective for their future upgrades, as BelleII, or they already have  
51 installed them, as ALICE.

52 Requirement imposed by accelerator are stringent and they will be even more with the increase  
53 of luminosity/intensity, in terms of radiation hardness, efficiency and occupancy, time resolution,  
54 material budget and power consumption.

55 Qual è invece la richiesta per la dosimetria?

56

<sup>57</sup> **Chapter 2**

<sup>58</sup> **Pixel detectors**

<sup>59</sup> **2.1 Hybrid pixels**

<sup>60</sup> Hybrid pixels are made of two parts (fig. 2.1a), the sensor and the electronics: for each pixel these  
<sup>61</sup> two parts are welded together through microconnection (bump bond).

<sup>62</sup> They provide a practical system where readout and sensor can be optimized separately, although  
<sup>63</sup> the testing is less easy-to-do since the sensor and the R/O must be connected together before.

<sup>64</sup> In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-  
<sup>65</sup> cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high  
<sup>66</sup> levels of radiation, and also expensive.

<sup>67</sup> A critical parameter for accelerator experiments is the material budget, which represents the main  
<sup>68</sup> limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are  
<sup>69</sup> thicker ( $\sim$  hundreds of  $\mu m$ ) than monolithic ones (even less than  $100 \mu m$ ), using the latter the  
<sup>70</sup> material budget can be down by a third: typical value for hybrid pixels is  $1.5 \% X_0$  per layer,  
<sup>71</sup> while for monolithic  $0.5 \% X_0$ .

<sup>72</sup> Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,  
<sup>73</sup> by the way, a bigger cooling system leading in turn to an increase in material too.

<sup>74</sup>

<sup>75</sup> DEPFET are the first attempt towards the integration of the front end (FE) on the sensor bulk:  
<sup>76</sup> they are typically mounted on a hybrid structure but they also integrate the first amplification  
<sup>77</sup> stage.

<sup>78</sup> Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor  
<sup>79</sup> (a p-channel in fig. 2.1b): an hole current flows from source to drain which is controlled by the  
<sup>80</sup> external gate and the internal gate together. The internal gate is made by a deep  $n^+$  implant  
<sup>81</sup> towards which electrons drift after being created in the depletion region (to know how the signal  
<sup>82</sup> is created in a pixel detector look at appendix A); the accumulation of electrons in the region  
<sup>83</sup> underneath the n implant changes the gate potential and controls the transistor current.

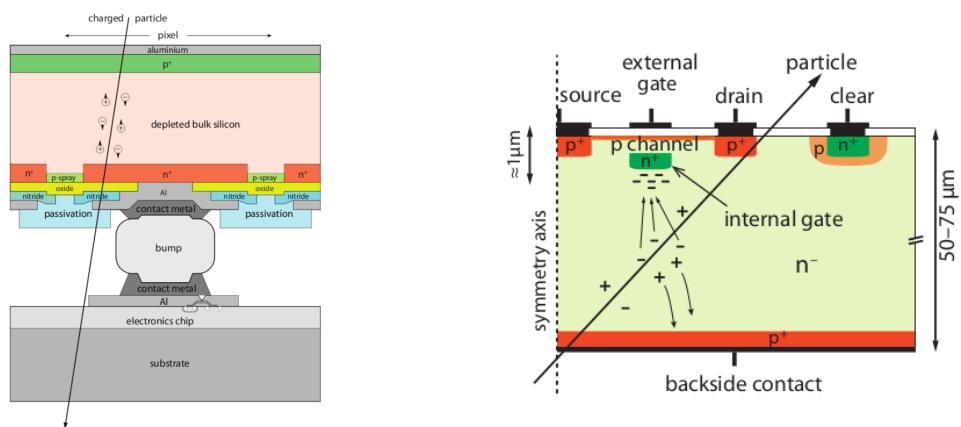


Figure 2.1: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

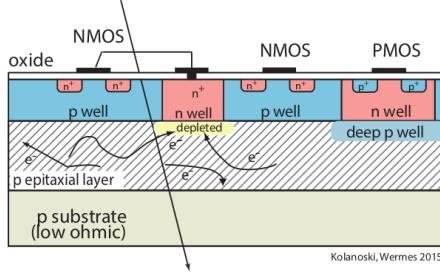


Figure 2.2: Concept cross-section of CMOS MPAS pixel

84 DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and  
 85 the large depletion region. But, since they need to be connected with ASIC the limiting factor still  
 86 is the material budget.

## 87 2.2 CMOS MAPS and DMPAS

88 Monolithic active pixels accommodate on the same wafer both the sensor and the front end elec-  
 89 tronics, with the second one implanted on top.

90 MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the  
 91 development of the electronic sector which guarantees the decrease in CMOS transistors dimension  
 92 at least every two years, as stated by the Moore's law<sup>1</sup>.

93 As a matter of fact the dimension of components, their organization on the pixel area and logic  
 94 density are important issues for the design and for the layout; typically different decisions are taken  
 95 for different purposes.

96 Monolithic active pixel can be distinguished between two main categories: MAPS and depleted  
 97 MAPS (DMAPS).

98 MAPS (figure a 2.2) have typically an epitaxial layer in range 1-20  $\mu\text{m}$  and because they are not  
 99 depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of  
 100 charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the  
 101 collection could be partial especially after the irradiation of the detector (look at A for radiation  
 102 damages), when the trapping probability become higher.

103 In figure 2.2 is shown as example of CMOS MAPS: the sensor in the scheme implements an  
 104 n well as collection diode; to avoid the others n wells (which contain PMOS transistor) of the  
 105 electronic circuit would compete in charge collection and to shield the CMOS circuit from the  
 106 substrate, additionally underlying deep p well are needed. DMAPS are instead MAPS depleted  
 107 with  $d$  typically in  $\sim 25\text{-}150 \mu\text{m}$  (eq. A.1) which extends from the diode to the deep p-well, and  
 108 sometimes also to the backside (in this case if one wants to collect the signal also on this electrode,  
 109 additional process must be done).

### 110 2.2.1 DMAPS: large and small fill factor

111 There are two different sensor-design approaches (figure 2.3) to DMAPS:

- 112 • large fill factor: a large collection electrode that is a large deep n-well and that host the  
 113 embedded electronics
- 114 • small fill factor: a small n-well is used as charge collection node

115 To implement a uniform and stronger electric field, DMAPS often uses large electrode design that  
 116 requires multiple wells (typically four including deep n and p wells); this layout adds on to the  
 117 standard terms of the total capacity of the sensor a new term (fig. 2.4), that contributes to the  
 118 total amplifier input capacity. In addition to the capacity between pixels ( $C_{pp}$ ) and between the  
 119 pixel and the backside ( $C_b$ ), a non-negligible contribution comes from the capacities between wells  
 120 ( $C_{SW}$  and  $C_{WW}$ ) needed to shield the embedded electronics. These capacities affect the thermal  
 121 and 1/f noise of the charge amplifier and the  $\tau_{CSA}$  too:

<sup>1</sup>Moore's law states that logic density doubles every two years.

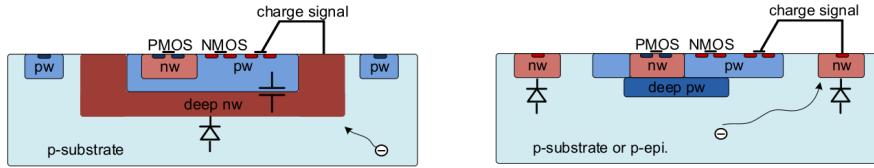


Figure 2.3: Concept cross-section with large and small fill factor

	small fill factor	large fill factor
small sensor C	✓ (< 5 fF)	✗ (~ 100-200 fF)
low noise	✓	✗
low cross talk	✓	✗
velocity performances	✓	✗ (~ 100 ns)
short drift paths	✗	✓
radiation hard	✗	✓

Table 2.1: Small and large fill factor DMAPS characteristics

$$ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.1)$$

$$\tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.2)$$

where  $g_m$  is the transconductance,  $\tau_{sh}$  is the shaping time.  
 Among the disadvantages coming from this large input capacity could be the coupling between the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this problem is especially connected with the intra wells capacities. So, larger charge collection electrode

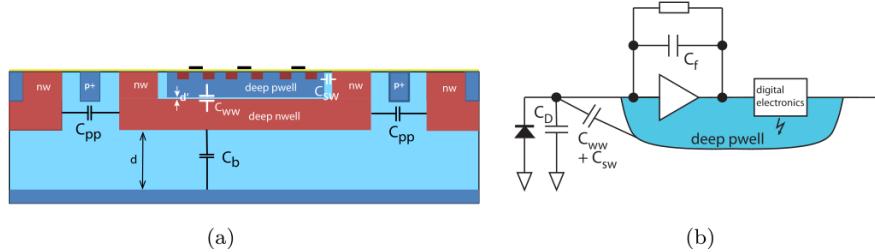


Figure 2.4:  $C_{pp}$ ,  $C_b$ ,  $C_{WW}$ ,  $C_{SW}$

sensors provide a uniform electric field in the bulk that results in short drift path and so in good collection properties, especially after irradiation, when trapping probability can become an issue. The drawback of a large fill-factor is the large capacity (~100 fF): this contributes to the noise and to a speed penalty and to a larger possibility of cross talk.

The small fill-factor variant, instead, benefits from a small capacity (5-20 fF), but suffers from a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando dei MAPS, devo ripetere qui?**

As we'll see these two different types of sensor require different amplifier: the large electrode one is coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.3.1).

### 2.2.2 A modified sensor

?? A process modification developed by CERN in collaboration with the foundries has become the standard solution to combine the characteristics of a small fill factor sensor (small input amplifier capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE upgrade about ten years [1].

A compromise between the two sensors could also be making smaller pixels, but this solution requires reducing the electronic circuit area, so a completely new pixel layout should be though.

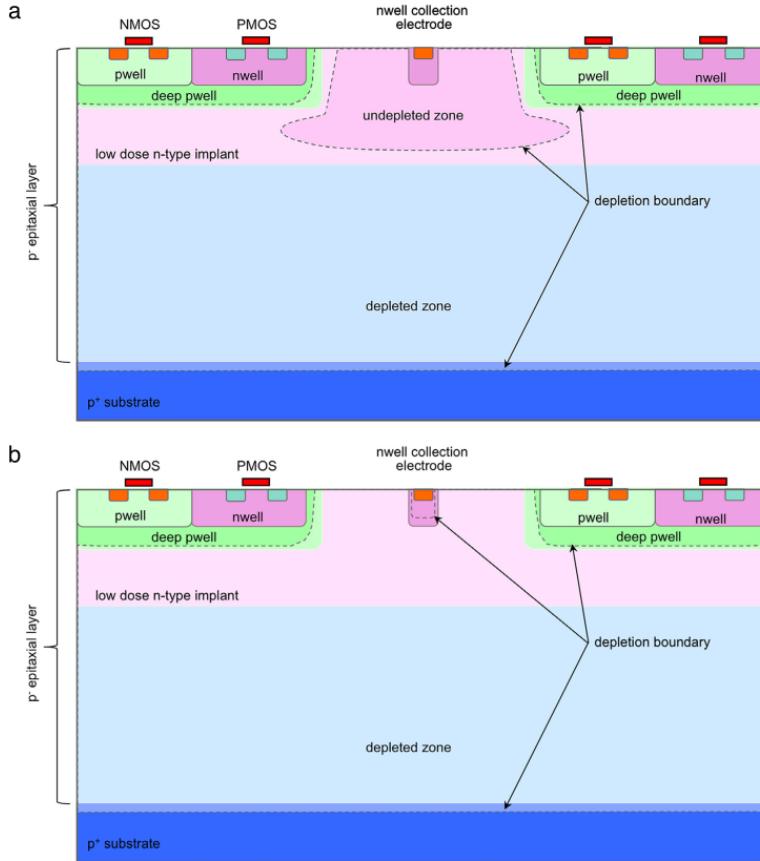


Figure 2.5: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

144 The modification consists in inserting a low dose implant under the electrode and one its advantage  
145 lies in its versatility: both standard and modified sensor are often produced for testing in fact.

146 Before the process modification the depletion region extends below the diode towards the sub-  
147 strate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.5).

148 After, two distinct pn junctions are built: one between the deep p well and the  $n^-$  layer, and the  
149 other between the  $n^-$  and the  $p^-$  epitaxial layer, extending to the all area of the sensor.

150 Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes  
151 can be biased separately<sup>2</sup> and this is beneficial to enhance the vertical electric field component.

152 The doping concentration is a trimmer parameter: it must be high enough to be greater than the  
153 epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be  
154 lower enough to allow the depletion without reaching too high bias.

### 155 2.3 Analog front end

156 After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.6), ready  
157 to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an  
158 efficient, high-speed readout architecture, consuming as low power as possible must be provided  
159 by the readout integrated electronics (ROIC).

160 Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually  
161 often is the only amplification stage) with a reset to the baseline mechanism and a leakage current  
162 compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be  
163 optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise  
164 before the amplification stage in order to not multiply that noise, and chose a reasonable threshold

<sup>2</sup>This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

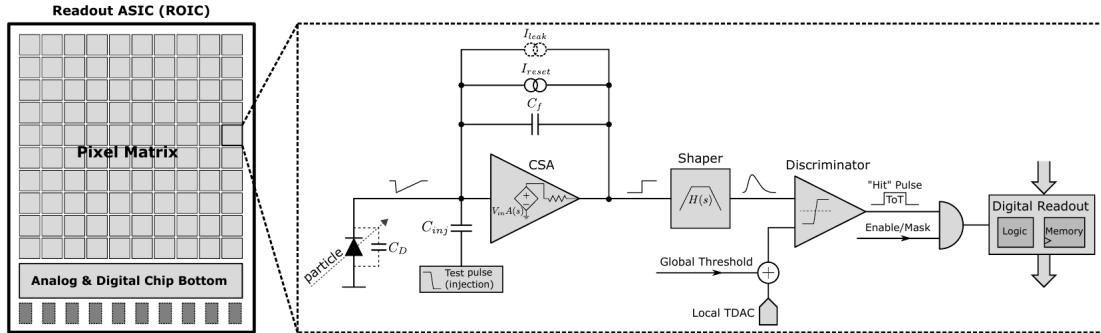


Figure 2.6: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

165 of the discriminator to cut noise-hits much as possible.

### 166 2.3.1 Preamplifier

167 Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled  
168 as an operational amplifier (OpAmp) where the gain is determined by the input and feedback  
169 impedance (first step in figure 2.6):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.3)$$

170 Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a  
171 voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the  
172 voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor  
173 MAPS whose signal is already enough high:  $v_{in} = Q/C_D \approx 3fC/100 \text{ pF} = 0.03 \text{ mV}$ , but it's fine  
174 for the small fill factor ones:  $v_{in} = Q/C_D \approx 3fC/3 \text{ pF} = 1 \text{ mV}$ .

175 In the case of a resistor feedback, if the signal duration time is longer than the discharge time  
176 ( $\tau = R_S C_D$ ) of the detector the system works as current amplifier, as the signal is immediately  
177 transmit to the amplifier; in the complementary case (signal duration longer than the discharge  
178 time) the system integrates the current on the  $C_D$  and operates as a voltage amplifier.

### 179 2.3.2 ALPIDE-like front end

180 I've already mentioned ALICE pixel detector talking about the new process modification, now the  
181 ALICE name comes up again talking about FE: this is because ALPIDE (ALice PIxel DEtector)  
182 is one of the first MAPS detector (TowerJazz 180 nm CMOS) installed <sup>3</sup>, therefore it is the current  
183 state-of-art and most of the following chips' FE are inspired by that, making it a standard in the  
184 FE design. **ARCADIA MD1** and **TJ-Monopix1** are no exception, this is why I'm going to explain  
185 some principals characteristics of how it works

186 The idea of the amplification stage is to transfer the charge from a bigger capacity[2],  $C_{source}$ ,  
187 to a smaller one,  $C_{out}$ : the input transistor M1 with current source IBIAS acts as a source follower  
188 and this forces the source of M1 to be equal to the gate input  $\Delta V_{PIX\_IN} = Q_{IN}/C_{IN}$ .

$$Q_{source} = C_{source} \Delta V_{PIX\_IN} \quad (2.4)$$

189 The current in M2 and the charge accumulates on  $C_{out}$  is fixed by the one on  $C_{source}$ :

$$\Delta V_{OUT\_A} = \frac{Q_{source}}{C_{OUT\_A}} = \frac{C_{source} \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_{Source}}{C_{OUT\_A}} \frac{Q_{IN}}{C_{IN}} \quad (2.5)$$

190 A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR  
191 set the baseline value of the signal on  $C_{OUT\_A}$  and the velocity to goes down to the baseline.

192 **IL RUOLO DI CURVFEED NON L'HO CAPITO.**

193 Finally IDB defines the charge threshold with which the signal  $OUT\_A$  must be compared: depending  
194 on if the signal is higher than the threshold or not, the  $OUT\_D$  is high or low respectively.

<sup>3</sup>It was installed in the Inner Tracking System during the second long shut down of the LHC in 2019

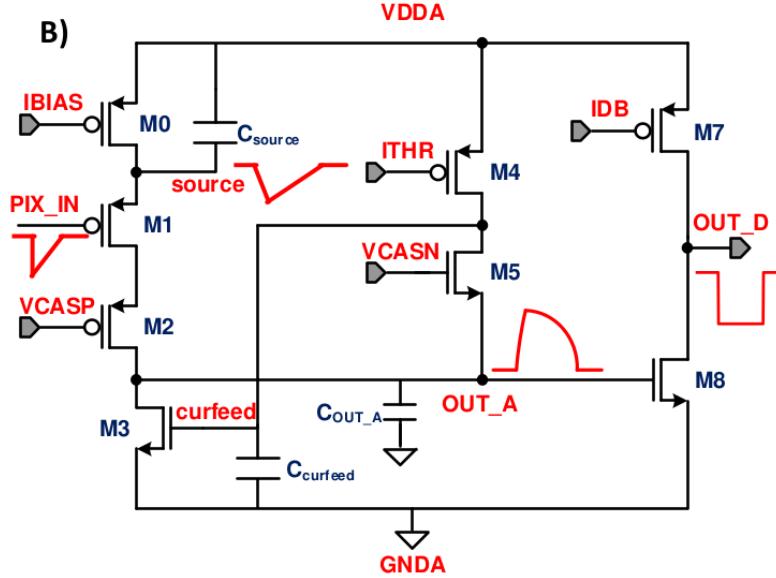


Figure 2.7: ALPIDE like FE

## 2.4 Readout logic

195 Readout logic includes the part of the circuit which takes the FE output signal, processes it and  
 196 then transmit it out of pixel and/or out of chip; depending on the situation of usage different  
 197 readout characteristics must be provided.

198 To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers  
 199 and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really  
 200 high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is  
 201 recorded).

202 A common compromise often made is to save the time over threshold (ToT) of the pulse in clock  
 203 cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen  
 204 bits but, being correlated and hopefully being linear with the deposited charge by the impinging  
 205 particle in the detector, it provides a sufficient information. The ToT digitalization usually takes  
 206 advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels'  
 207 matrix. The required timing precision is at least around 25 ns, that corresponds to the period of  
 208 bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is  
 209 40 MHz.

210 Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they  
 211 have been read, and then the ToT is obtained from their difference.

212 Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger  
 213 system decides if the hit must be store or not. On one hand the triggered-readout needs buffers  
 214 and storage memories, on the other the full readout, because there is no need to store hit data on  
 215 chip, needs an high enough bandwidth.

216 A triggered readout is fundamental in accelerator experiments where the quantity of data to store  
 217 is too large to be handled, and some selections have to be applied by the trigger: to give an order  
 218 of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100  
 219 MBit/s [3] (pag. 797).

220 Typically the trigger signal is processed in a few  $\mu s$ , so the pixel gets it only after a hundred clock  
 221 cycles from the hit arrival time: the buffer depth must than handle the higher trigger latency.

222 After having taken out the data from the pixel, it has to be transmitted to the end of column  
 223 (EoC) where a serializer deliver it out of chip, typically to an FPGA.

224 There are several ways of transmitting data from pixel to the end of column: one of the most  
 225 famous is the column-drain read out, developed for CMS and ATLAS experiments [4]. All the  
 226 pixels in a double-column share a data bus and only one pixel at a time, according to a priority  
 227 chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit  
 228 arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored

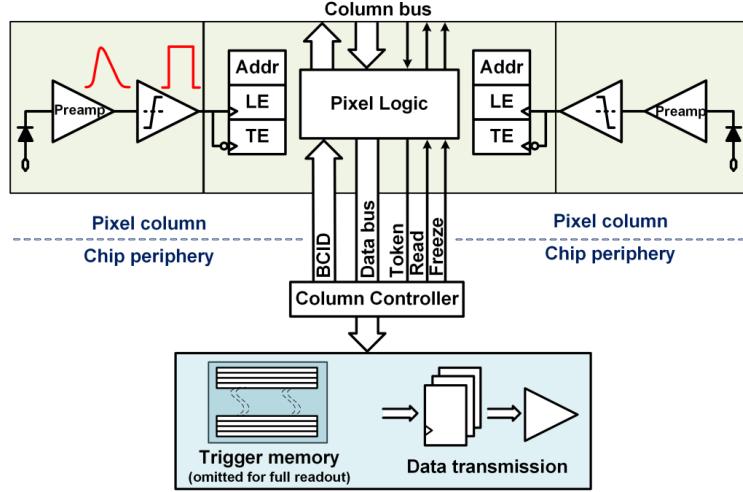


Figure 2.8: Column drain R/O scheme where ToT is saved

on a RAM until the SH does not allow the access to memory by data bus.  
Even if many readout architectures are based the column-drain one, it doesn't suit for large size matrices. The problem is that increasing the pixels on a column would also raise the number of pixels in the priority chain and that would result in a slowdown of the readout.

If there isn't any storage memory, the double-column behaves as a single server queue and the probability for a pixel of waiting a time  $T$  greater than  $t$ , with an input hit rate on the column  $\mu$  and an output bandwidth  $B_W$  is [5]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.6)$$

To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time  $\tau$  due to the AFE), for example imposing  $P(T > t) \sim 0.001$ , one obtains  $(B_W - \mu) t_t \sim 6$ , where  $t_t$  is the time needed to transfer the hit; since  $t_t$  is small, one must have  $B_W \gg \mu$ , that means a high bandwidth [5].

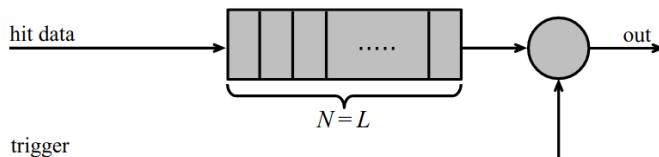


Figure 2.9: Block diagram of a pipeline buffer:  $N$  is the dimension of memory buffer and  $L$  is the trigger latency expressed in BCID cycles

Actually the previous one is an approximation since each pixel sees a different bandwidth depending on the position on the queue: the first one sees a full bandwidth, but the next sees a smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen by the pixel  $i$  is  $B_i = B - \sum_j \mu_j$ , where  $\mu_j$  is the hit rate of the  $j$ th pixel.

The efficiency requirement on the bandwidth and the hit rate becomes:  $B_{W,i} > \mu_i$ , where the index  $i$  means the constraint is for a single pixel; if all the  $N$  pixels on a column have the same rate  $\mu = N\mu_i$ , the condition reduces to  $B_W > \mu$ . The bandwidth must be chosen such that the mean time between hits of the last pixel in the readout chain is bigger than that.

In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed; this means that only information from channels where the signal exceeds the discriminator threshold are stored. Qualcosa sulla zero suppression? La metto qui questa affermazione?

If instead there is a local storage until a trigger signal arrives, the input rate to column bus  $\mu'$  is reduced compared to the hit rate  $\mu$  as:  $\mu' = \mu \times r \times t$ , where  $r$  is the trigger rate and  $t$  is the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth, but the limiting factor is the buffer depth: the amount of memory designed depends both on the

<sup>256</sup> expected rate  $\mu$  and on the trigger latency  $t$  as  $\propto \mu \times t$ , that means that the higher the trigger  
<sup>257</sup> latency and the lower the hit rate to cope with.

<sup>258</sup> In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels  
<sup>259</sup> into regions with shared storage. Let's compare two different situations: in the first one a buffer  
<sup>260</sup> is located on each pixel area, while in the second one a core of four pixels share a common buffer  
<sup>261</sup> (this architecture is commonly called FE-I4).

Consider a 50 kHz single pixel hits rate and a trigger latency of 5  $\mu s$ , the probability of losing

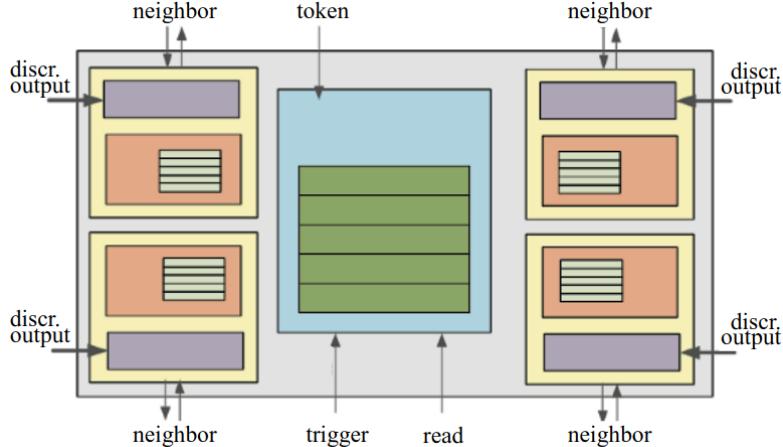


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is highlighted in light blue; latency counters and trigger management section are highlighted in green; hit processing blocks are highlighted in purple; ToT counters and ToT management units are highlighted in orange

<sup>262</sup> hits is:  
<sup>263</sup>

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.7)$$

<sup>264</sup> where I have assumed a Poissonian distribution with mean  $\nu = 0.25$  to describe the counts N.  
<sup>265</sup> To get an efficiency  $\epsilon$  greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.8)$$

<sup>266</sup> Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four  
<sup>267</sup> pixels the mean number of hits per trigger latency is  $\nu = 0.25 \times 4 = 1$ . To get an efficiency of  
<sup>268</sup> 99.9% (eq. 2.8) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

<sup>269</sup> **Chapter 3**

<sup>270</sup> **Use of pixels detector**

<sup>271</sup> A partire dal 2017, i sensori CMOS rappresentano l'89% delle vendite globali di sensori di immagine.  
<sup>272</sup> Ma praticamente dal 2010 in poi solo CMOS e non più CCD.

<sup>273</sup>

<sup>274</sup> **3.1 Tracking in HEP**

<sup>275</sup> Per gli acceleratori la richieste sono molto stringenti e lo saranno sempre di più con l'aumento dell'  
<sup>276</sup> intensità o della luminosità in termini di radiation hardness (per HL-LHC for example expected  
<sup>277</sup> in 5 anni 500 Mrad e NIEL di 10 alla 16), efficiency e occupancy (efficienza alta dopo tanta  
<sup>278</sup> radiazione e noise occupancy bassa), time resolution (bunch crossing 40 Mhz), material budget e  
<sup>279</sup> power consumption (material budget below 2 per cento e power consumption 500 mW/cm<sup>2</sup>)  
<sup>280</sup> Usati come tracciatori per misure di impulso e per misure di energia (per rigettare ) ad esempio  
<sup>281</sup> dati di fondo (topic fondamentale per BELLE-II).

<sup>282</sup> **Resolution**

<sup>283</sup> Depending on the type of signal reading the spatial resolution is  $\sigma_x = \frac{p}{\sqrt{12}}$  where p is the pitch  
<sup>284</sup> between pixels, or even better if other analogica information, as the charge, are read and capacitive  
<sup>285</sup> charge division method is applied.

<sup>286</sup> **3.1.1 Hybrid pixels: ATLAS, CMS and LHC-b**

<sup>287</sup> **3.1.2 CMOS MAPS: ALICE and STAR**

<sup>288</sup> **3.2 Application in medical imaging**

<sup>289</sup> **3.2.1 Medipix and Timepix**

<sup>290</sup> **3.2.2 Applicability to FLASH radiotherapy**

<sup>291</sup> **Chapter 4**

<sup>292</sup> **TJ-Monopix1**

<sup>293</sup>

- <sup>294</sup> • scrivere la differenza tra i FE
- <sup>295</sup> • fare disegno uguale a quello del mascheramento però con solo due coordinate
- <sup>296</sup> • scrivere delle misure cambiando i parametri del FE, e rifare le misure del FE con oscilloscopio e qualche plot
- <sup>297</sup> • scrivere misure del tempo morto e rifarle

<sup>299</sup> The TJ-Monopix1 is one of the chips fabricated by TowerJazz with 180 CMOS imaging process.  
<sup>300</sup> From the middle of 2013 a dedicated collaboration, RD 53 ('Development of pixel readout integrated circuits for extreme rate and radiation'), has been established with the specific goal to find  
<sup>301</sup> a sensor suitable as vertex detector for future upgrade of CMS and ATLAS experiments. Among  
<sup>302</sup> the main objects of study of the collaboration there are both hybrid pixels and monolithic options  
<sup>303</sup> as CMOS MAPS: fig 4.1 shows the intermediate MAPS-prototypes made by TowerJazz.

Besides the TowerJazz series, also LFoundry fabricated other similar sensors with 150 CMOS



Figure 4.1: Timeline in TowerJazz productions. In addition to Monopix series also the small electrode demonstrator TJ-Malta and mini-Malta have been produced and tested[6]. The Malta prototypes differ from TJ-Monopix in the readout: while Monopix implements a column-drain R/O, an asynchronous R/O without any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.

<sup>305</sup>  
<sup>306</sup> technology [7][8]: LF-Monopix.  
<sup>307</sup> The main differences between the LFoundry and TowerJazz's products (tab. 4.2), are in the sensor  
<sup>308</sup> structure rather than in the readout architecture, based on a column drain R/O with ToT capability  
<sup>309</sup> (LF-Monopix has 8 bits dedicated and TJ-Monopix 6 bits). Concerning the sensor, LFoundry  
<sup>310</sup> pixels are bigger and have a large-fill factor, while TJ-Monopix ones have a small fill-factor elec-  
<sup>311</sup> trode.

<sup>312</sup> The performances of both the detectors have been tested before and after irradiation ( $\sim$   
<sup>313</sup>  $10^{10} n_{eq}/cm^2$ ) and the result is, as expected since LF-Monopix is a large fill factor electrode (chap.  
<sup>314</sup> ??), that LF-Monopix is more radiation hard than TJ-Monopix whereas the main degradation of

	LF-Monopix1	TJ-Monopix1
Bulk Resistivity	p-type substrate <i>maggior</i> $2\text{k}\Omega\text{cm}$	p-epi. on a low $\rho$ substrate <i>maggior</i> $1\text{k}\Omega\text{cm}$
Pixel size	$50 \times 250 \mu\text{m}^2$	$26 \times 40 \mu\text{m}^2$
Depth	$100\text{-}750 \mu\text{m}$	$25 \mu\text{m}$
Capacity	$\sim 400 \text{ fF}$	$\sim 3 \text{ fF}$
Preamplifier	CSA	Voltage
Threshold trimming	on pixel (4-bit DAC)	global threshold
Readout mode	Fast column drain	Fast column drain
Consumption	$\sim 300 \text{ mW/cm}^2$	$\sim 120 \text{ mW/cm}^2$
Threshold	$1500 e^-$	$\sim 270 e^-$
ENC	$100 e^-$	$\sim 30 e^-$

Table 4.1: Main characteristics of TJ-Monopix and LF-Monopix [8]

Parameter	Value
Matrix size	
Pixel size	$26 \times 40 \mu\text{m}^2$
Depth	$25 \mu\text{m}$
BCID	40 MHz
ToT-bit	6
Power consumption	$\sim 120 \text{ mW/cm}^2$

Table 4.2

efficiency in TJ-Monopix chips is due to the low electric field in the pixel corner. On the other hand one more accidental consequence of the large fill factor size in LF-Monopix (the deep p-well covers  $\sim 55 \%$  of the pixel area) is a significant cross-talk problem.

## 4.1 The sensor

TJ-Monopix1 adopts the modification described in ?? that allows to achieve a planar depletion region near the electrode applying a relatively small reverse bias voltage: a low dose n implant is build on a high resistivity ( $\geq 1 \text{ k}\Omega \text{ cm}$ ), p-type epitaxial layer.

This modification improves the efficiency of the detector, especially after irradiation[]; however a Technology Computer Aided Design (TCAD) simulation has shown that a nonuniform electric field is still produced in the lateral regions after the modification; since the transversal component of the electric field drops at the pixel corner (this point in figure 4.2 is indicated by a star) the efficiency at the side is reduced.

On a sample of chip, the one I've tested in Pisa belongs to these, a second optimization have been made to enhance the lateral component of electric field and improve the efficiency and velocity in charge collection near the corners of the sensor: a portion of low dose implant has been removed, creating a step discontinuity in the pixel corner. A side effect is the weaker separation between the deep p-well and the p-substrate, that cannot be biased separately anymore to prevent the punchthrough. Moreover, to investigate the charge collection properties, as the threshold, the noise and the efficiency, pixels within the matrix feature a difference in the doping structure of the deep p-well: rows from 0 to 111 are fully covered by deep p-well (FDPW) under p-well near the sensor, while rows from 112 till the last 223 have a portion of deep p-well removed (RDPW). The removing enhance the lateral electric field component then resulting in a higher efficiency, as we'll see later.

338

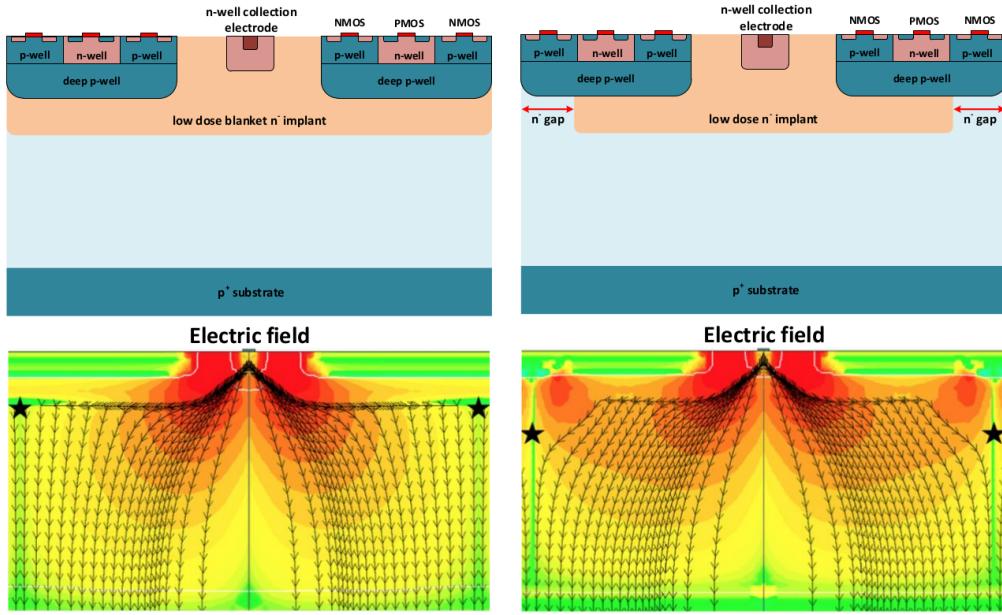


Figure 4.2: (a) The cross-section of a monolithic pixel in the TJ-Monopix 180 nm with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field

## 4.2 FE flavors

TJ-Monopix1 has been implemented in four different flavors, each one corresponding to a different sector on the matrix (fig. 4.3) and thus having a separate readout and data transmission, in order to explore different variations of the FE. The four flavors mainly differ in the reset input circuit. R resistenza di reset deve essere abbastanza grande in modo da far sì che il ritorno allo

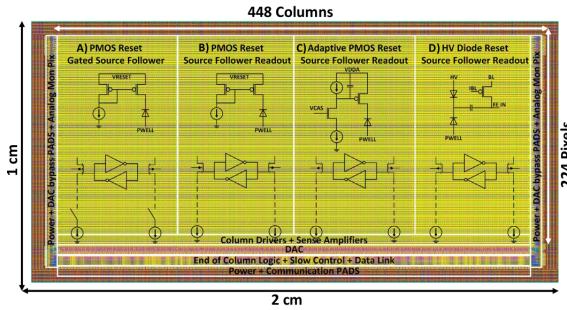


Figure 4.3

zero è abbastanza lento (non devi "interferire" con la tot slope e non devi più corto del tempo del preamplificatore, sennò hai perdita di segnale).

Baseline reset: all'input solitamente hai un PMOSS o un diodo;

The FE circuit 4.4 is ALPIDE-like, so it is similar to the one described in ??; a quanto già detto voglio però aggiungere due parole: come viene implementato il mascheramento dei pixels e il reset.

Prevedere un modo di mascherare gli screaming pixel, tipicamente pixels con manufacturing defects, è fondamentale per poter ridurre il rate molto alto di dati e non saturare la banda.

In the circuit in fig. 4.4 transistors M8, M9 and M10 implement are used to disable pixels-readout, where MASKH, MASKV and MASKD represent respectively the vertical, orizontal and diagonal coordinates of the pixel that one want to mask.

If all three transistors-signals are low, the discriminator is disabled and the pixel is masked. The masking is implemented in this way (with three cordinates instead of one) in order to avoid masking too many ghost pixels (fig. 4.5). Un modo standard che si usa di solito è allocare un registro su

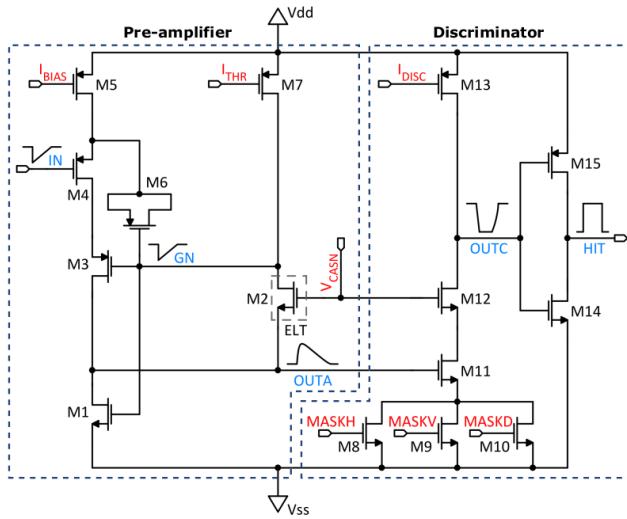


Figure 4.4

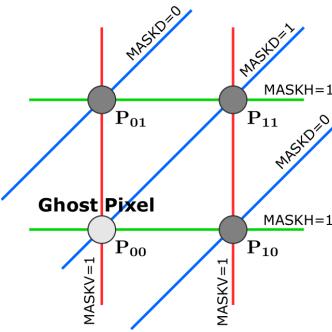


Figure 4.5

358 ogni pixel periphery: il vantaggio di questo modo è che si può disabilitare ogni pixel individualmente.  
 359 Questo metodo pur essendo più comodo richiede less amount of area ha però come drawback che  
 360 il registro può essere soggetto a SEU<sup>1</sup> problema non trascurabile in acceleratori come HL-LHC  
 361 adronici

362 The implemented approach of masking in Monopix-1 funziona però solo se il numero di pixel da  
 363 mascherare non è troppo alto dato che il numero di pixel unintentionally masked ("ghost pixels")  
 364 increase with the number of pixels masked.

365 Nel caso in cui solo due coordinate vengono utilizzate il numero di pixel unintentionally masked  
 366 scales with  $N^2$ , where N is the number of the intentionally masked; if instead three coordinates  
 367 are given the ghost pixels are  $N^\alpha$  where  $\alpha \min 2$ .

368

#### 369 4.2.1 FE parameters

370 Descrivo un po' le misure fatte sul fe e sul significato dei vari parametri.  
 371 it allows injecting pixels with a known charge in DAC units.

---

<sup>1</sup>SEU = Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché una particella deposita carica nell'elettronica che fa da memoria (registro/RAM/...). Questo tipo di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più carica di quanto farebbe una MIP.

Parameter	Meaning
IBIAS	
IDB	
ITHR	
VCASN	
VREF	
IREF	

Table 4.3

### 372 4.3 Readout logic

373 TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain  
 374 architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit  
 375 LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address.  
 376 Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is  
 377 already storing another one, the new data get lost. After being read, the data packet is sent to  
 378 the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (??). There  
 379 a FIFO is used to temporarily stored the data, which is transmitted to a computer through an  
 380 ethernet cable in a later time.

381 The access to the pixels' memory and the transmission of the data off-pixel is based on a Finite  
 382 State Machine (FSM) composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and  
 383 data transfer (DTA). The readout sequence starts with the TE of a pulse: the pixel immediately  
 384 tries to grab the column-bus turning up a hit flag signal called *token*. The token is used to control  
 385 the priority chain and propagates across the column indicating what pixel that must be read. To  
 386 start the readout and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal  
 387 is activated, and then a *read* signal controls the readout and the access to memory. During the  
 388 freeze, the state of the token for all pixels on the matrix remains settled: this does not forbid new  
 389 hits on other pixels from being recorded, but forbids pixels hit from turning on the token until the  
 390 freeze is ended. The freeze stays on until the token covers the whole priority chain and gets the  
 391 EoC: during that time new token cannot be turned on, and all hits arrived during a freeze will  
 392 turn on their token at the end of the previous freeze. Since the start of the token is used to assign  
 393 a timestamp to the hit, the token time has a direct impact on the time resolution measurement;  
 394 this could be a problem coping with high hits rate.

395 The analog FE circuit and the pixel control logic are connected by an edge detector which is  
 396 used to determine the LE and the TE of the hit pulse(fig. ?? (a)): when the TE is stored in the  
 397 first latch the edge detector is disabled and, if the **FREEZE** signal is not set yet, the readout starts.  
 398 At this point the HIT flag is set in a second latch and a token signal is produced and depending on  
 399 the value of **Token in** the pixel can be read or must wait until the **Token in** is off. In figure an OR  
 400 is used to manage the token propagation, but since a native OR logic port cannot be implemented  
 401 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly  
 402 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token  
 403 and to speed up the circuit optimized solution are often implemented. When the pixel become the  
 404 next to be read in the queue, and at the rising edge of the **READ** signal, the state of the pixel is  
 405 stored in a D-latch and the pixel is allowed to use the data bus; the TE and the HIT flag latches  
 406 are reset and a **READINT** signal that enable access of the RAM and ROM cells is produced.

407  
 408 The final data must provide all the hits' information: the pixel address, the ToT and the  
 409 timestamp; all those parts are assigned at different time during the R/O:

- 410 • **Pixel address:** while the row address (8-bits for each flavor) and the physical column in the  
 411 double-column (1-bit) are typically assigned by the in-pixel logic, the double column address  
 412 (6-bit) is appended by the EoC circuit.
- 413 • **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge detector  
 414 in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is range 0-64 clock cy-  
 415 cle which corresponds to 0-1.6  $\mu$ s**Timestamp:**ThetimeStampofthehitcorrespondstotheimewhenthepixelsetupthetoke  
 416 When the bits are joined up together the complete hit data packet is 27-bit.

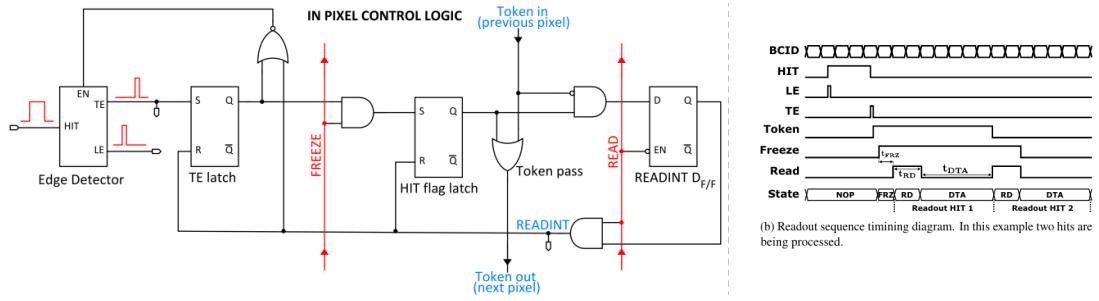


Figure 4.6

#### 417 4.3.1 Dead time measurement

418 Only one hit at a time can be stored on the pixel's RAM, so if The RAM on pixel can store only  
419 one hit at a time, so the dead time ...

420 To perform the test I've used the injection circuit available on matrix: it allows injecting pulses  
421 with fixed amplitude, period and width. Reducing the period between two consecutive pulses and  
422 finding the value when the efficiency decrease, one can estimate the dead time. Dal momento che  
423 c'è un solo serializzatore e che quindi la lettura è sequenziale per tutto il flavor e per quanto detto  
424 sul funzionamento del R/O, il  $\tau$  dipende in maniera lineare dal numero di pixel contenenti una hit.  
425 Per verificare l'andamento lineare e valutare quanto fosse il tempo morto in funzione del rate ho  
426 effettuato uno scan nel rate (diminuendo il periodo tra gli impulsi) e nel numero di pixel iniettati.

427 Il collo di bottiglia del tempo morto è dato dal fatto che c'è un unico serializzatore, infatti per  
428 trasmettere i dati dal pixel alla EoC è necessario un solo ciclo di clock dal momento che c'è un  
429 data bus da n-bit. Per definire meglio il  $\tau$  faccio riferimento alla fig ???: se una hit arriva su un  
430 pixel mentre ha il token alto allora la hit viene persa. Se una hit arriva su un pixel che non ha il  
431 token alto ma ha il freeze alto, allora non viene persa ma le viene assegnato un timestamp errato.

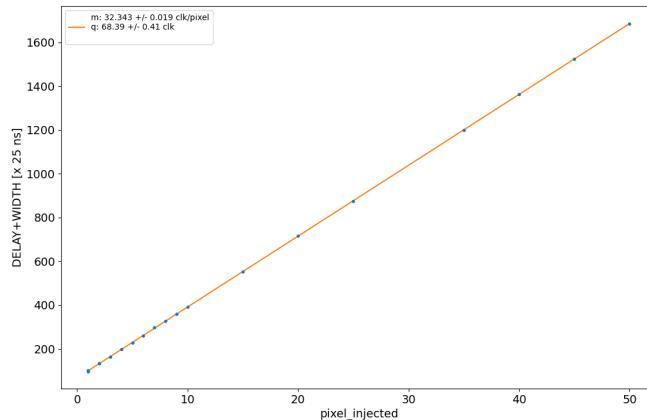


Figure 4.7

432 A tutte le hit di una iniezione che arrivano contemporaneamente viene assegnato lo stesso  
433 timestamp; quando le hit iniziano ad essere meno di quelle che mi aspetti. Mappa in funzione delle  
434 iniezioni di quali pixel hai letto.

# 435 Chapter 5

## 436 Arcadia-MD1

437 [9] [10]

438 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED  
439 Matisse a Md1 e Md2

### 440 5.1 The sensor

441 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node  
442 with six metal layer ???. The standard p-type substrate was replaced with an n-type floating zone  
443 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).

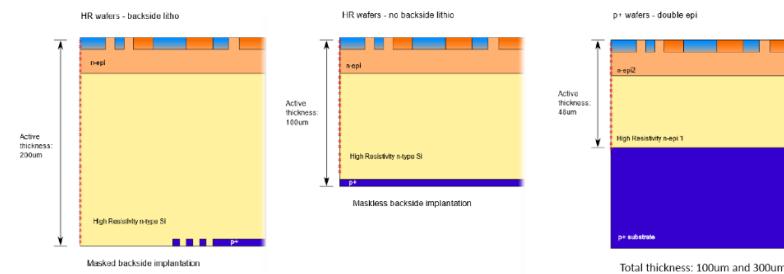


Figure 5.1

444  
445 Wafer thinning and backside litography were necessary to introduce a junction at the bottom  
446 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.  
447 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthrough  
448 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

449 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,  
450 COME VENGONO FATTI I MAPS COME FAI LE GIUNZIONI

451 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.  
452 It is operated in full depletion with fast charge collection by drift.

453 Prima SEED si occupa di studiare le prestazioni: oncept study with small-scale test struc-  
454 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo  
455 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il  
456 pwell e quanto al diodo. ..

### 457 5.2 Readout logic and data structure

#### 458 5.2.1 Matrix division and data-packets

459 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided  
460 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in

461 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei serializzatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

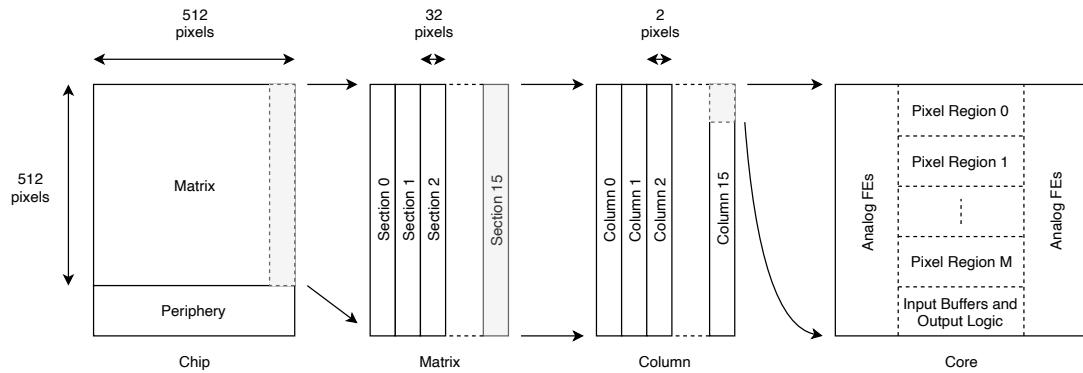


Figure 5.2

462

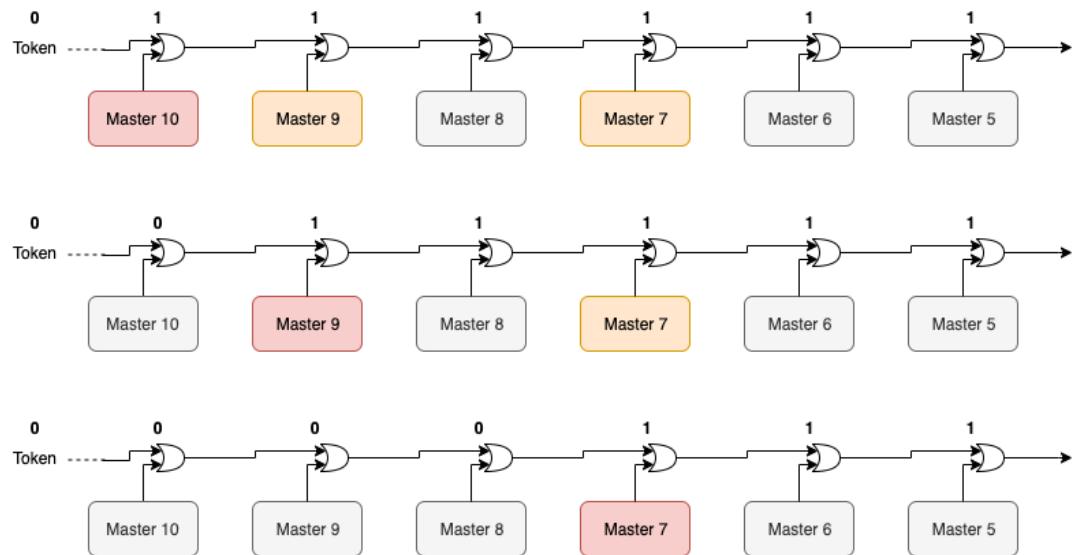


Figure 5.3

463 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le  
464 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,  
465 e devi accennare al timestamp

466 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively  
467 large core allows one to take full advantage of digital synthesis tools to implement complex func-  
468 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della  
469 review.

470

471 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column  
472 (512x2) Core (32x2) Region (4x2)

473 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

474 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for  
475 example 8b10b encoding n =5"

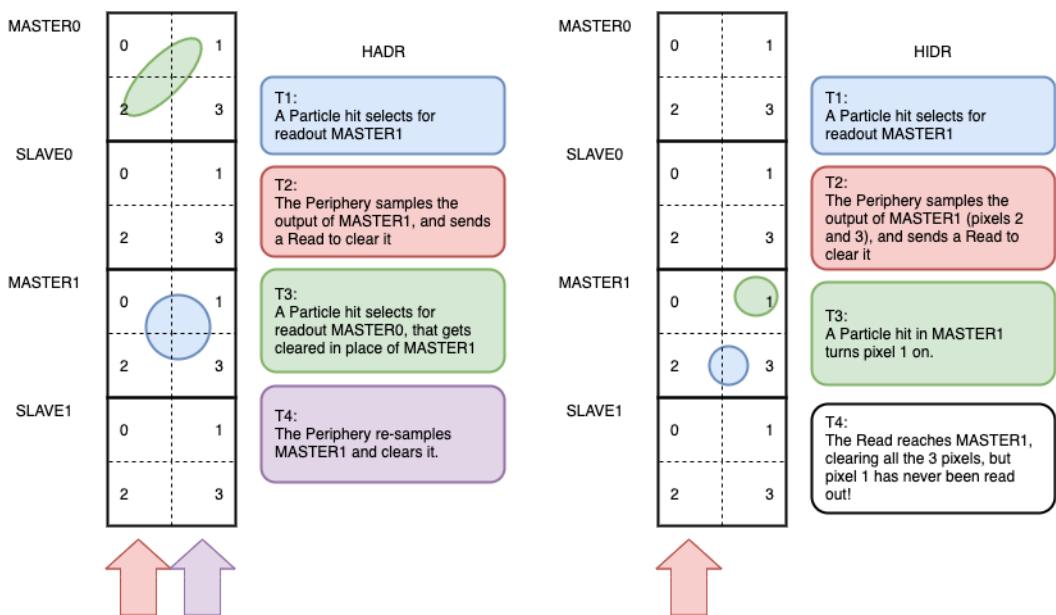


Figure 5.4

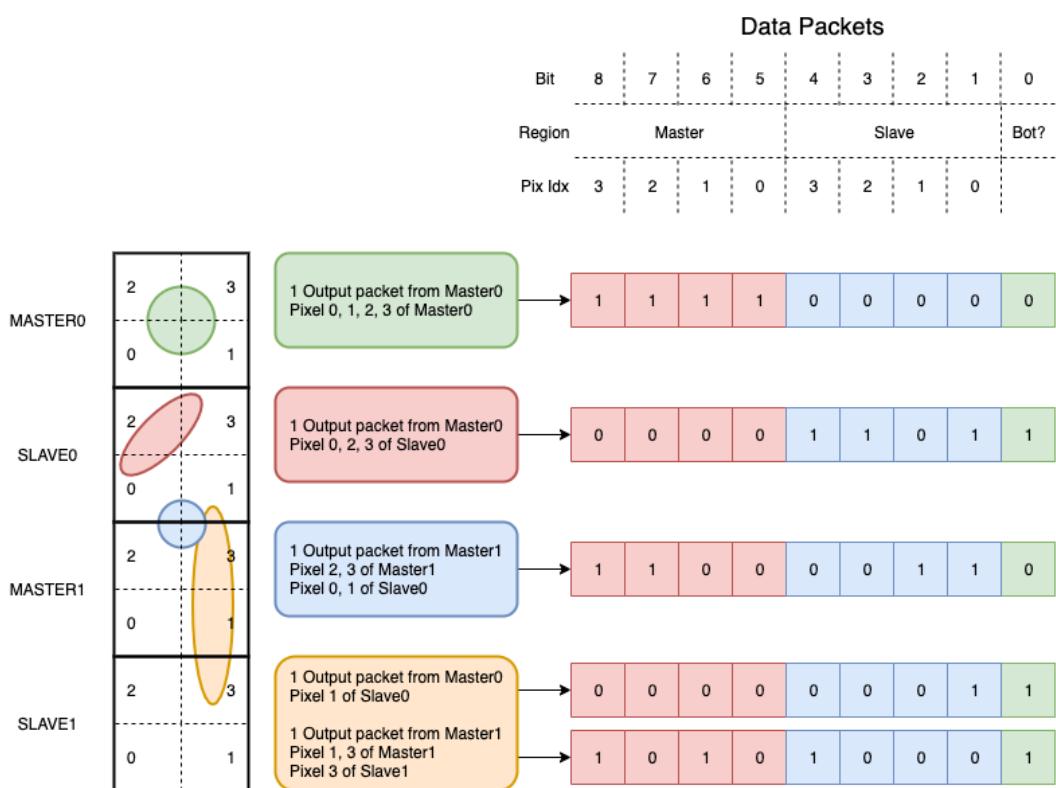


Figure 5.5

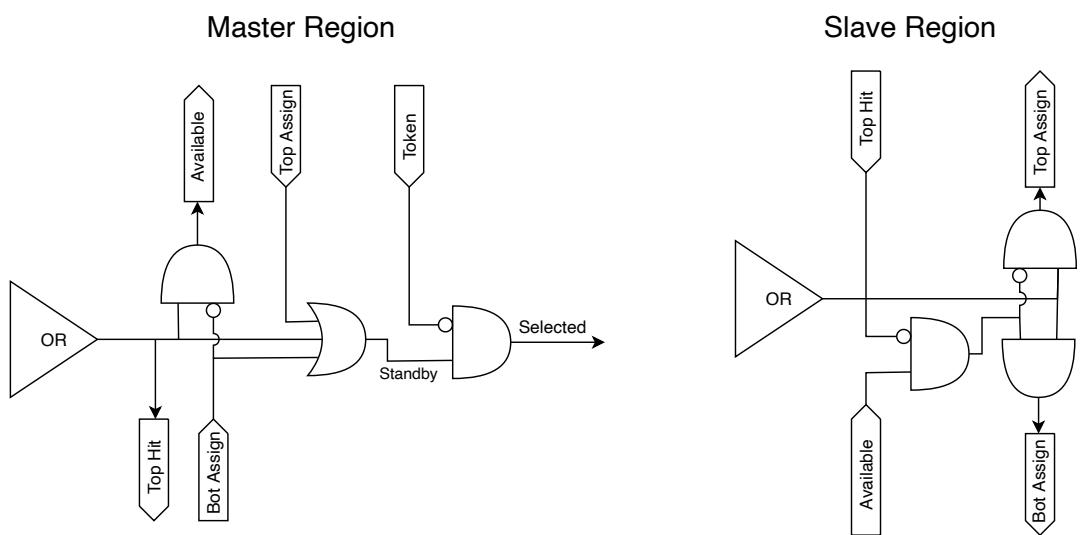


Figure 5.6

476 **Chapter 6**

477 **Threshold and noise  
characterization**  
478

479 **6.1 Threshold and noise: figure of merit for pixel detectors**

480 The signal to threshold ratio is the figure of merit for pixel detectors.

481  
482 la soglia deve essere abb alta da tagliare il rumore ma abb bassa da non perdere efficienza.  
483 Invece di prendere il rapporto segnale rumore prendi il rapporto segnale soglia. Perchè? la soglia  
484 è collegato al rumore, nel senso che: supponiamo di volere un occupancy di 10-4 allora sceglierò la  
485 soglia in base a questo. (plot su quaderno) Da questo conto trovo la minima soglia mettibile  
486 In realtà quello che faccio è mettere una soglia un po' più grande perchè il rate di rumore dipende  
487 da molti fattori quali la temperatura, l annealing ecc, e non voglio che cambiando leggermente uno  
488 di questi parametri vedo alzarsi molto il rate di rumore. In realtà non è solo il rumore sensibile a  
489 diversi fattori, ma anche la soglia: ad esempio la cosa classica è la variabilità della soglia da pixel  
490 a pixel.

491 In questo modo rumore e soglia diventano parenti.

492 Review pag 26.

493 The noise requirement can be expressed as:

494 Questo implica tra le altre cose che voglio poter assegnare delle soglie diverse a diversi pixel:

495 Drawback è dare spazio per registri e quantaltro.

496 Questo lascia però ancora aperto il problema temporale delle variazioni del rumore: problema per  
497 cui diventano necessarie le misure dei sensori dopo l'irraggiamento.

498  
499 Per arcadia i registri (c'è un DAC) per la soglia (VCASN) si trovano in periferia. Non fare  
500 trimming sulla soglia è uno dei problemi che si sono sempre incontrati: a casusa dei mismatch dei  
501 transistor le soglie efficaci pixel per pixel cambiano tanto. La larghezza della s curve è il noise se se  
502 assumi che il noise è gaussiano

503 Il trimming della soglia avviene con dei DAC: la dispersione della soglia dopo al tuning e dovuta  
504 al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.1)$$

505 dove il numero di bit cambia varia tra 3-7 tipicamente. Monopix è 7 Arcadia 6

506  
507 Each ROIC is different in this respect, but in general the minimum stable threshold was around  
508 2500 electrons (e) in 1st generation ROICs, whereas it will be around 500 e for the 3rd generation.  
509 This reduction has been deliberate: required by decreasing input signal values. Large pixels (2 104  
510 um<sup>2</sup>), thick sensors (maggiore di 200 um), and moderate sensor radiation damage for 1st generation  
511 detectors translated into expected signals of order 10 ke, while small pixels (0.25 104 um<sup>2</sup>), thinner  
512 sensors (100 um), and heavier sensor radiation damage will lead to signals as low as 2 ke at the  
513 HL-LHC

514 The ENC can be directly calculated by the Cumulative Distribution Function (CDF) (scurve)  
515 obtained from the discriminator "hit" pulse response to multiple charge injections

516 **6.2 TJ-Monopix1 characterization**

517 Com'è fatto il set up per le misure.  
518 FPGA BB, Chip con FE board, qualche foto  
519

520 **6.3 ARCADIA-MD1 characterization**

521 Com'è fatto il set up per le misure.  
522 FPGA BB, Chip con FE board, qualche foto  
523

524 **Appendix A**

525 **Pixels detector: a brief overview**

526 **A.1 Signal formation**

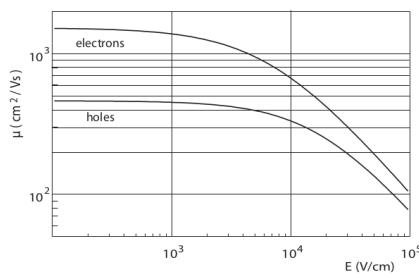
527 When a charge particle passes through a pixel and loses energy by ionization a part of that  
 528 energy is used to generate electron-hole pairs (another part is used for other processes, as the  
 529 lattice excitation) which are then separated by the electric field and collected at their respectively  
 530 electrodes ( $p$  for holes and  $n$  for electrons)<sup>1</sup>; by the drift of these charges, a signal  $i_e$  is generated  
 531 on the electrode  $e$  as stated by the Shockley–Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (\text{A.1})$$

532 where  $v(t)$  is the instantaneous velocity of the charge  $q$  and  $E_{WF}$  is the weighting field, that is the  
 533 field obtained biasing the electrode  $e$  with 1V and all the others with 0V. The drift velocity of the  
 534 charge depends on the electric field and on the mobility of the particle:

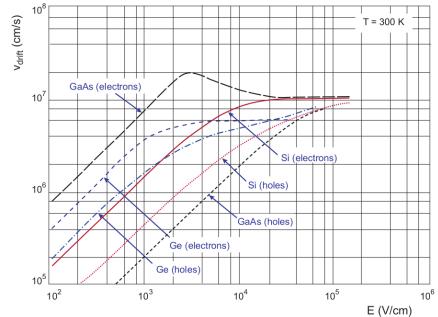
$$v = \mu(E) E \quad (\text{A.2})$$

535 where  $\mu(E)$  is a function of the electric field and is linear with  $E$  only for small  $E$ : at higher values  
 536 the probability of interactions with optical phonons increases and the mobility drops and this leads  
 537 to an independence of the velocity from the electric field (fig. A.1b).



(a) Typical values for electrons and holes mobility in

silicon at room temperature are  $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$ ,  $\mu_h = 500$

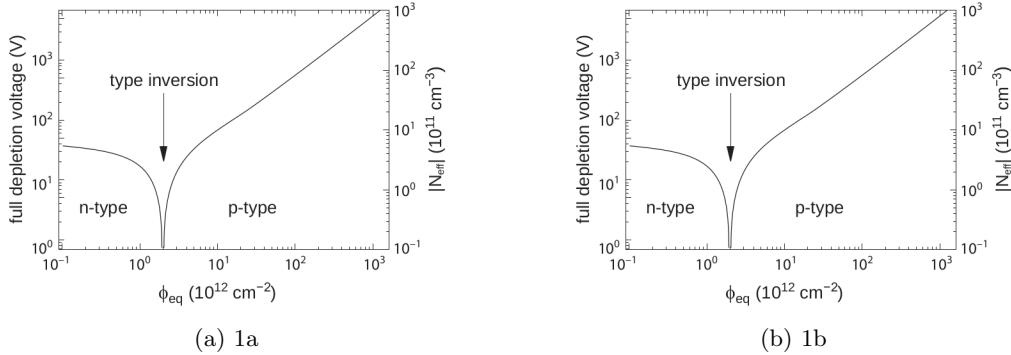


(b) Drift velocity at room temperature in different semiconductors

538 The average energy needed to create a pair at 300 K in silicon is  $w_i = 3.65 \text{ eV}$ , that is more  
 539 than the mean ionization energy because of the interactions with phonon, since for a minimum  
 540 ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is  
 541 0.28 keV/ $\mu$ , hence the number of e/h pairs is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (\text{A.3})$$

<sup>1</sup>Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout



CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALEMTE SI AGGIUNGE IL  
 FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. il FATTORE DI FANO È  
 0.115 NEL SILICIO. ecc It is fundamental that pairs e/h are produced in the depleted region  
 of the semiconductor where the probability of recombination with charge carriers is low to avoid  
 loss of signals. Pixel detectors are then commonly reverse biased: a positive bias is given to the  
 $n$  electrode and a negative to the  $p$  to grow the depletion zone in the epitaxial layer below the  
 electrode. The width of the depletion region is related with the external bias  $V_{ext}$ , the resistivity  
 $\rho$  and also with the dopant:

$$d_n \sim 0.55\sqrt{\frac{\rho}{\Omega cm}} \frac{V_{ext}}{V} \mu m \quad (A.4) \qquad \qquad d_p \sim 0.32\sqrt{\frac{\rho}{\Omega cm}} \frac{V_{ext}}{V} \mu m \quad (A.5)$$

For that reason high resistivity wafers ( $100 \Omega cm - k\Omega cm$ ) are typically preferred because they allow bigger depletion zone with smaller voltage bias.

## 555 A.2 Radiation damages

556 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they  
 557 are almost always installed near the interaction point where there is a high energy level of radiation.  
 558 At LHC the  $\phi_{eq}$  per year in the innermost pixel detector is  $10^{14} n_{eq}/cm^2$ ; this number reduces by  
 559 an order passing to the outer tracker layer [3] pag 341 Wermes. Here the high fluence of particles  
 560 can cause a damage both in the substrate of the detector and in the superficial electronics.

The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV neutrons. Differently, surface damages are principally due to ionizing energy loss.

**DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide ( $SiO_2$ ) can cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages are mostly less relevant than the previous one, since with the development of microelectronics and with the miniaturization of components (in electronic industry 6-7 nm transistors are already used, while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit is reduced.

Let's spend instead two more other words on the more-relevant substrate damages: the general result of high radiation level is the creation of new energy levels within the silicon band gap and depending on their energy-location their effect can be different, as described in the Shockley-Read-Hall (SRH) statistical model. The three main consequence of radiation damages are the changing of the effect doping concentration, the leakage current and the increasing of trapping probability.

**576      Changing of the effective doping concentration:** is associated with the creation/removal  
 577 of donors and acceptors center which trap respectively electrons/holes from the conduction band  
 578 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type<sup>2</sup>)  
 579 can happen: indeed it is quite common at not too high fluences ( $\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$ ). A changing

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<sup>2</sup>L'INVERSIONE OPPOSTA NON CE L'HAI PERCHÈ?

580 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime  
581 (eq.A.1) and sometimes can be difficult keeping to fully deplete the bulk.

582 **Leakage current:** is associated with the generation-recombination centers. It has a strong  
583 dependence with the temperature ( $I_{leak} \propto T^2$ ), whose solution is therefore to operate at lower  
584 temperature.

585 **Increase of trapping probability:** since the trapping probability is constant in the depleted  
586 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,  
587 that is the mean trapping path, decreases after irradiation and typical values are 125-250  $\mu m$  and  
588 must be compared with the thickness of the depleted region which () corresponds to the mean drift  
589 path.

590 Different choices for substrate resistivity, for junctions type and for detector design are typically  
591 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced  
592 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))  
593 for example, show a compensation effect for radiation damage; another example is the usage of  
594 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage  
595 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p  
596 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be  
597 placed near the diode.

598 **Appendix B**

599 **FLASH radiotherapy**

600 La radioterapia si usa nel 60 per cento dei pazienti, sia come cura che come trattamento palliativo.  
601 Si associa spesso ad altre cure e si può fare prima/durante/dopo un intervento.

602  
603 Si può fare in modi diversi: da dentro (brachytherapy) oppure da fuori (quella standard). Un  
604 requisito importante è la delinazione del target (non vuoi rischiare di beccare i tessuti sani), per  
605 cui prima tipicamente si fanno esami di imaginig del tumore. Tipicamente anche gli acceleratori  
606 stessi per la terapia sono provvisti di radiografia.

607 Un problema dei fotoni ad esempio è che il loro rilascio di dose è lineare, per cui danneggia  
608 anche i tessuti sani. Il problema dei protoni invece è che hanno un picco troppo stretto per cui non  
609 puoi coprire grosse zone e soprattutto se sbagli rischi davvero di danneggiare molto i tessuti sani.

610

611 **B.1 Cell survival curves**

612 Curva di efficacia del trattamento in funzione della dose:

$$\frac{S(D)}{S(0)} = e^{-F(D)} \quad (\text{B.1})$$

613 dove  $F(D)$

$$F(D) = \alpha D + \beta D^2 \quad (\text{B.2})$$

614 dove  $\alpha$  e  $\beta$  rappresentano due tipi di danno diversi: coefficients, experimentally determined, characterizing the radiation response of cells. In particular, alpha represents the rate of cell killing by single ionizing events, while beta indicates the maximal rate of cell killing by double hits observed when the repair mechanisms do not activate during the radiation exposure. Si ottiene una curva di sopravvivenza dove si vede la possibilità delle cellule di autoripararsi. A basse dosi infatti le cellule possono ripararsi.

620

621 Per introdurre l'effetto FLASH introduco prima la therapeutic window.

622

623 TCP è la tumor control Probability che indica la probabilità delle cellule del tumore di essere uccise dopo una certa dose (con in riferimento a dose in acqua)

624 Se una media di  $\mu(D)$  di cellule di tumore are killed con una dose D, la probabilità che n cellule sopravvivono è data da  $P(n|\mu)$  poisson:

$$P(n|\mu) = \frac{\mu(D)^n e^{-\mu(D)}}{n!} \quad (\text{B.3})$$

$$TCP(D) = P(n=0|\mu(D)) = e^{-\mu(D)} \quad (\text{B.4})$$

627 D'altra parte hai una probabilità di fare danno su normal tissue NTCP Normal Tissue Complication Probability, che rappresenta il problema principale e che limita la massima radiazione erogabile  
628 Una scelta bilanciata si applica guardando a questi due fattori; si usa il therapeutic index definito  
629 come TCP/NTCP.

631 La cosa ottimale è ampliare la finestra del therapeutic ratio.

632 CONV-RT 0.01-5 Gy/min. A typical RT regime today consists of daily fractions of 1.5 to 3  
633 Gy given over several weeks.

634 Nell Intra operative radiation therapy (IORT), where they reach values respectively about 20 and  
635 100 times greater than those of conventional radiation therapy.

636 FLASH vuole ultrahigh mean dose-rate (maggioranza di 40 Gy/s) in modo da ridurre anche il  
637 trattamento a meno di un secondo.

638

## 640 **B.2 FLASH effect**

641 Ci sono due effetti che affettano il flash effect e la sua applicabilità: Dose rate effect e oxygen

642

643 Cellule che esibiscono hypoxia (cioè cellule che non hanno ossigeno sono radioresistenti); al  
644 contrario normoxia e physoxia non lo sono. La presenza di ossigeno rende la curva steeper indicando  
645 che lo stesso danno si raggiunge a livelli di dose più bassi rispetto al caso senza ossigeno.

646 FIGURA con una curva a confronto con e senza ossigeno.

647 Typically, the OER is in the order of 2.5–3.5 for most cellular systems

648 Quindi si vogliono sfruttare questi effetti per diminuire la tossicità sui tessuti sani

649

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