Summary

Chapter 1

Introduction

Pixel detectors, members of the semiconductor detector family, have fastely been used since the first accelerator experiments for energy and position measurement. Because of their dimension (today $\sim$ 30 μm or even better) and their spatial resolution ($\sim$ 5-10 μm), with the availability of technology in 1980s they proved to be perfectly suitable for vertex detector in the inner layer of the detector.
Technological development has been costant from then on and today almost every high energy physics (HEP) experiment employs a pixels detector; hybrid pixel currently constitute the state-of-art for large scale pixel detector but experiments began to look at the more innovative monolitic active pixels (MAPS) as perspective for their future upgrades, as BelleII, or they already have installed them, as ALICE.

Requirement imposed by accelerator are stringent and they will be even more with the increase of luminosity/intensity, in terms of radiation hardness, efficiency and occupancy, time resolution, material budget and power consumption.

Qual è invece la richiesta per la dosimetria?

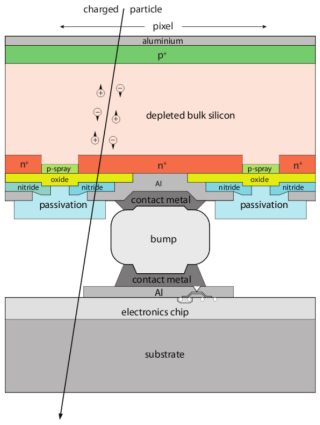
Chapter 2

Pixel detectors

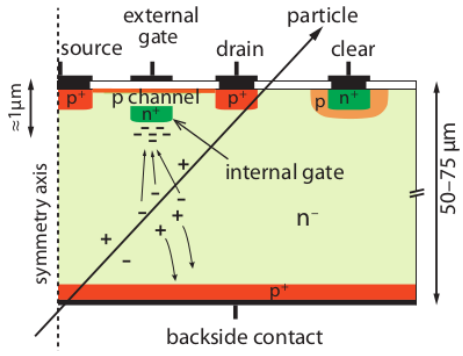
2.1 Hybrid pixels

Hybrid pixels are made by two parts (fig. 2.1a), the sensor and the electronics: for each pixel this two parts are welded together through microconnection (bump bond) using the so called flip-chipping technique.
Hybrid pixels provide a practical system where readout and sensor, being independent, can be optimize separately although the particular and sophisticated procedure to bond sensor and ASIC makes them difficult to produce and to test (sensor can't be test separatelly but need to be connected with the readout), delicate, especially for high levels of radiation, and also expensive.
An hot topic for accelerator experiment is the material budget that represents the main limit for momentum measurement resolution in a magnetic field; since hybrid are thicker ($\sim$ hundreds μm) than monolithic ones (even less than 100 μm), using the latter the material budget can be down by a third: typical value for hybrid pixels is 1.5 % X_0 per layer, while for MAPS is ????
Among other disadvantages of hybrid pixels there is the bigger power consumption that implies, by the way, a bigger cooling system that implies in turn increase in material too.

DEPFET are the first attempt towards the integration of the FE on the sensor bulk: they are typically mounted on a hybrid structure but they also integrate the first amplification stage.
Each pixel implements a MOSFET transistor (a p-channel in fig. 2.1b): an hole current flows from source to drain which is controlled by the external gate and the interlan gate together. The intenal gate is made by a deep $n+$ implant towards which electrons drfit after being created in the subrate; the accumulation of electrons in the region underneath the n implant changes the potential and controls the transistor current.
DEPFET typically have a good S/N ratio: this is due to the small capacity, the amplification on the pixel and the large deplation region (they are fully deplated and this provide a high number of e/h couple **??**). Since they need to be connect with ASIC the limiting factor still is the material budget.



(a) Concept cross section of hybrid pixel



(b) Concept cross section of a DEPFET

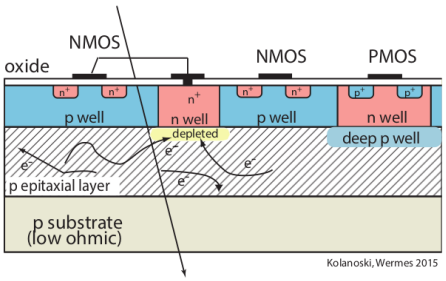


Figure 2.2: Concept cross section of MPAS pixel

2.2 CMOSS MAPS and DMPAS

Monolitic active pixels accomodate on the same wafer both the sensor and the front end electronics, with the second one implanted on top, a feature that makes them really advantageous.
MAPS have been first proposed and realized in 1990s and their usage has been enabled by the development of the electronic sector which guarantees the decrease in CMOS dimension at least every two years, as stated by the Moore's law[1].
As a matter of fact the dimension of componenents, their organization on the pixel area and logic density are important issues for the designers; typically different decisions are taken for different purposes. Related with this thematic there is the possibility of integrating or not on the pixel area a memory which would allow the use of a trigger.

Discorso fatto con Ludovico sul fatto che i CMOSS tirano meno rispetto al circuito analogico. Scrivi perchè si usano i CMOSS invece dei transistor: discorso sulla potenza e sull'elettronica digitale.
UNA COSA (TROVATA SULLE SLIDES IFIP DI FORTI)È CHE ELETTRONICA RICHIEDE BASSA RESISTIVITÀ MENTRE ALTA RHO È RICHIESRA PER IL SENSORE. UN ALTRO PROBLEMA DEL CONNUBIO TRA LE DUE PARTI È LA TEMPERATURA: ELETTRONICA LAVORA ANCHE A T ALTE, SENSORE NO PERCHÈ SENNO HAI LEACKAGE CURRENT

Monolithic active pixel can be distinguish beteween two main category: MAPS and depleted MAPS (DMAPS).

MAPS (figure a 2.2) have typically an epilayer in range 1-20 μm and because they are not depleted, the charge is mainly collected by diffusion rather then by drift. This makes the path of charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the collection could be partial expecially after an irradiation of the detector, when the trapping probability become highter.
DMAPS (figure b 2.2) are instead MAPS depleated with d typically in $\sim$ 25-150 μm (eq. A.1) which extends from the diode to the deep p well, and sometimes also to the the backside (in this case if one wants to collect the signal also on this electrode, additional process must be done).
The sensor in the scheme (figure 2.2) implements an n well as collection diode; to avoid the others n wells (which contain PMOS transistor) of the electronic circuit would compete in charge collection and to shield the CMOS circuit from the substrate, additionaly underlying deep p well are needed.

2.2.1 DMAPS: large and small fill factor

There are two different sensor-design approaches (figure 2.3) to DMAPS:

- large fill factor: a large collection electrode that is a large deep n-well and that host the embedded electronics
- small fill factor: a small n-well is used as charge collection node

To implement a uniform and stronger electric field, DMAPS often uses large electrode design that requires multiple wells (typically four including deep n and p wells); this layout adds on to the standard terms of the total capacity of the sensor a new term (fig. 2.4), that contributes to the

[1]Moore's law states that logic density doubles every two years.

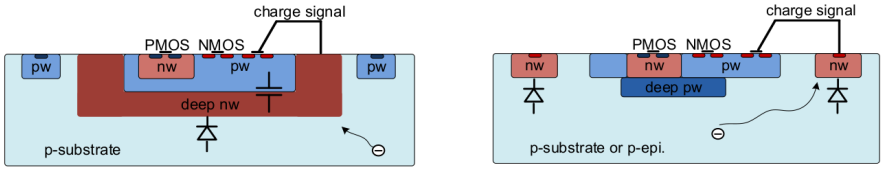


Figure 2.3: Concept cross section with large and small fill factor

	small fill factor	large fill factor
small sensor C	$\surd$ ($<$ 5 fF)	$\times$ ($\sim$ 100-200 fF)
low noise	$\surd$	$\times$
low cross talk	$\surd$	$\times$
velocity perfomances	$\surd$	$\times$ ($\sim$ 100 ns)
short drift paths	$\times$	$\surd$
radiation hard	$\times$	$\surd$

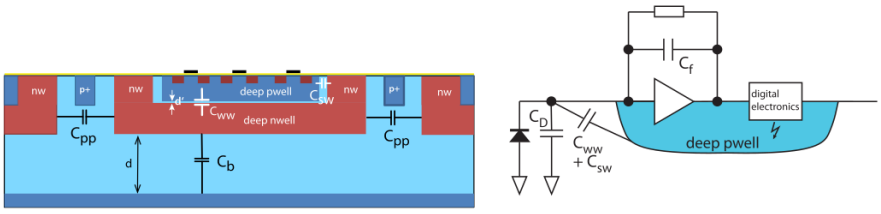
Table 2.1: Small and large fill factor DMAPS characteristics

total amplifier input capacity. In addition to the capacity between pixels (C_{pp}) and between the pixel and the backside (C_b), a non negligible contribution comes from the capacities between wells (C_{SW} and C_{WW}) needed to shield the embedded electronics. These capacities affect the thermal and 1/f noise of the charge amplifier and the τ_{CSA} too:

$$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{C_D^2}{\tau_{sh}} \qquad (2.1)$$

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{C_D}{C_f} \qquad (2.2)$$

where g_m is the transconductance, τ_{sh} is the shaping time.
By the way a big problem coming from this input capacity could be the coupling with the electronics resulting in cross talk: noise induced by a signal on neighbouring electrodes; since digital switching in the FE electronics do a lot of oscillations this problem is especially connected with the intra wells capacities. So, larger charge collection electrode sensors provide a uniform electric field in the bulk



(a) (b)

Figure 2.4: C_{pp}, C_b, C_{WW}, C_{SW}

that results in short drift path and so in good collection properties, especially after irradiation, when trapping probability can become an issue. The drawback of a large fill-factor is the large capacity ($\sim$100 fF): this contributes to the noise and to a speed penalty and to a larger possibility of cross talk.

The small fill-factor variant, indeed, benefits from a small capacity (5-20 fF), but suffers from a not uniform electric field.
These two different types of sensor require different amplifier: the large elctrode one is coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec **??**).

2.2.2 A modified sensor

A process modification that has become the standard solution to combine the carateristic of a small fill factor sensor (small input amplifier capacity) and of large fill factor sensor (uniform electric

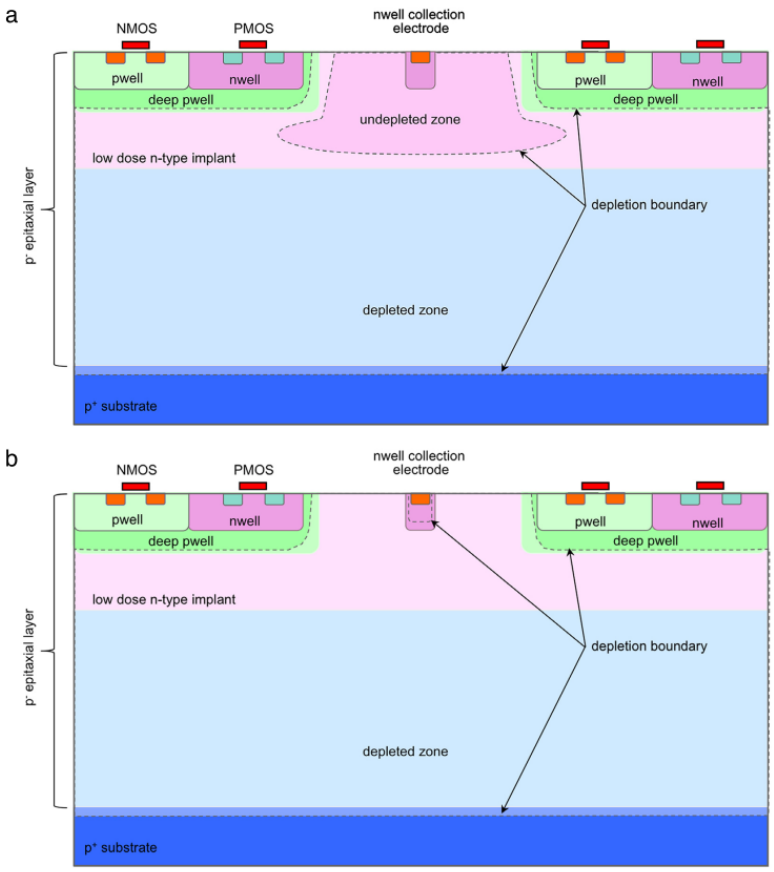


Figure 2.5: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the deplation is partial, while in (b) the pixel is fully depleted.

field) is the one carried out for ALICE upgrade about ten years [**AProcessModification**].
A compromise between the two sensors could also be making smaller pixels but this solution requires reducing the electronic circuit area, so a completelly new pixel layout should be think. The advantageous of the modification lies in its versatility: both standard and modified sensor are often produced for testing in fact.

The modification consists in inserting a low dose implant under the electrode: before the process modification the depletion region extends below the diode towards the substrate and it doesn't extend laterally so much even if a high bias is applied to the sensor (figure 2.5).
After two distinct pn junctions are built: one between the deep p well and the n^- layer, and the other between the n^- and the p^- epitaxial layer, extending to the all area of the sensor.
Since deep p well and the p-substrate are separated by the deplation region, the two p electrodes can be biased separatelly[2]; this is beneficial to enhance the vertical electric field component.
The doping concentration is a trimmer parameter: it must be high enought to be greater than the epitaxial layer to prevent the punchthrought between p-well and the substrate, but it must also be lower enought to allow the depletion without reaching too high bias.

2.3 Analog front end

After the creation of a signal on the electrode, the signal enters in the front end circuit (fig.2.6), ready to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an efficient, high-speed readout architecture, consuming as low power as possible must be provided by the read out integrated electronics (ROIC).
Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually

[2]This is true in general, but it can become false if other doping characteristics are implemented; we'll see that this is the case of Monopix1

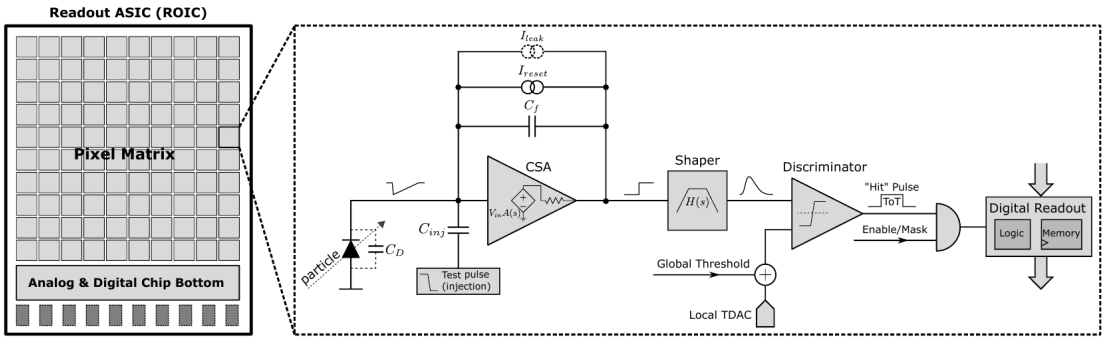


Figure 2.6: Readout FE scheme: il preampl è un CSA, ma se ci metti un feedback resistivo puoi fare un voltage o current amplifier

often is the only amplification stage) with a reset to the baseline mechanism and a leakage current compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise before the amplification stage in order to not moltiplicate that noise, and optimized the discriminator to cut noise-hits much as possible.

2.3.1 Preamplifier

Even if circuits on the silicon crystal are only costruct by CMOSS, a preamplifier can be modellized as an operational amplifier (OpAmp) where the gain is determined by the input and feedback impedance (first step in figure 2.6):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \tag{2.3}$$

Depending on whether a capacity or a resistance is used as feedback, respectevely a charge or a voltage amplifier is used: if the voltage input signal is large enought and have a sharp rise time, the voltage sensistive preamplifier is prefered. As already anticipated this flavor doen't suit to large fill factor MAPS whose signal is already enought high: $v_{in} = Q/C_D \approx 3\text{fC}/100\text{ pF} = 0.03$ mV, but it's fine for the small fill factor ones: $v_{in} = Q/C_D \approx 3\text{fC}/3\text{ pF} = 1$ mV.
In the case of a resistor feedback, if the signal duration time is longer than the discharge time ($R_S C_D$) of the detector the system works as current amplifier, as the signal is immediately trasmit to the amplifier; in the complementary case (signal duration longer than the discharge time) the system integrates the current on the C_D and operates as a voltage amplifier.

2.3.2 ALPIDE-like front end

I've already mentioned ALICE pixel dector talking about the new process modification, now the ALICE name comes up again talking about FE: this is because ALPIDE (ALice PIxel DEtector) is one of the first MAPS detector (TowerJazz 180 nm CMOS) installed [3], therefore it is the current state of art and most of the following designers took inspiration form that. Its FE became a standard for all the following chip: ARCADIA MD1 and Monopix1 are no exception, this is why I'm going to explain some principals characteristics of how it works[**ALPIDE-FE**]

Carica fa un segnale negagtivo di $\Delta V_{PIX\_IN} = Q_{IN}/C_{IN}$ su PIX IN. M1 fa da source follower con IBIAS , costringendo la tensione al source a seguire la tensione di M1 al gate.
This causes transfer of charge $Q_{source} = C_{source}\Delta V_{PIXIN}$ from C_{source} to C_{OUT} in case the current sink to GND is IBIAS. So ideally:

$$\Delta V_{OUT_A} = \frac{C_{Source}}{C_{OUTA}} \frac{Q_{IN}}{C_{IN}} \tag{2.4}$$

A second branch (M4, M5) is used to generate a low frequency feedback. The voltage bias VCASN and current bias ITHR define the baseline value of OUTA and the return to baseline after a particle

[3] It was installed in the Inner Tracking System during the second long shut down of the LHC in 2019

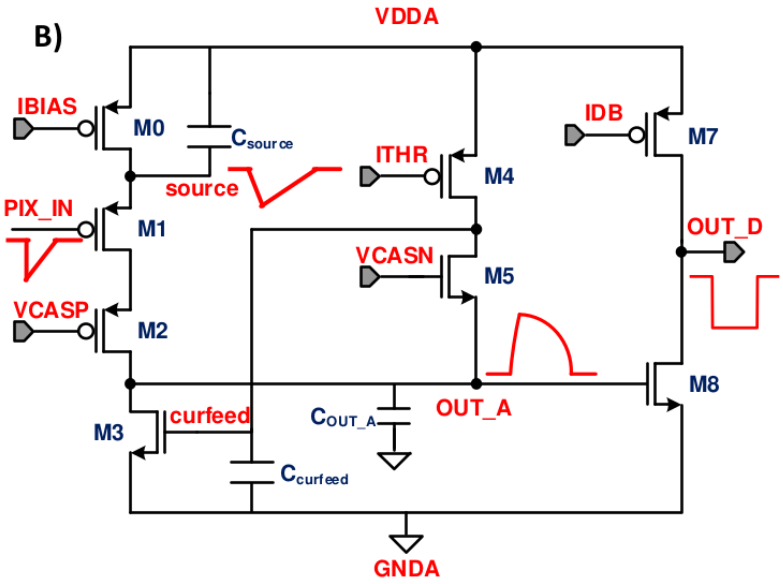


Figure 2.7: ALPIDE like FE

hit. The distance of the OUT A baseline voltage to the point where IM8 = IDB defines the charge threshold.

2.4 Readout logic

Readout logic includes the part of the circuit which takes the FE output singal, processes it and then trsamit it out of pixel and/or out of chip; depending on what data one wants to store, different readout characteristics must be provided.

To store the analogical informations (i.e. charge collected, evolution of signal in time, ...) big buffers and a big bandwidth are needed; the problem that doesn't occur, or better occur only really high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is recorded).
A common compromise often made is to save the time over threshold (ToT) of the pulse in clock cycle counts; this is a relatively coarse requirement (ToT could be trimmer to be less then a dozen bits) but, being correlated with the deposited charge by the impinging particle in the detector, it provides a sufficent information.

RISISTEMA: The ToT method is essentially a Time to Digital Conversion (TDC) using the BCID time stamp to measure the number of clock cycles during which the signal is higher than the discriminator threshold. The BCID time stamp is latched into local registers when the leading edge and trailing edge transitions are detected, and the ToT is obtained by their difference. The ToT should ideally be an almost linear function of the input charge, that is usually achieved by a constant current reset mechanism. The discharge current that determines the ToT slope is adjusted according to the desirable resolution, the BCID time stamp frequency and number of bits and the readout architecture capabilities

BANDA-MEMORIA-
Moreover the readout architetcture can be full, if every hit from every pixel must eventually make its way to the data output, or triggered, if hits are recorded during a trigger signal. Again, on the one hand the triggered-readout needs buffers and storage memories (therfore needs space on the pixel are to accomodate them), on the other the full readout, because there is no need to store hit data on chip, needs an high enough bandwidth.
I will now give some hints about the optimization between this two trends.

If all the pixels in a column share a data bus to the EoC and only one pixel at a time can be use and there aren't any storage memory, the column (si comporta) as a single server queue and the probability for waiting a time greater than t with an input hit rate μ in a column and an output

bandwidt B_W is:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \tag{2.5}$$

To avoid hit loss (let's neglect the contribution to the inefficency of the dead time τ), for example imponing $P(T > t)$ ∼0.001, one obtains $(B_W - \mu)t_t$ ∼6, where t_t is the time to transfer the hit; since t_t is small, one must have $B_W \gg \mu$, that means a high bandwidth.

If shift registers (SR) are used to transfer data instead of buses the bandwidth B_W of the SR corresponds to the clock speed; differently from the bus case, each pixel sees a different bandwidth depending on the position on the queue: the first pixel in the priority logic chain , that is the closest pixel to the EoC typically, sees a full bandwidth, but the next pixel sees less bandwidth because occasionally it will be blocked by data from the previou pixel.
Then the condition about the bandwidth and the hit rate become: $B_{W,i} > \mu_i$, where the index i means the requirement is for a single pixel. If all the pixels on the same column have the same rate $\mu = N\mu_i$ and the condition become $B_W > \mu$. The bandwidth must be chosen such that the mean time between hits of the last pixel in the readout chain is bigger than that.
Questa condizione tra banda e rate sulla colonna ci dice già una cosa importante: il fatto che l'algoritmo di lettura column drain non è scalabile: infatti se aumento il numero di pixel sulla stessa linea di lettura rischio di violare la condizione.
La scalabilità risiede quindi nel poter utilizzare tanti chip piccoli.

If instead the hits are stored in buffers until a trigger signal arrives, the input rate to column bus is reduced as $\mu' = \mu t$, where t is the trigger rate. This implies that $B_W \gtrsim \mu'$, that is a very relaxed condition on the bandwidth, but the limiting factor is the amount of memory which the pixel area can host; the amount needed depends on the trigger frequency $1/t$ as $\propto \mu/t$, that means that the highter the trigger frequency and the highter the hit rate that can be handled.
In order to have an efficient use of memory on pixel area it's convenient grouping pixels into regions with shared storage. Let's look what happens when single pixel local storage is used: for example, suppose to have a 50 kHz single pixel hits rate and a trigger frequency of 1/5 microseconds, allora il rapporto dei due è 0.25 e cioè il numero medio di hit perse per trigger signal.
usando la statistica di Poisson, uno dovrebbe storare 3 hit per pixel se volesse raggiungere il 99.9 per cento di efficienza.
Consideriamo cosa succede se faccio un gruppo di quattro pixel: allora se il rate medio di 1 hit sui 4 pixel (sempre 50 khz di single pixel) per ogni trigger signal, allora se volessi un'eff di 99.9 avrei bisogno di un buffer depht of 5 region-hits. Quindi significa che in media per ogni pixel avrei 5/4 = 1.25 buffer depht, minore di quello di prima.
L'architettura di lettura che colloca i pixel in regioni da 4 si chiama FE-I4.

One standard way to reduce the readout bandwidth is to implement the zero suppression on the pixel: only informations about channels with an hit (when signal exceeds the discriminator threshold) are read. Per gli esperimenti agli acceleratori, e soprattutto per gli esperimenti che intendono aumentare la luminosita, è sicuramente di particolare importanza l'occupancy dei pixel: sia il rate del noise va mantenuto basso, sia un bisogna prestare attenzione al pile up. L'occupancy tra le altre cose dipende dalla differenza tra threshold e offset del segnale, per cui uno può agire sulla soglia per poterla cambiare.
FORMULA? slide APSEL
Una soluzione potrebbe essere mettere un trigger e in sincro con il beam mettere il reset avviene ad ogni beam collision; questo consuma però un sacco di power.

2.4.1 Colum-drain readout

COLUM DRAIN READ OUT
Il modo con cui vengono lette le hit su una matrice è il column drain readout.
The simple 3T (three transistor) readout has a row select, a source-follower buffer and an input baseline reset;

Chapter 3

Use of pixels detector

3.1 Tracking in HEP

Per gli acceleratori la richieste sono molto stringenti e lo saranno sempre di più con l'aumento dell' intensità o della luminosità in termini di radiation hardness (per HL-LHC for example expected in 5 anni 500 Mrad e NIEL di 10 alla 16), efficiency e occupancy (efficienza alta dopo tanta radiazione e noise occupancy bassa), time resolution (bunch crossing 40 Mhz), material budget e power consumption (material budget below 2per cento e power consumption 500 mW/cm2)

Position measurement resolution

Depending on the type of signal reading the spatial resolution is $\sigma_x = \frac{p}{\sqrt{12}}$ where p is the pitch between pixels, or even better if other analogica information, as the charge, are read and capacitive charge division method is applied.

3.1.1 Who chose MAPS?

3.2 Dosimetry

3.2.1 Applicability to FLASH radiotherapy

Chapter 4

TJ-Monopix1

Subm. Aug. 2016, mentre monopix 2 sub a aprile 2020
TJ 180 nm CMOSS process was firstly used for Alice inner tracker system: ALPIDE (primo ad avere FE sul pixel e sparsiefied zero suppression readout).

TJ monopix ha un colum drain readout proven by the ATLAS FEI3 front end chip (I. Peric et al., The FEI3 readout chip for the ATLAS pixel detector, Nucl. Instrum. Meth. A 565 (2006) 178, ed. by J. Grosse-Knetter, H. Krueger, and N. Wermes (cit. on pp. 42, 50, 60))

Epitaxial layer thickness: più grande è e più carica viene depositata da una MIP, però devi fare attenzione alla forma della zona svuotata perchè può portare ad un aumento della charge sharing tra pixel vicini. Se il diodo è molto piccolo rischi che l'efficienza di collection è diminutia perchè l'intensità del campo elettrico è più bassa intorno al diodo, e hai più charge sharing.

50x50 um2 e l'elettrodo è 3 um

INput coupling: differenza tra AC (flavor HV) e DC. 4 flavors

4.1 Four FE flavors

4.2 Readout logic

viene da lf monopix
TJ-Monopix is a triggerless. It sends data whenever it gets hits. Only thing we can do is to record timetamp of the external triggers and correlate with the hits.

4.2.1 Data-packets structure

4.2.2 Dead time measurement

4.3 From TJ-Monopix1 to Obelix

Chapter 5

Arcadia-MD1

ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node with six metal layer **??**. The standard p-type substrate was replaced with an n-type floating zone material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).

Wafer thinning and backside litography were necessary to introduce a junction at the bottom surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side. C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthought è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL, COME VENGONO FATTI I MAPS COME FAI LE GIUNZIONI

It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.

It is operated in full depletion with fast charge collection by drift.

Prima SEED si occupa di studiare le prestazioni: oncept study with small-scale test structure (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il pwell e quanto al diodo. ..

5.1 Readout logic and data structure

5.1.1 Matrix division and data-packets

The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei serializzaatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le varie cordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve, e devi accennare al timestamp

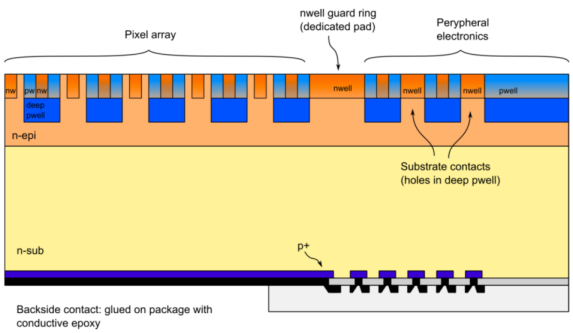


Figure 5.1: Concept cross section of one pixel

"A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively large core allows one to take full advantage of digital sybthesis tools to implement complex functionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della review.

5.2 From SEED to MD2

TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column (512x2) Core (32x2) Region (4x2)

Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

"DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for example 8b10b encoding n =5"

Chapter 6

Threshold and noise characterization

6.1 Threshold and noise: figure of merit for pixel detectors

The signal to threshold ratio is the figure of merit for pixel detectors.

la soglia deve essere abb alta da tagliare il rumore ma abb bassa da non perdere efficienza. Invece di prendere il rapporto segnale rumore prendi il rapporto segnale soglia. Perchè? la soglia è collegato al rumore, nel senso che: supponiamo di volere un occupancy di 10-4 allora sceglierò la soglia in base a questo. (plot su quaderno) Da questo conto trovo la minima soglia mettibile
In realtà quello che faccio è mettere una soglia un po' più grande perchè il rate di rumore dipende da molti fattori quali la temperatura, l anneling ecc, e non voglio che cambiando leggermente uno di questi parametri vedo alzarsi molto il rate di rumore. In realtà non è solo il rumore sensibile a diversi fattori, ma anche la soglia: ad esempio la cosa classica è la variabilità della soglia da pixel a pixel.
In questo modo rumore e soglia diventano parenti.
Review pag 26.

The noise requirement can be expressed as:

Questo implica tra le altre cose che voglio poter assegnare delle soglie diverse a diversi pixel: Drawback è dare spazio per registri e quantaltro.
Questo lascia però ancora aperto il problema temporale delle variazioni del rumore: problema per cui diventano necessarie le misure dei sensori dopo l'irraggiamento.

Per arcadia i registri (c'è un DAC) per la soglia (VCASN) si trovano in periferia. Non fare trimming sulla soglia è uno dei problemi che si sono sempre incontrati: a casusa dei mismatch dei transistor le soglie efficaci pixel per pixel cambiano tanto. La larghezza della s curve è il noise se assumi che il noise è gaussiano

Il trimming della soglia avviene con dei DAC: la dispersione della soglia dopo al tuning e dovuta al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \tag{6.1}$$

dove il numero di bit cambia varia tra 3-7 tipicamente. Monopix è 7 Arcadia 6

Each ROIC is different in this respect, but in general the minimum stable threshold was around 2500 electrons (e) in 1st generation ROICs, whereas it will be around 500 e for the 3rd generation. This reduction has been deliberate: required by decreasing input signal values. Large pixels (2 104 um2), thick sensors (maggiore di200 um), and moderate sensor radiation damage for 1st generation detectors translated into expected signals of order 10 ke, while small pixels (0.25 104 um2), thinner sensors (100 um), and heavier sensor radiation damage will lead to signals as low as 2 ke atthe HL-LHC
The ENC can be directly calculated by the Cumulative Distribution Function (CDF) (scurve) obtained from the discriminator "hit" pulse response to multiple charge injections

6.2 TJ-Monopix1 characterization

Com'è fatto il set up per le misure.
FPGA BB, Chip con FE board, qualche foto

6.3 ARCADIA-MD1 characterization

Com'è fatto il set up per le misure.
FPGA BB, Chip con FE board, qualche foto

Appendix A

Pixels detector: a brief overview

A.1 Signal formation

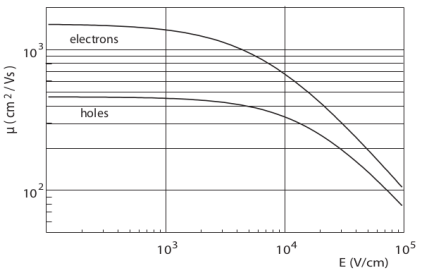
When a charge particle passes through a pixel and loses energy by ionization a part of that energy is used to generate electron-hole pairs (an other part is used for other processes, as the lattice excitation) which are then separated by the elettric field and collected at their respectivelly electrodes (p for holes and n for electrons)[1]; by the drift of these charges, a signal i_e is generated on the electrode e as stated by the Shockley–Ramo's theorem:

$$i_e(t) = -q\, v(t)\, E_{WF,e} \tag{A.1}$$

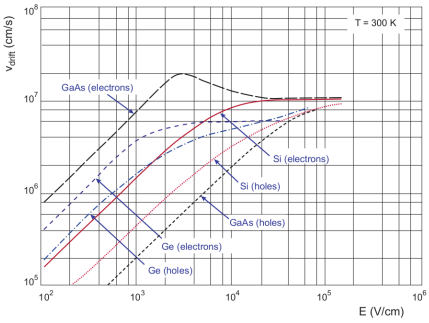
where $v(t)$ is the instantaneous velocity of the charge q and E_{WF} is the weighting field, that is the field obtained biasing the electrode e with 1V and all the others with 0V.
The drift velocity of the charge depends on the elettric field and on the mobility of the particle:

$$v = \mu(E)\, E \tag{A.2}$$

where $\mu(E)$ is a function of the electric field and is linear with E only for small E: at highter values the probability of interactions with optical phonons increases and the mobility drops and this leads to an indipendency of the velocity from the electric field (fig. A.1b).
SECONDO ME MANCA ANCORA UNA FRASE DI CONNESSIONE



(a) Typical values for elecrons and holes mobility in silicon at room temperature are $\mu_n \sim 1450\ cm^2/Vs$, $\mu_h = 500$

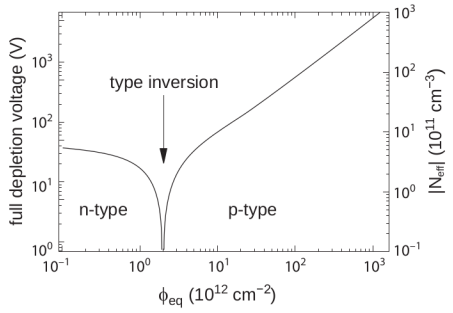


(b) Drift velocity at room temperature in different semiconductors

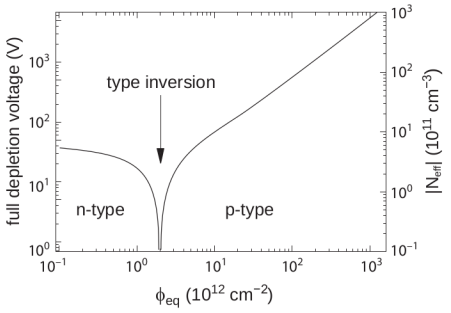
The average energy needed to create a pair at 300 K in silicon is $w_i = 3.65$ eV, that is more than the mean ionization energy because of the interactions with phonon, hence for a MIP the most probable value of charge released in the semiconductor (assuming a stopping power in silicum of 1 MeV g/cm^2) is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 100\, e/h \sim \frac{1.6\, 10^{-2} fC}{\mu m} \tag{A.3}$$

[1]Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout



(a) 1a



(b) 1b

It is foundamental that pairs e/h are produced in the depleted region of the semiconductor where the probability of recombination with charge carriers is low to avoid loss of signals.
Pixel detectors are then commonly reverse biased: a positive bias is given to the n electrode and a negative to the p to grow the depletion zone in the epitaxial layer below the electrode. The width of the depletion region is related with the extern bias V_{ext}, the resistivity ρ and also with the dopant:

$$d_n \sim 0.55\sqrt{\frac{\rho}{\Omega cm}\frac{V_{ext}}{V}}\mu m \qquad \text{(A.4)} \qquad\qquad d_p \sim 0.32\sqrt{\frac{\rho}{\Omega cm}\frac{V_{ext}}{V}}\mu m \qquad \text{(A.5)}$$

DA DOVE VENIVA QUESTA DIFFERENZA? DALLA MOBILITÀ MA NON MI RICORDO COME CI SI ARRIVAVA.
For that reason high resistivities wafer (100 $\Omega cm - k\Omega cm$) are typically prefered beacause they allow bigger deplation zone with smaller voltage bias.

A.2 Radiation dameges

Radiation hardeness is a fundamental requirement for pixels detector especially in HEP since they are almost always installed near the interaction point where there is a high energy level of radiation. At LHC the ϕ_{eq} per year in the innermost pixels detector is $10^{14} n_{eq}/cm^2$; this number reduces by an order passing to the outer tracker layer. (referenza: pag 341 Wermes)
Here the high fluence of particles can cause a damage both in the substrate of the detector and in the superficial electronics.

The first one has a principal non ionising nature (non ionizing energy loss, NIEL) since it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV neutrons. Differently, surface damages are principally due to ionising energy loss.

DUE PAROLE IN PIÙ SUL SURFACE DAMAGE
a charge accumulation in oxide (S_iO_2) can cause the generation of parasitic current with an obvious increase of the 1/f noise.
Anyway surface damages are less relevant then the previous one since with the development of microelectronics and with the miniaturization of components (in electronic industry 6-7 nm transistors are already used, while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit is reduced.

Let's spend instead two more other words on the more-relevant substrate damages: the general result of high radiation level is the creation of new energy levels within the silicon band gap and depending on their energy-location their effect can be different, as described in the Shockely-Read-Hall (SRH) statistical model. The three main consequence of radiation damages are the changing of the effect doping concentration, the leakage current and the increasing of trapping probability.

Changing of the effective doping concentration: is associated with the creation/removal of donors and acceptors center which trap respectively electrons/holes from the conduction band

and cause a change in effective space charge density. Even an inversion (p-type becomes n-type[2]) can happen: indeed it is quite common and happens at not too high fluences ($\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$). A changing in the doping concentration requires an adjust of the biasing of the sensor in time (eq.A.1) and sometimes can be difficult keeping to fully deplete the bulk.

Leakage current: is associated with the generation-recombination centres. It has a strong dependence with the temperature ($I_{leak} \propto T^2$), whose solution is therefore to operate at lower temperature.

Increase of trapping probability: È ASSOCIATA CON QUALE TIPO DI CREAZIONE DI LIVELLO ENERGETICO? since the trapping probability is costant in the depleted region, the collected charge decreases exponentially with the drift path. The exponential coefficient, that is the mean trapping path, decreases after irradiation and typical values are 125-250 μm and must be compared with the thickness of the depleted region which () corresponds to the mean drift path.

Different choises for substate resistivity, for junctions type and for detector design are typically made to fight radiation issues. Some material with high oxygen concentration (as crystall produced using Czochralki (Cz) or float-zone (Fz) process (CONTROLLA SE SONO LORO QUELLI GIUSTI)) for example, show a compensation effect for radiation damage; an other example is the usage of n+ -in-p/n sensors (even if p+ -in-n sensors are easier and chieper to obtain) to get advantage of inversion/to have not the inversion (since they are already p-type). After inversion the n+p boudary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be placed near the diode[3].

Radiation damage in CMOS circuits is entirely due to charge carriers generated by ionization in the dielectric layers of the process

[2]L'INVERSIONE OPPOSTA NON CE L'HAI PERCHÈ L'INVERSIONE È ASSOCIATA AD UN CAMBIO DELLA CONCETRAZIONE DA ... A ...
E COME MAI L'ALTRO NON È FAVORITO?

[3]With inversion some isolation process of electrodes can become important and p-spray/p-stop tecnique can eventually be applied. PERCHÈ CON L'INVERSIONE TI POTREBBE SERVIRE UNA TECNICA DI ISOLAMENTO?

Appendix B

FLASH radiotherapy

La radioterapia si usa nel 60 per cento dei pazienti, sia come cura che come trattamento palliativo. Si associa spesso ad altre cure e si può fare prima/durante/dopo un intervento.

Si può fare in modi diversi: da dentro (brachytherapy) oppure da fuori (quella standard). Un requisito importante è la delinazione del target (non vuoi rischiare di beccare i tessuti sani), per cui prima tipicamente si fanno esami di imaginig del tumore. TIpicamente anche gli acceleratori stessi per la terapia sono provvisti di radiografia.

Un problema dei fotoni ad esempio è che il loro rilascio di dose è lineare, per cui danneggi anche i tessuti sani. Il problema dei protoni invece è che hanno un picco troppo strtto per cui non puoi coprire grosse zone e sorpattuto se sbagli rischi davvero di danneggiare moooolto i tessuti sani.

B.1 Cell survival curves

Curva di efficacia del trattamento in funzione della dose:

$$\frac{S(D)}{S(0)} = e^{-F(D)} \tag{B.1}$$

dove F(D)

$$F(D) = \alpha D + \beta D^2 \tag{B.2}$$

dove α e β rappresentano due tipi di danno diversi: coefficients, experimentally determined, characterizing the radiation response of cells. In particularly, alpha represents the rate of cell killing by single ionizing events, while beta indicates the maximal rate of cell killing by double hits observed when the repair mechanisms do not activate during the radiation exposure. Si ottiene una curva di sopravvivenza dove si vede la possibilità delle cellule di autoripararsi. A basse dosi infatti le cellule possono ripararsi.

Per introdurre l'effetto FLASH instroduco prima la therapeutic window.

TCP è la tumor control Probability che indica la probabilità delle cellule del tumore di essere uccise dopo una certa dose (con in riferimento a dose in acqua)
Se una media di $\mu(D)$ di cellule di tumore are killed con una dose D, la probabilità che n cellule sopravvivono è data da $P(n|\mu)$ poisson:

$$P(n|\mu) = \frac{\mu(D)^n e^{-\mu(D)}}{n!} \tag{B.3}$$

$$TPC(D) = P(n = 0|\mu(D)) = e^{-\mu(D)} \tag{B.4}$$

D'altra parte hai una probabilità di fare danno su normal tissue NTCP Normal Tissue Complication Probability, che rappresenta il problema principale e che limita la massima radiazione erogabile Una scelta bilanciata si applica guardando a questi due fattori; si usa il therapeutic index definito come TCP/NTCP.

La cosa ottimale è ampliare la finestra del therapeutic ratio.

CONV-RT 0.01-5 Gy/min. A typical RT regime today consists of daily franctions of 1.5 to 3 Gy given over several weeks.
Nell Intra operative radiation therapy (IORT), where they reach values respectively about 20 and 100 times greater than those of conventional radiation therapy.

FLASH vuole ultrahigh mean dose-rate (maggione di 40 Gy/s) in modo da ridurere anche il trattamento a meno di un secondo.

B.2 FLASH effect

Ci sono due effetti che affect the flsh effect and la sua applicabilità: Dose rate effect e oxygen

Cellule che esibiscono hypoxia (cioè cellule che non hanno ossigeno sono radioresistenti); al contrario normoxia e physoxia non lo sono. la presenza di ossigeno rende la curva steeper indicando che lo stesso danno si raggiunge a livelli di dose più bassi rispetto al caso senza ossigeno.
FIGURA con una curva a confronto con e senza ossigeno.
Typically, the OER is in the order of 2.5–3.5 for most cellular systems

Quindi si vogliono sfruttare questi effetti per diminuire la tossicità sui tessuti sani