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# <sup>46</sup> Chapter 1

## <sup>47</sup> Introduction

<sup>48</sup> Pixel detectors, members of the semiconductor detector family, have significantly been used at the  
<sup>49</sup> accelerator experiments for energy and position measurement. Because of their dimension (today  
<sup>50</sup>  $\sim 30 \mu\text{m}$  or even better) and their spatial resolution ( $\sim 5\text{-}10 \mu\text{m}$ ), with the availability of technology  
<sup>51</sup> in 1980s they proved to be perfectly suitable for vertex detector in the inner layer of the detector.

<sup>52</sup> Despite the monolithic pixels came up with CCDs, invented in 1969 and fastly used in cameras,  
<sup>53</sup> their usage had to wait for microelectronics developement: in MAPS device the readout electronics  
<sup>54</sup> is build on the pixel's area, then the pixel dimension is limited by the dimension of transistors. This  
<sup>55</sup> constraint favoured the usage in physics experiment of hybrid pixels, which currently constitute  
<sup>56</sup> the state-of-art for large scale pixel detector. These ones are made by two different wafer each one  
<sup>57</sup> containing or the sensor or the ASIC, which are after joined together through microconnection.  
<sup>58</sup> This structure allows a separate optimization for the two components and makes hybrid pixels  
<sup>59</sup> flexible and versatile.

<sup>60</sup> Requirement imposed by accelerator are stringent and they will be even more with the increase  
<sup>61</sup> of luminosity in terms of radiation hardness, efficiency and occupancy, time resolution, material  
<sup>62</sup> budget and power consumption. For this reason experiments (as ATLAS, CMS, BelleII) began to  
<sup>63</sup> look at the more innovative and well-performing monolithic active pixels (MAPS) as perspective for  
<sup>64</sup> their future upgrades.

<sup>65</sup> Che condiziona la risoluzione e l'efficienza di ricostruzione della sua traccia, e consumi del  
<sup>66</sup> detector, sono diventati sempre più rilevanti; molti esperimenti (ATLAS, CMS, BelleII,...) stanno  
<sup>67</sup> infatti valutando la possibilità di sostituire gli ibridi con i MAPS, che per i tempi precedenti offrono  
<sup>68</sup> prestazioni migliori, a scapito di tempi di lettura mediamente più lunghi, vista anche la positiva  
<sup>69</sup> esperienza di ALICE ad LHC, primo esperimento ad introdurre un detector a pixel monolitico.

<sup>70</sup> During my thesys I studied and characterised two monolithic active pixel chips, TJ-Monopix1  
<sup>71</sup> and MD1; these devices, that are still prototypes, have been conceived and designed for physics  
<sup>72</sup> experiments at colliders, space experiments and also for medical applications.

<sup>73</sup> il primo, TJ-Monopix1, è un prototipo di un modello selezionato per l'upgrade di Belle II  
<sup>74</sup> durante il LSD nel 2025 (il chip finale si chiamerà OBELIX e avrà come sensore TJ-Monopix2,  
<sup>75</sup> successore di Monopix1); il secondo chip è stato progettato da ARCADIA che potrà avere, nelle  
<sup>76</sup> versioni future, applicazioni in fisica medica, in esperimenti nello spazio e ai collider.

<sup>77</sup> Le differenze principali tra i due chip risiedono nel segnale fornito in output (Monopix fornisce il  
<sup>78</sup> tempo sopra soglia dell'impulso triangolare, proporzionale alla carica rilasciata nel sensore, mentre  
<sup>79</sup> arcadia fornisce un segnale puramente digitale), nella sequenza di readout dei pixel (monopix ha  
<sup>80</sup> una lettura puramente sequenziale di tipo "column drain") mentre arcadia ha una lettura più  
<sup>81</sup> moderna che consente di poter aggregare dati durante la trasmissione (ad esempio nel caso di  
<sup>82</sup> formazione di cluster e creazione di hti su pixel adiacenti).

<sup>83</sup> I performed a threshold and noise characterization ( $\sim 400 \text{ e}^-$  and  $\sim 15 \text{ e}^-$ ) of TJ-Monopix1 in  
<sup>84</sup> order

<sup>85</sup> Tra i test con Monopix1 ho effettuato una caratterizzazione in soglia ( $\sim 400 \text{ e}^-$ ) e rumore ( $\sim$   
<sup>86</sup>  $15 \text{ e}^-$ ) al fine di visualizzare la dispersione di questi valori sulla matrice; per poter minimizzare la

87 dispersione sulla matrice e avere una più uniforme selezione della soglia (che è globale su tutta  
88 la matrice), le versioni successive di TJ-Monopix1 includono e includeranno la possibilità di fare  
89 piccole correzioni (3 bit per pixel vengono allocati in Monopix2) di quest'ultima pixel per pixel.  
90 Per poter fornire le misure dei segnale fornito, tempo sopra soglia ToT, in elettroni, che assieme  
91 alle lacune vengono create dal passaggio della particella incidente e che quindi sono la quantità  
92 fisica "importante" nella misura, è stata necessaria una calibrazione assoluta dell'oggetto. Per  
93 quest'ultima e per altri test ?? mi sono servita di sorgenti radiattive come il ferro 55 (emissione di  
94 un fotone gamma a 5.9 kev e dello stronio 90 il cui spettro dell'elettrone emesso ha un end point  
95 a x) e dei cosmici. Inoltre ho partecipato ai test di Monopix1 su fascio: abbiamo testato il chip in  
96 una modalità diversa da quella per cui è stato progettato (tracking) e più simile al funzionamento  
97 delle CCD, in cui non si cerca di distinguere il singolo elettrone incidente ma si integra in un  
98 singolo segnale di output la carica rilasciata da più elettroni incidenti. Il fascio utilizzato (elettroni  
99 da 7-9 MeV) è un fascio ad altissima intensità e verrà utilizzato per fare ricerca su radioterapia  
100 ad alto rate (l'acceleratore è in grado di rilasciare dosi -con riferimento in acqua- fino a 40 Gy/s,  
101 corrispondenti ad un numero di particelle di ..). Per quanto riguarda, invece, le misure sul chip  
102 MD1, ho partecipato ai test elettrici e sul front end di un prototipo non ancora completamente  
103 funzionante. Un nuovo chip dovrebbe arrivare nei prossimi giorni a Pisa.

<sup>104</sup> **Chapter 2**

<sup>105</sup> **Pixel detectors**

<sup>106</sup> I pixel detector fanno parte della famiglia dei detector a semiconduttore e il loro funzionamento si  
<sup>107</sup> basa sulla creazione di coppie elettrone lacuna all'interno del bulk. Dalla creazione della particella  
<sup>108</sup> incidente di queste coppie e facendole driftare attraverso l'applicazione di un campo elettrico, si  
<sup>109</sup> ottiene quindi un segnale all'interno del rivelatore correlabile all'energia della particella incidente.  
<sup>110</sup> Il campo elettrico applicato, lo spessore della zona di svuotamento, le modalità con cui il  
<sup>111</sup> segnale viene processato e trasmesso all'esterno del rivelatore sono caratteristiche specifiche del  
<sup>112</sup> tipo di chip. In questo capitolo tratterò dunque i principali tipi di rivelatori a pixel, sofferandomi  
<sup>113</sup> in particolare sui pixel monoliti.

<sup>114</sup> **2.1 Signal formation**

<sup>115</sup> When a charge particle passes through a pixel and loses energy by ionization a part of that  
<sup>116</sup> energy is used to generate electron-hole pairs (another part is used for other processes, as the  
<sup>117</sup> lattice excitation) which are then separated by the electric field and collected at their respectively  
<sup>118</sup> electrodes (*p* for holes and *n* for electrons)<sup>1</sup>; by the drift of these charges, a signal  $i_e$  is generated  
<sup>119</sup> on the electrode *e* as stated by the Shockley-Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (2.1)$$

<sup>120</sup> where  $v(t)$  is the instantaneous velocity of the charge  $q$  and  $E_{WF}$  is the weighting field, that is the  
<sup>121</sup> field obtained biasing the electrode *e* with 1V and all the others with 0V. The drift velocity of the  
<sup>122</sup> charge depends on the electric field and on the mobility of the particle:

$$v = \mu(E) E \quad (2.2)$$

<sup>123</sup> where  $\mu(E)$  is a function of the electric field and is linear with  $E$  only for small  $E$ : at higher values  
<sup>124</sup> the probability of interactions with optical phonons increases and the mobility drops and this leads  
<sup>125</sup> to an independence of the velocity from the electric field (fig. 2.1b).

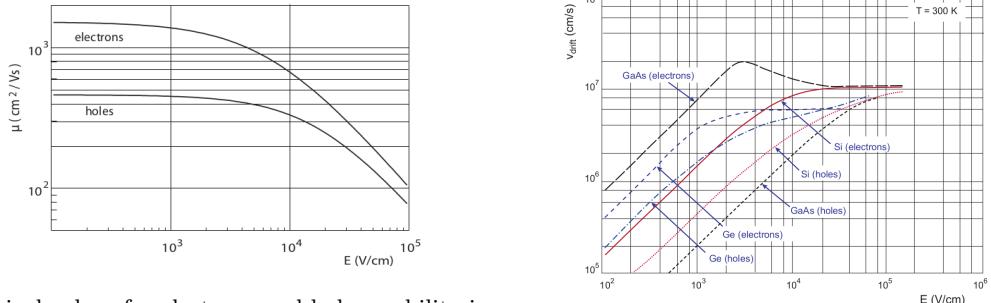
<sup>126</sup> The average energy needed to create a pair at 300 K in silicon is  $w_i = 3.65$  eV, that is more  
<sup>127</sup> than the mean ionization energy because of the interactions with phonon, since for a minimum  
<sup>128</sup> ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is  
<sup>129</sup> 0.28 keV/ $\mu$ m, hence the number of electrons-vacuum pairs is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (2.3)$$

<sup>130</sup> CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALMENTE SI AGGIUNGE IL  
<sup>131</sup> FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. IL FATTORE DI FANO È  
<sup>132</sup> 0.115 NEL SILICIO. ecc

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<sup>1</sup>Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout



(a) Typical values for electrons and holes mobility in silicon at room temperature are  $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$ , (b) Drift velocity at room temperature in different semiconductors

133 It is fundamental that pairs e/h are produced in the depleted region of the semiconductor where  
 134 the probability of recombination with charge carriers is low to avoid loss of signals. Pixel detectors  
 135 are then commonly reverse biased: a positive bias is given to the  $n$  electrode and a negative to the  
 136  $p$  to grow the depletion zone in the epitaxial layer below the electrode. The width of the depletion  
 137 region is related with the external bias  $V_{ext}$ , the resistivity  $\rho$  and also with the dopant:

$$d_n \sim 0.55 \sqrt{\frac{\rho}{\Omega \text{cm}}} \frac{V_{ext}}{V} \mu\text{m} \quad (2.4) \quad d_p \sim 0.32 \sqrt{\frac{\rho}{\Omega \text{cm}}} \frac{V_{ext}}{V} \mu\text{m} \quad (2.5)$$

138

139

141 For that reason high resistivity wafers ( $100 \Omega \text{cm} - k\Omega \text{cm}$ ) are typically preferred because they  
 142 allow bigger depletion zone with smaller voltage bias. **Metto il disegno "standard" di una giunzione**

## 143 2.2 CCDs

144 descrivi come sono fatte e come funziona il readout Tens of ms due to the need to transfer the  
 145 charge signals pixel by pixel through a single output circuit For photon imaging the need of high  
 146 assorbtion efficiency, per cui usi materiali con alto Z

## 147 2.3 Hybrid pixels

148 METTI IN EVIDENZAZ CHE PUOI FARE UN READOUT CON TECNOLOGIA CMOS. Metti  
 149 in evidenza che sono più veloci Hybrid pixels are made of two parts (fig. 2.2a), the sensor and the  
 150 electronics: for each pixel these two parts are welded together through microconnection (bump  
 151 bond).

152 They provide a practical system where readout and sensor can be optimized separately, although  
 153 the testing is less easy-to-do since the sensor and the R/O must be connected together before.

154 In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-  
 155 cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high  
 156 levels of radiation, and also expensive.

157 A critical parameter for accelerator experiments is the material budget, which represents the main  
 158 limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are  
 159 thicker ( $\sim$  hundreds of  $\mu\text{m}$ ) than monolithic ones (even less than  $100 \mu\text{m}$ ), using the latter the  
 160 material budget can be down by a third: typical value for hybrid pixels is  $1.5 \% X_0$  per layer,  
 161 while for monolithic  $0.5 \% X_0$ .

162 Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,  
 163 by the way, a bigger cooling system leading in turn to an increase in material too.

164

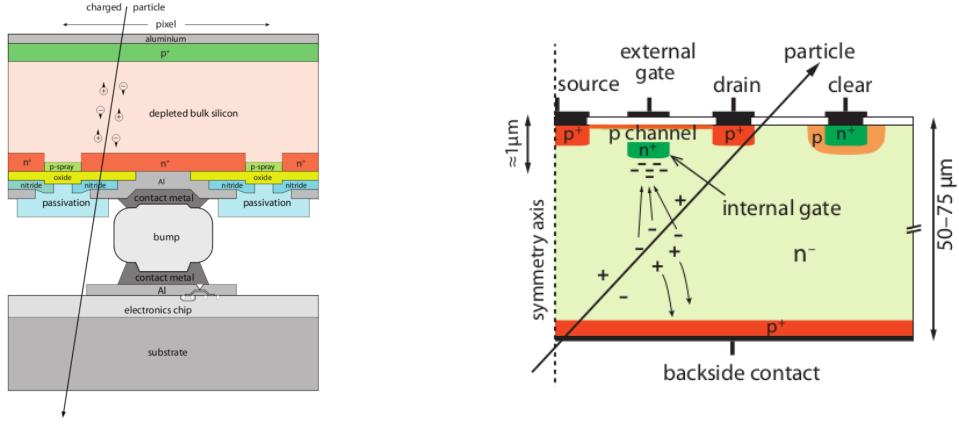


Figure 2.2: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

DEPFET are the first attempt towards the integration of the front end (FE) on the sensor bulk: they are typically mounted on a hybrid structure but they also integrate the first amplification stage.

Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor (a p-channel in fig. 2.2b): an hole current flows from source to drain which is controlled by the external gate and the internal gate together. The internal gate is made by a deep  $n+$  implant towards which electrons drift after being created in the depletion region (to know how the signal is created in a pixel detector look at appendix A); the accumulation of electrons in the region underneath the  $n$  implant changes the gate potential and controls the transistor current.

DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and the large depletion region. But, since they need to be connected with ASIC the limiting factor still is the material budget.

## 2.4 CMOS MAPS and DMPAS

With respect to CCDs, the radiation tolerance could be greatly increased by sensing the signal charge within its own pixel, instead of transporting it over thousands of pixels. The readout speed could also be dramatically increased by in-pixel amplitude discrimination, followed by sparse readout of only the hit pixels. Monolithic active pixels accommodate on the same wafer both the sensor and the front end electronics, with the second one implanted on top within a depth of about 1 μm below the surface.

MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the development of the electronic sector which guarantees the decrease in CMOS transistors dimension at least every two years, as stated by the Moore's law<sup>2</sup>.

As a matter of fact the dimension of components, their organization on the pixel area and logic density are important issues for the design and for the layout; typically different decisions are taken for different purposes.

Monolithic active pixel can be distinguished between two main categories: MAPS and depleted MAPS (DMPAS).

MAPS (figure a 2.3) have typically an epitaxial layer in range 1 μm to 20 μm and because they are not depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the collection could be partial especially after the irradiation of the detector (look at A for radiation damages), when the trapping probability become higher.

In figure 2.3 is shown as example of CMOS MAPS: the sensor in the scheme implements an  $n$  well as collection diode; to avoid the others  $n$  wells (which contain PMOS transistor) of the electronic

<sup>2</sup>Moore's law states that logic density doubles every two years.

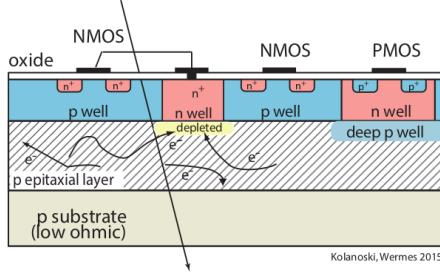


Figure 2.3: Concept cross-section of CMOS MPAS pixel

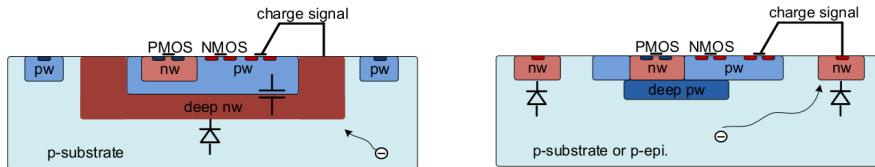


Figure 2.4: Concept cross-section with large and small fill factor

199 circuit would compete in charge collection and to shield the CMOS circuit from the substrate,  
200 additionally underlying deep p well are needed. DMAPS are instead MAPS depleted with  $d$   
201 typically in  $\sim 25 \mu\text{m}$  to  $150 \mu\text{m}$  (eq. 2.1) which extends from the diode to the deep p-well, and  
202 sometimes also to the backside (in this case if one wants to collect the signal also on this electrode,  
203 additional process must be done).

#### 204 2.4.1 DMAPS: large and small fill factor

205 There are two different sensor-design approaches (figure 2.4) to DMAPS:

- 206 • large fill factor: a large collection electrode that is a large deep n-well and that host the  
207 embedded electronics
- 208 • small fill factor: a small n-well is used as charge collection node

209 To implement a uniform and stronger electric field, DMAPS often uses large electrode design that  
210 requires multiple wells (typically four including deep n and p wells); this layout adds on to the  
211 standard terms of the total capacity of the sensor a new term (fig. 2.5), that contributes to the  
212 total amplifier input capacity. In addition to the capacity between pixels ( $C_{pp}$ ) and between the  
213 pixel and the backside ( $C_b$ ), a non-negligible contribution comes from the capacities between wells  
214 ( $C_{SW}$  and  $C_{WW}$ ) needed to shield the embedded electronics. These capacities affect the thermal  
215 and 1/f noise of the charge amplifier and the  $\tau_{CSA}$  too:

$$216 \quad ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.6) \qquad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.7)$$

217 where  $g_m$  is the transconductance,  $\tau_{sh}$  is the shaping time.

218 Among the disadvantages coming from this large input capacity could be the coupling between  
219 the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring  
220 electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this prob-  
221 lem is especially connected with the intra wells capacities. So, larger charge collection electrode  
222 sensors provide a uniform electric field in the bulk that results in short drift path and so in good  
223 collection properties, especially after irradiation, when trapping probability can become an issue.  
224 The drawback of a large fill-factor is the large capacity ( $\sim 100 \text{ fF}$ ): this contributes to the noise  
225 and to a speed penalty and to a larger possibility of cross talk.

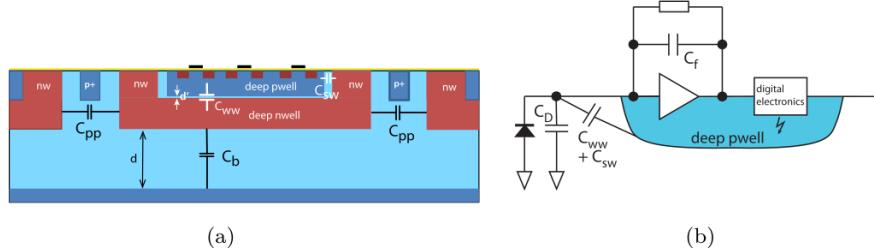


Figure 2.5:  $C_{pp}$ ,  $C_b$ ,  $C_{WW}$ ,  $C_{SW}$

	small fill factor	large fill factor
small sensor C	✓ ( $< 5 \text{ fF}$ )	$\times (\sim 100 \text{ pF})$
low noise	✓	$\times$
low cross talk	✓	$\times$
velocity performances	✓	$\times (\sim 100 \text{ ns})$
short drift paths	$\times$	✓
radiation hard	$\times$	✓

Table 2.1: Small and large fill factor DMAPS characteristics

226        The small fill-factor variant, instead, benefits from a small capacity (5 fF to 20 fF), but suffers  
 227        from a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando  
 228        dei MAPS, devo ripetere qui?**

229        As we'll see these two different types of sensor require different amplifier: the large electrode one is  
 230        coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.5.1).

#### 231        2.4.2 A modified sensor

232        A process modification developed by CERN in collaboration with the foundries has become the  
 233        standard solution to combine the characteristics of a small fill factor sensor (small input amplifier  
 234        capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE  
 235        upgrade about ten years [1].

236        A compromise between the two sensors could also be making smaller pixels, but this solution  
 237        requires reducing the electronic circuit area, so a completely new pixel layout should be though.  
 238        The modification consists in inserting a low dose implant under the electrode and one its advantage  
 239        lies in its versatility: both standard and modified sensor are often produced for testing in fact.

240        Before the process modification the depletion region extends below the diode towards the sub-  
 241        strate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.6).  
 242        After, two distinct pn junctions are built: one between the deep p well and the  $n^-$  layer, and the  
 243        other between the  $n^-$  and the  $p^-$  epitaxial layer, extending to the all area of the sensor.  
 244        Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes  
 245        can be biased separately<sup>3</sup> and this is beneficial to enhance the vertical electric field component.  
 246        The doping concentration is a trimmer parameter: it must be high enough to be greater than the  
 247        epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be  
 248        lower enough to allow the depletion without reaching too high bias.

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<sup>3</sup>This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

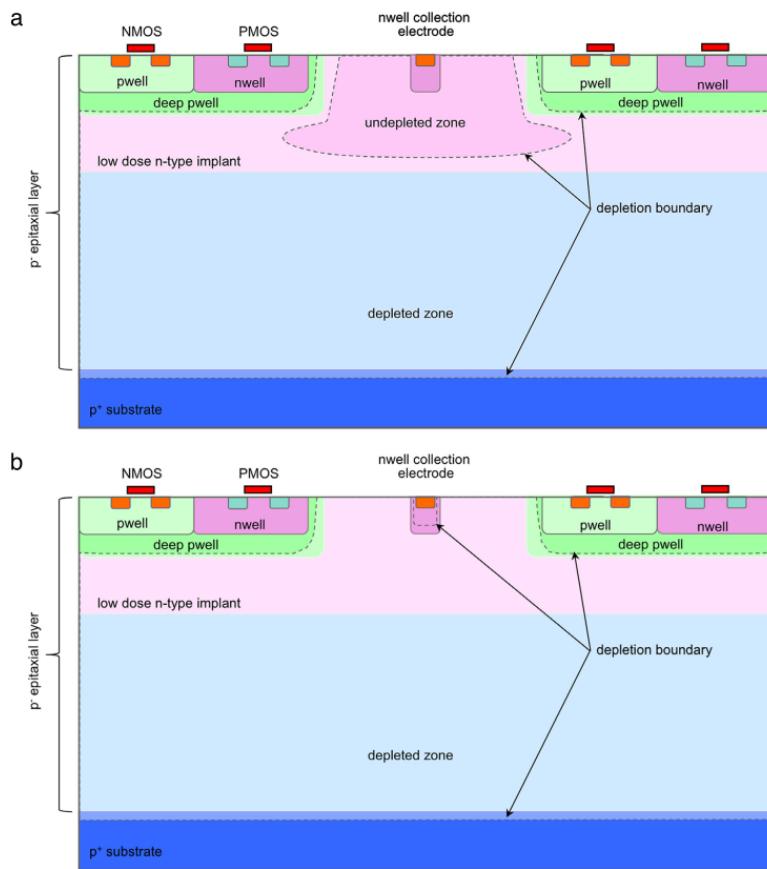


Figure 2.6: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

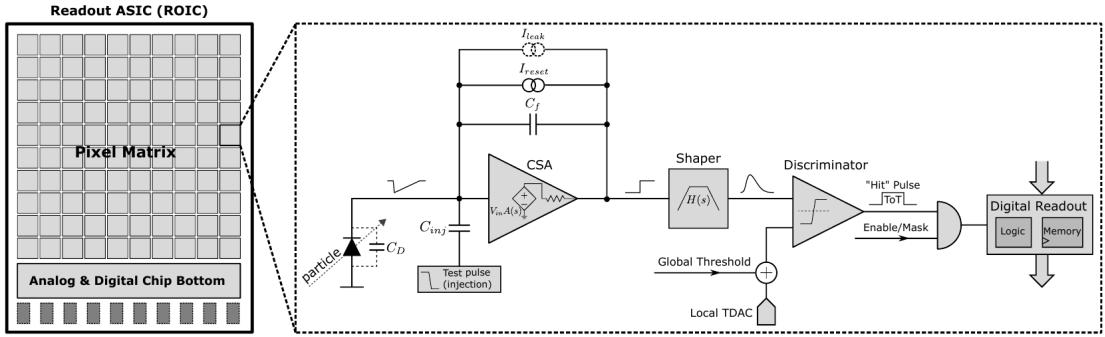


Figure 2.7: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

## 249 2.5 Analog front end

250 After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.7), ready  
 251 to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an  
 252 efficient, high-speed readout architecture, consuming as low power as possible must be provided  
 253 by the readout integrated electronics (ROIC).

254 Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually  
 255 often is the only amplification stage) with a reset to the baseline mechanism and a leakage current  
 256 compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be  
 257 optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise  
 258 before the amplification stage in order to not multiply that noise, and chose a reasonable threshold  
 259 of the discriminator to cut noise-hits much as possible.

### 260 2.5.1 Preamplifier

261 Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled  
 262 as an operational amplifier (OpAmp) where the gain is determined by the input and feedback  
 263 impedance (first step in figure 2.7):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.8)$$

264 Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a  
 265 voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the  
 266 voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor  
 267 MAPS whose signal is already enough high:  $v_{in} = Q/C_D \approx 3fC/100 \text{ pF} = 0.03 \text{ mV}$ , but it's fine  
 268 for the small fill factor ones:  $v_{in} = Q/C_D \approx 3fC/3 \text{ pF} = 1 \text{ mV}$ .

269 In the case of a resistor feedback, if the signal duration time is longer than the discharge time  
 270 ( $\tau = R_S C_D$ ) of the detector the system works as current amplifier, as the signal is immediately  
 271 trasmit to the amplifier; in the complementary case (signal duration longer than the discharge  
 272 time) the system integrates the current on the  $C_D$  and operates as a voltage amplifier.

## 273 2.6 Readout logic

274 Readout logic includes the part of the circuit which takes the FE output signal, processes it and  
 275 then transmit it out of pixel and/or out of chip; depending on the situation of usage different  
 276 readout characteristics must be provided.

277 To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers  
 278 and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really

279 high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is  
 280 recorded).

281 A common compromise often made is to save the time over threshold (ToT) of the pulse in clock  
 282 cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen  
 283 bits but, being correlated and hopefully being linear with the deposited charge by the impinging  
 284 particle in the detector, it provides a sufficient information. The ToT digitalization usually takes  
 285 advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels' matrix.  
 286 The required timing precision is at least around 25 ns, that corresponds to the period of  
 287 bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is  
 288 40 MHz.

289 Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they  
 have been read, and then the ToT is obtained from their difference.

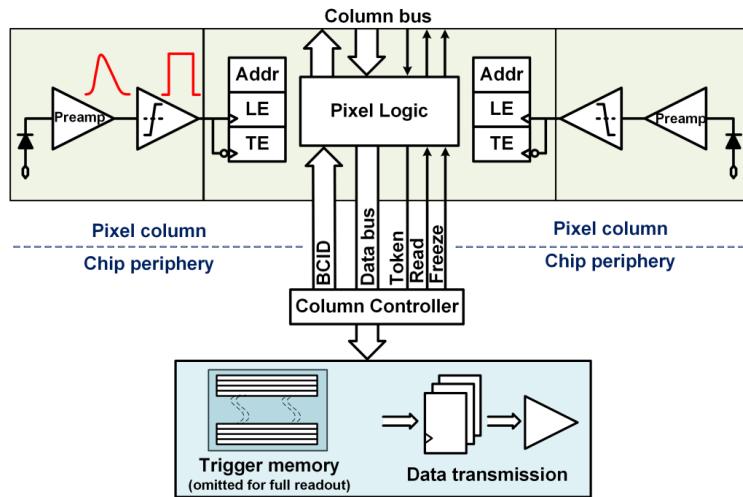


Figure 2.8: Column drain R/O scheme where ToT is saved

290 Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger  
 291 system decides if the hit must be store or not. On one hand the triggered-readout needs buffers  
 292 and storage memories, on the other the full readout, because there is no need to store hit data on  
 293 chip, needs an high enough bandwidth.

294 A triggered readout is fundamental in accelerator experiments where the quantity of data to store  
 295 is too large to be handled, and some selections have to be applied by the trigger: to give an order  
 296 of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100  
 297 MBit/s [2] (pag. 797).

298 Typically the trigger signal is processed in a few  $\mu s$ , so the pixel gets it only after a hundred clock  
 299 cycles from the hit arrival time: the buffer depth must than handle the higher trigger latency.

300 After having taken out the data from the pixel, it has to be transmitted to the end of column  
 301 (EoC) where a serializer deliver it out of chip, typically to an FPGA.

302 There are several ways of transmitting data from pixel to the end of column: one of the most  
 303 famous is the column-drain read out, developed for CMS and ATLAS experiments [3]. All the  
 304 pixels in a double-column share a data bus and only one pixel at a time, according to a priority  
 305 chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit  
 306 arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored  
 307 on a RAM until the SH does not allow the access to memory by data bus.

308 Even if many readout architectures are based the column-drain one, it doesn't suit for large size  
 309 matrices. The problem is that increasing the pixels on a column would also raise the number of  
 310 pixels in the priority chain and that would result in a slowdown of the readout.

311 If there isn't any storage memory, the double-column behaves as a single server queue and the  
 312 probability for a pixel of waiting a time  $T$  greater than  $t$ , with an input hit rate on the column  $\mu$

<sup>314</sup> and an output bandwidth  $B_W$  is [4]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.9)$$

<sup>315</sup> To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time  $\tau$  due to the  
<sup>316</sup> AFE), for example imposing  $P_T > t \sim 0.001$ , one obtains  $(B_W - \mu) t_t \sim 6$ , where  $t_t$  is the time  
<sup>317</sup> needed to transfer the hit; since  $t_t$  is small, one must have  $B_W \gg \mu$ , that means a high bandwidth  
[4].

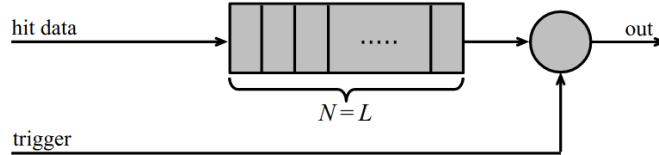


Figure 2.9: Block diagram of a pipeline buffer: N is the dimension of memory buffer and L is the trigger latency expressed in BCID cycles

<sup>318</sup> Actually the previous one is an approximation since each pixel sees a different bandwidth de-  
<sup>319</sup> pending on the position on the queue: the first one sees a full bandwidth, but the next sees a  
<sup>320</sup> smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen  
<sup>321</sup> by the pixel  $i$  is  $B_i = B - \sum_j \mu_j$ , where  $\mu_j$  is the hit rate of the  $j$ th pixel.

<sup>322</sup> The efficiency requirement on the bandwidth and the hit rate becomes:  $B_{W,i} > \mu_i$ , where the  
<sup>323</sup> index  $i$  means the constraint is for a single pixel; if all the N pixels on a column have the same  
<sup>324</sup> rate  $\mu = N\mu_i$ , the condition reduces to  $B_W > \mu$ . The bandwidth must be chosen such that the  
<sup>325</sup> mean time between hits of the last pixel in the readout chain is bigger than that.

<sup>326</sup> In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed;  
<sup>327</sup> this means that only information from channels where the signal exceeds the discriminator thresh-  
<sup>328</sup> old are stored. Qualcosa sulla zero suppression? La metto qui questa affermazione?

<sup>329</sup> If instead there is a local storage until a trigger signal arrives, the input rate to column bus  
<sup>330</sup>  $\mu'$  is reduced compared to the hit rate  $\mu$  as:  $\mu' = \mu \times r \times t$ , where  $r$  is the trigger rate and  $t$  is  
<sup>331</sup> the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth,  
<sup>332</sup> but the limiting factor is the buffer depth: the amount of memory designed depends both on the  
<sup>333</sup> expected rate  $\mu$  and on the trigger latency  $t$  as  $\propto \mu \times t$ , that means that the higher the trigger  
<sup>334</sup> latency and the lower the hit rate to cope with.

<sup>335</sup> In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels  
<sup>336</sup> into regions with shared storage. Let's compare two different situations: in the first one a buffer  
<sup>337</sup> is located on each pixel area, while in the second one a core of four pixels share a common buffer  
<sup>338</sup> (this architecture is commonly called FE-I4).

<sup>339</sup> Consider a 50 kHz single pixel hits rate and a trigger latency of 5  $\mu s$ , the probability of losing  
<sup>340</sup> hits is:

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.10)$$

<sup>341</sup> where I have assumed a Poissonian distribution with mean  $\nu = 0.25$  to describe the counts N.

<sup>342</sup> To get an efficiency  $\epsilon$  greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.11)$$

<sup>343</sup> Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four pixels  
<sup>344</sup> the mean number of hits per trigger latency is  $\nu = 0.25 \times 4 = 1$ . To get an efficiency of 99.9% (eq.  
<sup>345</sup> 2.11) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

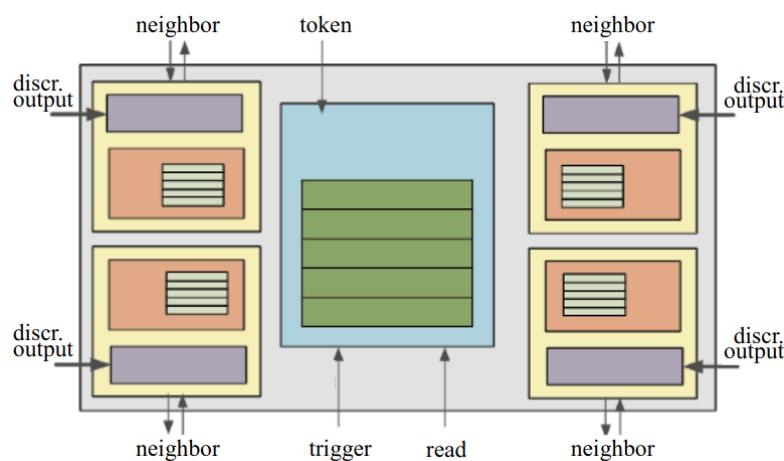


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is highlighted in light blue; latency counters and trigger management section are highlighted in green; hit processing blocks are highlighted in purple; ToT counters and ToT management units are highlighted in orange

## <sup>347</sup> Chapter 3

# <sup>348</sup> Use of pixel detectors

<sup>349</sup> There always was a tight relation between the development of cameras and pixel detectors since  
<sup>350</sup> 1969, when the idea of CCDs, thanks to whom Boyle and Smith were awarded the Nobel Prize in  
<sup>351</sup> Physics in 2009, revolutionized photography allowing light to be captured electronically instead of  
<sup>352</sup> on film. Even though the CMOS technology was already known when CCDs spread, the costs of  
<sup>353</sup> productions were too high to allow the diffusion of these sensors for which needed to wait until  
<sup>354</sup> 1990s. From that period on, the fast diffusion of CMOS was mainly due to the less cost than  
<sup>355</sup> CCD, and the less power required for supply. Nowadays CCDs are still preferred over MAPS in  
<sup>356</sup> astronomy, where the astronomical sources' rate are low enough to cope with tens of ms for the  
<sup>357</sup> readout.

<sup>358</sup> The principal use cases of pixel detectors are particle tracking and imaging: in the former case  
<sup>359</sup> individual charged particles have to be identified, in the latter instead an image is obtained by  
<sup>360</sup> the usually un-triggered accumulation of the impinging radiation. Also the demands on detectors  
<sup>361</sup> performance depends on their usage, in particular tracking requires high spatial resolution, fast  
<sup>362</sup> readout and radiation hardness.

### <sup>363</sup> 3.1 Tracking in HEP

<sup>364</sup> At first the physics world overlooked the CCDs, and all pixel in general, as against the gaseous  
<sup>365</sup> detector for tracking: there was no need to replace these ones which had a sufficient good resolution  
<sup>366</sup> ( $100\text{ }\mu\text{m}$ ). Since 1974, with the measurement of the invariant mass of the **j psi** and the affirmation  
<sup>367</sup> of the quark model, all experiments start to look for better spatial resolutions in order to achieve  
<sup>368</sup> the possibility of reconstructing short lived particle.

<sup>369</sup> Historically, the first pixel detector employed in particle physics was a CCD: it was installed in  
<sup>370</sup> the spectrometer at the CERN's Super Proton Synchrotron (SPS) by the ACCMOR Collaboration  
<sup>371</sup> (Amsterdam, CERN, Cracow, Munich, Oxford, RAL) at mid 1980s, with the purpose of studying  
<sup>372</sup> the recently-discovered charm particles. The second famous usage of CCDs took place at SLAC  
<sup>373</sup> in the Large Detector (SLD) during the two years 1996-98. **Cosa vedono di così importante da**  
<sup>374</sup> **dire che servono i pixel detector?** From that period on particle tracking in experiments have been  
<sup>375</sup> transformed radically: it was mandatory for HEP experiments to build an inner vertex detector.  
<sup>376</sup> In 1991, the more demanding environments led to the development of hybrid pixel detectors:  
<sup>377</sup> a dedicated collaboration, RD19, was established at CERN with the specific goal to define a  
<sup>378</sup> semiconductor micropattern detector with an incorporated signal processing at a microscopic level.  
<sup>379</sup> In those years a wide set of prototypes of hybrid pixel has been manufactured; among the greatest  
<sup>380</sup> productions a mention goes to the huge ATLAS and CMS vertex detectors. From the middle of  
<sup>381</sup> 2013 a second collaboration, RD 53, has been established with the new goal to find a pixel detector  
<sup>382</sup> suitable for phase II future upgrades of those experiments. Even if the collaboration is specifically  
<sup>383</sup> focused on design of hybrid pixel readout chips (aiming to 65 nm technique so that the electronics  
<sup>384</sup> fits within the pixel area), also other options have been taken in account and many test have been  
<sup>385</sup> done on MAPS for example. Requirements imposed by HL-LHC will become higher in time: for

example, a dose and radiation of 5 Mrad and 1016NIEL are expected after 5 years of operation. Time resolution, material budget and power consumption are also issues for the upgrade: a time resolution better than 25 ns for a bunch crossing frequency of 40 MHz, a material budget lower than 2% and a power consumption lower than 500 mW/cm<sup>2</sup> are required.

Amidst the solutions proposed 3D silicon detector, invented by Sherwood Parker in 1995, and MAPS are the most promising. In 3D sensors the electrode is a narrow column of n-type implanted vertically across the bulk instead of being implanted on the wafer's surface. The charge produced by the impinging particle is then drifted transversally within the pixel, and, as the mean path between two electrode can be sufficient low, the trap probability is not an issue. 3D pixels have been already proved in ATLAS tracker [quando?](#). Even if 3D detector are adequately radiation hard, MAPS architecture looked very promising from the beginning: they overcome both the CCDs long reading time and the hybrid problems (I have already explained in section ?? the benefits of MAPS). Experiments such as ALICE at LHC and STAR at RHIC have already introduced the CMOS MAPS technology in their detectors. ALICE Tracking System (ITS2), upgraded during the LHC long shut down in 2019-20, was the first large-area ( $\sim 10 \text{ m}^2$  covered by 2.5 Gpixels) silicon vertex detector based on CMOS MAPS.

### 3.1.1 Hybrid pixels at LHC and at SuperKEKB

#### ATLAS

With CMS, ATLAS is one of two general-purpose detectors at the LHC and has the largest volume detector ever constructed for a particle collider (46 m long and 25 m in diameter). The Inner Detector consists of three different systems all immersed in a magnetic field parallel to the beam axis whose main components are: the pixel, the micro-strips and transition radiation trackers. Concerning the pixel detector, 92 million pixels are divided in 4 barrel layers and 3 disks in each end-cap region, covering a total area of 1.9 m<sup>2</sup> and having a 15 kW of power consumption.

As stated by the ATLAS collaboration the pixel detector is exposed by an extreme particle flux: "By the end of Run 3<sup>1</sup>, the number of particles that will have hit the innermost pixel layers will be comparable to the number it would receive if it were placed only a few kilometres from the Sun during a solar flare". Considering that the particle density will increase even more with HL-LHC, radiation hardness is definitively target to achieve.

The most ambitious goal is employ a MAPS-based detector for the inner-layer barrels, and for this reason the RD53 collaboration is performing many test on MAPS prototypes, as Monopix of which I will talk about in section ??.

Up to now this possibility will be eventually implemented during the second phase of the HL-LHC era, as at the start of high-luminosity operation the selected option is the hybrid one. The sensor will be bonded with ITkPix, the first full-scale 65 nm hybrid pixel-readout chip developed by the RD53 collaboration. Regarding the sensor, a valuable option is using 3D pixels, which have already proved themselves in ATLAS, for the insertable B layer (IBL).[qualcosa in più sui 3d](#). The number of pixels will be increased of a factor about 7, passing from 92 millions to 6 billion.

#### CMS

[da scrivere](#) 124 million pixels; cylindrical layers roughly at 3cm, 7cm, 11cm and 16cm and disks at either end, and so will be vital in reconstructing the tracks of very short-lived particles. Each of these silicon pixels is 100um by 150um, even with only around 50 microwatts per pixel, the total power output is 7.5kW-

#### LHCb

LHCb is a dedicated heavy-flavour physics experiment that exploits pp interactions at 14 TeV at LHC. It was the last experiment to upgrade the vertex detector, the Vertex Locator (VELO),

<sup>1</sup>Run 3 start in June 2022

432 replacing the silicon-strip with pixels in May 2022. As the instantaneous luminosity in Run3 is  
433 increased by a factor  $\lesssim 10$ , much of the readout electronics and of the trigger system have been  
434 developed in order to cope with the large interaction rate. To place the detector as close as possible  
435 to the beampipe and reach a better track reconstruction resolution, the VELO has a surprising  
436 feature: it can be moved. During the injection of LHC protons it is parket at 3 cm from the beams  
437 and only when the stability is reach it is brought at  $\sim 5$  mm. Radiation hardness as well as readout  
438 speed are then a priority for the detectors: that's why the collaboration opted for a hybrid system.  
439 The Velopix is made bonding sensors, each measuring  $55 \times 55$  micrometers, 200  $\mu\text{m}$ -thick to a  
440 200  $\mu\text{m}$ -thick ASIC specially developed for LHCb and coming from the Medipix family (sec. ??),  
441 which can handles hit rates up to 900 MHz per chip. Since the detector is operated under vacuum  
442 near the beam pipe, the heat removal is particularly difficult and evaporative CO<sub>2</sub> microchannel  
443 cooling are used.

#### 444 **BelleII**

445 The current vertex detector of BelleII, VXD, is made of a pixel detector (PXD), fabricated with  
446 2 layers of DEPFET-based pixels, and 4 layers of a double-sided silicon strip detectors (SVD)[5].  
447 Due to the small capacitance of the collection node, DEPFET presents a high signal-to-noise ratio  
448 (in 30-50) thanks to the low intrinsic noise and to the large signal achieved with the fully depleted  
449 bulk: pixels are thinned to 75  $\mu\text{m}$  in the active region, then a MIP is supposed to create a signal of  
450  $\sim 6000 e^-$ , while the typical noise of DEPFET is around 200  $e^-$ . The ASIC read out is still based  
451 on a rolling shutter logic, with an integration time of 20  $\mu\text{s}$ . In order to reduce the data-storage  
452 memory PXD hits are only used to improve spatial resolution of tracks: the SVD informations are  
453 used by the High Level Trigger (HLT) to look for regions of interest in the pixel ladders just by  
454 extrapolating back the tracks found in the tracker detector, and this method allows to store only  
455 data belonging to these areas; the PXD hits are then used in offline track fit to improve the vertex  
456 resolution.

457 MAPS have been proposed for the replacement of VXD during the Long Shut Down 2 (LSD2)  
458 foreseen around 2026-27; the new vertex detector, VTX, should be made of 5 layers fabricated  
459 by the optimized Belle II pixel sensor (OBELIX), a detector based on TJ-Monopix have been  
460 selected (look at chapter ??). The main advantages VTX should bring are a obvious improving  
461 in the track and vertex resolution (14  $\mu\text{m}$  before upgrade,  $\lesssim 10 \mu\text{m}$  expected after upgrade) and a  
462 reduction in the  $X_0$  (da.. a..), a higher background tolerance because of the smaller sensor than  
463 strips dimension and a low bandwidth due to the on-chip sparsification.

#### 464 **3.1.2 First attempts to MAPS**

##### 465 **MIMOSA at EUDET and STAR**

466 MIMOSA [6][7] (standing for Minimum Ionizing MOS Active pixel sensor), designed in 2008,  
467 prefigured the architecture of MAPS for coming vertex detector being the first large scale sensor  
468 to be employed as detector. MIMOSA-26 equiped the final version of EUDET high resolution  
469 beam telescope both at CERN-SPS and at DESY while the MIMOSA-28 devices are used for  
470 the first MAPS-based vertex detector at the STAR experiment. MIMOSA-26 is fabricated in a  
471 350 nm, and a module features 1152 columns, split into 18 independent groups, and 576 rows, with  
472 square pixels having a side of 18.4  $\mu\text{m}$  length; therefore, because of the small dimension, charge  
473 sharing is an issue aggiungi qualcosa. The readout is done in a rolling shutter mode: the chip is  
474 an Active Pixels (APS) and therefore it incorporates the amplification on pixel, while the signal  
475 discrimination and zero-suppression logic are placed at the EoC, where is also placed a memory.  
476 The chip is an Active Pixels (APS) and therefore it incorporates the amplification on pixel, while  
477 the signal discrimination and zero-suppression logic are placed at the EoC: the readout is done in  
478 a rolling shutter mode with a frame integration time that can be lowered down to 85 ms, and a  
479 memory allowing to store up to six hits is.

480 The EUDET telescope, equipped with six sensor planes, requires highly granular and thin pixel

481 detectors in order to achieve an excellent track resolution (around  $2\text{ }\mu\text{m}$ ) even at the rather low  
 482 particle energies of up to 6 GeV. The STAR experiment at the Relativistic Heavy Ion Collide  
 483 (RHIC) accelerator at the Brookhaven National Laboratory (BNL) is the first to include MAPS  
 484 in the vertex detector[8]. The main tracking detector in STAR is a TPC with radii 60-190 cm  
 485 embedded in a 0.5 T solenoidal magnetic field, that provides a pointing resolution of approximately  
 486 1 mm. The pixel detector, PXL, is a part of a 3-detector system, Heavy Flavor Tracker (HFT), that  
 487 has been added to the pre-existing STAR apparatus just before the 2014 Run in order to improve  
 488 the impact parameter resolution and to enable the direct reconstruction of hadronic decays of heavy  
 489 flavor mesons and baryons. The Heavy Flavor Tracker (HFT) is composed by the Silicon Strip  
 490 Detector (SSD), the Intermediate Silicon Tracker (IST) and the Pixel Detector (PXL); the first  
 491 one is placed at 22 cm from the beam pipe and consists of double sided strips with  $95\text{ }\mu\text{m}$  inter-strip  
 492 pitch, the second one, placed at 14 cm, is made of single sided silicon pads with  $600\text{ }\mu\text{m} \times 6\text{ mm}$  pitch  
 493 and the last one made by two layers is placed at 2.8 cm and 8 cm fabricated with ULTIMATE2 (also  
 494 known as MIMOSA-28), a successor of MIMOSA-26 sensor, with pitch  $20.7\text{ }\mu\text{m}$  and thinned down  
 495 to  $50\text{ }\mu\text{m}$ . An area of  $0.16\text{ m}^2$  are covered by 400 MAPS sensor, corresponding to 356 millions of  
 496 pixels divided into array size of  $928 \times 960$ . Each pixel includes circuitry for readout, amplification,  
 497 and Correlated Double Sampling (CDS) for signal extraction and noise subtraction and the frame  
 498 integration time is  $185.6\text{ }\mu\text{s}$ ; after the subtraction the signal to noise ratio is  $\sim 30$ , with a noise  
 499 between 10-12 electrons and a signal of  $1000\text{ e}^-$ . Thanks to the HFT system and the PXL, STAR  
 500 achieved a track pointing resolution  $46\text{ }\mu\text{m}$  for  $750\text{ MeV}/c$  kaons, and better than  $30\text{ }\mu\text{m}$  for particle  
 501 momenta bigger than  $1\text{ GeV}/c$ : this performance enabled the study of D-meson production with a  
 high significance signal.

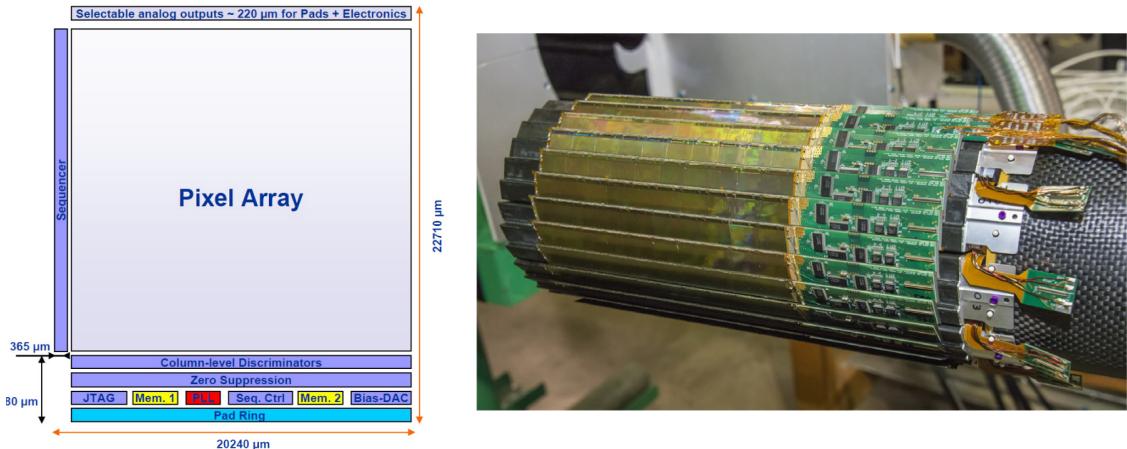


Figure 3.1: (a) The HFT PXL detector; (b) Block-diagram of the ULTIMATE-2 sensor

502

### 503 ALPIDE at ALICE

504 ALICE (A Large Ion Collider Experiment) is a detector dedicated to heavy-ion physics and to the  
 505 study of the condensed phase of the chromodynamics at the LHC. The tracking detector consists of  
 506 the Inner Tracking System (ITS), the gaseous Time Projection Chamber (TPC) and the Transition  
 507 Radiation Detector (TRD), and all those are embedded in a magnetic field of 0.5 T. The ITS is  
 508 made by six layers of detectors, two for each type, from the interaction point outwards: Silicon  
 509 Pixel Detector (SPD), Silicon Drift Detector (SDD) and Silicon Strip Detector (SSD). Contrary  
 510 to the others LHC experiments, ALICE tracker is placed in a quite different environments: the  
 511 expected dose is smaller by two order of magnitude and the rate of interactions is few MHz instead  
 512 of 40 MHz, but the number of particles comes out of each interaction is higher (the SPS is invested  
 513 by a density of particles of  $\sim 100\text{ cm}^{-2}$ ). The reconstruction of very complicated events with a large  
 514 number of particle is a challenge, hence to segment and to minimize the amount of material, which  
 515 may cause secondary interaction complicating further the event topology, is considered a viable

strategy. The detector employs the ALPIDE chip, developed by ALICE collaboration, fabricated in the 180 nm CMOS Imaging Sensor process of TowerJazz, whose design takes full advantage of process feature which allows full circuitry within the pixel matrix. Thanks to the reduction of the material budget, ITS2 obtained an amazing improvement both in the position measurement and in the momentum resolution, improving the efficiency of track reconstruction for particle with very low transverse momentum (by a factor 6 at  $pT \sim 0.1$  GeV/c). Further advancements in CMOS MAPS technology are being aggressively pursued for the ALICE ITS3 vertex detector upgrades (foreseen around 2026-27), with the goals of further reducing the sensor thickness and improving the readout speed of the devices, while keeping power consumption at a minimum.

## 3.2 Other applications

Historically for imaging purpose the CCDs were the favoured device: they can be used as single photon counter or integrating and collecting the charge released by more impinging particles. The utilisation in the first case is similar to the tracking one, except that the requirements are less tight, so much that two noteworthy of microchips originally meant for detectors in particle physics at the LHC, and later employed in other fields are Medipix and Timepix. They are read-out chips developed by the Medipix Collaborations since early 1990s. For two decades, different Medipix generations have been produced, having a rough correlation with the feature size used: Medipix2 (1999) used 250 nm feature size CMOS while Medipix3 (2005) 130 nm. The aim of the fourth collaboration (2016), instead, is designing pixel read-out chips that prepared for **TSV processing and may be tiled on all four sides. DOVREI METTERE DUE RIGHE SU TSV OPPURE TAGLIARE.** For photons imaging other materials with higher atomic charge than silicon could be preferred, as a high photon absorption efficiency is needed: it was for this reason that Medipix2 was bump bonded to identically segmented sensors of both silicon and GaAs.

The applications in scientific imaging vary from astrophysics and medical imaging to more exotic domains as studies of protein dynamics, art authentication and dosimetry. The most important employment of Medipix is as X-ray single photon counting in industrial and medical radiography and in 3D computed tomography. Thanks to a New-Zealand company, the MARS Bioimaging detector has been fabricated, which is capable of resolving the photons energy and produce 3D coloured images. Besides tracking in HEP (I have already cited the use of Timepix3 is in the beam telescope of the LHCb VELO), an important use of Timepix is in dosimetry **Timepix Detector for Imaging in Ion Beam Radiotherapy- aggiungi qualche info** A small-Timepix detector with the dimension of a USB can also be found at the International Space Station, where it is exploited for radiation, principally made of heavy-ion, monitoring.

### 3.2.1 Applicability to FLASH radiotherapy

A possible new application of pixels detector is dosimetry or beam monitoring of charge particles in high intensity radiography. The radiological treatment is a common method used in 60% of tumors both as palliative care and as treatment. It can be given before, after or during a surgery, (Intra operative radiation therapy-IORT) and many different types of radiations (photons, electrons, protons and ions, which mainly are hydrogen and carbon) can be used to irradiate the affected tissues. Exploiting the ionizing energy loss, that can be parametrized by the Linear Energy Transfer (LET), a biological damage can be delivered to the tissue: while  $\alpha$  and  $\beta$  particles are high LET radiations with values in  $100\text{ keV}/\mu\text{m}$  to  $200\text{ keV}/\mu\text{m}$ , x-rays and gamma-rays are low LET radiations with values in range  $0.2\text{ keV}/\mu\text{m}$  to  $2\text{ keV}/\mu\text{m}$ .

If x-ray photons, with energy in 4 MeV to 25 MeV are used, the ionization is caused by the Compton electrons and is more in the superficial layers of the tissue due to the exponential attenuation of the beam. The hadrons energy loss, instead, is strongly localized in the last region of the track, that is the Bragg peak. Ion beam enables better focusing of the radiation thereby improves the sparing of the surrounding healthy tissues; on the other hand the delivered dose distribution depends more on the patient's density tissues (e.g. bones, swelling, fat). **Ensuring the target**

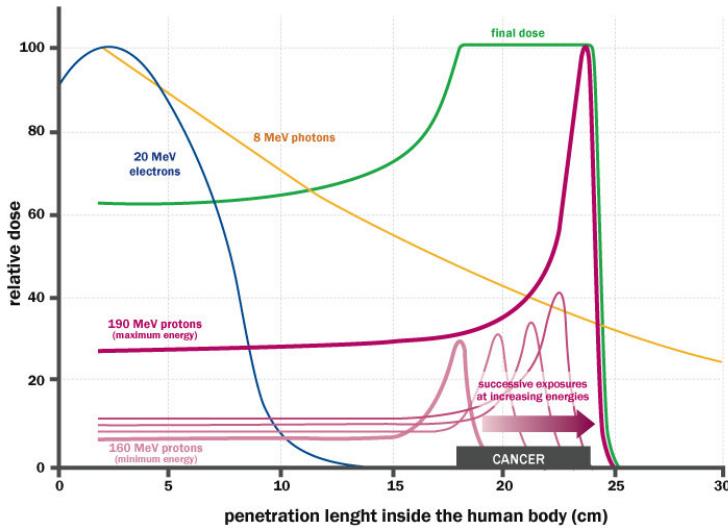


Figure 3.2: The Spread Out Bragg Peak (SOBP) curve (green), which is a constant dose distribution, is obtained from the superposition of many Bragg peak of hadrons with different energy.

	CONV-RT	FLASH-RT
Dose rate	0.03 Gy/s	40 Gy/s
Intra pulse dose rate	100 Gy/s	106 Gy/s
Treatment duration	~minutes	$\lesssim 500$ ms
DDP	0.3 mGy	1 Gy to 10 Gy
Pulse width	3 $\mu$ s	$\sim 2$ $\mu$ s

Table 3.1: Typical value of treatment parameters

coverage is a fundamental objective in radiotherapy and is closely connected to the choice of the particles. Electrons cover the target since they tend to spread out and can cover a field size of a few cm<sup>2</sup> at a distance of a few cm from the source. Instead, the limited size of the beam for protons and photons from ultra high dose rate microbeam radiation therapy (MRT), for which FLASH effect was seen, requires the scanning of target. The radiobiological consequences of scanning both in spatial-fractionation and in prolonged exposure, which might not be sufficient to maintain a high mean dose rate to trigger FLASH effect, need to be explored. To date, the FLASH effect has been most commonly demonstrated using low-energy electron linacs

Recently<sup>2</sup> a promising method for RT at ultra high dose rate (at least 40 Gy/s) and for this reason called FLASH-RT[9], instead of CONV-RT (0.03 Gy/s), came out. This treatment takes advantages of biological differences between tumors and healthy tissues: it is characterized by reducing normal tissue toxicity and maintaining equivalent tumor damage. The response to dose can be described by the survival fraction probability, describing the fraction of surviving cell as a function of the dose:

$$S(D) = S(0) e^{-(\alpha D + \beta D^2)} \quad (3.1)$$

where  $\alpha$  and  $\beta$  respectively represents the rate of cell killing by single ionizing events and by double hits. Hence, at high doses the density of damages increases and the cells repair becomes more difficult. Even if the FLASH effect is not yet completely understood and the underlying mechanisms are not clear, it looks like there are two different recipes which are involved:

<sup>2</sup>The first evidences has been observed on a mice experiments in 1966 and in 2014 by the group of Favaudon and Vozenin. After this, many test on cats and pigs have been performed, and also there has been a clinical trial on a cutaneous tumor-patient

583 • **The dose rate:** higher dose rate produce bigger damages (fig. 3.3(a)) since this prevent  
584 cells from sparing.

585 • **The presence or absence of oxygen:** while hypoxic cells are very resistant to radiation,  
586 normal oxygenated cells are highly radiosensitive. This is because if molecules containing  $O_2$   
587 break due to the impinging radiation, then the oxygen can build Reactive Oxygen Species  
588 (ROS) (fig.3.3(b))

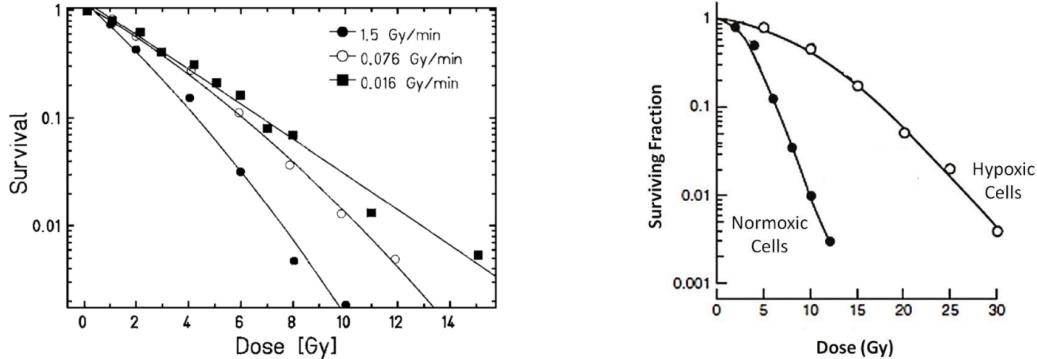


Figure 3.3: (a) Survival curve for different dose rate and (b) for different oxygen cell content

589 The Tumor Control Probability (TCP) and the Normal Tissue Complication (NTC) functions  
590 parametrize respectively the efficiency of damaging on the tumor after having released a certain  
591 dose and the probability of not affecting the healthy tissues. The intermediate zone between the  
592 increase of the TC and of the NTC is called therapeutic window, and the wider it is and the more  
593 effective the treatment is.

#### 594 Dosimetric problems

595 Finding dosimeters suitable for online monitoring of the beam at ultra high dose rate is still an  
596 open issue since almost all standard online dosimeters show saturation problems. Differently,  
597 radiochromic films, which are the standard passive dosimeters, show dose-rate independence up to  
598 109 Gy/s. **Cosa sono i radiochromic films and they do not have the same accuracy of other detectors.**  
599 The principal detectors for reference dosimetry which provide real-time dose measurement are  
600 Ionization Chambers (IC), that show saturation issue at dose per pulse (DDP) two orders of  
601 magnitude lower than the ones used for FLASH-RT. **da qui in poi** ICs devono essere calibrate  
602 secondo la metrologia , per cui grazie a protocolli di calibrazione e introducendo dei fattori correttivi  
603 si riesce a fare una misura di dose.  $k_{sat}$  which accounts for the loss of charge collected due to  
604 recombination. Doppi problemi sia di saturazione dovuta a ion recombination sia di scariche, must  
605 be carefully accounted for: questo doppio effetto è dato dal fatto che, creandosi tante cariche nella  
606 camera, che va ad annullare il campo elettrico di drift. Questo ovviamente paralizza le cariche che  
607 non driftano più, ma che anzi si ricombinano ed inoltre facilita la formazione di scariche. Per DDP  
608 minori di 1 mGy il fattore correttivo è minore al 5%, poi però aumenta substantially.

609 Scintillators have reusable, non-exhaustible scintillation centers. However, the system has a  
610 total deadtime given by both the crystal scintillation time and the electronics read-out deadtime.

611 Semiconductors show a nonreversible saturation beyond a threshold around 15 cGy/p. The  
612 scintillator used, shows a negligible saturation up to 1 Gy/p, but it increases significantly up to at  
613 least 11 Gy/p, and it reaches a cutoff value between 11 and 36 Gy/p.

614 Scintillator dosimeters are widely used in radiotherapy. They are usually operating in counting-  
615 mode where each detected signal is processed by read-out electronics. However, the system has a  
616 total deadtime given by both the crystal scintillation time and the electronics read-out deadtime.  
617 When a scintillator dosimeter is used in integrator-mode the signal is integrated over the entire  
618 irradiation time. A deadtime, due to the decay time of the scintillating material, is considered on  
619 average every N recorded pulses, where N is the number of scintillation centres in the dosimeter.

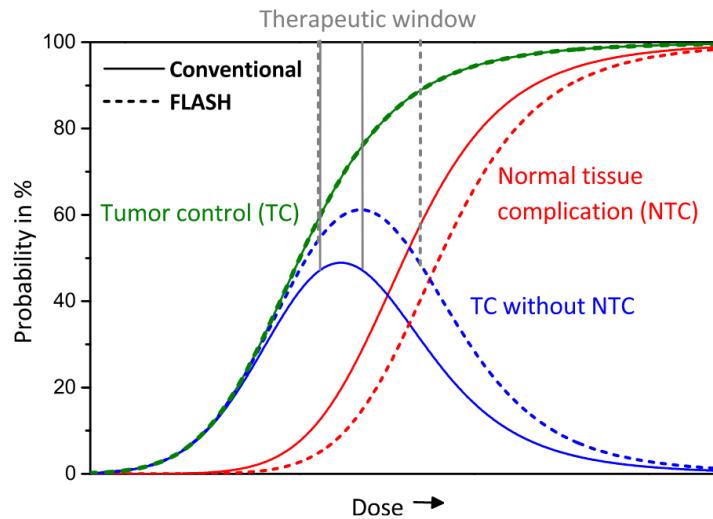


Figure 3.4: Illustration of dependence of TCP, NTCP and therapeutic window on dose, for CONV-RT ad FLASH-RT.

620        Besides saturation two other requirements for online dosimeters are high temporal and space res-  
 621        olutions. Si potrebbe pensare di poter usare i pixel detector as beam monitor che hanno risoluzioni  
 622        spaziali anche inferiori al 10 um e ris temporali -qua dare un valore è più difficile perchè per i  
 623        maps la risoluzione temporale dipende da l occupancy. Uno dei problemi è però il lungo dead time  
 624        introdotto dal lungo tempo di readout (ricorrdiamo che sopportano circa 100 Mhz/cm<sup>2</sup>).

625

# Chapter 4

626

## TJ-Monopix1

627 TJ-Monopix1 is a small electrode DMAPS with fast R/O capability, fabricated by TowerJazz  
628 foundry in 180 nm CMOS imaging process. It is part, together with prototypes from other series  
629 such as TJ-MALTA, of the ongoing R&D efforts aimed at developing DMAPS in commercial CMOS  
630 processes, that could cope with the requirements at accelerator experiments. Both TJ-Monopix  
631 and TJ-MALTA series [10], produced with the same technology by TowerJazz (the timeline of the  
632 foundry products is shown in figure 4.1), are small electrode demonstrators and principally differ in  
633 the readout design: while Monopix implements a column-drain R/O, an asynchronous R/O without  
634 any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.



Figure 4.1: Timeline in TowerJazz productions in 180 nm CMOS imaging process

635 Another Monopix series, but in 150 nm CMOS technology, has been produced by LFoundry [11].  
636 The main differences between the LF-Monopix1 and the TJ-Monopix1 (summarized in table 4.2),  
637 lay in the sensor rather than in the readout architecture, as both chips implement a fast column  
638 drain R/O with ToT capability [12][13]. Concerning the sensors, either are based on a p-type  
639 substrate, but with slightly different resistivities; in addition LFoundry pixels are larger, thicker  
640 and have a large fill factor (the very deep n-well covers ~55% of the pixel area). The primary  
641 consequence is that LF-Monopix1 pixels have a higher capacity resulting in higher consumption  
642 and noise. As I discussed in section 2.4.1, the fact that LF-Monopix has a large fill factor electrode  
643 is expected to improve its radiation hardness. Indeed, a comparison of the performance of the  
644 two chips showed that TJ-Monopix suffers a comparatively larger degradation of efficiency after  
645 irradiation, due to the low electric field in the pixel corner; on the other hand, a drawback of the  
646 large fill factor in LF-Monopix is a significant cross-talk.

647 The TJ-Monopix1 chip contains, apart from the pixels matrix, all the required support blocks  
648 used for configuration and testing:

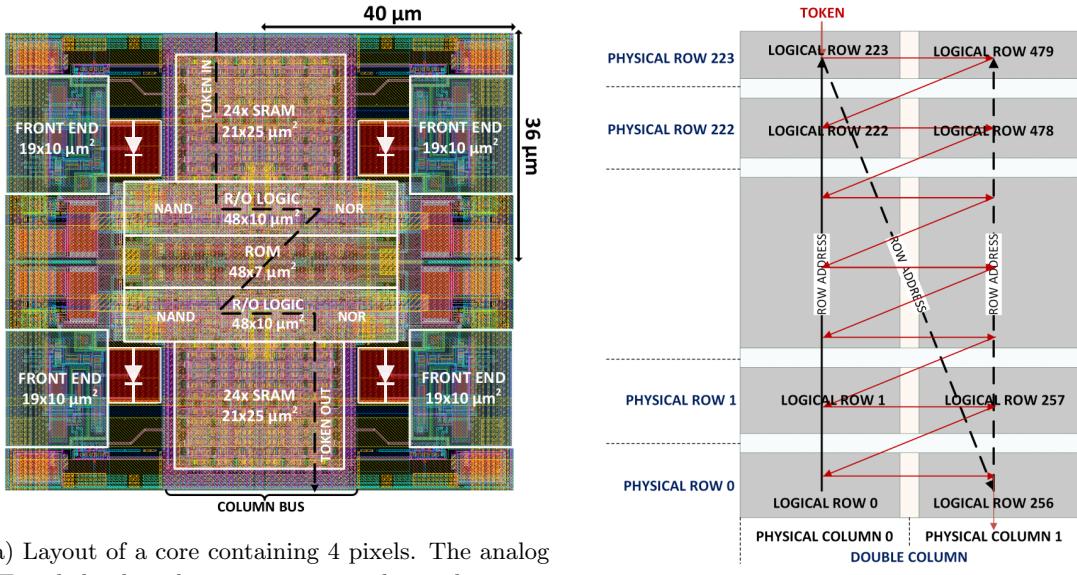
- 649 • the whole matrix contains  $224 \times 448$  pixels, yielding a total active area approximately equal  
650 to  $145 \text{ mm}^2$  over a total area of  $1 \times 2 \text{ cm}^2$ ;

	LF-Monopix1	TJ-Monopix1
Resistivity	$>2 \text{ k}\Omega\text{cm}$	$>1 \text{ k}\Omega\text{cm}$
Pixel size	$50 \times 250 \mu\text{m}^2$	$36 \times 40 \mu\text{m}^2$
Depth	$100\text{-}750 \mu\text{m}$	$25 \mu\text{m}$
Capacity	$\sim 400 \text{ fF}$	$\sim 3 \text{ fF}$
Preamplifier	charge	voltage
Threshold trimming	on pixel (4-bit DAC)	global threshold
ToT	8 bits	6 bits
Consumption	$\sim 300 \text{ mW/cm}^2$	$\sim 120 \text{ mW/cm}^2$
Threshold	$1500 e^-$	$\sim 270 e^-$
ENC	$100 e^-$	$\sim 30 e^-$

Table 4.1: Main characteristics of Monopix1 produced by TowerJazz and LFoundry [12][13]

- at the chip periphery are placed some 7-bit Digital to Analog Converter (DAC), used to generate the analog bias voltage and current levels and to configuire the FE;
- at the EoC is placed a serializer to transferred datas immediately, indeed no trigger memory is implemented in this prototypes;
- the matrix power pads are distributed at the sides
- four pixels which have analog output and which can be monitored with an oscilloscope, and therefore used for testing

Pixels are grouped in  $2 \times 2$  cores (fig. 4.2a): this layout allows to separate the analog and the digital electronics area in order to reduce the possible interference between the two parts. In addition it semplifies the routing of data as pixels on double column share the same column-bus to EoC. Therefore pixels can be addressed through the physical column/row or through the logical column/row, as shown in fig. 4.2b: in figure is also highlighted the token propagation path, whose I will discuss later.



(a) Layout of a core containing 4 pixels. The analog FE and the digital part are separated in order to reduce cross-talk be

(b)

Parameter	Value
Matrix size	$1 \times 2 \text{ cm}^2$
Pixel size	$36 \times 40 \mu\text{m}^2$
Depth	$25 \mu\text{m}$
Electrode size	$2 \mu\text{m}$
BCID	40 MHz
ToT-bit	6
Power consumption	$\sim 120 \text{ mW/cm}^2$

Table 4.2

## 664 4.1 The sensor

665 As already anticipated, TJ-Monopix1 has a p-type epitaxial layer and a n doped small collection  
 666 electrode ( $2 \mu\text{m}$  in diameter); to avoid the n-wells housing the PMOS transistors competing for the  
 667 charge collection, a deep p-well substrate, common to all the pixel FE area, is used. TJ-Monopix1  
 668 adopts the modification described in section 2.4.2 that allows to achieve a planar depletion region  
 669 near the electrode applying a relatively small reverse bias voltage. This modification improves the  
 670 efficiency of the detector, especially after irradiation, however a simulation of the electric field in  
 671 the sensor, made with the software TCAD (Technology Computer Aided Design), shows that a  
 672 nonuniform field is still produced in the lateral regions of the pixel compromising the efficiency  
 673 at the corner. Two variations to the process have been proposed in order to further enhance the  
 674 transversal component of electric field at the pixel borders: on a sample of chip, which includes the  
 675 one in Pisa, a portion of low dose implant has been removed, creating a step discontinuity in the  
 676 deep p-well corner (fig. 4.3); the second solution proposed[MOUSTAKAS THESYS, PAG 58]  
 677 consists in adding an extra deep p-well near the pixel edge. A side effect of the alteration in the  
 678 low dose implant is that the separation between the deep p-well and the p-substrate becomes weak  
 679 to the point that they cannot be biased separately to prevent the punchthrough.

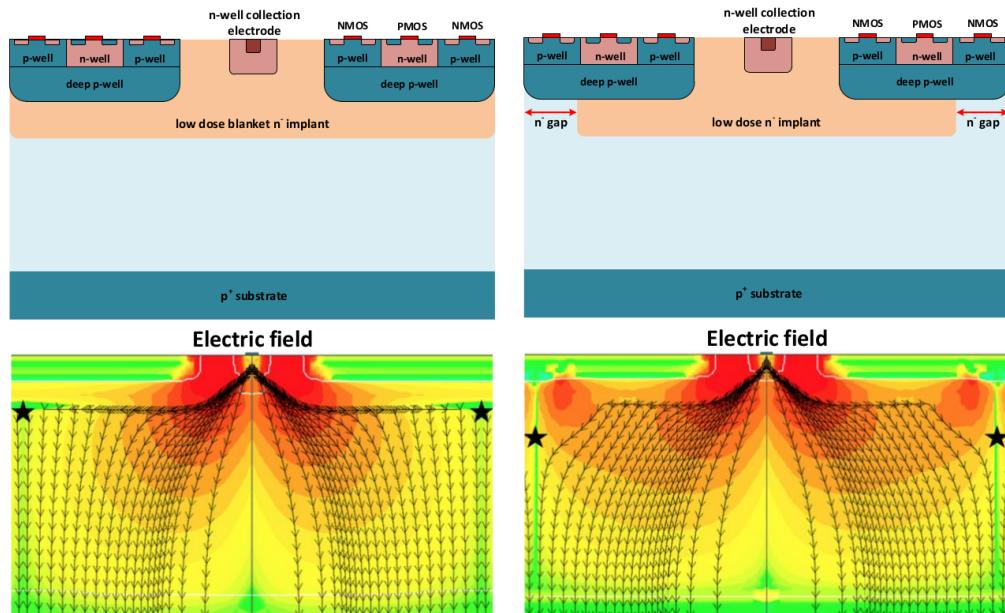


Figure 4.3: (a) The cross-section of a monolithic pixel in the TJ-Monopix with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field. this point in figure is indicated by a star . transversal component of the electric field drops at the pixel corner

Moreover, to investigate the charge collection properties, pixels within the matrix are split between bottom top half and bottom half and feature a variation in the coverage of the deep p-well: the electronics area can be fully covered or not. In particular the pixels belonging to rows from 0 to 111 are fully covered (FDPW) and pixels belonging to rows from 112 to 223 have a reduced p-well (RDPW), resulting in a enhancement of the lateral component of the electric field.

## 4.2 Front end

The matrix is split in four sections, each one corresponding to a different flavor of the FE. The four variation have been implemented in order to test the data-bus readout circuits and the input reset modes.

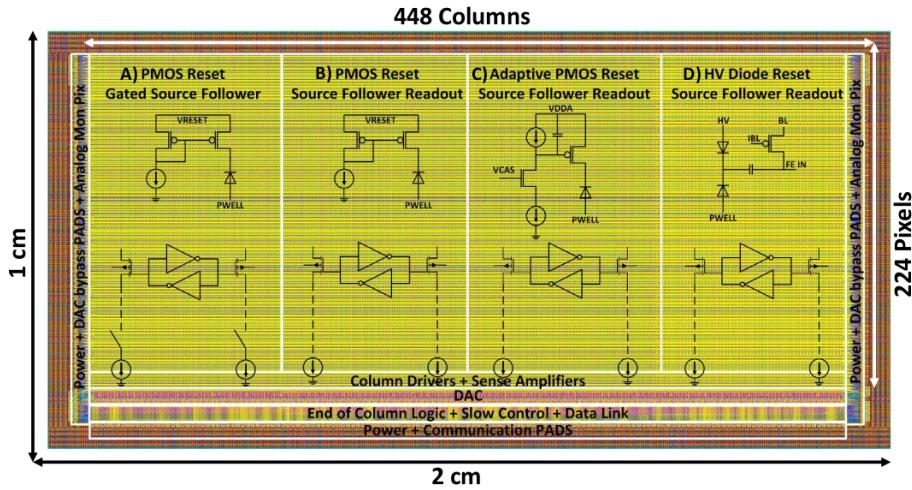


Figure 4.4

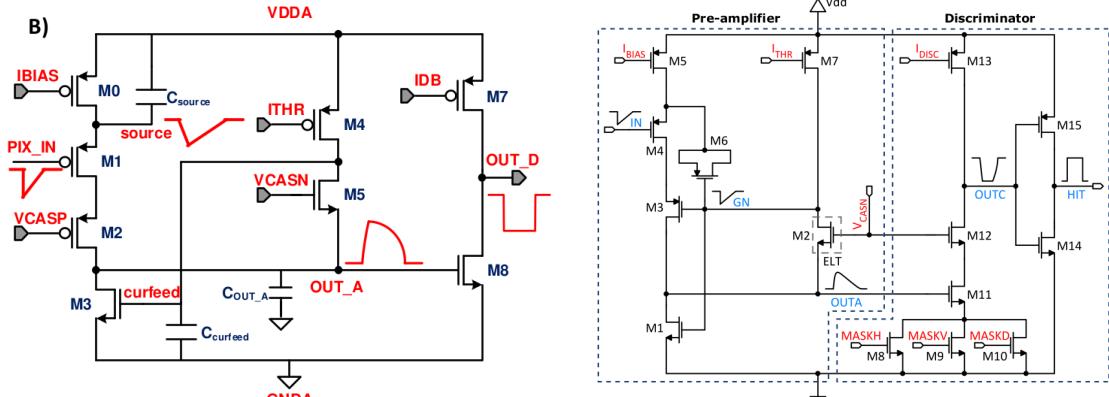
All the flavors implement a source-follower double-column bus readout: the standard variation is the flavor B, that features a PMOS input reset (referred as "PMOS reset"). Flavor A is identical to flavor B except for the realization of the source follower (it is a gated one) that aim to reduce the power consumption. **Cosa significa?** C instead implements a novel leakage compensation circuit. Moreover the collection electrode in flavors A, B, C is DC-coupled to the front-end input, while in D is AC-coupled, providing to apply a high bias voltage; for this reason flavor D is called "HV flavor".

**Principio generale:** R resistenza di reset deve essere abbastanza grande in modo da far sì che il ritorno allo zero è abbastanza lento (non devi "interferire" con la tot slope e non deve essere più corto del tempo del preamplificatore, sennò hai perdita di segnale). **Baseline reset:** all'input solitamente hai un PMOSS o un diodo; R reset

### 4.2.1 ALPIDE-like

ALPIDE chips, developed by the ALICE collaboration, implemented a standard FE to the point that many CMOS MAPS detectors used a similar FE and are called "ALPIDE-like". Considering that both TJ-Monopix1 and ARCADIA-MD1 have an ALPIDE-like FE, I am going to explain the broad principles of the early FE stage. The general idea is of the amplification to transfer the charge from a bigger capacity[14],  $C_{source}$ , to a smaller one,  $C_{out}$ : the input transistor M1 with current source IBIAS acts as a source follower and this forces the source of M1 to be equal to the gate input  $\Delta V_{PIX\_IN} = Q_{IN}/C_{IN}$ .

$$Q_{source} = C_{source} \Delta V_{PIX\_IN} \quad (4.1)$$



(a) ALPIDE-like

(b)

708 The current in M2 and the charge accumulates on  $C_{out}$  is fixed by the one on  $C_{source}$ :

$$\Delta V_{OUT\_A} = \frac{Q_{source}}{C_{OUT\_A}} = \frac{C_{source}\Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_{Source}}{C_{OUT\_A}} \frac{Q_{IN}}{C_{IN}} \quad (4.2)$$

709 A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR  
710 set the baseline value of the signal on  $C_{OUT\_A}$  and the velocity to goes down to the baseline.

### 711 IL RUOLO DI CURVFEED NON L'HO CAPITO.

712 Finally IDB defines the charge threshold with which the signal  $OUT\_A$  must be compared: de-  
713 pending on if the signal is higher than the threshold or not, the  $OUT\_D$  is high or low respectively.

714 The actual circuit implemented in TJ-Monopix1 is shown in figure 4.5b: the principal difference  
715 lays in the addition of disableing pixels' readout. This possibility is uttermost important in order to  
716 reduce the hit rate and to avoid saturating the bandwidth due to the noisy pixels, which typically  
717 are those with manufacturing defects. In the circuit transistors M8, M9 and M10 have the function  
718 of disabling registers with coordinates MASKH, MASKV and MASKD (respectively vertical, ori-  
719 zontal and diagonal) from readout: if all three transistors-signals are low, the pixel's discriminator  
720 is disabled. Compared with a configurable masking register which would allow disableing pixels  
721 individually, to use a triple redundancy reduces the sensistivity to SEU but also gives amount of  
722 intentionally masked ("ghost") pixels. This approach is suitable only for extremely small number  
723 N of pixel has to be masked: if two coordinate projection scheme had been implemented, the  
724 number of ghost pixels would have scale with  $N^2$ , if instead three coordinates are used, the N's  
exponential is lower than 2 (fig. 4.6)

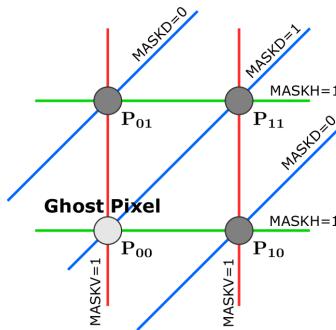


Figure 4.6

725

Parameter	Meaning	
IBIAS	mainly controls the rise time	yes? check
IDB	sets the discriminator threshold	yes
ITHR	sets the velocity of the return to the baseline	yes
ICASN	sets the baseline of the signal	yes
VRESET	sets the gain of the preamplifier	yes
IRESET	sets the gain of the preamplifier	no

Table 4.3: FE parameters which must be setted through the DAQ. "Function" means that higher parameter implies higher value

## 726 4.3 Readout logic

727 TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain  
 728 architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit  
 729 LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address.  
 730 Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is  
 731 already storing a previous one, the new data get lost. After being read, the data packet is sent to  
 732 the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (4.7). There  
 733 a FIFO is used to temporarily stored the data, which is transmitted to a computer through an  
 734 ethernet cable in a later time.

735 The access to the pixels' memory and the transmission of the data to the EoC, following  
 736 a priority chain, is managed by control signals and is based on a Finite State Machine (FSM)  
 737 composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and data transfer (DTA).  
 738 The readout sequence (??) starts with the TE of a pulse: the pixel immediately tries to grab the  
 739 column-bus turning up a hit flag signal called *token*. The token is used to control the priority chain  
 740 and propagates across the column indicating what pixel that must be read. To start the readout  
 741 and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal is activated, and  
 742 then a *read* signal controls the readout and the access to memory. During the freeze, the state of  
 743 the token for all pixels on the matrix remains settled: this does not forbid new hits on other pixels  
 744 from being recorded, but forbids pixels hit from turning on the token until the freeze is ended. The  
 745 freeze stays on until the token covers the whole priority chain and gets the EoC: during that time  
 746 new token cannot be turned on, and all hits arrived during a freeze will turn on their token at the  
 747 end of the previous freeze. Since the start of the token is used to assign a timestamp to the hit,  
 748 the token time has a direct impact on the time resolution measurement; this could be a problem  
 749 coping with high hits rate.

750 The analog FE circuit and the pixel control logic are connected by an edge detector which is  
 751 used to determine the LE and the TE of the hit pulse(fig. 4.9): when the TE is stored in the first  
 752 latch the edge detector is disabled and, if the **FREEZE** signal is not set yet, the readout starts. At  
 753 this point the HIT flag is set in a second latch and a token signal is produced and depending on  
 754 the value of **Token in** the pixel can be read or must wait until the **Token in** is off. In figure an OR  
 755 is used to manage the token propagation, but since a native OR logic port cannot be implemented  
 756 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly  
 757 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token  
 758 and to speed up the circuit optimized solution are often implemented. When the pixel become the  
 759 next to be read in the queue, and at the rising edge of the **READ** signal, the state of the pixel is  
 760 stored in a D-latch and the pixel is allowed to use the data bus; the TE and the HIT flag latches  
 761 are reset and a **READINT** signal that enable access of the RAM and ROM cells is produced.

762  
 763 The final data must provide all the hits' information: the pixel address, the ToT and the  
 764 timestamp. All those parts are assigned and appended at different time during the R/O chain:

- 765 • **Pixel address:** while the double column address (6-bit) is appended by the EoC circuit,

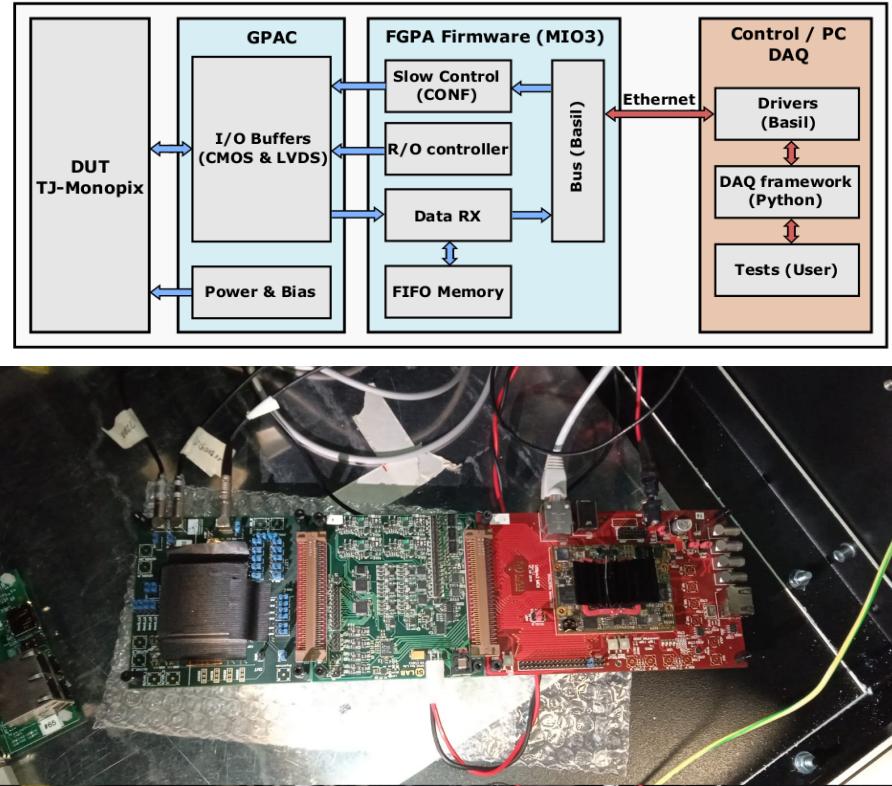


Figure 4.7: Main caption

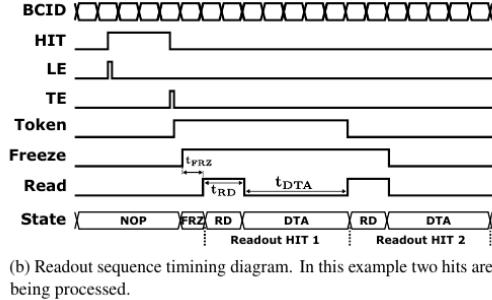


Figure 4.8: Readout timing diagram: in this example two hits are being processed

the row address (8-bits for each flavor) and the physical column in the doublet (1-bit) are assigned by the in-pixel logic

- **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge detector in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is range 0-64 clock cycle which corresponds to 0-1.6  $\mu$ s
- **Timestamp:** The timestamp of the hit correspond to the time when the pixel set up the token; it is assigned by the FPGA, that uses the LE, TE and a 640 MHz clock to derive it. For all those hits which arrived while the matrix is frozen, the timestamp is no more correlated with the time of arrival of the particle

When the bits are joined up together the complete hit data packet is 27-bit.

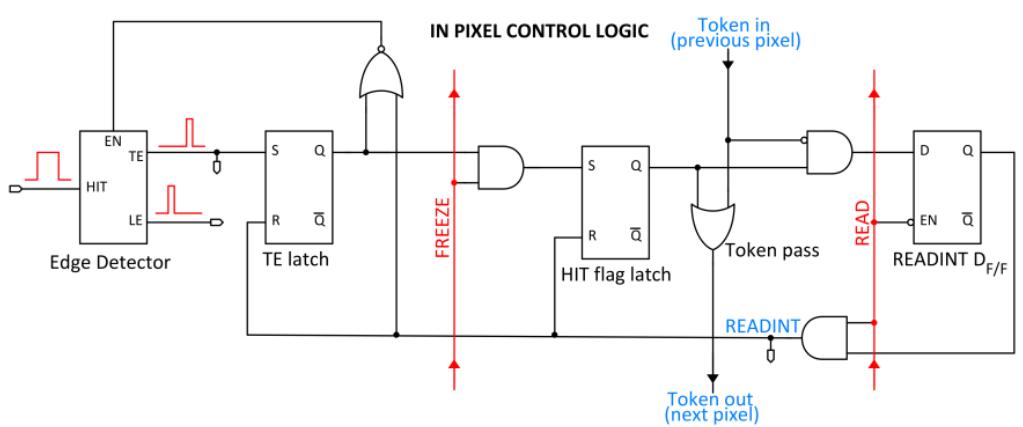


Figure 4.9

# 776 Chapter 5

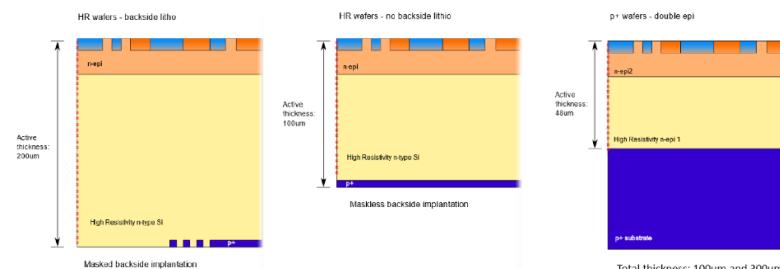
## 777 Arcadia-MD1

778 [15] [16]

779 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED  
780 Matisse a Md1 e Md2

### 781 5.1 The sensor

782 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node  
783 with six metal layer ??. The standard p-type substrate was replaced with an n-type floating zone  
784 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).



785 Figure 5.1

786 Wafer thinning and backside lithography were necessary to introduce a junction at the bottom  
787 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.  
788 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthrough  
789 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

790 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,  
791 COME VENGONO FATI I MAPS COME FAI LE GIUNZIONI

792 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.

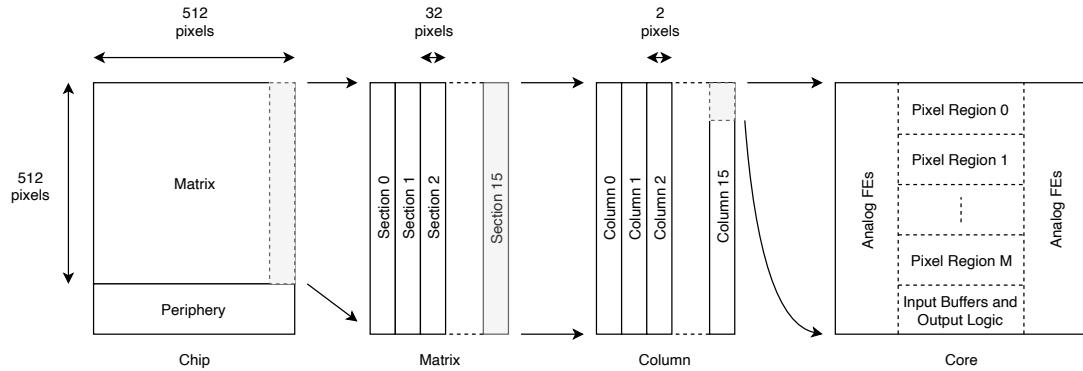
793 It is operated in full depletion with fast charge collection by drift.

794 Prima SEED si occupa di studiare le prestazioni: concept study with small-scale test struc-  
795 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo  
796 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il  
797 pwell e quanto al diodo. ..

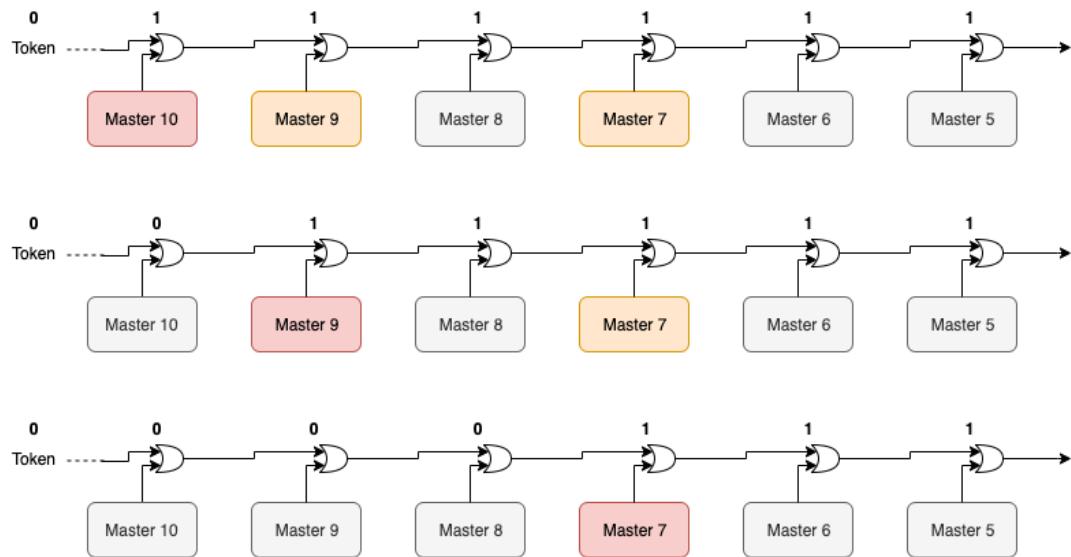
## 798 5.2 Readout logic and data structure

### 799 5.2.1 Matrix division and data-packets

800 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided  
 801 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in  
 802 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei  
 serializzaatori: sono 16 ma possono essere ridotti ad uno in modalità spazio



803 Figure 5.2



804 Figure 5.3

805 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le  
 806 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,  
 e devi accennare al timestamp

807 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively  
 808 large core allows one to take full advantage of digital synthesis tools to implement complex func-  
 809 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della  
 810 review.

811  
 812 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column  
 813 (512x2) Core (32x2) Region (4x2)

814 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

815 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for  
 816 example 8b10b encoding n =5"

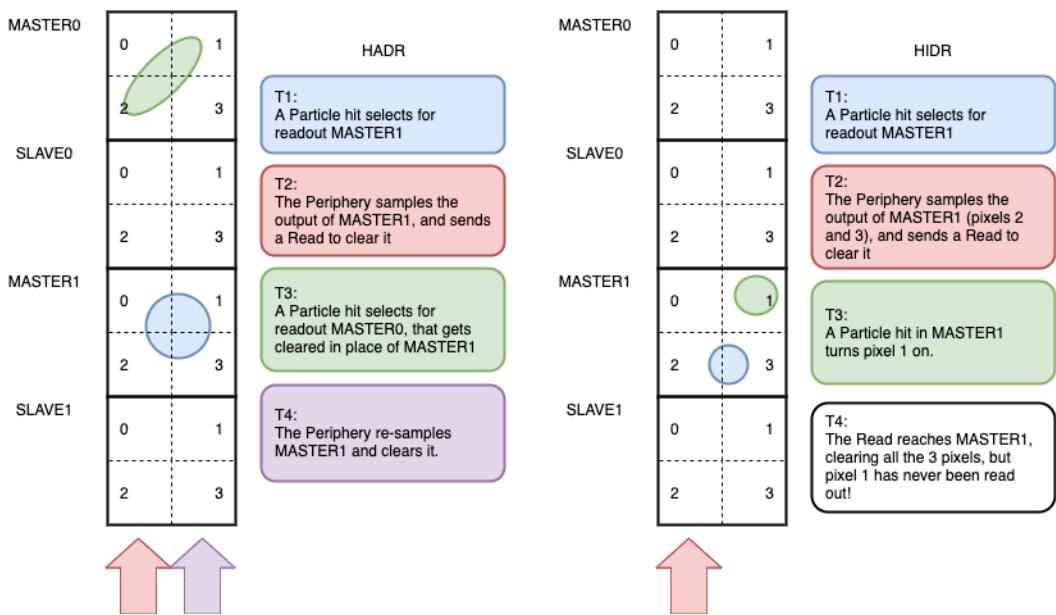


Figure 5.4

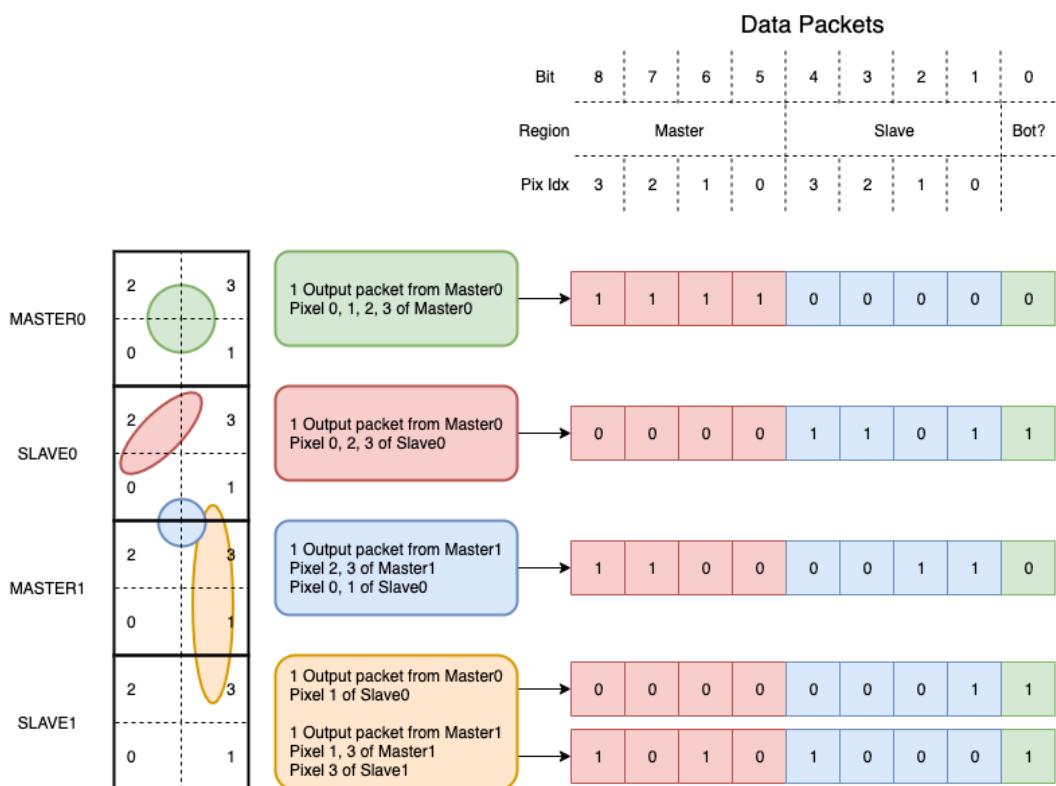


Figure 5.5

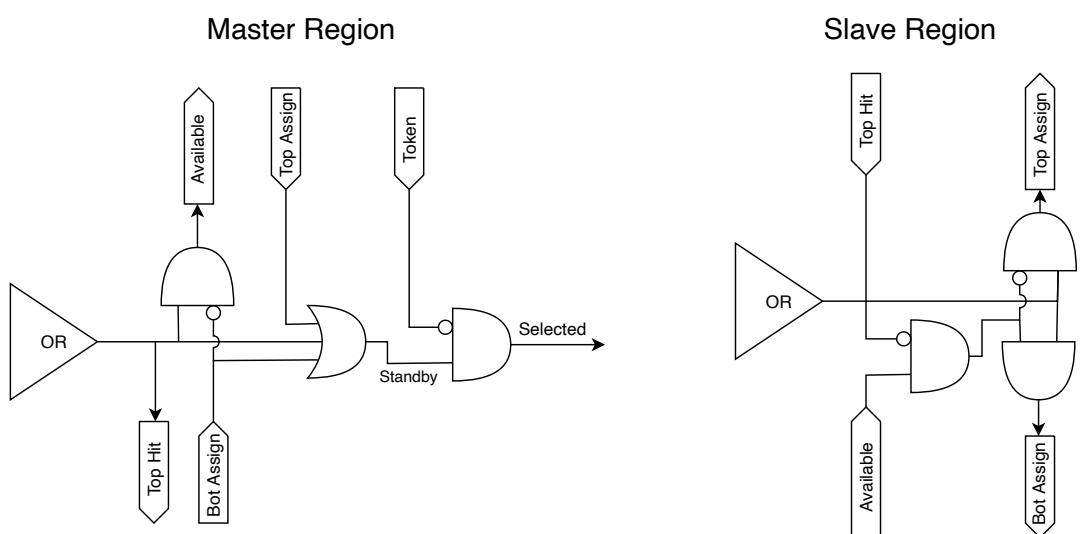


Figure 5.6

817 **Chapter 6**

818 **Threshold and noise  
characterization**

820 **6.1 TJ-Monopix1 characterization**

821 **6.1.1 Front end parameters**

822 **6.1.2 Threshold and noise: figure of merit for pixel detectors**

823 Una caratterizzazione di soglia e rumore è necessaria in quanto questi valori condizionano sia le  
824 condizioni di operatività di questi chip, che le performance. Infact, the signal to threshold ratio  
825 may be considered as the figure of merit for pixel detectors rather than the signal to noise ratio.  
826 The threshold has to be low enough to mantain a high signal efficiency, but also high enough to  
827 cut the noise: for a low threshold many pixels can fire at the same time and a positive feedback  
828 can set off a chain reaction eventually, causing all the other pixels to fire. Thus, the noise sets a  
829 lower bound to the threshold: if an occupancy  $\leq 10^{-4}$  is required, for example, this correspond  
830 to the Gaussian 1-sided tail fraction for  $3.7\sigma$ . In this case, if the noise is  $100\text{e-}$ , for example, the  
831 threshold must be higher than  $3.7 \times 100\text{e-}$ . Typically this argument sets only a minimal bound to  
832 the threshold since the variation with time and from pixel to pixel have to be taken into account:  
833 the temperature, the annealing (for example, the radiation damages in the oxide layer causes shift of  
834 MOSFET threshold voltage) and the process parameters variation across the wafer (as for example  
835 process mismatch between transistors). A requirement for the FE noise (the ENC is the equivalent  
836 input charge noise) is:

$$ENC < \sqrt{(T/3.7)^2 - T_{RMS}^2(x) - T_{RMS}^2(t)} \quad (6.1)$$

837 where the T is the threshold set,  $T_{RMS}$  is the threshold variation during time (t) and across the  
838 matrix (x).

839 For this reason is desiderable the possibility of changing and adapting the setting parameters of  
840 the FE, both in time and in space: this parameters are usually set by Digital to Analog Converter  
841 (DAC) with a number of bit in a typical range of 3-7.

842 DAC elements require a lot of space that may be not enough on the pixel area. Therefore,  
843 the FE parameters are typically global, which means that they are assigned for the whole chip,  
844 or they can be assigned for regions the matrix is divided into. The former case corresponds to  
845 TJ-Monopix1's design in which 7 bits are used for a total 127-DAC possible values, while the latter  
846 corresponds to the ARCADIA-MD1's one, [where quanti bit??](#). An other possibility, for example  
847 implemented in TJ-Monopix2, is allocate the space on each pixel for a subset of bits, then combining  
848 the global threshold with a fine tuning.

849 To measure the threshold and noise of pixels a possible way is a scan with different known  
850 injected charge at a fixed threshold, that corresponds to the value where the efficiency of the  
851 signal exceeds the 50%. Therefore, for a fixed threshold (I set IDB = 40 DAC to perform the

scan) I have used the injection circuit available on the chip to inject 100 pulses for each input charge. The injection comes on a capacity at the input of the FE circuit, whose mean value is 230 aF (in section ?? I'll present the calibration of the signal from which I also found the value of this capacity across the matrix). For the PMOS flavors: since the DAC are biased at 1.8 V, the Least significant Bit (LSB) corresponds to a voltage of 14.7 mV from which the charge for LSB  $1.43 \text{ e-}/\text{mV}$  and the conversion factor from DAC to electrons  $20.3 \text{ e-}/\text{DAC}$  are obtained. While this value is equivalent for all the PMOS flavor, the HV flavor is expected to have a different conversion factor,  $\sim 33 \text{ e-}/\text{DAC}$ , because of the different input capacity. Besides the charge, also the duration and the period of the injection pulse can be set; it is important to make the duration short enough to have the falling edge during the dead time of the pixel (in particular during the FREEZE signal) in order to avoid the undershoot, coming at high input charge, triggering the readout and reading spurious hits. Since the injection circuit is coupled in AC to the FE, if the falling edge of the pulse is sharp enough to produce an undershoot, this can be seen as a signal.

Assuming a gaussian noise, it can be described through the error function; actually, since the error function has y bounded between -1 and +1, the function I need is a modification of the  $erf$ :

$$f(x, \mu, \sigma) = \frac{1}{2} \left( 1 + erf \left( \frac{x - \mu}{\sigma\sqrt{2}} \right) \right) \quad (6.2)$$

$$erf(z) = \frac{2}{\sqrt{\pi}} e^{-z^2} dz \quad (6.3)$$

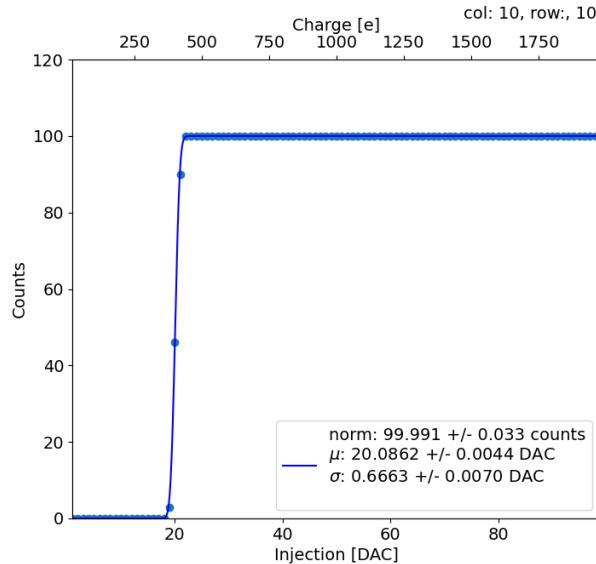


Figure 6.1: S curve for pixel (10, 10) of the PMOS flavor. The conversion of charge injected from DAC to electrons has been done assuming a conversion factor of  $20 \text{ e-}/\text{DAC}$ .

The mean minimum stable threshold evolved through different generation of chips: in the 1st generation it was around  $2500 \text{ e-}$  while in the 3rd (corresponding to nowadays chips) is less than  $500 \text{ e-}$ . This allows in thinner sensors with smaller signals: from  $16000 \text{ e-}$  produced in  $200 \mu\text{m}$ , the signal expected moved down to  $2000 \text{ e-}$  produced in  $25 \mu\text{m}$ . According with this ??, the threshold of TJ-Monopix1 is around  $500 \text{ e-}$ . **I successivi prototipi hanno una soglia e un rumore più bassi, ad esempio TJ-Monopix2 ha una soglia e un rumore...** The values of the threshold and the noise for the flavor are reported in tables 6.2

- disperione della soglia dovuta al DAC e confronta con il valore misurato
- dipendenza della soglia da IDB
- dipendenza della soglia dal gain

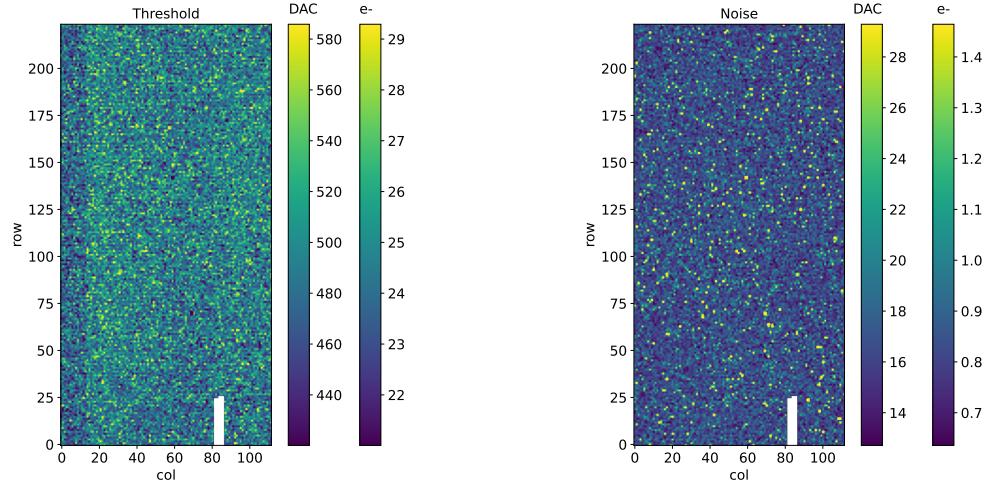
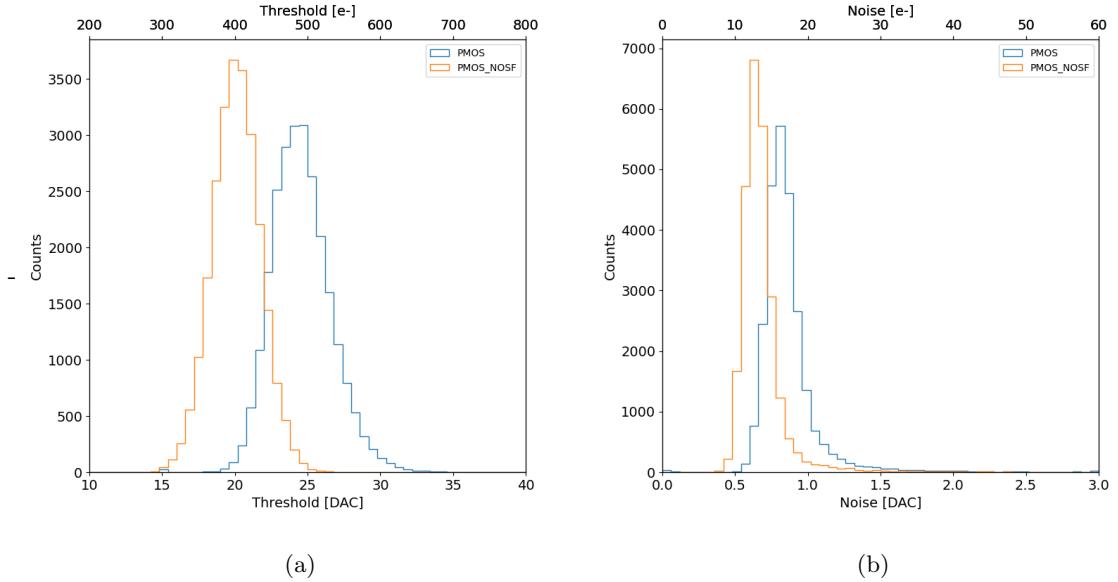


Figure 6.3

878 La dispersione della soglia dopo al tuning e dovuta al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.4)$$

879 I also have perfmorm a scan for different IDB value to verified the trend of the threshold. **METTI**  
880 **plot della media della gaussiana in funzione di IDB**

881 Dipendenza dal guadagno: per valutare l'impatto del discriminatore sul rumore uno dovrebbe  
882 convertire il segnale in uscita in segnale in carica all'ingresso. In questo modo si avrebbe:

$$ENC_{DISC} = \frac{V_{noise}^{RMS}}{G} \quad (6.5) \qquad \qquad \qquad ENC_{DISC} = \frac{V_{mis}^{RMS}}{G} \quad (6.6)$$

883

884

886 where  $V_{noise}^{RMS}$  is the RMS noise and  $V_{mis}^{RMS}$  is the mismatch voltage at the discriminator input  
887 and G is the gain of the preamplifier. Quindi, as the gain is increased, the discriminator influence

	DAC units	electrons
Threshold	$24.529 \pm 0.049$ u: $24.433 \pm 0.049$ d: $24.623 \pm 0.051$	
Threshold dispersion	$1.848 \pm 0.033$ u: $1.867 \pm 0.034$ d: $1.825 \pm 0.035$	
Noise	$0.8222 \pm 0.0043$ u: $0.8225 \pm 0.0045$ d: $0.8221 \pm 0.0043$	
Noise dispersion	$0.0975 \pm 0.0030$ u: $0.0968 \pm 0.0031$ d: $0.0970 \pm 0.0030$	

Table 6.1: Flavor PMOS

888 in noise and threshold mismatch performance is reduced. Although the discriminator noise is relatively low compared to the preamplifier noise and can be neglected, the contribution to threshold  
 889 dispersion can be significant due to the threshold variation of transistor M11  
 890

### 891 6.1.3 Calibration of the ToT

892 Abbiamo già detto che Monopix uno fornisce una misura della carica rilasciata dalla particella  
 893 incidente attraverso il Time over Threshold of a triangular pulse e che il ToT viene salvato come  
 894 variabile a 6 bit (da cui un range 0-64 escluso) con clock a 40 MHz, per cui per un bit si hanno  
 895 25 ns. Per poter associare questo tempo ad una carica è necessaria una calibrazione del segnale:  
 896 utilizzando l'iniezione è possibile studiare l'andamento del ToT con la carica iniettata. Poichè,  
 897 come già detto, l'impulso di iniezione dipende dalla C di iniezione, che sarà diversa per ogni pixel,  
 898 per effettuare una corrispondenza tra tot ad elettroni è necessaria una calibrazione assoluta di  
 899 questa capacità.

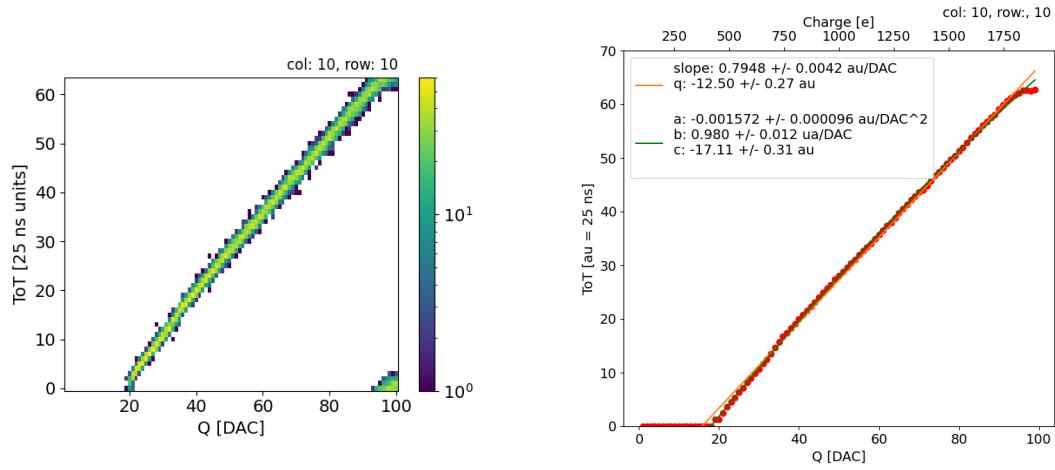


Figure 6.4: (a) ToT rollover for pixel (10,10). The ToT is in range 0-64 since it is represented by 6 bit; (b)

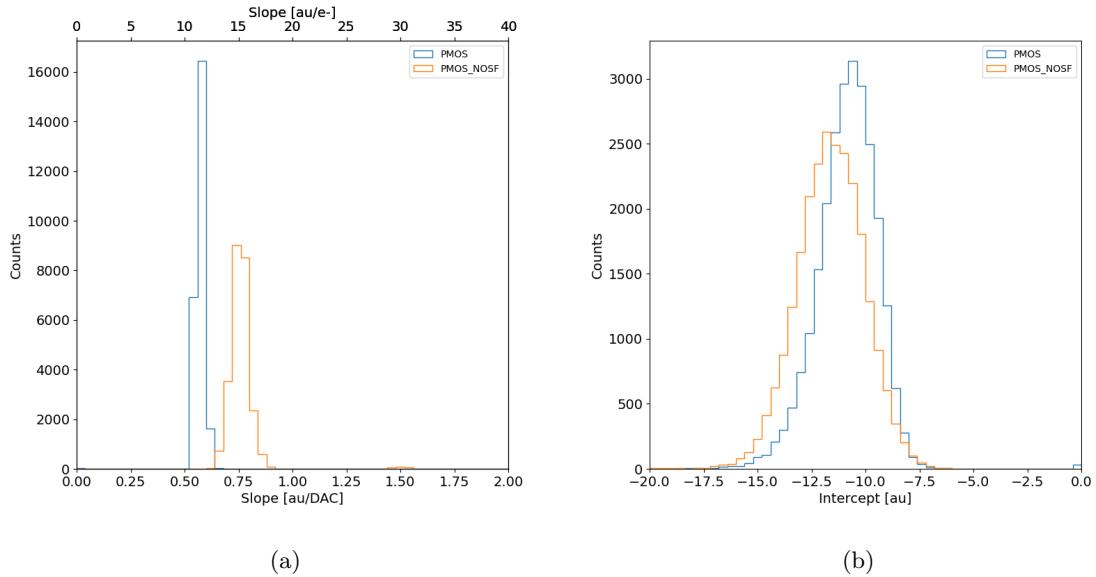


Figure 6.6

### 900    Absolute calibration

901    Per effettuare quest'ultima serve un segnale di cui si conosce il valore in elettroni con una ragionevole  
 902    precisione: per questo motivo la linea generata da un fotone da 5.9 keV di dec del ferro 55 può  
 903    risultare comoda. Questo fotone viene assorbito nel silicio con una lambda di..  
 904    considerando uno spessore dello strato epitassiale svuotato di 25  $\mu\text{m}$  quindi la P di essere assorbito  
 905    è: Il fotone fa fotoelettrico ed emette un elettrone della stessa energia del fotone; ricordando che  
 906    una particella carica produce mediamente una coppia electron-vacuum every 3.65 eV, then the  
 907    signal produced by the Fe55 source is expected to be 1616 e $-$ .

908    Il picco del ferro corrisponde agli eventi dove c'è assorbimento totale sul pixel e quindi dove  
 909    vengono raccolti tutti i 1616 elettroni, mentre nella coda a sx del picco cadono tutti gli eventi con  
 910    assorbimento parziale e/o incompleto dovuto anche a charge sharing. Motivo per cui ad esempio  
 911    in monopix due hanno fatto i pixel più piccoli: per ridurre la charge sharing riducendo così nel  
 912    segnale la coda a sx. Notiamo negli istogrammi alle figure 7.1 e 7.1 che tra i pixel ci può essere  
 913    una visibile differenza tra quanto il picco sia pronunciato. In particolare questa differenza mosgtra

	PMOS	HV
Slope [au/DAC]	$0.57145 \pm 0.00025$	
Slope dispersion [au/DAC]	$0.01685 \pm 0.00016$	
Intercept [au]	$-10.824 \pm 0.019$	
Intercept dispersion [au]	$1.225 \pm 0.013$	

Table 6.2

914 che per le righe da 0-111 e 112-224 ..

915 Parla della differenza tra fit sopra e sotto nella amtrice

$$f(x, m, q, N, \mu, \sigma) = m x + q + \frac{N}{\sigma \sqrt{2\pi}} e^{-\frac{1}{2}(\frac{(x-\mu)}{\sigma})^2} \quad (6.7)$$

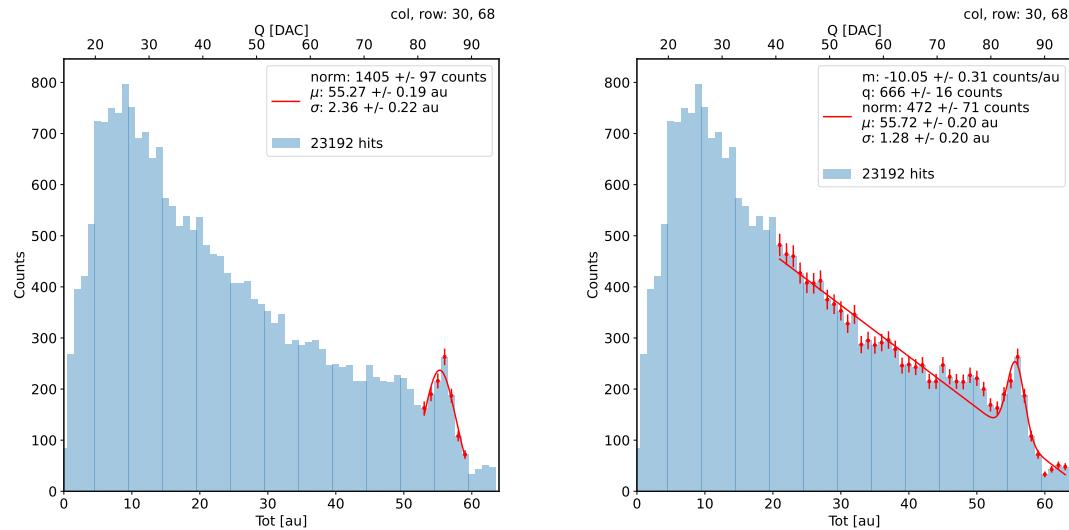


Figure 6.7: due pixel per far vedere la differenza tra i fit

#### 916 6.1.4 Fe vs bias

- 917 • rate vs bias
- 918 • posizione del picco del ferro vs bias
- 919 • eventi sotto il picco vs eventi nella coda

#### 920 6.1.5 Measurements with radioactive sources

921 CI metterei i plot con ferro, stronzio e cosmici ToT con doppia scala (calibrata in elettroni e non  
922 in ToT) hit per cluster dimensione cluster hit map di un paio di tracce?

#### 923 6.1.6 Dead time measurements

924 The hit loss is due to analog and digital pile up: the first one occurs when a new hit arrives during  
925 the pre-amplifier response, the second instead, which is the more relevant contribution with high  
926 rate, while the information of the previous hit has not yet been transferred to the periphery. As  
927 only one hit at a time can be stored on the pixel's RAM, until the data have completed the path

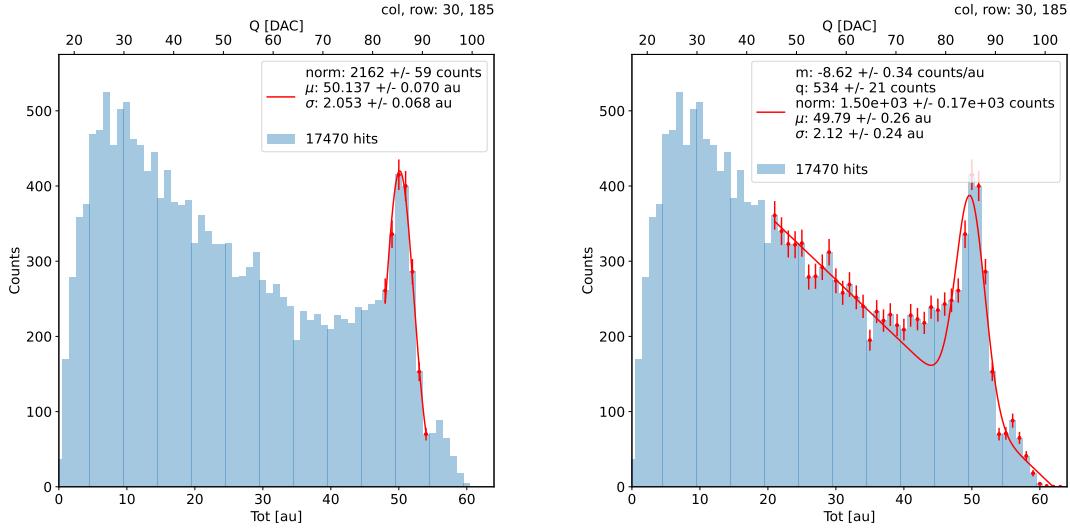


Figure 6.8: due pixel per far vedere la differenza tra i fit

to get out, the pixel is paralyzed and the dead time  $\tau$  almost corresponds with the time needed to transmit the data-packets off-chip. Since the exportation of data from pixel to the EoC occurs via a 21-bits data bus, only one clock cycle is needed to transfer the data to the end of column and the dead time bottleneck is given by the bandwidth of the serializer at the EoC. In our setup the serializer operates at 40 MHz, thus to transmit a data packet (27-bit considering the addition at the EoC) at least 675 ns are needed. For what we have said so far, the R/O is completely sequential and therefore is expected a linear dependence of the reading time on the number of pixels to read:

$$\tau = 25 \text{ ns} \times (\alpha N + \beta) \quad (6.8)$$

where  $\alpha$  and  $\beta$  are parameters dependent on the readout chain setting.

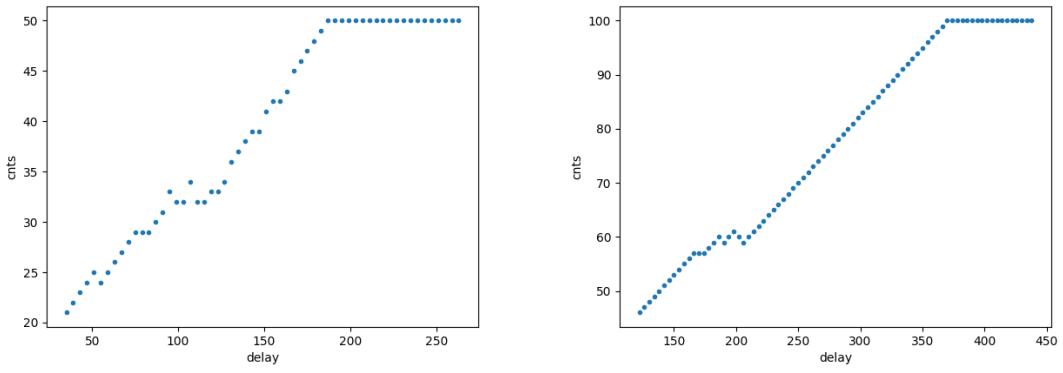
To measure and test the linearity of the reading time with the number of pixels firing, I have used the injection mode available on the chip. Indeed, the injection mode allows fixing not only the amplitude of the pulse, which corresponds to the charge in DAC units, but also the period and the width. I have injected a fix number of pulses (100) and looked for the rate when the efficiency decreases. Moreover to test that there is no dependence of the digital readout time from the charge of the pulse, I have tried to change the amplitude of the pulse injected, but the parameters found were consistent with the default configuration ones.

*Al posto degli esempi con 5 e 10 pixels metterei un esempio dell'efficienza vs il periodo quando leggo un singolo pixel. Una cosa che volevo fare era anche provare a fittare la slope con cui l'efficienza scende: se la slope è uguale per tutti il readout diventa completamente predittivo.*

While the single pixel reading time and the dead time do not depend on the position on the pixel matrix and are equal to 106 (46+60) clock counts within 1 clock count, on the other hand the  $\tau$  depends on the pixel position on the matrix when more than one pixel are firing. In particular the priority chain goes from row 224 to row 0, and from col 0 to 112, that means the last pixels to be read is the one on the bottom right corner of the matrix.

In figure 6.11 is reported the reading time versus the number of pixels injected; the R/O parameters that control the reading time and their default values are reported on table ??.

The factor  $\alpha$ , referring to eq. 6.8 is proportional to the difference (STOP\_FREEZE - START\_READ), while the offset  $\beta$  lies between 5 and 15 clock counts. Since through the injection a random hit rate on the matrix can't be simulated, as the coordinates of the pixels to inject must be specified, for convenience I used the pixels on the same column/row. No difference in the  $\alpha$  and  $\beta$  coefficients has been observed between the two cases.



(a) efficiency vs DELAY 5 pixels

(b) efficiency vs DELAY per 10pixels

Parameter	Value [DAC]	Value [ $\mu$ s]
START_FREEZE	64	1.6
STOP_FREEZE	100	2.5
START_READ	66	1.65
STOP_READ	68	1.7

Table 6.3: Default configuration of the R/O parameters

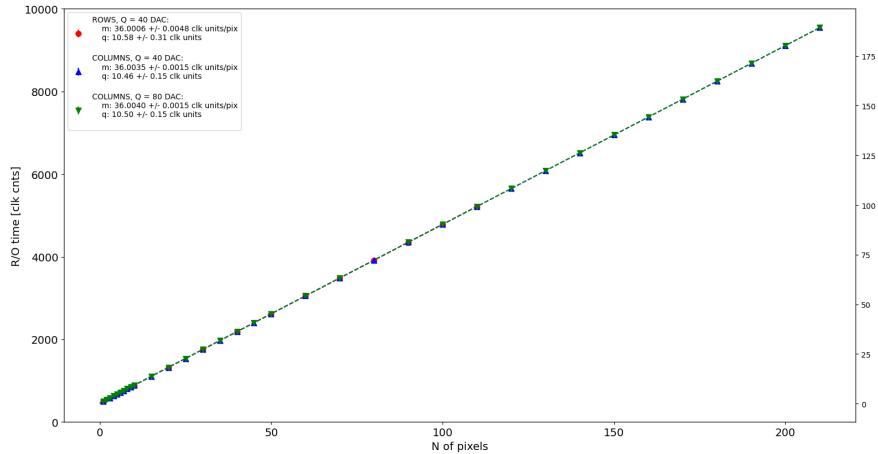


Figure 6.10

958 Ci sarebbe da spiegare perchè i parametri che usiamo noi come default non sono quelli che  
 959 minimizzano il tempo di lettura. La spiegazione è che "Abbiamo copiato i valori dal repository  
 960 di quelli di Bonn". Un'altra domanda potrebbe essere: come mai non ho esplorato una zona più  
 961 vasta per i parametri del R/O. Cambiando molto i parametri del R/O la lettura non funzionava  
 962 per niente: ad esempio CONF\_STOP\_FREEZE non può essere impostato nè sopra 105 nè sotto 95

## 963 6.2 ARCADI-MD1 characterization

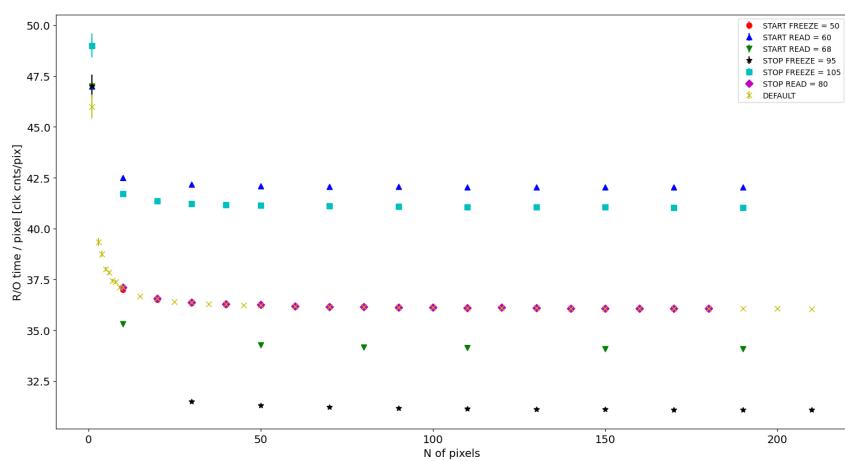


Figure 6.11

964 **Chapter 7**

965 **Test beam measurements**

966 **7.1 Testbeam motivation**

967 Possibilità di integrare carica sul pixel: due elettroni consecutivi su un pixel ogni quanto arrivano?

968 Vogliamo sfruttare l'analog pile up, per fare questo dobbiamo fare attenzione a non finire nel  
969 digital pile up Devi avere che il tot dell'elettrone (cioè MIP) è maggiore del deltat medio; in questo  
970 caso potresti riuscire ad integrare carica. Non è possibile rivelare singoli elettroni in quanto l'hit  
971 rate è troppo alto per le dosi messe a disposizioni con il fascio. Una formula di conversione è:

$$R[Hz/cm^2] = \frac{DPP[Gy]}{1.6 \cdot 10^{10} S[g/cm^2]} \quad (7.1)$$

972 where S is the stopping power in water,  $2.17 \text{ g/cm}^2$  The medium is ordinarily water, since dosimetric  
973 protocols are based on measurements in water as reference

974 La struttura del fascio e le varie quantità che si usano per descriverlo sono riportate in figure  
975 7.1. Ricordo i valori tipici che stanno in tabella in table ??.

976 **7.2 Apparatus description**

977 **7.3 Measurements**

978 Numero di hit in funzione del DDP. Spettri con e senza collimatori.

**Table 1.** Terminology used throughout the text.

Term	Symbol	Description
intra-pulse dose-rate	—	The duration of a single pulse. <sup>a</sup>
	$\bar{D}$	Mean dose-rate for a multi-pulse delivery.
pulse repetition frequency	$\dot{D}_p$	Dose-rate in a single pulse. <sup>a</sup>
	DPP	Dose in a single pulse. <sup>a</sup>
	PRF	Number of pulses delivered per unit time. <sup>a</sup>
	$t_i$	Total irradiation time from the beginning of the first delivered pulse to the end of the last delivered pulse.
ultrahigh dose-rate	—	Radiation delivered with mean dose-rate of $> \sim 40 \text{ Gy s}^{-1}$ .
	—	Ultrahigh dose-rate RT that presents decreased damage to normal tissues compared to RT delivered with conventional dose-rate of $\sim 0.04 \text{ Gy s}^{-1}$ .

<sup>a</sup>Pulses are considered to be macro-pulses unless otherwise stated (see also figure 1).

<sup>b</sup>In literature sometimes referred to as the instantaneous dose-rate.

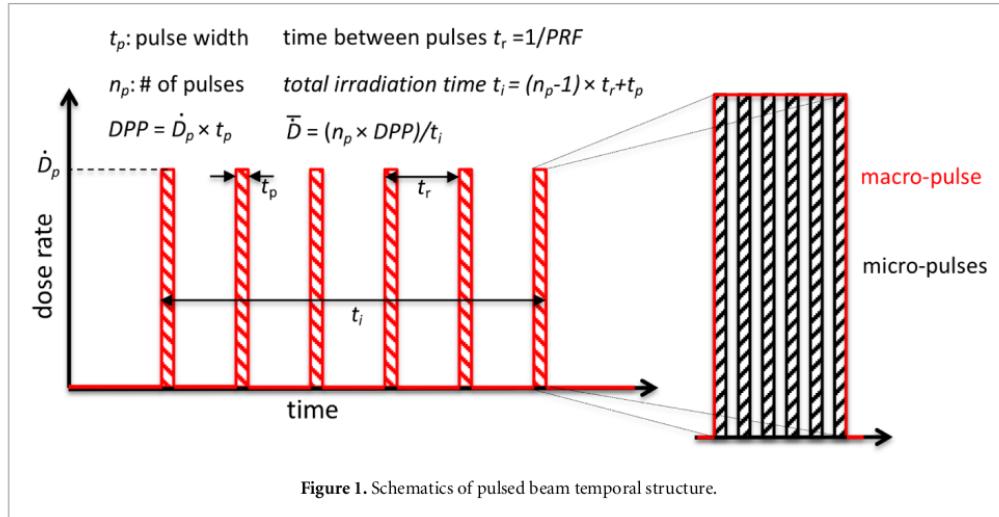


Figure 7.1

## 979 Appendix A

# 980 Pixels detector: a brief overview

### 981 A.1 Radiation damages

982 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they  
 983 are almost always installed near the interaction point where there is a high energy level of radiation.  
 984 At LHC the  $\phi_{eq}$  per year in the innermost pixel detector is  $10^{14} n_{eq}/cm^2$ ; this number reduces by  
 985 an order passing to the outer tracker layer [2] pag 341 Wermes. Here the high fluence of particles  
 986 can cause a damage both in the substrate of the detector and in the superficial electronics.

987 The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but  
 988 it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the  
 989 NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV  
 990 neutrons. Differently, surface damages are principally due to ionizing energy loss.

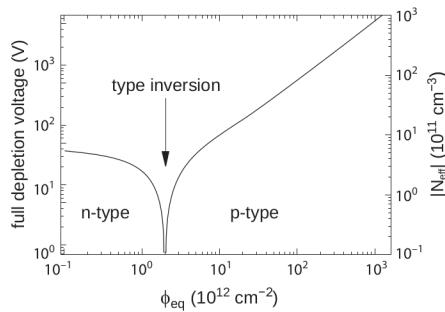
991 **DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide ( $SiO_2$ ) can  
 992 cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages  
 993 are mostly less relevant than the previous one, since with the development of microelectronics and  
 994 with the miniaturization of components (in electronic industry 6-7 nm transistors are already used,  
 995 while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit  
 996 is reduced.

997 Let's spend instead two more other words on the more-relevant substrate damages: the general  
 998 result of high radiation level is the creation of new energy levels within the silicon band gap and  
 999 depending on their energy-location their effect can be different, as described in the Shockley-Read-  
 1000 Hall (SRH) statistical model. The three main consequence of radiation damages are the changing  
 1001 of the effect doping concentration, the leakage current and the increasing of trapping probability.

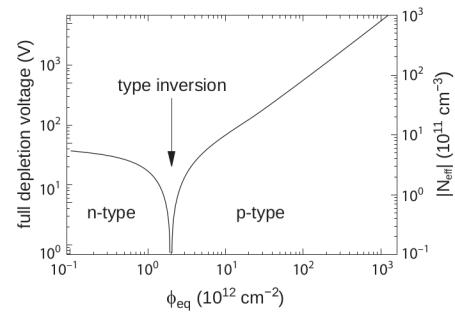
1002 **Changing of the effective doping concentration:** is associated with the creation/removal  
 1003 of donors and acceptors center which trap respectively electrons/holes from the conduction band  
 1004 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type<sup>1</sup>)

---

<sup>1</sup>L'INVERSIONE OPPOSTA NON CE L'HA PERCHÈ?



(a) 1a



(b) 1b

1005 can happen: indeed it is quite common at not too high fluences ( $\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$ ). A changing  
1006 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime  
1007 (eq.2.1) and sometimes can be difficult keeping to fully deplete the bulk.

1008 **Leakage current:** is associated with the generation-recombination centers. It has a strong  
1009 dependence with the temperature ( $I_{leak} \propto T^2$ ), whose solution is therefore to operate at lower  
1010 temperature.

1011 **Increase of trapping probability:** since the trapping probability is constant in the depleted  
1012 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,  
1013 that is the mean trapping path, decreases after irradiation and typical values are 125-250  $\mu m$  and  
1014 must be compared with the thickness of the depleted region which () corresponds to the mean drift  
1015 path.

1016 Different choices for substrate resistivity, for junctions type and for detector design are typically  
1017 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced  
1018 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))  
1019 for example, show a compensation effect for radiation damage; another example is the usage of  
1020 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage  
1021 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p  
1022 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be  
1023 placed near the diode.

1024 Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché  
1025 una particella deposita carica nell'elettronica che fa da memoria registro/RAM/.... Questo tipo  
1026 di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti  
1027 tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip  
1028 in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più  
1029 carica di quanto farebbe una MIP. Questo metodo pur essendo più comodo richiede less amount of  
1030 area ha però come drawback che il registro può essere soggetto a SEU problema non trascurabile  
1031 in acceleratori come HL-LHC adronici

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