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⁴⁵ Chapter 1

⁴⁶ Introduction

⁴⁷ Pixel detectors, members of the semiconductor detector family, have significantly been used at the
⁴⁸ accelerator experiments for energy and position measurement. Because of their dimension (today
⁴⁹ $\sim 30 \mu\text{m}$ or even better) and their spatial resolution ($\sim 5\text{-}10 \mu\text{m}$), with the availability of technology
⁵⁰ in 1980s they proved to be perfectly suitable for vertex detector in the inner layer of the detector.

⁵¹ Despite the monolithic pixels came up with CCDs, invented in 1969 and fastly used in cameras,
⁵² their usage had to wait for microelectronics developement: in MAPS device the readout electronics
⁵³ is build on the pixel's area, then the pixel dimension is limited by the dimension of transistors. This
⁵⁴ constraint favoured the usage in physics experiment of hybrid pixels, which currently constitute
⁵⁵ the state-of-art for large scale pixel detector. These ones are made by two different wafer each one
⁵⁶ containing or the sensor or the ASIC, which are after joined together through microconnection.
⁵⁷ This structure allows a separate optimization for the two components and makes hybrid pixels
⁵⁸ flexible and versatile.

⁵⁹ Requirement imposed by accelerator are stringent and they will be even more with the increase
⁶⁰ of luminosity in terms of radiation hardness, efficiency and occupancy, time resolution, material
⁶¹ budget and power consumption. For this reason experiments (as ATLAS, CMS, BelleII) began to
⁶² look at the more innovative and well-performing monolithic active pixels (MAPS) as perspective for
⁶³ their future upgrades.

⁶⁴ Che condiziona la risoluzione e l'efficienza di ricostruzione della sua traccia, e consumi del
⁶⁵ detector, sono diventati sempre più rilevanti; molti esperimenti (ATLAS, CMS, BelleII,...) stanno
⁶⁶ infatti valutando la possibilità di sostituire gli ibridi con i MAPS, che per i tempi precedenti offrono
⁶⁷ prestazioni migliori, a scapito di tempi di lettura mediamente più lunghi, vista anche la positiva
⁶⁸ esperienza di ALICE ad LHC, primo esperimento ad introdurre un detector a pixel monolitico.

⁶⁹ During my thesys I studied and characterised two monolithic active pixel chips, TJ-Monopix1
⁷⁰ and MD1; these devices, that are still prototypes, have been conceived and designed for physics
⁷¹ experiments at colliders, space experiments and also for medical applications.

⁷² il primo, TJ-Monopix1, è un prototipo di un modello selezionato per l'upgrade di Belle II
⁷³ durante il LSD nel 2025 (il chip finale si chiamerà OBELIX e avrà come sensore TJ-Monopix2,
⁷⁴ successore di Monopix1); il secondo chip è stato progettato da ARCADIA che potrà avere, nelle
⁷⁵ versioni future, applicazioni in fisica medica, in esperimenti nello spazio e ai collider.

⁷⁶ Le differenze principali tra i due chip risiedono nel segnale fornito in output (Monopix fornisce il
⁷⁷ tempo sopra soglia dell'impulso triangolare, proporzionale alla carica rilasciata nel sensore, mentre
⁷⁸ arcadia fornisce un segnale puramente digitale), nella sequenza di readout dei pixel (monopix ha
⁷⁹ una lettura puramente sequenziale di tipo "column drain") mentre arcadia ha una lettura più
⁸⁰ moderna che consente di poter aggregare dati durante la trasmissione (ad esempio nel caso di
⁸¹ formazione di cluster e creazione di hti su pixel adiacenti).

⁸² I performed a threshold and noise characterization ($\sim 400 \text{ e}^-$ and $\sim 15 \text{ e}^-$) of TJ-Monopix1 in
⁸³ order

⁸⁴ Tra i test con Monopix1 ho effettuato una caratterizzazione in soglia ($\sim 400 \text{ e}^-$) e rumore (\sim
⁸⁵ 15 e^-) al fine di visualizzare la dispersione di questi valori sulla matrice; per poter minimizzare la

86 dispersione sulla matrice e avere una più uniforme selezione della soglia (che è globale su tutta
87 la matrice), le versioni successive di TJ-Monopix1 includono e includeranno la possibilità di fare
88 piccole correzioni (3 bit per pixel vengono allocati in Monopix2) di quest'ultima pixel per pixel.
89 Per poter fornire le misure dei segnale fornito, tempo sopra soglia ToT, in elettroni, che assieme
90 alle lacune vengono create dal passaggio della particella incidente e che quindi sono la quantità
91 fisica "importante" nella misura, è stata necessaria una calibrazione assoluta dell'oggetto. Per
92 quest'ultima e per altri test ?? mi sono servita di sorgenti radiattive come il ferro 55 (emissione di
93 un fotone gamma a 5.9 kev e dello stronio 90 il cui spettro dell'elettrone emesso ha un end point
94 a x) e dei cosmici. Inoltre ho partecipato ai test di Monopix1 su fascio: abbiamo testato il chip in
95 una modalità diversa da quella per cui è stato progettato (tracking) e più simile al funzionamento
96 delle CCD, in cui non si cerca di distinguere il singolo elettrone incidente ma si integra in un
97 singolo segnale di output la carica rilasciata da più elettroni incidenti. Il fascio utilizzato (elettroni
98 da 7-9 MeV) è un fascio ad altissima intensità e verrà utilizzato per fare ricerca su radioterapia
99 ad alto rate (l'acceleratore è in grado di rilasciare dosi -con riferimento in acqua- fino a 40 Gy/s,
100 corrispondenti ad un numero di particelle di ..). Per quanto riguarda, invece, le misure sul chip
101 MD1, ho partecipato ai test elettrici e sul front end di un prototipo non ancora completamente
102 funzionante. Un nuovo chip dovrebbe arrivare nei prossimi giorni a Pisa.

103 **Chapter 2**

104 **Pixel detectors**

105 I pixel detector fanno parte della famiglia dei detector a semiconduttore e il loro funzionamento si
106 basa sulla creazione di coppie elettrone lacuna all'interno del bulk. Dalla creazione della particella
107 incidente di queste coppie e facendole driftare attraverso l'applicazione di un campo elettrico, si
108 ottiene quindi un segnale all'interno del rivelatore correlabile all'energia della particella incidente.
109 Il campo elettrico applicato, lo spessore della zona di svuotamento, le modalità con cui il
110 segnale viene processato e trasmesso all'esterno del rivelatore sono caratteristiche specifiche del
111 tipo di chip. In questo capitolo tratterò dunque i principali tipi di rivelatori a pixel, sofferandomi
112 in particolare sui pixel monoliti.

113 **2.1 Signal formation**

114 When a charge particle passes through a pixel and loses energy by ionization a part of that
115 energy is used to generate electron-hole pairs (another part is used for other processes, as the
116 lattice excitation) which are then separated by the electric field and collected at their respectively
117 electrodes (p for holes and n for electrons)¹; by the drift of these charges, a signal i_e is generated
118 on the electrode e as stated by the Shockley-Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (2.1)$$

119 where $v(t)$ is the instantaneous velocity of the charge q and E_{WF} is the weighting field, that is the
120 field obtained biasing the electrode e with 1V and all the others with 0V. The drift velocity of the
121 charge depends on the electric field and on the mobility of the particle:

$$v = \mu(E) E \quad (2.2)$$

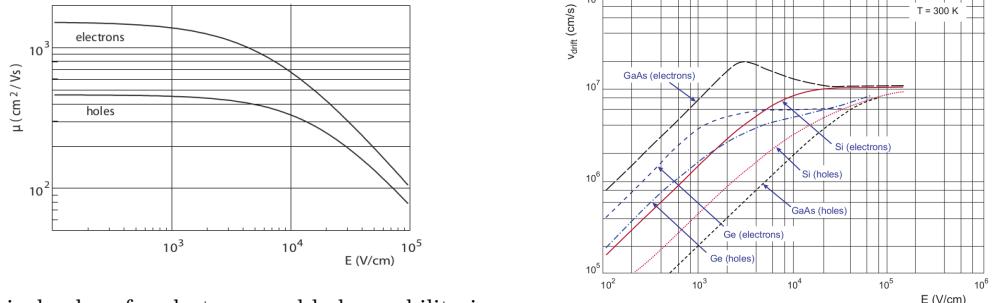
122 where $\mu(E)$ is a function of the electric field and is linear with E only for small E : at higher values
123 the probability of interactions with optical phonons increases and the mobility drops and this leads
124 to an independence of the velocity from the electric field (fig. 2.1b).

125 The average energy needed to create a pair at 300 K in silicon is $w_i = 3.65$ eV, that is more
126 than the mean ionization energy because of the interactions with phonon, since for a minimum
127 ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is
128 0.28 keV/ μ m, hence the number of electrons-vacuum pairs is:

$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (2.3)$$

129 CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALEMTE SI AGGIUNGE IL
130 FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. IL FATTORE DI FANO È
131 0.115 NEL SILICIO. ecc

¹Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout



(a) Typical values for electrons and holes mobility in silicon at room temperature are $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$, (b) Drift velocity at room temperature in different semiconductors

132 It is fundamental that pairs e/h are produced in the depleted region of the semiconductor where
 133 the probability of recombination with charge carriers is low to avoid loss of signals. Pixel detectors
 134 are then commonly reverse biased: a positive bias is given to the n electrode and a negative to the
 135 p to grow the depletion zone in the epitaxial layer below the electrode. The width of the depletion
 136 region is related with the external bias V_{ext} , the resistivity ρ and also with the dopant:

$$d_n \sim 0.55 \sqrt{\frac{\rho}{\Omega \text{cm}}} \frac{V_{ext}}{V} \mu\text{m} \quad (2.4) \quad d_p \sim 0.32 \sqrt{\frac{\rho}{\Omega \text{cm}}} \frac{V_{ext}}{V} \mu\text{m} \quad (2.5)$$

137

139

140 For that reason high resistivity wafers ($100 \Omega \text{cm} - k\Omega \text{cm}$) are typically preferred because they
 141 allow bigger depletion zone with smaller voltage bias. **Metto il disegno "standard" di una giunzione**

142 2.2 CCDs

143 descrivi come sono fatte e come funziona il readout Tens of ms due to the need to transfer the
 144 charge signals pixel by pixel through a single output circuit For photon imaging the need of high
 145 assorbtion efficiency, per cui usi materiali con alto Z

146 2.3 Hybrid pixels

147 METTI IN EVIDENZAZ CHE PUOI FARE UN READOUT CON TECNOLOGIA CMOS. Metti
 148 in evidenza che sono più veloci Hybrid pixels are made of two parts (fig. 2.2a), the sensor and the
 149 electronics: for each pixel these two parts are welded together through microconnection (bump
 150 bond).

151 They provide a practical system where readout and sensor can be optimized separately, although
 152 the testing is less easy-to-do since the sensor and the R/O must be connected together before.

153 In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-
 154 cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high
 155 levels of radiation, and also expensive.

156 A critical parameter for accelerator experiments is the material budget, which represents the main
 157 limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are
 158 thicker (\sim hundreds of μm) than monolithic ones (even less than $100 \mu\text{m}$), using the latter the
 159 material budget can be down by a third: typical value for hybrid pixels is $1.5 \% X_0$ per layer,
 160 while for monolithic $0.5 \% X_0$.

161 Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,
 162 by the way, a bigger cooling system leading in turn to an increase in material too.

163

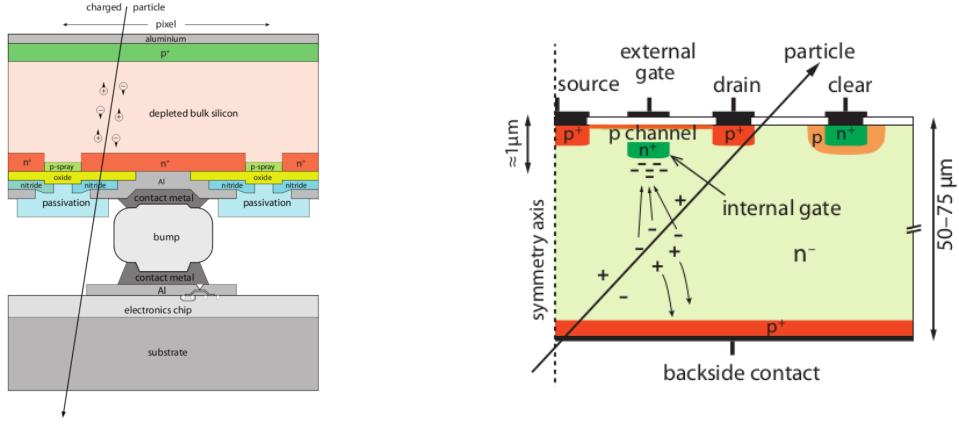


Figure 2.2: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

DEPFET are the first attempt towards the integration of the front end (FE) on the sensor bulk: they are typically mounted on a hybrid structure but they also integrate the first amplification stage.

Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor (a p-channel in fig. 2.2b): an hole current flows from source to drain which is controlled by the external gate and the internal gate together. The internal gate is made by a deep $n+$ implant towards which electrons drift after being created in the depletion region (to know how the signal is created in a pixel detector look at appendix A); the accumulation of electrons in the region underneath the n implant changes the gate potential and controls the transistor current.

DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and the large depletion region. But, since they need to be connected with ASIC the limiting factor still is the material budget.

2.4 CMOS MAPS and DMPAS

With respect to CCDs, the radiation tolerance could be greatly increased by sensing the signal charge within its own pixel, instead of transporting it over thousands of pixels. The readout speed could also be dramatically increased by in-pixel amplitude discrimination, followed by sparse readout of only the hit pixels. Monolithic active pixels accommodate on the same wafer both the sensor and the front end electronics, with the second one implanted on top within a depth of about 1 μm below the surface.

MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the development of the electronic sector which guarantees the decrease in CMOS transistors dimension at least every two years, as stated by the Moore's law².

As a matter of fact the dimension of components, their organization on the pixel area and logic density are important issues for the design and for the layout; typically different decisions are taken for different purposes.

Monolithic active pixel can be distinguished between two main categories: MAPS and depleted MAPS (DMPAS).

MAPS (figure a 2.3) have typically an epitaxial layer in range 1 μm to 20 μm and because they are not depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the collection could be partial especially after the irradiation of the detector (look at A for radiation damages), when the trapping probability become higher.

In figure 2.3 is shown as example of CMOS MAPS: the sensor in the scheme implements an n well as collection diode; to avoid the others n wells (which contain PMOS transistor) of the electronic

²Moore's law states that logic density doubles every two years.

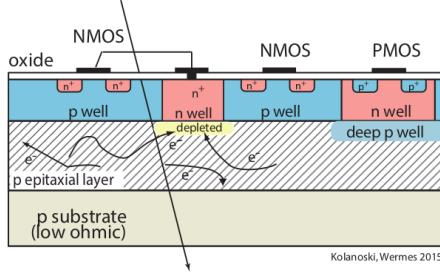


Figure 2.3: Concept cross-section of CMOS MPAS pixel

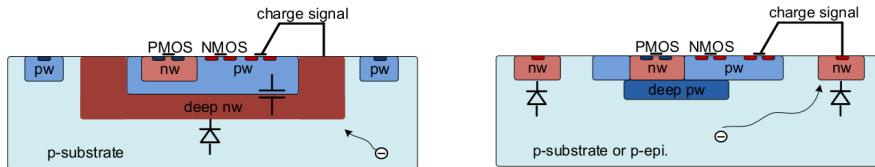


Figure 2.4: Concept cross-section with large and small fill factor

198 circuit would compete in charge collection and to shield the CMOS circuit from the substrate,
 199 additionally underlying deep p well are needed. DMAPS are instead MAPS depleted with d
 200 typically in $\sim 25 \mu\text{m}$ to $150 \mu\text{m}$ (eq. 2.1) which extends from the diode to the deep p-well, and
 201 sometimes also to the backside (in this case if one wants to collect the signal also on this electrode,
 202 additional process must be done).

203 2.4.1 DMAPS: large and small fill factor

204 There are two different sensor-design approaches (figure 2.4) to DMAPS:

- 205 • large fill factor: a large collection electrode that is a large deep n-well and that host the
 206 embedded electronics
- 207 • small fill factor: a small n-well is used as charge collection node

208 To implement a uniform and stronger electric field, DMAPS often uses large electrode design that
 209 requires multiple wells (typically four including deep n and p wells); this layout adds on to the
 210 standard terms of the total capacity of the sensor a new term (fig. 2.5), that contributes to the
 211 total amplifier input capacity. In addition to the capacity between pixels (C_{pp}) and between the
 212 pixel and the backside (C_b), a non-negligible contribution comes from the capacities between wells
 213 (C_{SW} and C_{WW}) needed to shield the embedded electronics. These capacities affect the thermal
 214 and 1/f noise of the charge amplifier and the τ_{CSA} too:

$$215 \quad ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.6) \quad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.7)$$

216 where g_m is the transconductance, τ_{sh} is the shaping time.

217 Among the disadvantages coming from this large input capacity could be the coupling between
 218 the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring
 219 electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this prob-
 220 lem is especially connected with the intra wells capacities. So, larger charge collection electrode
 221 sensors provide a uniform electric field in the bulk that results in short drift path and so in good
 222 collection properties, especially after irradiation, when trapping probability can become an issue.
 223 The drawback of a large fill-factor is the large capacity ($\sim 100 \text{ fF}$): this contributes to the noise
 224 and to a speed penalty and to a larger possibility of cross talk.

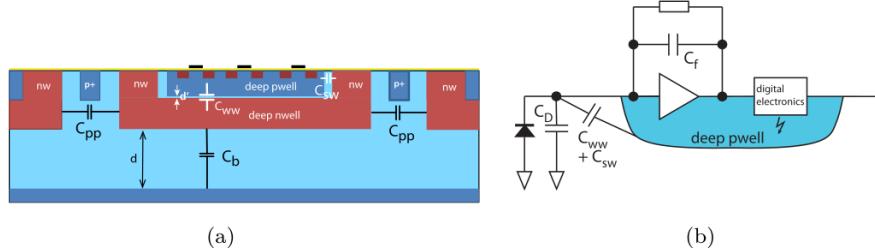


Figure 2.5: C_{pp} , C_b , C_{WW} , C_{SW}

	small fill factor	large fill factor
small sensor C	✓ (< 5 fF)	✗ (~ 100 200 fF)
low noise	✓	✗
low cross talk	✓	✗
velocity performances	✓	✗ (~100 ns)
short drift paths	✗	✓
radiation hard	✗	✓

Table 2.1: Small and large fill factor DMAPS characteristics

225 The small fill-factor variant, instead, benefits from a small capacity (5 fF to 20 fF), but suffers
 226 from a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando
 227 dei MAPS, devo ripetere qui?**

228 As we'll see these two different types of sensor require different amplifier: the large electrode one is
 229 coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.5.1).

230 2.4.2 A modified sensor

231 A process modification developed by CERN in collaboration with the foundries has become the
 232 standard solution to combine the characteristics of a small fill factor sensor (small input amplifier
 233 capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE
 234 upgrade about ten years [1].

235 A compromise between the two sensors could also be making smaller pixels, but this solution
 236 requires reducing the electronic circuit area, so a completely new pixel layout should be though.
 237 The modification consists in inserting a low dose implant under the electrode and one its advantage
 238 lies in its versatility: both standard and modified sensor are often produced for testing in fact.

239 Before the process modification the depletion region extends below the diode towards the sub-
 240 strate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.6).
 241 After, two distinct pn junctions are built: one between the deep p well and the n^- layer, and the
 242 other between the n^- and the p^- epitaxial layer, extending to the all area of the sensor.
 243 Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes
 244 can be biased separately³ and this is beneficial to enhance the vertical electric field component.
 245 The doping concentration is a trimmer parameter: it must be high enough to be greater than the
 246 epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be
 247 lower enough to allow the depletion without reaching too high bias.

³This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

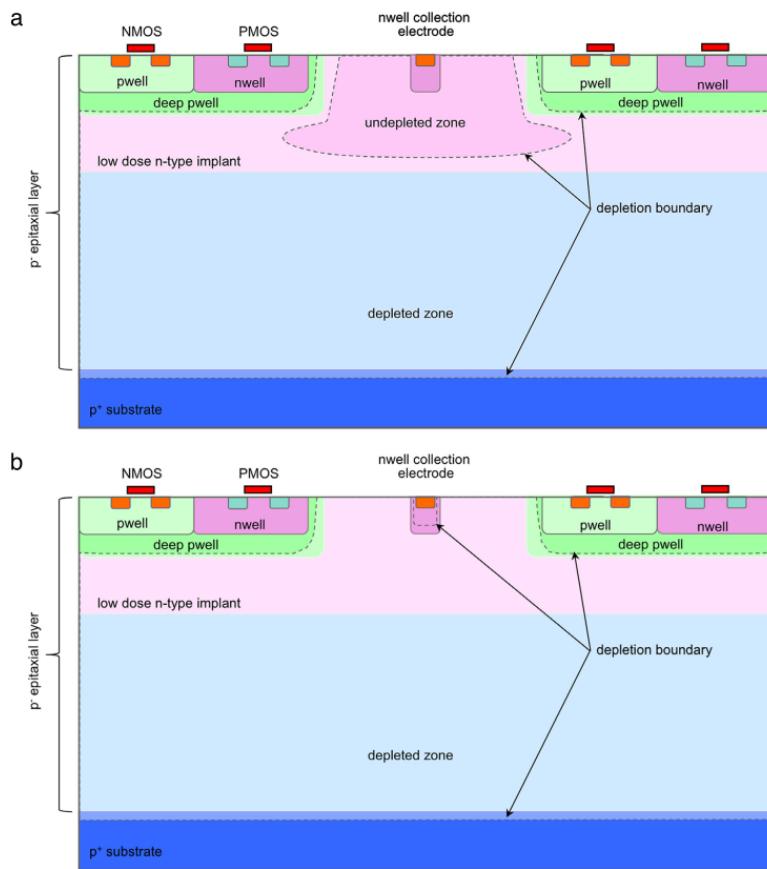


Figure 2.6: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

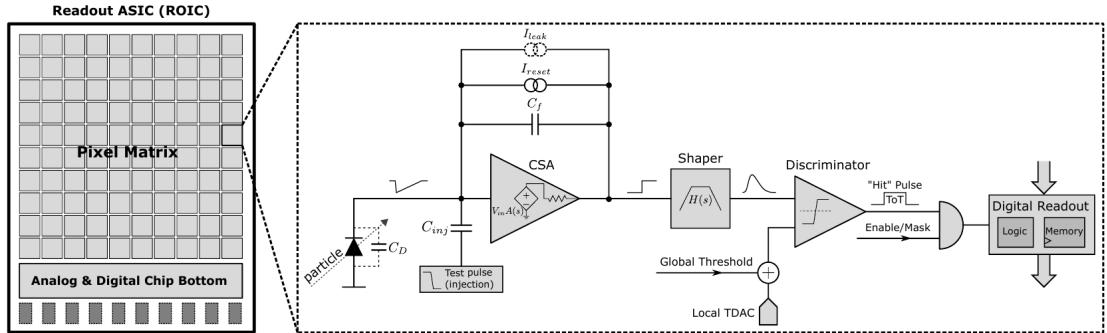


Figure 2.7: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

2.5 Analog front end

After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.7), ready to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an efficient, high-speed readout architecture, consuming as low power as possible must be provided by the readout integrated electronics (ROIC).

Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually often is the only amplification stage) with a reset to the baseline mechanism and a leakage current compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise before the amplification stage in order to not multiply that noise, and chose a reasonable threshold of the discriminator to cut noise-hits much as possible.

2.5.1 Preamplifier

Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled as an operational amplifier (OpAmp) where the gain is determined by the input and feedback impedance (first step in figure 2.7):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.8)$$

Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor MAPS whose signal is already enough high: $v_{in} = Q/C_D \approx 3fC/100 pF = 0.03 mV$, but it's fine for the small fill factor ones: $v_{in} = Q/C_D \approx 3fC/3 pF = 1 mV$.

In the case of a resistor feedback, if the signal duration time is longer than the discharge time ($\tau = R_S C_D$) of the detector the system works as current amplifier, as the signal is immediately trasmit to the amplifier; in the complementary case (signal duration longer than the discharge time) the system integrates the current on the C_D and operates as a voltage amplifier.

2.6 Readout logic

Readout logic includes the part of the circuit which takes the FE output signal, processes it and then transmit it out of pixel and/or out of chip; depending on the situation of usage different readout characteristics must be provided.

To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really

278 high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is
 279 recorded).

280 A common compromise often made is to save the time over threshold (ToT) of the pulse in clock
 281 cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen
 282 bits but, being correlated and hopefully being linear with the deposited charge by the impinging
 283 particle in the detector, it provides a sufficient information. The ToT digitalization usually takes
 284 advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels' matrix.
 285 The required timing precision is at least around 25 ns, that corresponds to the period of
 286 bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is
 287 40 MHz.

288 Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they
 have been read, and then the ToT is obtained from their difference.

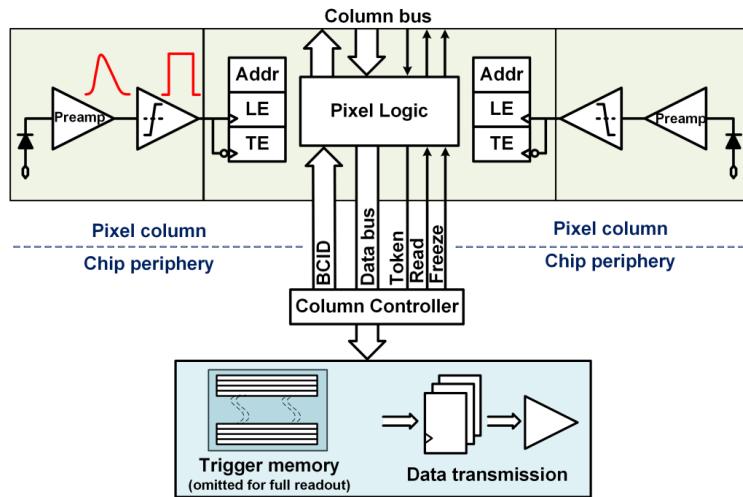


Figure 2.8: Column drain R/O scheme where ToT is saved

290 Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger
 291 system decides if the hit must be store or not. On one hand the triggered-readout needs buffers
 292 and storage memories, on the other the full readout, because there is no need to store hit data on
 293 chip, needs an high enough bandwidth.

294 A triggered readout is fundamental in accelerator experiments where the quantity of data to store
 295 is too large to be handled, and some selections have to be applied by the trigger: to give an order
 296 of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100
 297 MBit/s [2] (pag. 797).

298 Typically the trigger signal is processed in a few μs , so the pixel gets it only after a hundred clock
 299 cycles from the hit arrival time: the buffer depth must than handle the higher trigger latency.

300 After having taken out the data from the pixel, it has to be transmitted to the end of column
 301 (EoC) where a serializer deliver it out of chip, typically to an FPGA.

302 There are several ways of transmitting data from pixel to the end of column: one of the most
 303 famous is the column-drain read out, developed for CMS and ATLAS experiments [3]. All the
 304 pixels in a double-column share a data bus and only one pixel at a time, according to a priority
 305 chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit
 306 arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored
 307 on a RAM until the SH does not allow the access to memory by data bus.

308 Even if many readout architectures are based the column-drain one, it doesn't suit for large size
 309 matrices. The problem is that increasing the pixels on a column would also raise the number of
 310 pixels in the priority chain and that would result in a slowdown of the readout.

311 If there isn't any storage memory, the double-column behaves as a single server queue and the
 312 probability for a pixel of waiting a time T greater than t , with an input hit rate on the column μ

³¹³ and an output bandwidth B_W is [4]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.9)$$

³¹⁴ To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time τ due to the
³¹⁵ AFE), for example imposing $P_T > t \sim 0.001$, one obtains $(B_W - \mu) t_t \sim 6$, where t_t is the time
³¹⁶ needed to transfer the hit; since t_t is small, one must have $B_W \gg \mu$, that means a high bandwidth
[4].

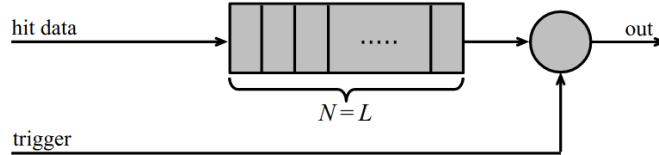


Figure 2.9: Block diagram of a pipeline buffer: N is the dimension of memory buffer and L is the trigger latency expressed in BCID cycles

³¹⁷

³¹⁸ Actually the previous one is an approximation since each pixel sees a different bandwidth de-
³¹⁹ pending on the position on the queue: the first one sees a full bandwidth, but the next sees a
³²⁰ smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen
³²¹ by the pixel i is $B_i = B - \sum_j \mu_j$, where μ_j is the hit rate of the j th pixel.

³²² The efficiency requirement on the bandwidth and the hit rate becomes: $B_{W,i} > \mu_i$, where the
³²³ index i means the constraint is for a single pixel; if all the N pixels on a column have the same
³²⁴ rate $\mu = N\mu_i$, the condition reduces to $B_W > \mu$. The bandwidth must be chosen such that the
³²⁵ mean time between hits of the last pixel in the readout chain is bigger than that.

³²⁶ In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed;
³²⁷ this means that only information from channels where the signal exceeds the discriminator thresh-
³²⁸ old are stored. Qualcosa sulla zero suppression? La metto qui questa affermazione?

³²⁹ If instead there is a local storage until a trigger signal arrives, the input rate to column bus
³³⁰ μ' is reduced compared to the hit rate μ as: $\mu' = \mu \times r \times t$, where r is the trigger rate and t is
³³¹ the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth,
³³² but the limiting factor is the buffer depth: the amount of memory designed depends both on the
³³³ expected rate μ and on the trigger latency t as $\propto \mu \times t$, that means that the higher the trigger
³³⁴ latency and the lower the hit rate to cope with.

³³⁵ In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels
³³⁶ into regions with shared storage. Let's compare two different situations: in the first one a buffer
³³⁷ is located on each pixel area, while in the second one a core of four pixels share a common buffer
³³⁸ (this architecture is commonly called FE-I4).

³³⁹ Consider a 50 kHz single pixel hits rate and a trigger latency of 5 μs , the probability of losing
³⁴⁰ hits is:

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.10)$$

³⁴¹ where I have assumed a Poissonian distribution with mean $\nu = 0.25$ to describe the counts N.

³⁴² To get an efficiency ϵ greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.11)$$

³⁴³ Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four pixels
³⁴⁴ the mean number of hits per trigger latency is $\nu = 0.25 \times 4 = 1$. To get an efficiency of 99.9% (eq.
³⁴⁵ 2.11) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

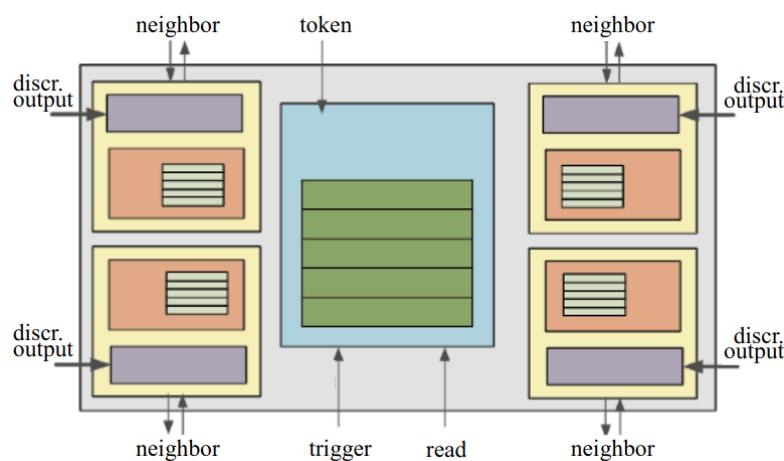


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is highlighted in light blue; latency counters and trigger management section are highlighted in green; hit processing blocks are highlighted in purple; ToT counters and ToT management units are highlighted in orange

³⁴⁶ Chapter 3

³⁴⁷ Use of pixel detectors

³⁴⁸ There always was a tight relation between the development of cameras and pixel detectors since
³⁴⁹ 1969, when the idea of CCDs, thanks to whom Boyle and Smith were awarded the Nobel Prize in
³⁵⁰ Physics in 2009, revolutionized photography allowing light to be captured electronically instead of
³⁵¹ on film. Even though the CMOS technology was already known when CCDs spread, the costs of
³⁵² productions were too high to allow the diffusion of these sensors for which needed to wait until
³⁵³ 1990s. From that period on, the fast diffusion of CMOS was mainly due to the less cost than
³⁵⁴ CCD, and the less power required for supply. Nowadays CCDs are still preferred over MAPS in
³⁵⁵ astronomy, where the astronomical sources' rate are low enough to cope with tens of ms for the
³⁵⁶ readout.

³⁵⁷ The principal use cases of pixel detectors are particle tracking and imaging: in the former case
³⁵⁸ individual charged particles have to be identified, in the latter instead an image is obtained by
³⁵⁹ the usually un-triggered accumulation of the impinging radiation. Also the demands on detectors
³⁶⁰ performance depends on their usage, in particular tracking requires high spatial resolution, fast
³⁶¹ readout and radiation hardness.

³⁶² 3.1 Tracking in HEP

³⁶³ At first the physics world overlooked the CCDs, and all pixel in general, as against the gaseous
³⁶⁴ detector for tracking: there was no need to replace these ones which had a sufficient good resolution
³⁶⁵ ($100\text{ }\mu\text{m}$). Since 1974, with the measurement of the invariant mass of the **j psi** and the affirmation
³⁶⁶ of the quark model, all experiments start to look for better spatial resolutions in order to achieve
³⁶⁷ the possibility of reconstructing short lived particle.

³⁶⁸ Historically, the first pixel detector employed in particle physics was a CCD: it was installed in
³⁶⁹ the spectrometer at the CERN's Super Proton Synchrotron (SPS) by the ACCMOR Collaboration
³⁷⁰ (Amsterdam, CERN, Cracow, Munich, Oxford, RAL) at mid 1980s, with the purpose of studying
³⁷¹ the recently-discovered charm particles. The second famous usage of CCDs took place at SLAC
³⁷² in the Large Detector (SLD) during the two years 1996-98. **Cosa vedono di così importante da**
³⁷³ **dire che servono i pixel detector?** From that period on particle tracking in experiments have been
³⁷⁴ transformed radically: it was mandatory for HEP experiments to build an inner vertex detector.
³⁷⁵ In 1991, the more demanding environments led to the development of hybrid pixel detectors:
³⁷⁶ a dedicated collaboration, RD19, was established at CERN with the specific goal to define a
³⁷⁷ semiconductor micropattern detector with an incorporated signal processing at a microscopic level.
³⁷⁸ In those years a wide set of prototypes of hybrid pixel has been manufactured; among the greatest
³⁷⁹ productions a mention goes to the huge ATLAS and CMS vertex detectors. From the middle of
³⁸⁰ 2013 a second collaboration, RD 53, has been established with the new goal to find a pixel detector
³⁸¹ suitable for phase II future upgrades of those experiments. Even if the collaboration is specifically
³⁸² focused on design of hybrid pixel readout chips (aiming to 65 nm technique so that the electronics
³⁸³ fits within the pixel area), also other options have been taken in account and many test have been
³⁸⁴ done on MAPS for example. Requirements imposed by HL-LHC will become higher in time: for

example, a dose and radiation of 5 Mrad and 1016NIEL are expected after 5 years of operation. Time resolution, material budget and power consumption are also issues for the upgrade: a time resolution better than 25 ns for a bunch crossing frequency of 40 MHz, a material budget lower than 2% and a power consumption lower than 500 mW/cm² are required.

Amidst the solutions proposed 3D silicon detector, invented by Sherwood Parker in 1995, and MAPS are the most promising. In 3D sensors the electrode is a narrow column of n-type implanted vertically across the bulk instead of being implanted on the wafer's surface. The charge produced by the impinging particle is then drifted transversally within the pixel, and, as the mean path between two electrode can be sufficient low, the trap probability is not an issue. 3D pixels have been already proved in ATLAS tracker [quando?](#). Even if 3D detector are adequately radiation hard, MAPS architecture looked very promising from the beginning: they overcome both the CCDs long reading time and the hybrid problems (I have already explained in section ?? the benefits of MAPS). Experiments such as ALICE at LHC and STAR at RHIC have already introduced the CMOS MAPS technology in their detectors. ALICE Tracking System (ITS2), upgraded during the LHC long shut down in 2019-20, was the first large-area ($\sim 10 \text{ m}^2$ covered by 2.5 Gpixels) silicon vertex detector based on CMOS MAPS.

3.1.1 Hybrid pixels at LHC and at SuperKEKB

ATLAS

With CMS, ATLAS is one of two general-purpose detectors at the LHC and has the largest volume detector ever constructed for a particle collider (46 m long and 25 m in diameter). The Inner Detector consists of three different systems all immersed in a magnetic field parallel to the beam axis whose main components are: the pixel, the micro-strips and transition radiation trackers. Concerning the pixel detector, 92 million pixels are divided in 4 barrel layers and 3 disks in each end-cap region, covering a total area of 1.9 m² and having a 15 kW of power consumption.

As stated by the ATLAS collaboration the pixel detector is exposed by an extreme particle flux: "By the end of Run 3¹, the number of particles that will have hit the innermost pixel layers will be comparable to the number it would receive if it were placed only a few kilometres from the Sun during a solar flare". Considering that the particle density will increase even more with HL-LHC, radiation hardness is definitively target to achieve.

The most ambitious goal is employ a MAPS-based detector for the inner-layer barrels, and for this reason the RD53 collaboration is performing many test on MAPS prototypes, as Monopix of which I will talk about in section ??.

Up to now this possibility will be eventually implemented during the second phase of the HL-LHC era, as at the start of high-luminosity operation the selected option is the hybrid one. The sensor will be bonded with ITkPix, the first full-scale 65 nm hybrid pixel-readout chip developed by the RD53 collaboration. Regarding the sensor, a valuable option is using 3D pixels, which have already proved themselves in ATLAS, for the insertable B layer (IBL).[qualcosa in più sui 3d](#). The number of pixels will be increased of a factor about 7, passing from 92 millions to 6 billion.

CMS

[da scrivere](#) 124 million pixels; cylindrical layers roughly at 3cm, 7cm, 11cm and 16cm and disks at either end, and so will be vital in reconstructing the tracks of very short-lived particles. Each of these silicon pixels is 100um by 150um, even with only around 50 microwatts per pixel, the total power output is 7.5kW-

LHCb

LHCb is a dedicated heavy-flavour physics experiment that exploits pp interactions at 14 TeV at LHC. It was the last experiment to upgrade the vertex detector, the Vertex Locator (VELO),

¹Run 3 start in June 2022

431 replacing the silicon-strip with pixels in May 2022. As the instantaneous luminosity in Run3 is
432 increased by a factor $\lesssim 10$, much of the readout electronics and of the trigger system have been
433 developed in order to cope with the large interaction rate. To place the detector as close as possible
434 to the beampipe and reach a better track reconstruction resolution, the VELO has a surprising
435 feature: it can be moved. During the injection of LHC protons it is parket at 3 cm from the beams
436 and only when the stability is reach it is brought at ~ 5 mm. Radiation hardness as well as readout
437 speed are then a priority for the detectors: that's why the collaboration opted for a hybrid system.
438 The Velopix is made bonding sensors, each measuring 55×55 micrometers, 200 μm -thick to a
439 200 μm -thick ASIC specially developed for LHCb and coming from the Medipix family (sec. ??),
440 which can handles hit rates up to 900 MHz per chip. Since the detector is operated under vacuum
441 near the beam pipe, the heat removal is particularly difficult and evaporative CO₂ microchannel
442 cooling are used.

443 **BelleII**

444 The current vertex detector of BelleII, VXD, is made of a pixel detector (PXD), fabricated with
445 2 layers of DEPFET-based pixels, and 4 layers of a double-sided silicon strip detectors (SVD)[5].
446 Due to the small capacitance of the collection node, DEPFET presents a high signal-to-noise ratio
447 (in 30-50) thanks to the low intrinsic noise and to the large signal achieved with the fully depleted
448 bulk: pixels are thinned to 75 μm in the active region, then a MIP is supposed to create a signal of
449 $\sim 6000 e^-$, while the typical noise of DEPFET is around 200 e^- . The ASIC read out is still based
450 on a rolling shutter logic, with an integration time of 20 μs . In order to reduce the data-storage
451 memory PXD hits are only used to improve spatial resolution of tracks: the SVD informations are
452 used by the High Level Trigger (HLT) to look for regions of interest in the pixel ladders just by
453 extrapolating back the tracks found in the tracker detector, and this method allows to store only
454 data belonging to these areas; the PXD hits are then used in offline track fit to improve the vertex
455 resolution.

456 MAPS have been proposed for the replacement of VXD during the Long Shut Down 2 (LSD2)
457 foreseen around 2026-27; the new vertex detector, VTX, should be made of 5 layers fabricated
458 by the optimized Belle II pixel sensor (OBELIX), a detector based on TJ-Monopix have been
459 selected (look at chapter ??). The main advantages VTX should bring are a obvious improving
460 in the track and vertex resolution (14 μm before upgrade, $\lesssim 10 \mu\text{m}$ expected after upgrade) and a
461 reduction in the X_0 (da.. a..), a higher background tolerance because of the smaller sensor than
462 strips dimension and a low bandwidth due to the on-chip sparsification.

463 **3.1.2 First attempts to MAPS**

464 **MIMOSA at EUDET and STAR**

465 MIMOSA [6][7] (standing for Minimum Ionizing MOS Active pixel sensor), designed in 2008,
466 prefigured the architecture of MAPS for coming vertex detector being the first large scale sensor
467 to be employed as detector. MIMOSA-26 equiped the final version of EUDET high resolution
468 beam telescope both at CERN-SPS and at DESY while the MIMOSA-28 devices are used for
469 the first MAPS-based vertex detector at the STAR experiment. MIMOSA-26 is fabricated in a
470 350 nm, and a module features 1152 columns, split into 18 independent groups, and 576 rows, with
471 square pixels having a side of 18.4 μm length; therefore, because of the small dimension, charge
472 sharing is an issue aggiungi qualcosa. The readout is done in a rolling shutter mode: the chip is
473 an Active Pixels (APS) and therefore it incorporates the amplification on pixel, while the signal
474 discrimination and zero-suppression logic are placed at the EoC, where is also placed a memory.
475 The chip is an Active Pixels (APS) and therefore it incorporates the amplification on pixel, while
476 the signal discrimination and zero-suppression logic are placed at the EoC: the readout is done in
477 a rolling shutter mode with a frame integration time that can be lowered down to 85 ms, and a
478 memory allowing to store up to six hits is.

479 The EUDET telescope, equipped with six sensor planes, requires highly granular and thin pixel

480 detectors in order to achieve an excellent track resolution (around $2\text{ }\mu\text{m}$) even at the rather low
 481 particle energies of up to 6 GeV. The STAR experiment at the Relativistic Heavy Ion Collide
 482 (RHIC) accelerator at the Brookhaven National Laboratory (BNL) is the first to include MAPS
 483 in the vertex detector[8]. The main tracking detector in STAR is a TPC with radii 60-190 cm
 484 embedded in a 0.5 T solenoidal magnetic field, that provides a pointing resolution of approximately
 485 1 mm. The pixel detector, PXL, is a part of a 3-detector system, Heavy Flavor Tracker (HFT), that
 486 has been added to the pre-existing STAR apparatus just before the 2014 Run in order to improve
 487 the impact parameter resolution and to enable the direct reconstruction of hadronic decays of heavy
 488 flavor mesons and baryons. The Heavy Flavor Tracker (HFT) is composed by the Silicon Strip
 489 Detector (SSD), the Intermediate Silicon Tracker (IST) and the Pixel Detector (PXL); the first
 490 one is placed at 22 cm from the beam pipe and consists of double sided strips with $95\text{ }\mu\text{m}$ inter-strip
 491 pitch, the second one, placed at 14 cm, is made of single sided silicon pads with $600\text{ }\mu\text{m} \times 6\text{ mm}$ pitch
 492 and the last one made by two layers is placed at 2.8 cm and 8 cm fabricated with ULTIMATE2 (also
 493 known as MIMOSA-28), a successor of MIMOSA-26 sensor, with pitch $20.7\text{ }\mu\text{m}$ and thinned down
 494 to $50\text{ }\mu\text{m}$. An area of 0.16 m^2 are covered by 400 MAPS sensor, corresponding to 356 millions of
 495 pixels divided into array size of 928×960 . Each pixel includes circuitry for readout, amplification,
 496 and Correlated Double Sampling (CDS) for signal extraction and noise subtraction and the frame
 497 integration time is $185.6\text{ }\mu\text{s}$; after the subtraction the signal to noise ratio is ~ 30 , with a noise
 498 between 10-12 electrons and a signal of 1000 e^- . Thanks to the HFT system and the PXL, STAR
 499 achieved a track pointing resolution $46\text{ }\mu\text{m}$ for $750\text{ MeV}/c$ kaons, and better than $30\text{ }\mu\text{m}$ for particle
 500 momenta bigger than $1\text{ GeV}/c$: this performance enabled the study of D-meson production with a
 high significance signal.

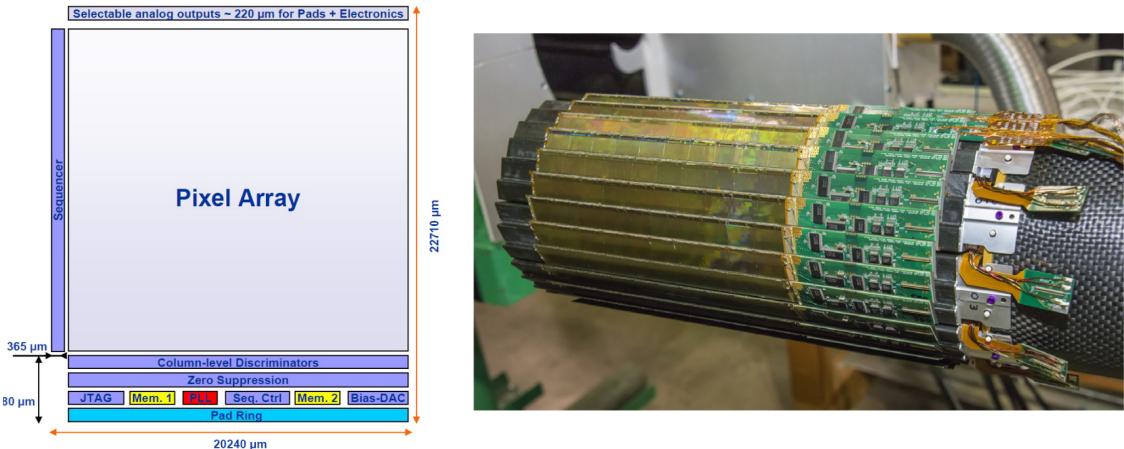


Figure 3.1: (a) The HFT PXL detector; (b) Block-diagram of the ULTIMATE-2 sensor

501

502 ALPIDE at ALICE

503 ALICE (A Large Ion Collider Experiment) is a detector dedicated to heavy-ion physics and to the
 504 study of the condensed phase of the chromodynamics at the LHC. The tracking detector consists of
 505 the Inner Tracking System (ITS), the gaseous Time Projection Chamber (TPC) and the Transition
 506 Radiation Detector (TRD), and all those are embedded in a magnetic field of 0.5 T. The ITS is
 507 made by six layers of detectors, two for each type, from the interaction point outwards: Silicon
 508 Pixel Detector (SPD), Silicon Drift Detector (SDD) and Silicon Strip Detector (SSD). Contrary
 509 to the others LHC experiments, ALICE tracker is placed in a quite different environments: the
 510 expected dose is smaller by two order of magnitude and the rate of interactions is few MHz instead
 511 of 40 MHz, but the number of particles comes out of each interaction is higher (the SPS is invested
 512 by a density of particles of $\sim 100\text{ cm}^{-2}$). The reconstruction of very complicated events with a large
 513 number of particle is a challenge, hence to segment and to minimize the amount of material, which
 514 may cause secondary interaction complicating further the event topology, is considered a viable

strategy. The detector employs the ALPIDE chip, developed by ALICE collaboration, fabricated in the 180 nm CMOS Imaging Sensor process of TowerJazz, whose design takes full advantage of process feature which allows full circuitry within the pixel matrix. Thanks to the reduction of the material budget, ITS2 obtained an amazing improvement both in the position measurement and in the momentum resolution, improving the efficiency of track reconstruction for particle with very low transverse momentum (by a factor 6 at $pT \sim 0.1$ GeV/c). Further advancements in CMOS MAPS technology are being aggressively pursued for the ALICE ITS3 vertex detector upgrades (foreseen around 2026-27), with the goals of further reducing the sensor thickness and improving the readout speed of the devices, while keeping power consumption at a minimum.

3.2 Other applications

Historically for imaging purpose the CCDs were the favoured device: they can be used as single photon counter or integrating and collecting the charge released by more impinging particles. The utilisation in the first case is similar to the tracking one, except that the requirements are less tight, so much that two noteworthy of microchips originally meant for detectors in particle physics at the LHC, and later employed in other fields are Medipix and Timepix. They are read-out chips developed by the Medipix Collaborations since early 1990s. For two decades, different Medipix generations have been produced, having a rough correlation with the feature size used: Medipix2 (1999) used 250 nm feature size CMOS while Medipix3 (2005) 130 nm. The aim of the fourth collaboration (2016), instead, is designing pixel read-out chips that prepared for **TSV processing and may be tiled on all four sides. DOVREI METTERE DUE RIGHE SU TSV OPPURE TAGLIARE.** For photons imaging other materials with higher atomic charge than silicon could be preferred, as a high photon absorption efficiency is needed: it was for this reason that Medipix2 was bump bonded to identically segmented sensors of both silicon and GaAs.

The applications in scientific imaging vary from astrophysics and medical imaging to more exotic domains as studies of protein dynamics, art authentication and dosimetry. The most important employment of Medipix is as X-ray single photon counting in industrial and medical radiography and in 3D computed tomography. Thanks to a New-Zealand company, the MARS Bioimaging detector has been fabricated, which is capable of resolving the photons energy and produce 3D coloured images. Besides tracking in HEP (I have already cited the use of Timepix3 is in the beam telescope of the LHCb VELO), an important use of Timepix is in dosimetry **Timepix Detector for Imaging in Ion Beam Radiotherapy- aggiungi qualche info** A small-Timepix detector with the dimension of a USB can also be found at the International Space Station, where it is exploited for radiation, principally made of heavy-ion, monitoring.

3.2.1 Applicability to FLASH radiotherapy

A possible new application of pixels detector is dosimetry or beam monitoring of charge particles in high intensity radiography. The radiological treatment is a common method used in 60% of tumors both as palliative care and as treatment. It can be given before, after or during a surgery, (Intra operative radiation therapy-IORT) and many different types of radiations (photons, electrons, protons and ions, which mainly are hydrogen and carbon) can be used to irradiate the affected tissues. Exploiting the ionizing energy loss, that can be parametrized by the Linear Energy Transfer (LET), a biological damage can be delivered to the tissue: while α and β particles are high LET radiations with values in $100\text{ keV}/\mu\text{m}$ to $200\text{ keV}/\mu\text{m}$, x-rays and gamma-rays are low LET radiations with values in range $0.2\text{ keV}/\mu\text{m}$ to $2\text{ keV}/\mu\text{m}$.

If x-ray photons, with energy in 4 MeV to 25 MeV are used, the ionization is caused by the Compton electrons and is more in the superficial layers of the tissue due to the exponential attenuation of the beam. The hadrons energy loss, instead, is strongly localized in the last region of the track, that is the Bragg peak. Ion beam enables better focusing of the radiation thereby improves the sparing of the surrounding healthy tissues; on the other hand the delivered dose distribution depends more on the patient's density tissues (e.g. bones, swelling, fat). **Ensuring the target**

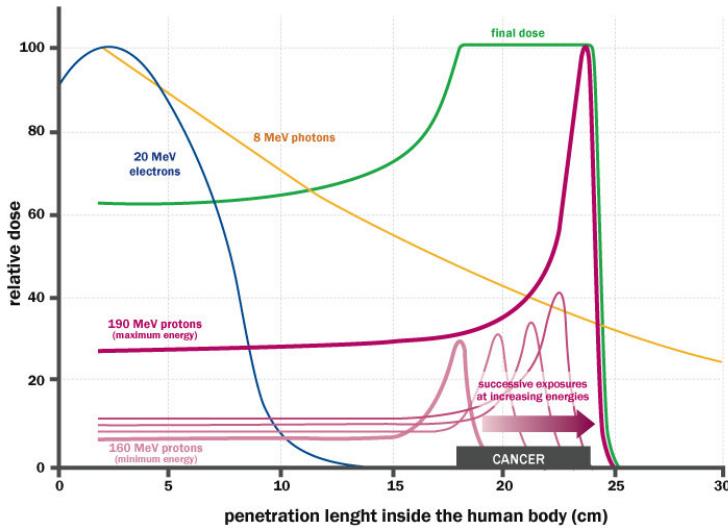


Figure 3.2: The Spread Out Bragg Peak (SOBP) curve (green), which is a constant dose distribution, is obtained from the superposition of many Bragg peak of hadrons with different energy.

	CONV-RT	FLASH-RT
Dose rate	0.03 Gy/s	40 Gy/s
Intra pulse dose rate	100 Gy/s	106 Gy/s
Treatment duration	~minutes	$\lesssim 500$ ms
DDP	0.3 mGy	1 Gy to 10 Gy
Pulse width	3 μ s	~ 2 μ s

Table 3.1: Typical value of treatment parameters

coverage is a fundamental objective in radiotherapy and is closely connected to the choice of the particles. Electrons cover the target since they tend to spread out and can cover a field size of a few cm² at a distance of a few cm from the source. Instead, the limited size of the beam for protons and photons from ultra high dose rate microbeam radiation therapy (MRT), for which FLASH effect was seen, requires the scanning of target. The radiobiological consequences of scanning both in spatial-fractionation and in prolonged exposure, which might not be sufficient to maintain a high mean dose rate to trigger FLASH effect, need to be explored. To date, the FLASH effect has been most commonly demonstrated using low-energy electron linacs

Recently² a promising method for RT at ultra high dose rate (at least 40 Gy/s) and for this reason called FLASH-RT[9], instead of CONV-RT (0.03 Gy/s), came out. This treatment takes advantages of biological differences between tumors and healthy tissues: it is characterized by reducing normal tissue toxicity and maintaining equivalent tumor damage. The response to dose can be described by the survival fraction probability, describing the fraction of surviving cell as a function of the dose:

$$S(D) = S(0) e^{-(\alpha D + \beta D^2)} \quad (3.1)$$

where α and β respectively represents the rate of cell killing by single ionizing events and by double hits. Hence, at high doses the density of damages increases and the cells repair becomes more difficult. Even if the FLASH effect is not yet completely understood and the underlying mechanisms are not clear, it looks like there are two different recipes which are involved:

²The first evidences has been observed on a mice experiments in 1966 and in 2014 by the group of Favaudon and Vozenin. After this, many test on cats and pigs have been performed, and also there has been a clinical trial on a cutaneous tumor-patient

582 • **The dose rate:** higher dose rate produce bigger damages (fig. 3.3(a)) since this prevent
583 cells from sparing.

584 • **The presence or absence of oxygen:** while hypoxic cells are very resistant to radiation,
585 normal oxygenated cells are highly radiosensitive. This is because if molecules containing O_2
586 break due to the impinging radiation, then the oxygen can build Reactive Oxygen Species
587 (ROS) (fig.3.3(b))

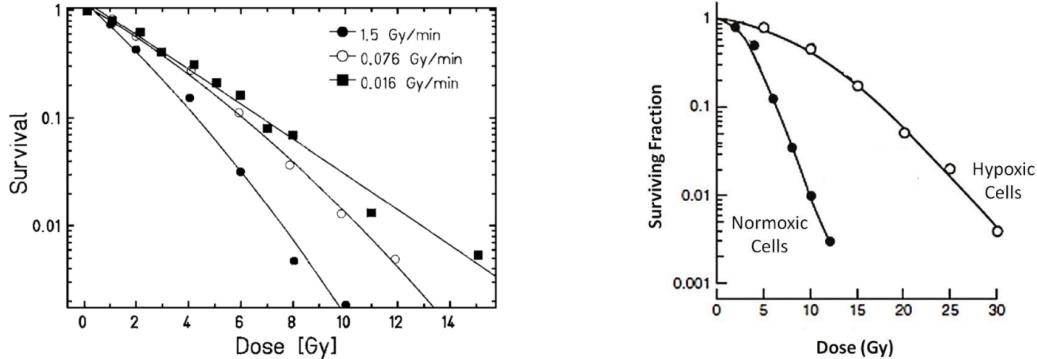


Figure 3.3: (a) Survival curve for different dose rate and (b) for different oxygen cell content

588 The Tumor Control Probability (TCP) and the Normal Tissue Complication (NTC) functions
589 parametrize respectively the efficiency of damaging on the tumor after having released a certain
590 dose and the probability of not affecting the healthy tissues. The intermediate zone between the
591 increase of the TC and of the NTC is called therapeutic window, and the wider it is and the more
592 effective the treatment is.

593 Dosimetric problems

594 Finding dosimeters suitable for online monitoring of the beam at ultra high dose rate is still an
595 open issue since almost all standard online dosimeters show saturation problems. Differently,
596 radiochromic films, which are the standard passive dosimeters, show dose-rate independence up to
597 109 Gy/s. **Cosa sono i radiochromic films and they do not have the same accuracy of other detectors.**
598 The principal detectors for reference dosimetry which provide real-time dose measurement are
599 Ionization Chambers (IC), that show saturation issue at dose per pulse (DDP) two orders of
600 magnitude lower than the ones used for FLASH-RT. **da qui in poi** ICs devono essere calibrate
601 secondo la metrologia , per cui grazie a protocolli di calibrazione e introducendo dei fattori correttivi
602 si riesce a fare una misura di dose. k_{sat} which accounts for the loss of charge collected due to
603 recombination. Doppi problemi sia di saturazione dovuta a ion recombination sia di scariche, must
604 be carefully accounted for: questo doppio effetto è dato dal fatto che, creandosi tante cariche nella
605 camera, che va ad annullare il campo elettrico di drift. Questo ovviamente paralizza le cariche che
606 non driftano più, ma che anzi si ricombinano ed inoltre facilita la formazione di scariche. Per DDP
607 minori di 1 mGy il fattore correttivo è minore al 5%, poi però aumenta substantially.

608 Scintillators have reusable, non-exhaustible scintillation centers. However, the system has a
609 total deadtime given by both the crystal scintillation time and the electronics read-out deadtime.

610 Semiconductors show a nonreversible saturation beyond a threshold around 15 cGy/p. The
611 scintillator used, shows a negligible saturation up to 1 Gy/p, but it increases significantly up to at
612 least 11 Gy/p, and it reaches a cutoff value between 11 and 36 Gy/p.

613 Scintillator dosimeters are widely used in radiotherapy. They are usually operating in counting-
614 mode where each detected signal is processed by read-out electronics. However, the system has a
615 total deadtime given by both the crystal scintillation time and the electronics read-out deadtime.
616 When a scintillator dosimeter is used in integrator-mode the signal is integrated over the entire
617 irradiation time. A deadtime, due to the decay time of the scintillating material, is considered on
618 average every N recorded pulses, where N is the number of scintillation centres in the dosimeter.

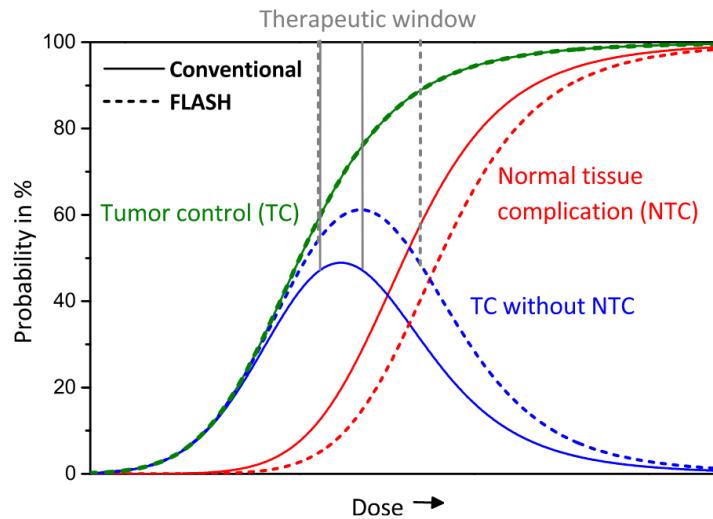


Figure 3.4: Illustration of dependence of TCP, NTCP and therapeutic window on dose, for CONV-RT ad FLASH-RT.

619 Besides saturation two other requirements for online dosimeters are high temporal and space res-
 620 olutions. Si potrebbe pensare di poter usare i pixel detector as beam monitor che hanno risoluzioni
 621 spaziali anche inferiori al 10 um e ris temporali -qua dare un valore è più difficile perchè per i
 622 maps la risoluzione temporale dipende da l occupancy. Uno dei problemi è però il lungo dead time
 623 introdotto dal lungo tempo di readout (ricorrdiamo che sopportano circa 100 Mhz/cm²).

624

Chapter 4

625

TJ-Monopix1

626 TJ-Monopix1 is a small electrode DMAPS with fast R/O capability, fabricated by TowerJazz
 627 foundry in 180 nm CMOS imaging process. It is part, together with prototypes from other series
 628 such as TJ-MALTA, of the ongoing R&D efforts aimed at developing DMAPS in commercial CMOS
 629 processes, that could cope with the requirements at accelerator experiments. Both TJ-Monopix
 630 and TJ-MALTA series [10], produced with the same technology by TowerJazz (the timeline of the
 631 foundry products is shown in figure 4.1), are small electrode demonstrators and principally differ in
 632 the readout design: while Monopix implements a column-drain R/O, an asynchronous R/O without
 633 any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.



Figure 4.1: Timeline in TowerJazz productions in 180 nm CMOS imaging process

634 Another Monopix series, but in 150 nm CMOS technology, has been produced by LFoundry [11].
 635 The main differences between the LF-Monopix1 and the TJ-Monopix1 (summarized in table 4.2),
 636 lay in the sensor rather than in the readout architecture, as both chips implement a fast column
 637 drain R/O with ToT capability [12][13]. Concerning the sensors, either are based on a p-type
 638 substrate, but with slightly different resistivities; in addition LFoundry pixels are larger, thicker
 639 and have a large fill factor (the very deep n-well covers ~55% of the pixel area). The primary
 640 consequence is that LF-Monopix1 pixels have a higher capacity resulting in higher consumption
 641 and noise. As I discussed in section 2.4.1, the fact that LF-Monopix has a large fill factor electrode
 642 is expected to improve its radiation hardness. Indeed, a comparison of the performance of the
 643 two chips showed that TJ-Monopix suffers a comparatively larger degradation of efficiency after
 644 irradiation, due to the low electric field in the pixel corner; on the other hand, a drawback of the
 645 large fill factor in LF-Monopix is a significant cross-talk.

646 The TJ-Monopix1 chip contains, apart from the pixels matrix, all the required support blocks
 647 used for configuration and testing:

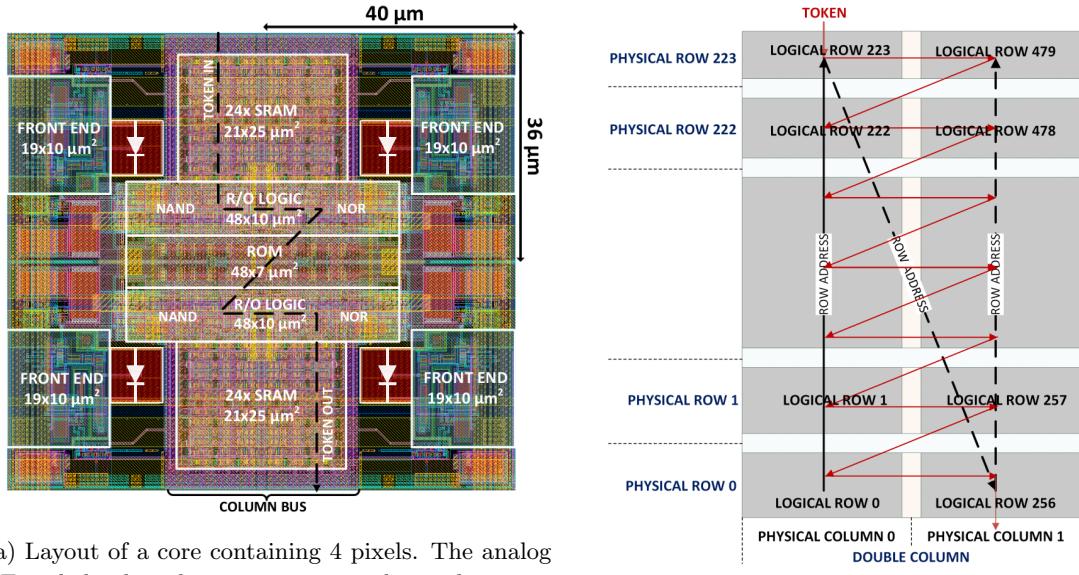
- 648 • the whole matrix contains 224×448 pixels, yielding a total active area approximately equal
 649 to 145 mm^2 over a total area of $1 \times 2 \text{ cm}^2$;

	LF-Monopix1	TJ-Monopix1
Resistivity	$>2 \text{ k}\Omega\text{cm}$	$>1 \text{ k}\Omega\text{cm}$
Pixel size	$50 \times 250 \mu\text{m}^2$	$36 \times 40 \mu\text{m}^2$
Depth	$100\text{-}750 \mu\text{m}$	$25 \mu\text{m}$
Capacity	$\sim 400 \text{ fF}$	$\sim 3 \text{ fF}$
Preamplifier	charge	voltage
Threshold trimming	on pixel (4-bit DAC)	global threshold
ToT	8 bits	6 bits
Consumption	$\sim 300 \text{ mW/cm}^2$	$\sim 120 \text{ mW/cm}^2$
Threshold	$1500 e^-$	$\sim 270 e^-$
ENC	$100 e^-$	$\sim 30 e^-$

Table 4.1: Main characteristics of Monopix1 produced by TowerJazz and LFoundry [12][13]

- at the chip periphery are placed some 7-bit Digital to Analog Converter (DAC), used to generate the analog bias voltage and current levels and to configuire the FE;
- at the EoC is placed a serializer to transferred datas immediately, indeed no trigger memory is implemented in this prototypes;
- the matrix power pads are distributed at the sides
- four pixels which have analog output and which can be monitored with an oscilloscope, and therefore used for testing

Pixels are grouped in 2×2 cores (fig. 4.2a): this layout allows to separate the analog and the digital electronics area in order to reduce the possible interference between the two parts. In addition it semplifies the routing of data as pixels on double column share the same column-bus to EoC. Therefore pixels can be addressed through the physical column/row or through the logical column/row, as shown in fig. 4.2b: in figure is also highlighted the token propagation path, whose I will discuss later.



(a) Layout of a core containing 4 pixels. The analog FE and the digital part are separated in order to reduce cross-talk be

(b)

Parameter	Value
Matrix size	$1 \times 2 \text{ cm}^2$
Pixel size	$36 \times 40 \mu\text{m}^2$
Depth	$25 \mu\text{m}$
Electrode size	$2 \mu\text{m}$
BCID	40 MHz
ToT-bit	6
Power consumption	$\sim 120 \text{ mW/cm}^2$

Table 4.2

663 4.1 The sensor

664 As already anticipated, TJ-Monopix1 has a p-type epitaxial layer and a n doped small collection
 665 electrode ($2 \mu\text{m}$ in diameter); to avoid the n-wells housing the PMOS transistors competing for the
 666 charge collection, a deep p-well substrate, common to all the pixel FE area, is used. TJ-Monopix1
 667 adopts the modification described in section 2.4.2 that allows to achieve a planar depletion region
 668 near the electrode applying a relatively small reverse bias voltage. This modification improves the
 669 efficiency of the detector, especially after irradiation, however a simulation of the electric field in
 670 the sensor, made with the software TCAD (Technology Computer Aided Design), shows that a
 671 nonuniform field is still produced in the lateral regions of the pixel compromising the efficiency
 672 at the corner. Two variations to the process have been proposed in order to further enhance the
 673 transversal component of electric field at the pixel borders: on a sample of chip, which includes the
 674 one in Pisa, a portion of low dose implant has been removed, creating a step discontinuity in the
 675 deep p-well corner (fig. 4.3); the second solution proposed[MOUSTAKAS THESYS, PAG 58]
 676 consists in adding an extra deep p-well near the pixel edge. A side effect of the alteration in the
 677 low dose implant is that the separation between the deep p-well and the p-substrate becomes weak
 678 to the point that they cannot be biased separately to prevent the punchthrough.

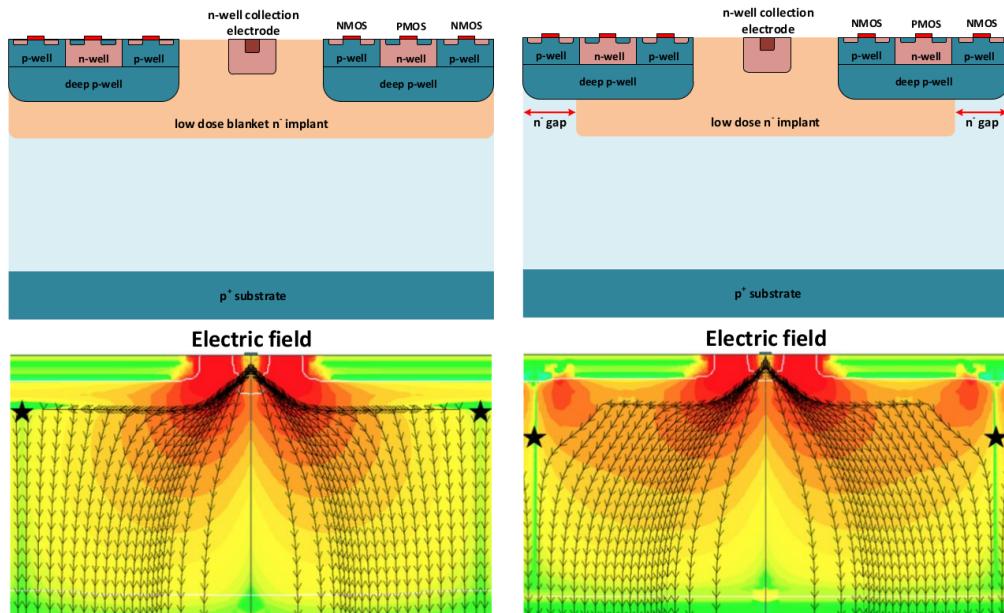


Figure 4.3: (a) The cross-section of a monolithic pixel in the TJ-Monopix with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field. this point in figure is indicated by a star . transversal component of the electric field drops at the pixel corner

679 Moreover, to investigate the charge collection properties, pixels within the matrix are split
 680 between bottom top half and bottom half and feature a variation in the coverage of the deep
 681 p-well: the electronics area can be fully covered or not. In particular the pixels belonging to rows
 682 from 0 to 111 are fully covered (FDPW) and pixels belonging to rows from 112 to 223 have a
 683 reduced p-well (RDPW), resulting in a enhancement of the lateral component of the electric field.

684 4.2 Front end

685 The matrix is split in four sections, each one corresponding to a different flavor of the FE. The
 686 four variation have been implemented in order to test the data-bus readout circuits and the input
 687 reset modes.

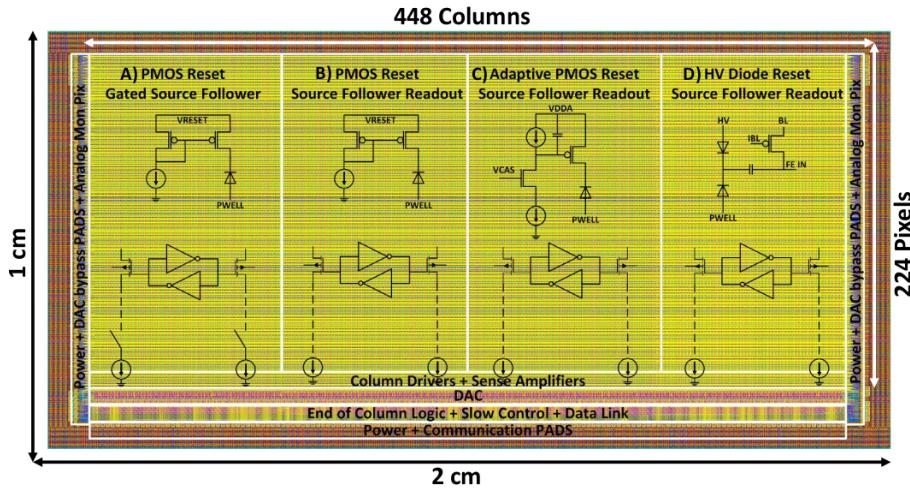


Figure 4.4

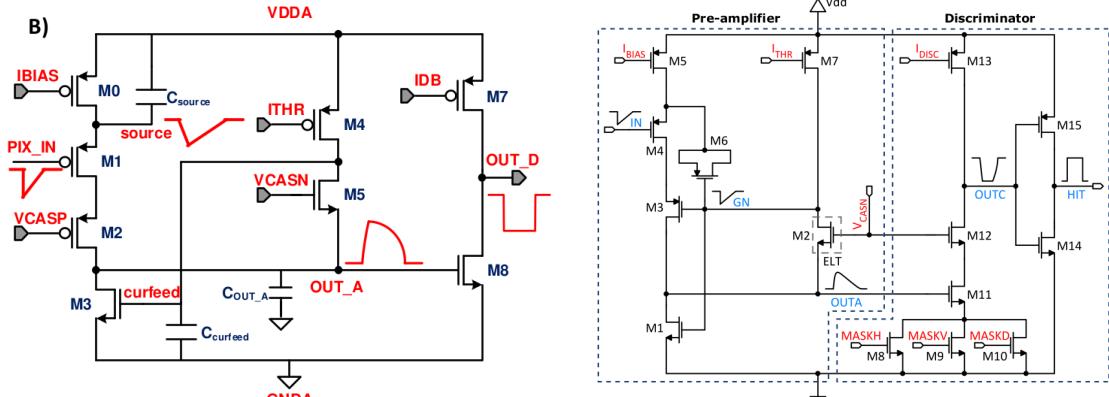
687 All the flavors implement a source-follower double-column bus readout: the standard variation
 688 is the flavor B, that features a PMOS input reset (referred as "PMOS reset"). Flavor A is identical
 689 to flavor B except for the realization of the source follower (it is a gated one) that aim to reduce
 690 the power consumption.cosa significa? C instead implements a novel leakage compensation circuit.
 691 Moreover the collection electrode in flavors A, B, C is DC-coupled to the front-end input, while
 692 in D is AC-coupled, providing to apply a high bias voltage; for this reason flavor D is called "HV
 693 flavor".

694 Principio generale: R resistenza di reset deve essere abbastanza grande in modo da far sì che
 695 il ritorno allo zero è abbastanza lento (non devi "interferire" con la tot slope e non deve essere
 696 più corto del tempo del preamplificatore, sennò hai perdita di segnale). Baseline reset: all'input
 697 solitamente hai un PMOSS o un diodo; R reset

698 4.2.1 ALPIDE-like

700 ALPIDE chips, developed by the ALICE collaboration, implemented a standard FE to the point
 701 that many CMOS MAPS detectors used a similar FE and are called "ALPIDE-like". Considering
 702 that both TJ-Monopix1 and ARCADIA-MD1 have an ALPIDE-like FE, I am going to explain the
 703 broad principles of the early FE stage. The general idea is of the amplification to transfer the
 704 charge from a bigger capacity[14], C_{source} , to a smaller one, C_{out} : the input transistor M1 with
 705 current source IBIAS acts as a source follower and this forces the source of M1 to be equal to the
 706 gate input $\Delta V_{PIX_IN} = Q_{IN}/C_{IN}$.

$$Q_{source} = C_{source} \Delta V_{PIX_IN} \quad (4.1)$$



(a) ALPIDE-like

(b)

707 The current in M2 and the charge accumulates on C_{out} is fixed by the one on C_{source} :

$$\Delta V_{OUT_A} = \frac{Q_{source}}{C_{OUT_A}} = \frac{C_{source} \Delta V_{PIX_IN}}{C_{OUT_A}} = \frac{C_{Source}}{C_{OUT_A}} \frac{Q_{IN}}{C_{IN}} \quad (4.2)$$

708 A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR
709 set the baseline value of the signal on C_{OUT_A} and the velocity to goes down to the baseline.

710 IL RUOLO DI CURVFEED NON L'HO CAPITO.

711 Finally IDB defines the charge threshold with which the signal OUT_A must be compared: de-
712 pending on if the signal is higher than the threshold or not, the OUT_D is high or low respectively.

713 The actual circuit implemented in TJ-Monopix1 is shown in figure 4.5b: the principal difference
714 lays in the addition of disableing pixels' readout. This possibility is uttermost important in order to
715 reduce the hit rate and to avoid saturating the bandwidth due to the noisy pixels, which typically
716 are those with manufacturing defects. In the circuit transistors M8, M9 and M10 have the function
717 of disabling registers with coordinates MASKH, MASKV and MASKD (respectively vertical, ori-
718 zontal and diagonal) from readout: if all three transistors-signals are low, the pixel's discriminator
719 is disabled. Compared with a configurable masking register which would allow disableing pixels
720 individually, to use a triple redundancy reduces the sensistivity to SEU but also gives amount of
721 intentionally masked ("ghost") pixels. This approach is suitable only for extremely small number
722 N of pixel has to be masked: if two coordinate projection scheme had been implemented, the
723 number of ghost pixels would have scale with N^2 , if instead three coordinates are used, the N's
exponential is lower than 2 (fig. 4.6)

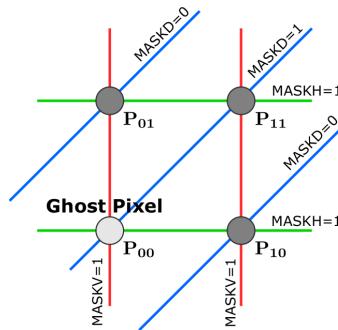


Figure 4.6

724

Parameter	Meaning	
IBIAS	mainly controls the rise time	yes? check
IDB	sets the discriminator threshold	yes
ITHR	sets the velocity of the return to the baseline	yes
ICASN	sets the baseline of the signal	yes
VRESET	sets the gain of the preamplifier	yes
IRESET	sets the gain of the preamplifier	no

Table 4.3: FE parameters which must be setted through the DAQ. "Function" means that higher parameter implies higher value

725 4.3 Readout logic

726 TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain
 727 architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit
 728 LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address.
 729 Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is
 730 already storing a previous one, the new data get lost. After being read, the data packet is sent to
 731 the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (4.7). There
 732 a FIFO is used to temporarily stored the data, which is transmitted to a computer through an
 733 ethernet cable in a later time.

734 The access to the pixels' memory and the transmission of the data to the EoC, following
 735 a priority chain, is managed by control signals and is based on a Finite State Machine (FSM)
 736 composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and data transfer (DTA).
 737 The readout sequence (??) starts with the TE of a pulse: the pixel immediately tries to grab the
 738 column-bus turning up a hit flag signal called *token*. The token is used to control the priority chain
 739 and propagates across the column indicating what pixel that must be read. To start the readout
 740 and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal is activated, and
 741 then a *read* signal controls the readout and the access to memory. During the freeze, the state of
 742 the token for all pixels on the matrix remains settled: this does not forbid new hits on other pixels
 743 from being recorded, but forbids pixels hit from turning on the token until the freeze is ended. The
 744 freeze stays on until the token covers the whole priority chain and gets the EoC: during that time
 745 new token cannot be turned on, and all hits arrived during a freeze will turn on their token at the
 746 end of the previous freeze. Since the start of the token is used to assign a timestamp to the hit,
 747 the token time has a direct impact on the time resolution measurement; this could be a problem
 748 coping with high hits rate.

749 The analog FE circuit and the pixel control logic are connected by an edge detector which is
 750 used to determine the LE and the TE of the hit pulse(fig. 4.9): when the TE is stored in the first
 751 latch the edge detector is disabled and, if the **FREEZE** signal is not set yet, the readout starts. At
 752 this point the HIT flag is set in a second latch and a token signal is produced and depending on
 753 the value of **Token in** the pixel can be read or must wait until the **Token in** is off. In figure an OR
 754 is used to manage the token propagation, but since a native OR logic port cannot be implemented
 755 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly
 756 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token
 757 and to speed up the circuit optimized solution are often implemented. When the pixel become the
 758 next to be read in the queue, and at the rising edge of the **READ** signal, the state of the pixel is
 759 stored in a D-latch and the pixel is allowed to use the data bus; the TE and the HIT flag latches
 760 are reset and a **READINT** signal that enable access of the RAM and ROM cells is produced.

761
 762 The final data must provide all the hits' information: the pixel address, the ToT and the
 763 timestamp. All those parts are assigned and appended at different time during the R/O chain:

- 764 • **Pixel address:** while the double column address (6-bit) is appended by the EoC circuit,

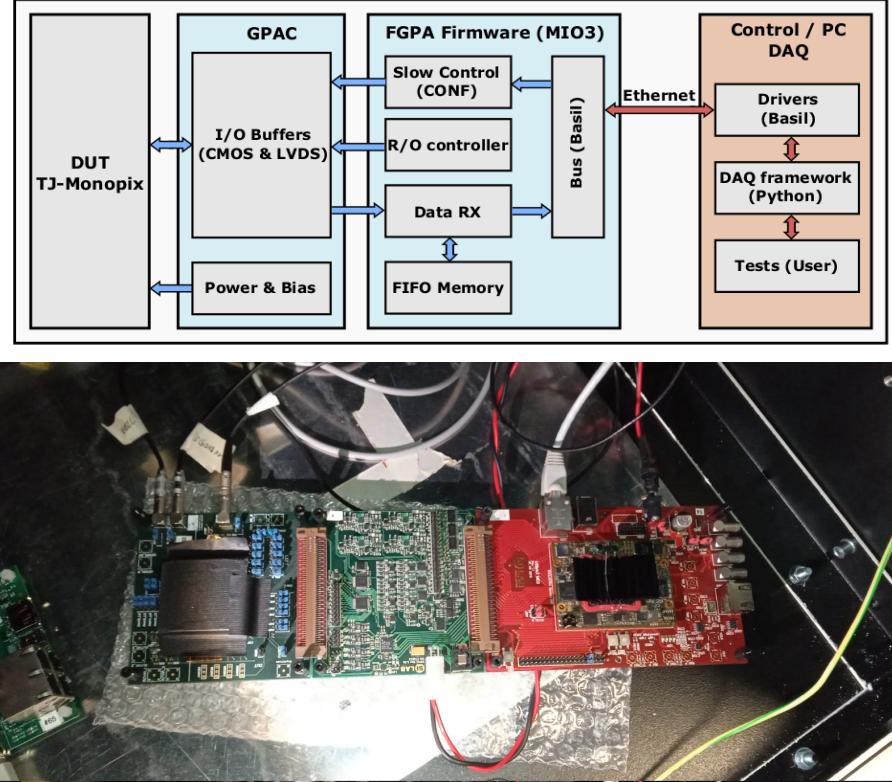


Figure 4.7: Main caption

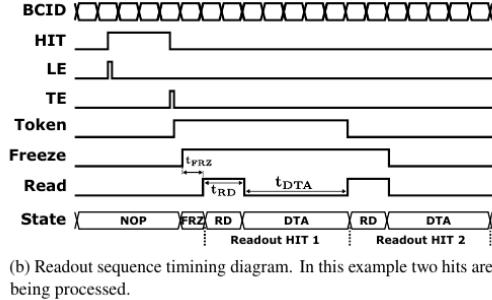


Figure 4.8: Readout timing diagram: in this example two hits are being processed

the row address (8-bits for each flavor) and the physical column in the doublet (1-bit) are assigned by the in-pixel logic

- **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge detector in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is range 0-64 clock cycle which corresponds to 0-1.6 μ s
- **Timestamp:** The timestamp of the hit correspond to the time when the pixel set up the token; it is assigned by the FPGA, that uses the LE, TE and a 640 MHz clock to derive it. For all those hits which arrived while the matrix is frozen, the timestamp is no more correlated with the time of arrival of the particle

When the bits are joined up together the complete hit data packet is 27-bit.

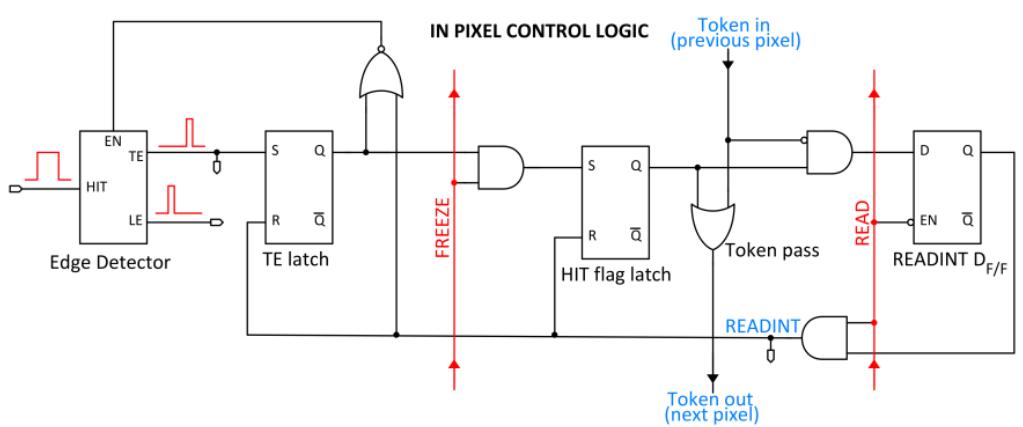


Figure 4.9

775

Chapter 5

776

Arcadia-MD1

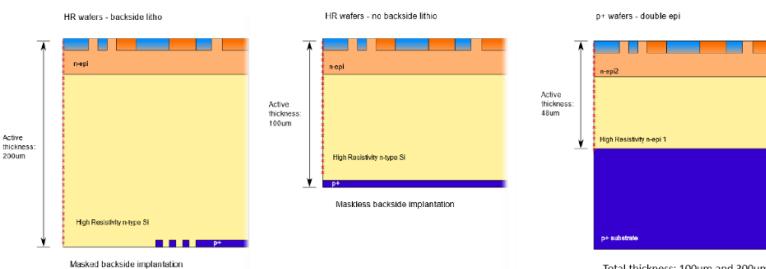
777 [15] [16]

778 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED
779 Matisse a Md1 e Md2

780

5.1 The sensor

781 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node
782 with six metal layer ??. The standard p-type substrate was replaced with an n-type floating zone
783 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).



784 Figure 5.1

785 Wafer thinning and backside lithography were necessary to introduce a junction at the bottom
786 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.
787 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthrough
788 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

789 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,
790 COME VENGONO FATI I MAPS COME FAI LE GIUNZIONI

791 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.

792 It is operated in full depletion with fast charge collection by drift.

793 Prima SEED si occupa di studiare le prestazioni: concept study with small-scale test struc-
794 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo
795 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il
796 pwell e quanto al diodo. ..

797 5.2 Readout logic and data structure

798 5.2.1 Matrix division and data-packets

799 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided
800 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in
801 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei
serializzaatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

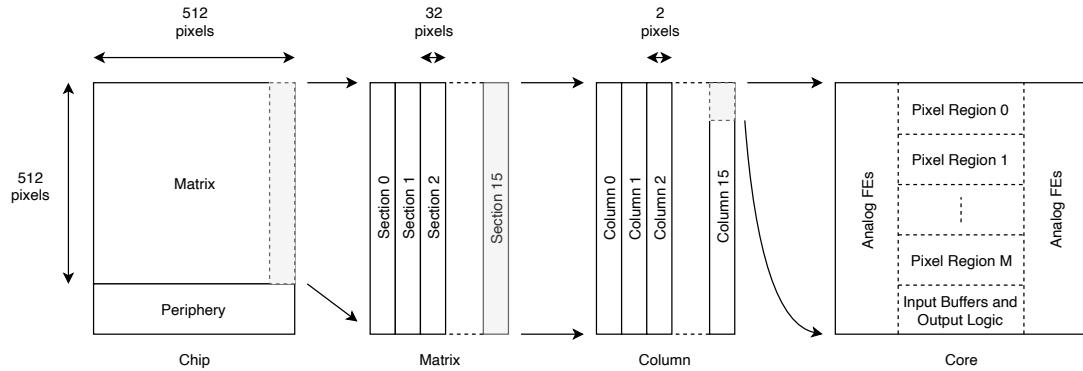


Figure 5.2

802

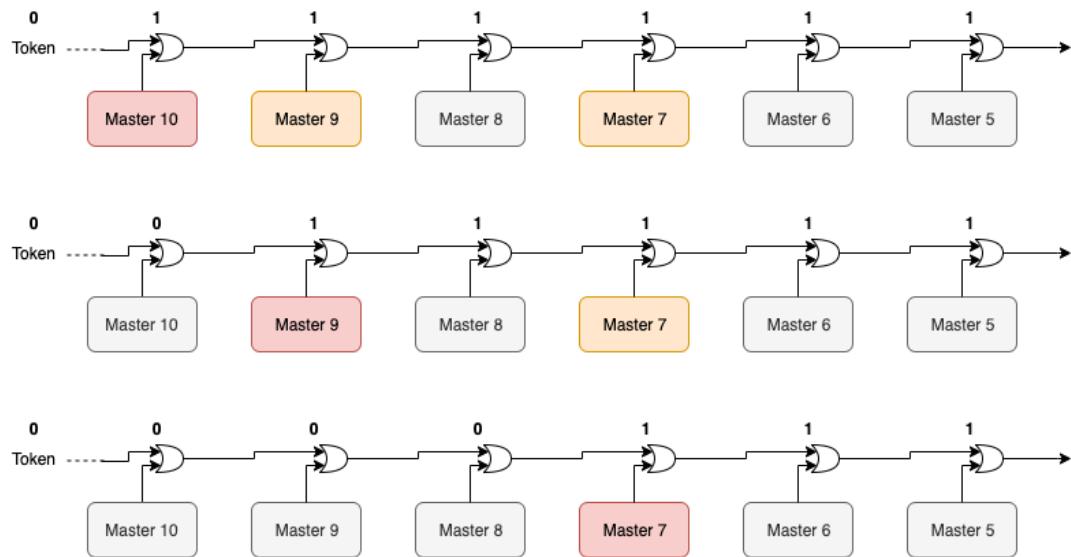


Figure 5.3

803 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le
804 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,
805 e devi accennare al timestamp

806 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively
807 large core allows one to take full advantage of digital synthesis tools to implement complex func-
808 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della
809 review.

810

811 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column
812 (512x2) Core (32x2) Region (4x2)

813 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

814 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for
815 example 8b10b encoding n =5"

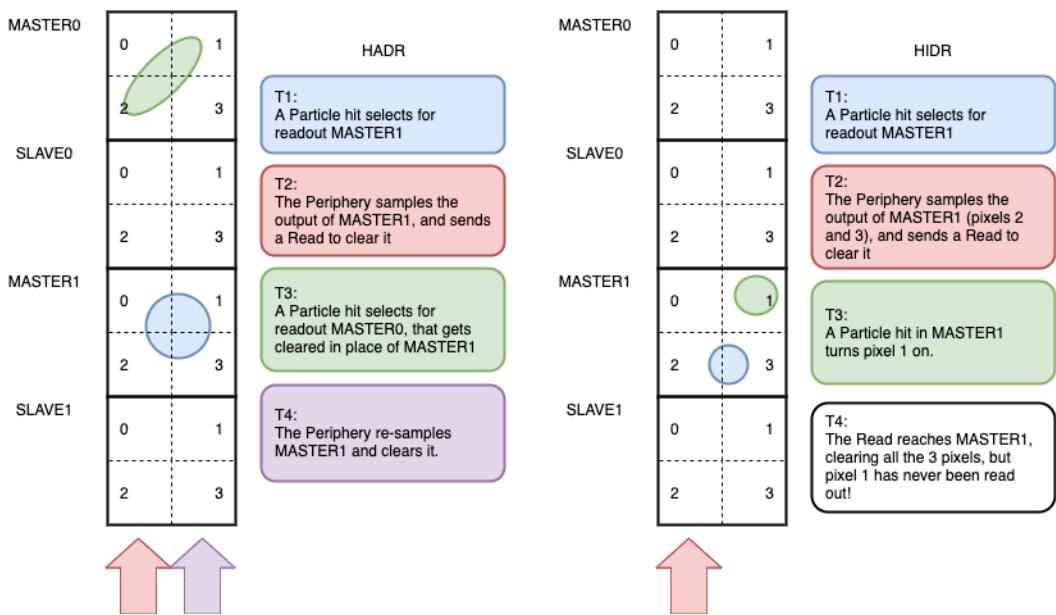


Figure 5.4

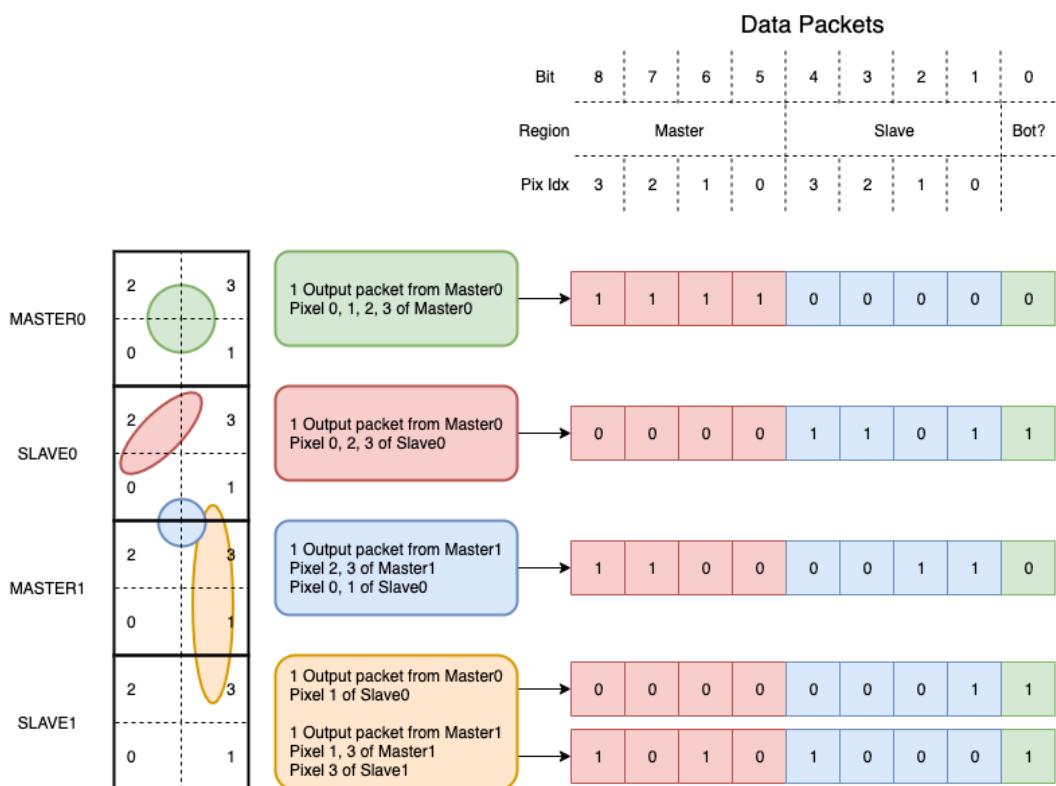


Figure 5.5

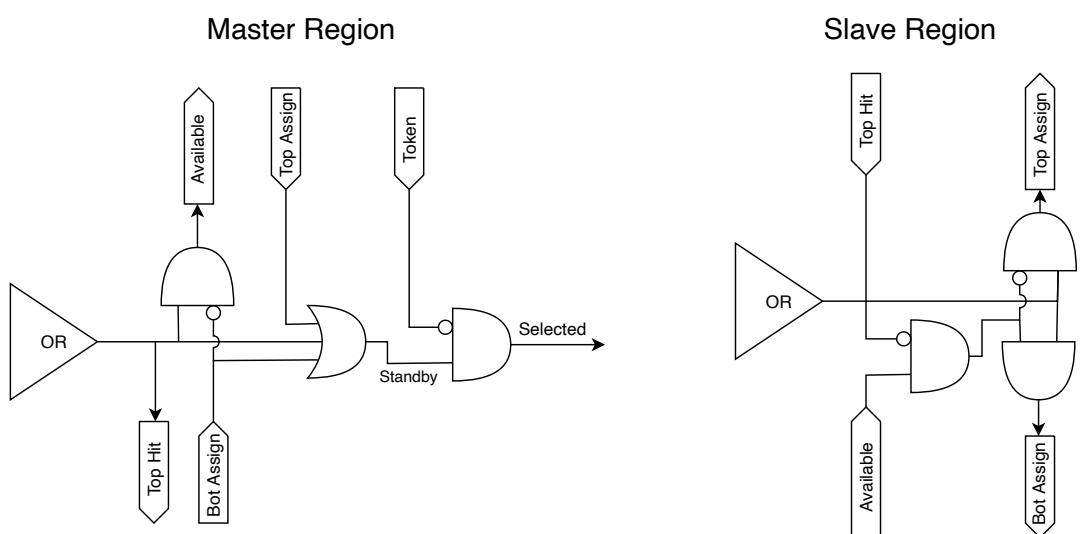


Figure 5.6

816 **Chapter 6**

817 **Threshold and noise
characterization**

819 **6.1 TJ-Monopix1 characterization**

820 **6.1.1 Threshold and noise: figure of merit for pixel detectors**

821 Una caratterizzazione di soglia e rumore è necessaria in quanto questi valori condizionano sia le
822 condizioni di operatività di questi chip, che le performance. Infact, the signal to threshold ratio
823 may be considered as the figure of merit for pixel detectors rather than the signal to noise ratio.
824 The threshold has to be low enough to mantain a high signal efficiency, but also high enough to
825 cut the noise: for a low threshold many pixels can fire at the same time and a positive feedback
826 can set off a chain reaction eventually, causing all the other pixels to fire. Thus, the noise sets a
827 lower bound to the threshold: if an occupancy $\leq 10^{-4}$ is required, for example, this correspond
828 to the Gaussian 1-sided tail fraction for 3.7σ . In this case, if the noise is 100e^- , for example, the
829 threshold must be higher than $3.7 \times 100\text{e}^-$. Typically this argument sets only a minimal bound to
830 the threshold since the variation with time and from pixel to pixel have to be taken into account:
831 the temperature, the annealing (for example, the radiation damages in the oxide layer causes shift of
832 MOSFET threshold voltage) and the process parameters variation across the wafer (as for example
833 process mismatch between transistors). A requirement for the FE noise (the ENC is the equivalent
834 input charge noise) is:

$$ENC < \sqrt{(T/3.7)^2 - T_{RMS}^2(x) - T_{RMS}^2(t)} \quad (6.1)$$

835 where the T is the threshold set, T_{RMS} is the threshold variation during time (t) and across the
836 matrix (x).

837 For this reason is desiderable the possibility of changing and adapting the setting parameters of
838 the FE, both in time and in space: this parameters are usually set by Digital to Analog Converter
839 (DAC) with a number of bit in a typical range of 3-7.

840 DAC elements require a lot of space that may be not enough on the pixel area. Therefore,
841 the FE parameters are typically global, which means that they are assigned for the whole chip,
842 or they can be assigned for regions the matrix is divided into. The former case corresponds to
843 TJ-Monopix1's design in which 7 bits are used for a total 127-DAC possible values, while the latter
844 corresponds to the ARCADIA-MD1's one, [where quanti bit??](#). An other possibility, for example
845 implemented in TJ-Monopix2, is allocate the space on each pixel for a subset of bits, then combinig
846 the global threshold with a fine tuning.

847 To measure the threshold and noise of pixels a possible way is a scan with different known
848 injected charge at a fixed threshold, that corresponds to the value where the efficiency of the
849 signal exceeds the 50%. Therefore, for a fixed threshold (I set IDB = 40 DAC to perform the
850 scan) I have used the injection circuit available on the chip to inject 100 pulses for each input
851 charge. The injection comes on a capacity at the input of the FE circuit, whose mean value is

852 230 aF (in section ?? I'll present the calibration of the signal from which I also found the value of
 853 this capacity across the matrix). For the PMOS flavors: since the DAC are biased at 1.8 V, the
 854 Least significant Bit (LSB) corresponds to a voltage of 14.7 mV from which the charge for LSB
 855 $1.43 \text{ e-}/\text{mV}$ and the conversion factor from DAC to electrons $20.3 \text{ e-}/\text{DAC}$ are obtained. While
 856 this value is equivalent for all the PMOS flavor, the HV flavor is expected to have a different
 857 conversion factor, $\sim 33 \text{ e-}/\text{DAC}$, because of the different input capacity.

858 Besides the charge, also the duration and the period of the injection pulse can be set; it is
 859 important to make the duration short enough to have the falling edge during the dead time of
 860 the pixel (in particular during the FREEZE signal) in order to avoid the afterpulse, coming at
 861 high input charge, triggering the readout and reading spurious hits. **Questo problema è legato
 862 solamente all'impulso di iniezione di carica e non si ha invece con acquisizioni con sorgenti, come
 863 abbiamo verificato, e anche perchè. Immagine afterpulse oscilloscopio?**

864 Assuming a gaussian noise, it can be described through the error function; actually, since the
 865 error function has y bounded between -1 and +1, the function I need is a modification of the *erf*:

$$f(x, \mu, \sigma) = \frac{1}{2} \left(1 + \operatorname{erf} \left(\frac{x - \mu}{\sigma \sqrt{2}} \right) \right) \quad (6.2)$$

$$\operatorname{erf}(z) = \frac{2}{\sqrt{\pi}} e^{-z^2} dx \quad (6.3)$$

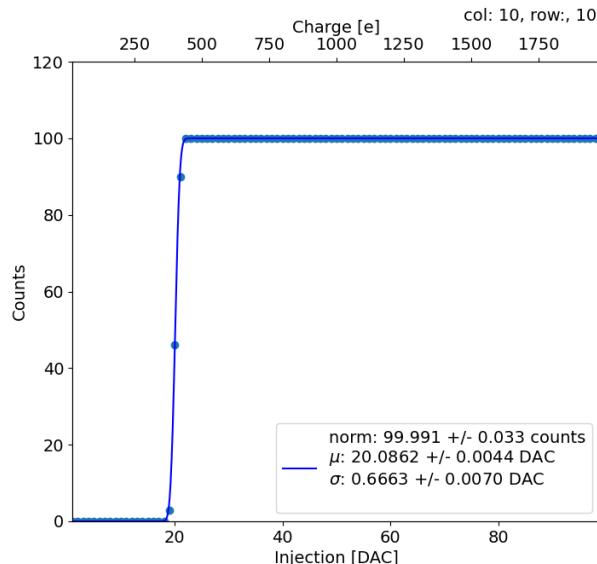


Figure 6.1: S curve for pixel (10, 10) of the PMOS flavor. The conversion of charge injected from DAC to electrons has been done assuming a conversion factor of $20 \text{ e-}/\text{DAC}$.

867 The mean minimum stable threshold modified through different generation of chips: in the 1st
 868 generation it was around 2500 e- while in the 3rd (corresponding to nowadays chips) is less than
 869 500 e- . This allows in thinner sensors with smaller expected: from 16000 e- produced in $200 \mu\text{m}$,
 870 down to 2000 e- produced in $25 \mu\text{m}$. According with this ??, the threshold of TJ-Monopix1 is
 871 around 500 e- . **I successivi prototipi hanno una soglia e un rumore più bassi, ad esempio TJ-
 872 Monopix2 ha una soglia e un rumore...**

873 La dispersione della soglia dopo al tuning e dovuta al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.4)$$

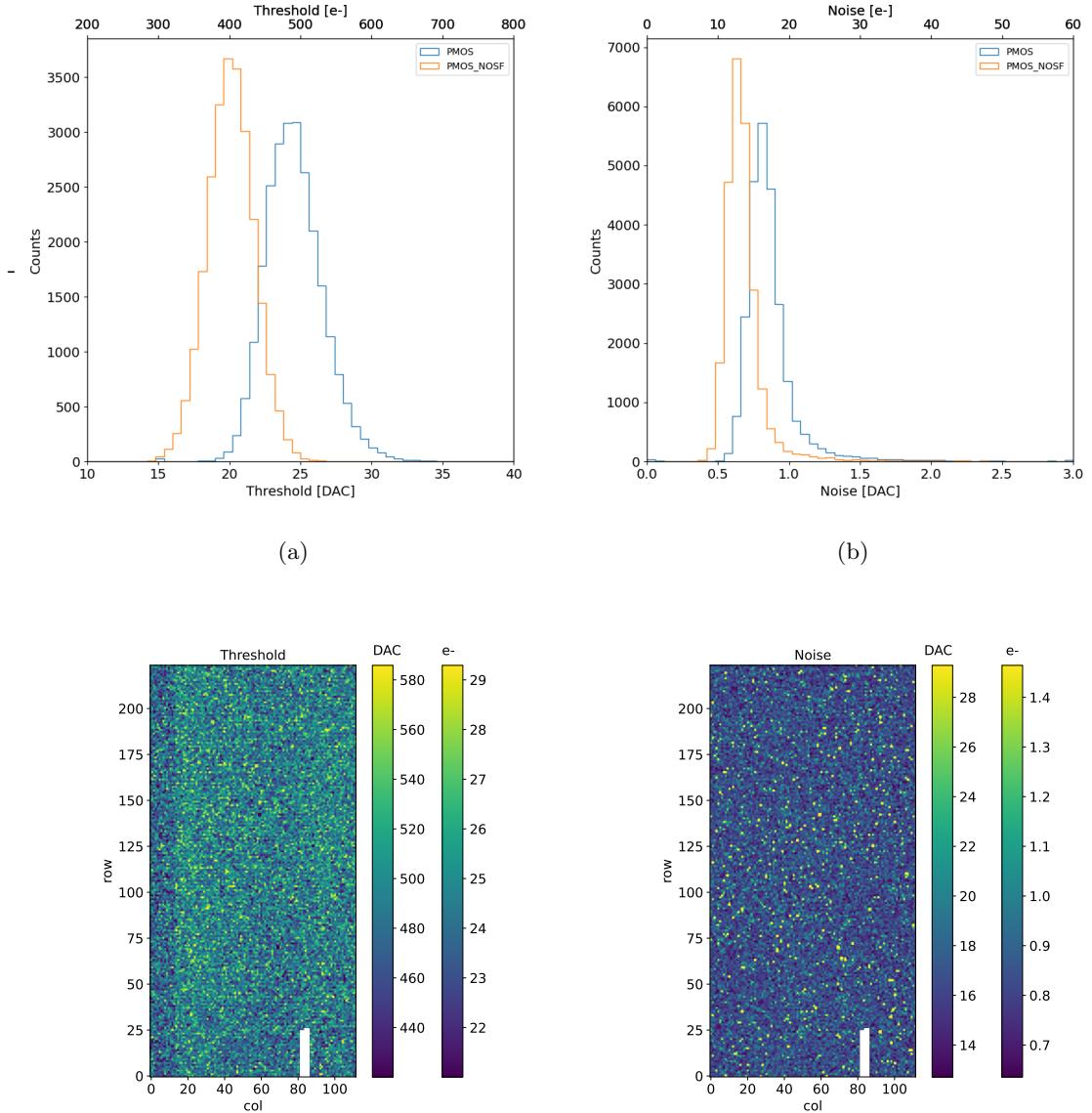


Figure 6.3

874 6.1.2 Calibration of the ToT

875 Absolute calibration

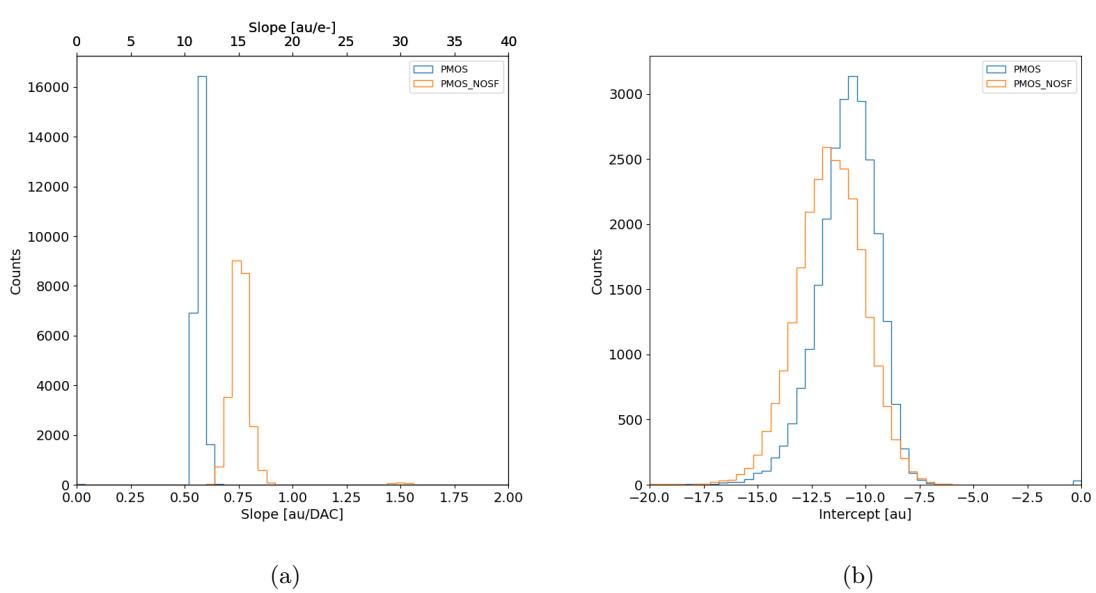
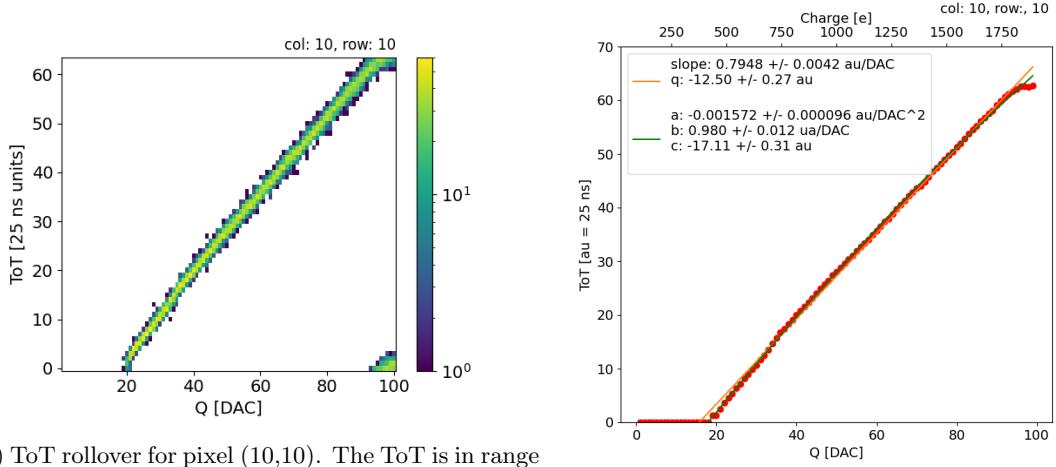
$$f(x, m, q, N, \mu, \sigma) = m x + q + \frac{N}{\sigma \sqrt{2\pi}} e^{-\frac{1}{2} \left(\frac{(x-\mu)}{\sigma} \right)^2} \quad (6.5)$$

876 6.1.3 Fe vs bias

- 877 • rate vs bias
- 878 • posizione del picco del ferro vs bias
- 879 • eventi sotto il picco vs eventi nella coda

	DAC units	electrons
Threshold	24.529 ± 0.049 u: 24.433 ± 0.049 d: 24.623 ± 0.051	
Threshold dispersion	1.848 ± 0.033 u: 1.867 ± 0.034 d: 1.825 ± 0.035	
Noise	0.8222 ± 0.0043 u: 0.8225 ± 0.0045 d: 0.8221 ± 0.0043	
Noise dispersion	0.0975 ± 0.0030 u: 0.0968 ± 0.0031 d: 0.0970 ± 0.0030	

Table 6.1: Flavor PMOS



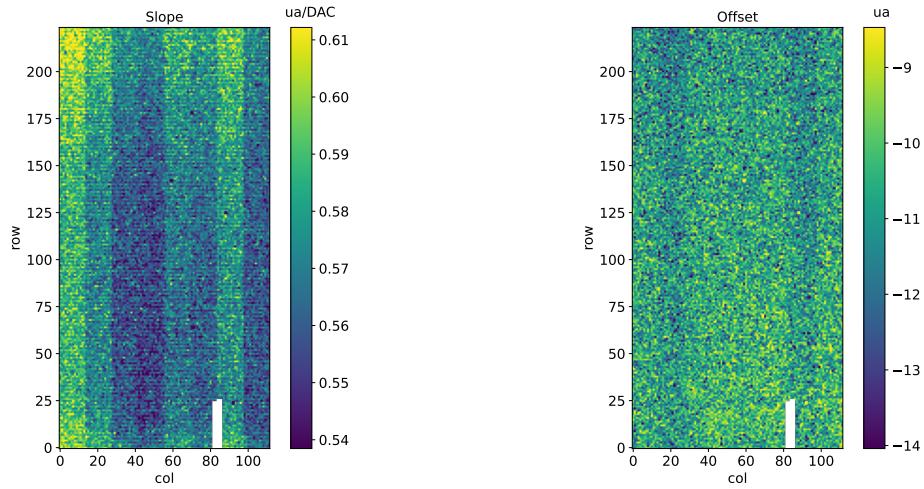


Figure 6.6

	PMOS	HV
Slope [au/DAC]	0.57145 ± 0.00025	
Slope dispersion [au/DAC]	0.01685 ± 0.00016	
Intercept [au]	-10.824 ± 0.019	
Intercept dispersion [au]	1.225 ± 0.013	

Table 6.2

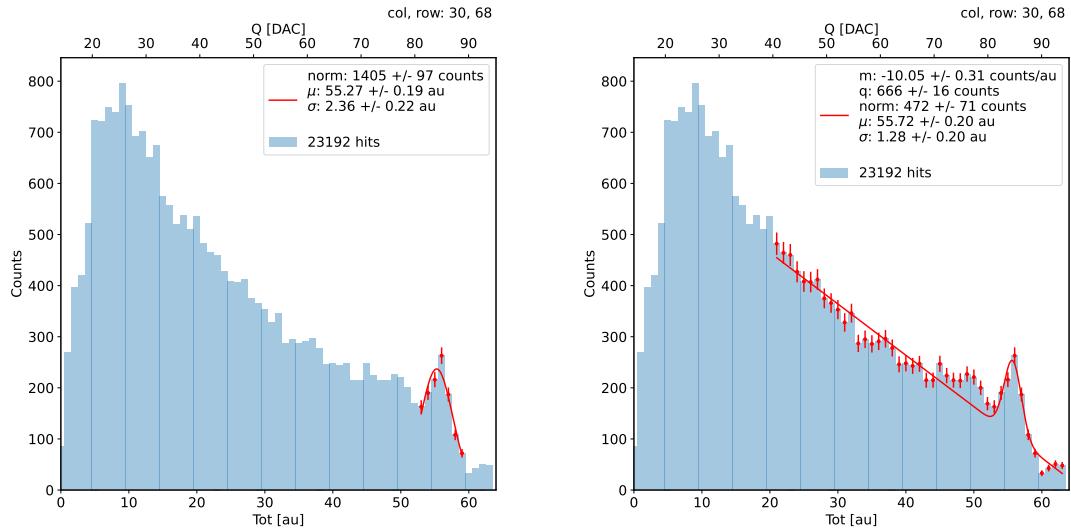


Figure 6.7: due pixel per far vedere la differenza tra i fit

6.1.4 Measurements with radioactive sources

CI metterei i plot con ferro, stronzio e cosmici ToT con doppia scala (calibrata in elettroni e non in ToT) hit per cluster dimensione cluster hit map di un paio di tracce?

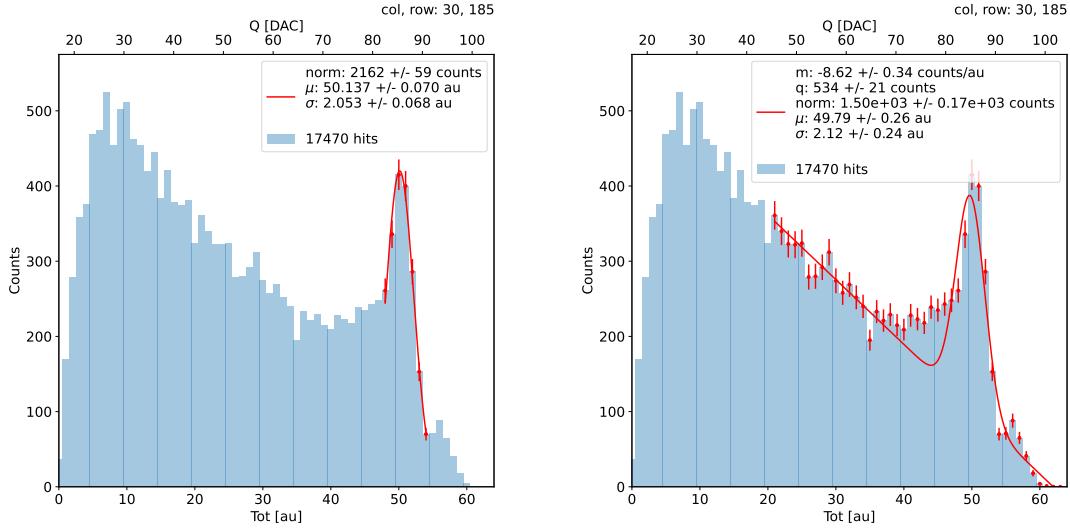


Figure 6.8: due pixel per far vedere la differenza tra i fit

6.1.5 Dead time measurements

The hit loss is due to analog and digital pile up: the first one occurs when a new hit arrives during the pre-amplifier response, the second instead, which is the more relevant contribution with high rate, while the information of the previous hit has not yet been transferred to the periphery. As only one hit at a time can be stored on the pixel's RAM, until the data have completed the path to get out, the pixel is paralyzed and the dead time τ almost corresponds with the time needed to transmit the data-packets off-chip. Since the exportation of data from pixel to the EoC occurs via a 21-bits data bus, only one clock cycle is need to transfer the data to the end of column and the dead time bottleneck is given by the bandwidth of the serializer at the EoC. In our setup the serializer operates at 40 MHz, thus to transmit a data packet (27-bit considering the addition at the EoC) at least 675 ns are needed. For what we have said so far, the R/O is completely sequential and therefore is expected a linear dependence of the reading time on the number of pixels to read:

$$\tau = 25 \text{ ns} \times (\alpha N + \beta) \quad (6.6)$$

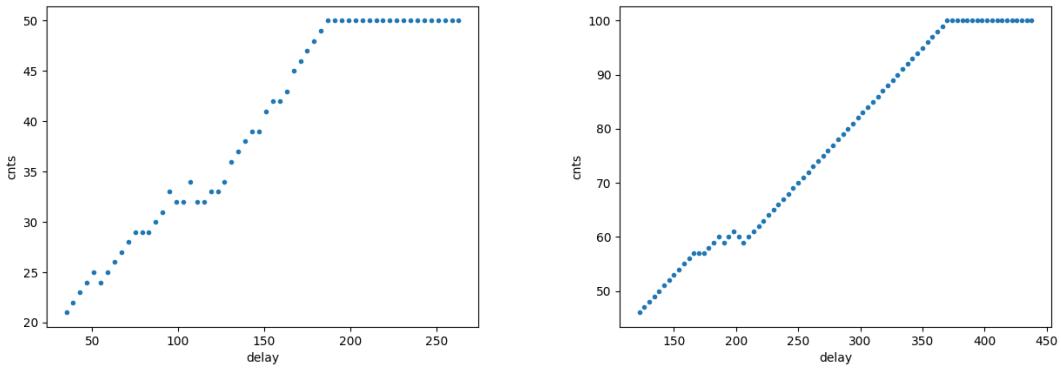
where α and β are parameters dependent on the readout chain setting.

To measure and test the linearity of the reading time with the number of pixels firing, I have used the injection mode available on the chip. Indeed, the injection mode allows fixing not only the amplitude of the pulse, which corresponds to the charge in DAC units, but also the period and the width. I have injected a fix number of pulses (100) and looked for the rate when the efficiency decreases. Moreover to test that there is no dependece of the digital readout time from the charge of the pulse, I have try to change the amplitude of the pulse injected, but the parameters found were consistent with the default configuration ones.

Al posto degli esempi con 5 e 10 pixels metterei un esempio dell'efficienza vs il periodo quando leggo un singolo pixel. Una cosa che volevo fare era anche provare a fissare la slope con cui l'efficienza scende: se la slope è uguale per tutti il readout diventa completamente predittivo.

While the single pixel reading time and the dead time do not depend on the position on the pixel matrix and are equal to 106 (46+60) clock counts within 1 clock count, on the other hand the τ depends on the pixel position on the matrix when more than one pixel are firing. In particular the priority chain goes from row 224 to row 0, and from col 0 to 112, that means the last pixels to be read is the one on le bottom right corner of the matrix.

In figure 6.11 is reported the reading time versus the number of pixels injected; the R/O parameters that control the reading time and their default values are reported on table ??.



(a) efficiency vs DELAY 5 pixels

(b) efficiency vs DELAY per 10pixels

Parameter	Value [DAC]	Value [μ s]
START_FREEZE	64	1.6
STOP_FREEZE	100	2.5
START_READ	66	1.65
STOP_READ	68	1.7

Table 6.3: Default configuration of the R/O parameters

913 The factor α , referring to eq. 6.6 is proportional to the difference (STOP_FREEZE - START_READ),
 914 while the offset β lies between 5 and 15 clock counts. Since through the injection a random hit rate
 915 on the matrix can't be simulated, as the coordinates of the pixels to inject must be specified, for
 916 convenience I used the pixels on the same column/row. No difference in the α and β coefficients
 has been observed between the two case.

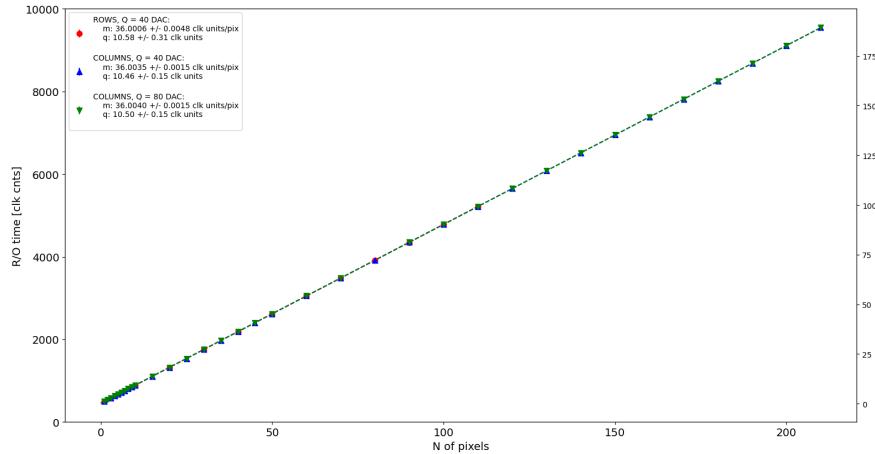


Figure 6.10

917
 918 Ci sarebbe da spiegare perchè i parametri che usiamo noi come default non sono quelli che
 919 minimizzano il tempo di lettura. La spiegazione è che "Abbiamo copiato i valori dal repository
 920 di quelli di Bonn". Un'altra domanda potrebbe essere: come mai ho esplorato una zona più
 921 vasta per i parametri del R/O. Cambiando molto i parametri del R/O la lettura non funzionava
 922 per niente: ad esempio CONF_STOP_FREEZE non può essere impostato nè sopra 105 nè sotto 95

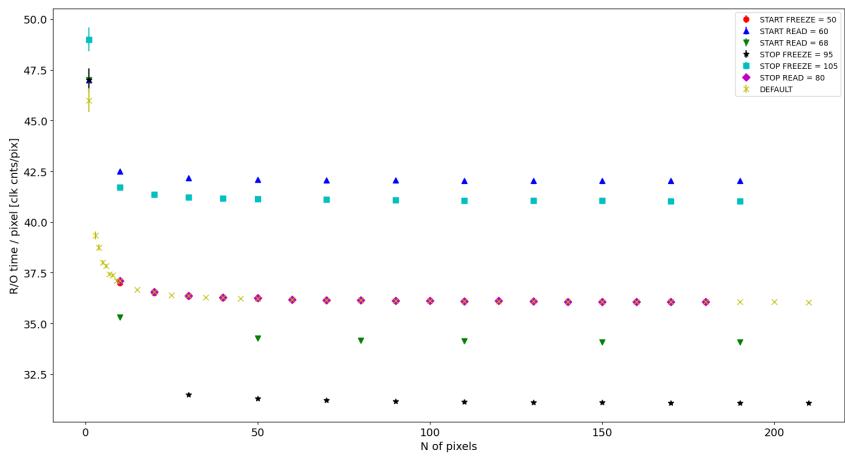


Figure 6.11

923 6.2 ARCADIA-MD1 characterization

924 **Chapter 7**

925 **Test beam measurements**

926 **7.1 Testbeam motivation**

927 Possibilità di integrare carica sul pixel: due elettroni consecutivi su un pixel ogni quanto arrivano?

928 Vogliamo sfruttare l'analog pile up, per fare questo dobbiamo fare attenzione a non finire nel
929 digital pile up Devi avere che il tot dell'elettrone (cioè MIP) è maggiore del deltat medio; in questo
930 caso potresti riuscire ad integrare carica. Non è possibile rivelare singoli elettroni in quanto l'hit
931 rate è troppo alto per le dosi messe a disposizioni con il fascio. Una formula di conversione è:

$$R[\text{Hz}/\text{cm}^2] = \frac{DPP[\text{Gy}]}{1.6 \cdot 10^{10} S[\text{g}/\text{cm}^2]} \quad (7.1)$$

932 where S is the stopping power in water, 2.17 g/cm^2 The medium is ordinarily water, since dosimetric
933 protocols are based on measurements in water as reference

934 La struttura del fascio e le varie quantità che si usano per descriverlo sono riportate in figure
935 7.1. Ricordo i valori tipici che stanno in tabella in table ??.

936 **7.2 Apparatus description**

937 **7.3 Measurements**

938 Numero di hit in funzione del DDP. Spettri con e senza collimatori.

Table 1. Terminology used throughout the text.

Term	Symbol	Description
intra-pulse dose-rate	—	The duration of a single pulse. ^a
	\bar{D}	Mean dose-rate for a multi-pulse delivery.
pulse repetition frequency	\dot{D}_p	Dose-rate in a single pulse. ^a
	DPP	Dose in a single pulse. ^a
	PRF	Number of pulses delivered per unit time. ^a
	t_i	Total irradiation time from the beginning of the first delivered pulse to the end of the last delivered pulse.
ultrahigh dose-rate	—	Radiation delivered with mean dose-rate of $> \sim 40 \text{ Gy s}^{-1}$.
	—	Ultrahigh dose-rate RT that presents decreased damage to normal tissues compared to RT delivered with conventional dose-rate of $\sim 0.04 \text{ Gy s}^{-1}$.

^aPulses are considered to be macro-pulses unless otherwise stated (see also figure 1).

^bIn literature sometimes referred to as the instantaneous dose-rate.

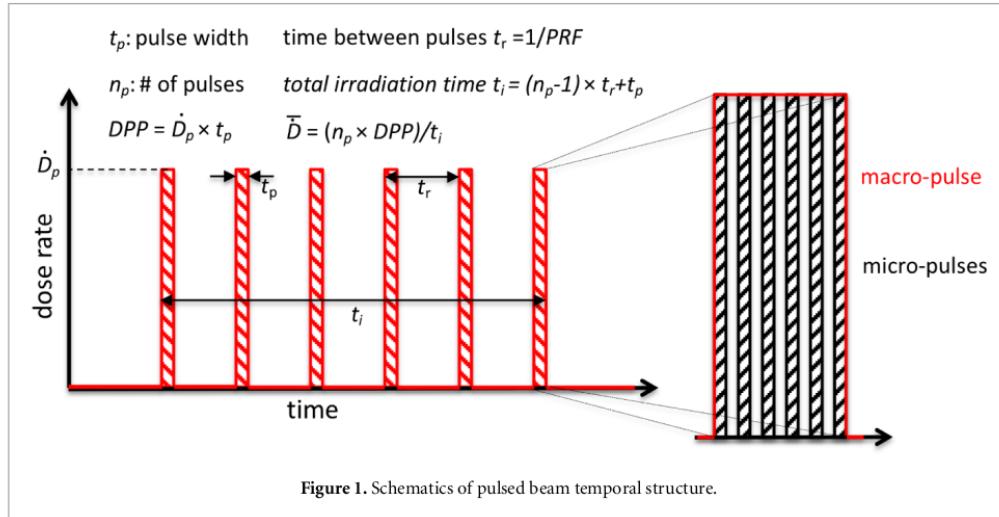


Figure 7.1

939 Appendix A

940 Pixels detector: a brief overview

941 A.1 Radiation damages

942 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they
 943 are almost always installed near the interaction point where there is a high energy level of radiation.
 944 At LHC the ϕ_{eq} per year in the innermost pixel detector is $10^{14} n_{eq}/cm^2$; this number reduces by
 945 an order passing to the outer tracker layer [2] pag 341 Wermes. Here the high fluence of particles
 946 can cause a damage both in the substrate of the detector and in the superficial electronics.

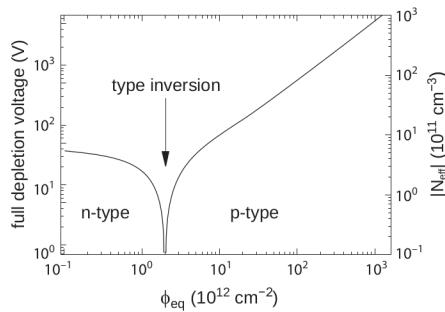
947 The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but
 948 it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the
 949 NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV
 950 neutrons. Differently, surface damages are principally due to ionizing energy loss.

951 **DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide (SiO_2) can
 952 cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages
 953 are mostly less relevant than the previous one, since with the development of microelectronics and
 954 with the miniaturization of components (in electronic industry 6-7 nm transistors are already used,
 955 while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit
 956 is reduced.

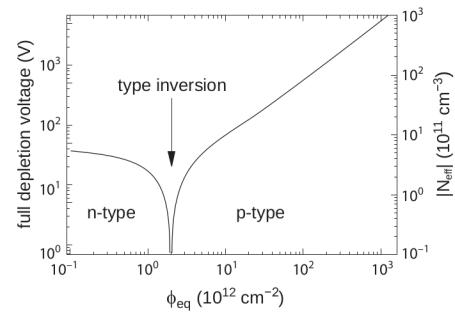
957 Let's spend instead two more other words on the more-relevant substrate damages: the general
 958 result of high radiation level is the creation of new energy levels within the silicon band gap and
 959 depending on their energy-location their effect can be different, as described in the Shockley-Read-
 960 Hall (SRH) statistical model. The three main consequence of radiation damages are the changing
 961 of the effect doping concentration, the leakage current and the increasing of trapping probability.

962 **Changing of the effective doping concentration:** is associated with the creation/removal
 963 of donors and acceptors center which trap respectively electrons/holes from the conduction band
 964 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type¹)

¹L'INVERSIONE OPPOSTA NON CE L'HA PERCHÈ?



(a) 1a



(b) 1b

965 can happen: indeed it is quite common at not too high fluences ($\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$). A changing
966 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime
967 (eq.2.1) and sometimes can be difficult keeping to fully deplete the bulk.

968 **Leakage current:** is associated with the generation-recombination centers. It has a strong
969 dependence with the temperature ($I_{leak} \propto T^2$), whose solution is therefore to operate at lower
970 temperature.

971 **Increase of trapping probability:** since the trapping probability is constant in the depleted
972 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,
973 that is the mean trapping path, decreases after irradiation and typical values are 125-250 μm and
974 must be compared with the thickness of the depleted region which () corresponds to the mean drift
975 path.

976 Different choices for substrate resistivity, for junctions type and for detector design are typically
977 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced
978 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))
979 for example, show a compensation effect for radiation damage; another example is the usage of
980 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage
981 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p
982 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be
983 placed near the diode.

984 Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché
985 una particella deposita carica nell'elettronica che fa da memoria registro/RAM/.... Questo tipo
986 di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti
987 tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip
988 in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più
989 carica di quanto farebbe una MIP. Questo metodo pur essendo più comodo richiede less amount of
990 area ha però come drawback che il registro può essere soggetto a SEU problema non trascurabile
991 in acceleratori come HL-LHC adronici

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