

# Summary

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<sup>43</sup> Characterization of monolithic CMOS pixel sensors for charged particle detectors and for high  
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<sup>45</sup> **Chapter 1**

<sup>46</sup> **Introduction**

<sup>47</sup> Pixel detectors, members of the semiconductor detector family, have significantly been used at the  
<sup>48</sup> accelerator experiments for energy and position measurement. Because of their dimension (today  
<sup>49</sup>  $\sim 30 \mu\text{m}$  or even better) and their spatial resolution ( $\sim 5\text{-}10 \mu\text{m}$ ), with the availability of technology  
<sup>50</sup> in 1980s they proved to be perfectly suitable for vertex detector in the inner layer of the detector.

<sup>51</sup> Despite the monolithic pixels came up with CCDs, invented in 1969 and fastly used in cameras,  
<sup>52</sup> their usage had to wait for microelectronics developement: in MAPS device the readout electronics  
<sup>53</sup> is build on the pixel's area, then the pixel dimension is limited by the dimension of transistors. This  
<sup>54</sup> constraint favoured the usage in physics experiment of hybrid pixels, which currently constitute  
<sup>55</sup> the state-of-art for large scale pixel detector. These ones are made by two different wafer each one  
<sup>56</sup> containing or the sensor or the ASIC, which are after joined together through microconnection.  
<sup>57</sup> This structure allows a separate optimization for the two components and makes hybrid pixels  
<sup>58</sup> flexible and versatile.

<sup>59</sup> Requirement imposed by accelerator are stringent and they will be even more with the increase  
<sup>60</sup> of luminosity in terms of radiation hardness, efficiency and occupancy, time resolution, material  
<sup>61</sup> budget and power consumption. For this reason experiments (as ATLAS, CMS, BelleII) began to  
<sup>62</sup> look at the more innovative and well-performing monolithic active pixels (MAPS) as perspective for  
<sup>63</sup> their future upgrades.

<sup>64</sup> Che condiziona la risoluzione e l'efficienza di ricostruzione della sua traccia, e consumi del  
<sup>65</sup> detector, sono diventati sempre più rilevanti; molti esperimenti (ATLAS, CMS, BelleII,..) stanno  
<sup>66</sup> infatti valutando la possibilità di sostituire gli ibridi con i MAPS, che per i temi precedenti offrono  
<sup>67</sup> prestazioni migliori, a scapito di tempi di lettura mediamente più lunghi, vista anche la positiva  
<sup>68</sup> esperienza di ALICE ad LHC, primo esperimento ad introdurre un detector a pixel monolitico.

<sup>69</sup> During my thesys I studied and characterised two monolithic active pixel chips, TJ-Monopix1  
<sup>70</sup> and MD1; this devices, that are still prototypes, have been conceived and designed for physics  
<sup>71</sup> experiments at colliders, space experiments and also for medical applications.

<sup>72</sup> il primo, TJ-Monopix1, è un prototipo di un modello selezionato per l'upgrade di Belle II  
<sup>73</sup> durante il LSD nel 2025 (il chip finale si chiamerà OBELIX e avrà come sensore TJ-Monopix2,  
<sup>74</sup> successore di Monopix1); il secondo chip è stato progettato da ARCADIA che potrà avere, nelle  
<sup>75</sup> versioni future, applicazioni in fisica medica, in esperimenti nello spazio e ai collider.

<sup>76</sup> Le differenze principali tra i due chip risiedono nel segnale fornito in output (Monopix fornisce il  
<sup>77</sup> tempo sopra soglia dell'impulso triangolare, proporzionale alla carica rilasciata nel sensore, mentre  
<sup>78</sup> arcadia fornisce un segnale puramente digitale), nella sequenza di readout dei pixel (monopix ha  
<sup>79</sup> una lettura puramente sequenziale di tipo "column drain") mentre arcadia ha una lettura più  
<sup>80</sup> moderna che consente di poter aggregare dati durante la trasmissione (ad esempio nel caso di  
<sup>81</sup> formazione di cluster e creazione di hti su pixel adiacenti).

<sup>82</sup> I performed a threshold and noise characterization ( $\sim 400 \text{ e}^-$  and  $\sim 15 \text{ e}^-$ ) of TJ-Monopix1 in  
<sup>83</sup> order

<sup>84</sup> Tra i test con Monopix1 ho effettuato una caratterizzazione in soglia ( $\sim 400 \text{ e}^-$ ) e rumore ( $\sim$   
<sup>85</sup>  $15 \text{ e}^-$ ) al fine di visualizzare la dispersione di questi valori sulla matrice; per poter minimizzare la  
<sup>86</sup> dispersione sulla matrice e avere una più uniforme selezione della soglia (che è globale su tutta  
<sup>87</sup> la matrice), le versioni successive di TJ-Monopix1 includono e includeranno la possibilità di fare  
<sup>88</sup> piccole correzioni (3 bit per pixel vengono allocati in Monopix2) di quest'ultima pixel per pixel.  
<sup>89</sup> Per poter fornire le misure dei segnale fornito, tempo sopra soglia ToT, in elettroni, che assieme

90 alle lacune vengono create dal passaggio della particella incidente e che quindi sono la quantità  
91 fisica "importante" nella misura, è stata necessaria una calibrazione assoluta dell'oggetto. Per  
92 quest'ultima e per altri test ?? mi sono servita di sorgenti radiattive come il ferro 55 (emissione di  
93 un fotone gamma a 5.9 kev e dello stronzio 90 il cui spettro dell'elettrone emesso ha un end point  
94 a x) e dei cosmici. Inoltre ho partecipato ai test di Monopix1 su fascio: abbiamo testato il chip in  
95 una modalità diversa da quella per cui è stato progettato (tracking) e più simile al funzionamento  
96 delle CCD, in cui non si cerca di distinguere il singolo elettrone incidente ma si integra in un  
97 singolo segnale di output la carica rilasciata da più elettroni incidenti. Il fascio utilizzato (elettroni  
98 da 7-9 MeV) è un fascio ad altissima intensità e verrà utilizzato per fare ricerca su radioterapia  
99 ad alto rate (l'acceleratore è in grado di rilasciare dosi -con riferimento in acqua- fino a 40 Gy/s,  
100 corrispondenti ad un numero di particelle di ..). Per quanto riguarda, invece, le misure sul chip  
101 MD1, ho partecipato ai test elettrici e sul front end di un prototipo non ancora completamente  
102 funzionante. Un nuovo chip dovrebbe arrivare nei prossimi giorni a Pisa.

<sup>103</sup> **Chapter 2**

<sup>104</sup> **Pixel detectors**

<sup>105</sup> I pixel detector fanno parte della famiglia dei detector a semiconduttore e il loro funzionamento si  
<sup>106</sup> basa sulla creazione di coppie elettrone lacuna all'interno del bulk. Dalla creazione della particella  
<sup>107</sup> incidente di queste coppie e facendole driftare attraverso l'applicazione di un campo elettrico, si  
<sup>108</sup> ottiene quindi un segnale all'interno del rivelatore correlabile all'energia della particella incidente.  
<sup>109</sup> Il campo elettrico applicato, lo spessore della zona di svuotamento, le modalità con cui il  
<sup>110</sup> segnale viene processato e trasmesso all'esterno del rivelatore sono caratteristiche specifiche del  
<sup>111</sup> tipo di chip. In questo capitolo tratterò dunque i principali tipi di rivelatori a pixel, sofferandomi  
<sup>112</sup> in particolare sui pixel monoliti.

<sup>113</sup> **2.1 Signal formation**

<sup>114</sup> When a charge particle passes through a pixel and loses energy by ionization a part of that  
<sup>115</sup> energy is used to generate electron-hole pairs (another part is used for other processes, as the  
<sup>116</sup> lattice excitation) which are then separated by the electric field and collected at their respectively  
<sup>117</sup> electrodes (*p* for holes and *n* for electrons)<sup>1</sup>; by the drift of these charges, a signal  $i_e$  is generated  
<sup>118</sup> on the electrode *e* as stated by the Shockley-Ramo's theorem:

$$i_e(t) = -q v(t) E_{WF,e} \quad (2.1)$$

<sup>119</sup> where  $v(t)$  is the instantaneous velocity of the charge  $q$  and  $E_{WF}$  is the weighting field, that is the  
<sup>120</sup> field obtained biasing the electrode *e* with 1V and all the others with 0V. The drift velocity of the  
<sup>121</sup> charge depends on the electric field and on the mobility of the particle:

$$v = \mu(E) E \quad (2.2)$$

<sup>122</sup> where  $\mu(E)$  is a function of the electric field and is linear with  $E$  only for small  $E$ : at higher values  
<sup>123</sup> the probability of interactions with optical phonons increases and the mobility drops and this leads  
<sup>124</sup> to an independence of the velocity from the electric field (fig. 2.1b).

<sup>125</sup> The average energy needed to create a pair at 300 K in silicon is  $w_i = 3.65$  eV, that is more  
<sup>126</sup> than the mean ionization energy because of the interactions with phonon, since for a minimum  
<sup>127</sup> ionizing particle (MIP) the most probable value (MPV) of charge released in the semiconductor is  
<sup>128</sup> 0.28 keV/ $\mu$ , hence the number of e/h pairs is:

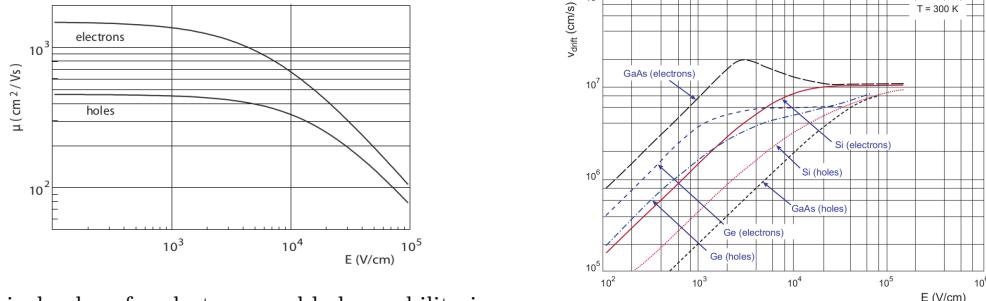
$$\langle \frac{dE}{dx} \rangle \frac{1}{w_i} \sim 80 \text{ e}/\text{h} \sim \frac{1.28 \cdot 10^{-2} fC}{\mu m} \quad (2.3)$$

<sup>129</sup> CON UN'INCERTEZZA CHE È RADICE DI N; ED EVENTUALEMTE SI AGGIUNGE IL  
<sup>130</sup> FATTORE DI FANO NEL CASO DI ASSORBIMENTO TOTALE. IL FATTORE DI FANO È  
<sup>131</sup> 0.115 NEL SILICIO. ecc

<sup>132</sup> It is fundamental that pairs e/h are produced in the depleted region of the semiconductor where  
<sup>133</sup> the probability of recombination with charge carriers is low to avoid loss of signals. Pixel detectors

---

<sup>1</sup>Even if in principle both the electrode can be used to read a signal, for pixel detectors, where the number of channel and the complexity of readout are high, only one is actually used. In strip and pad detectors, instead, is more common a dual-side readout



(a) Typical values for electrons and holes mobility in silicon at room temperature are  $\mu_n \sim 1450 \text{ cm}^2/\text{Vs}$ ,  $\mu_h = 500$   
(b) Drift velocity at room temperature in different semiconductors

134 are then commonly reverse biased: a positive bias is given to the  $n$  electrode and a negative to the  
135  $p$  to grow the depletion zone in the epitaxial layer below the electrode. The width of the depletion  
136 region is related with the external bias  $V_{ext}$ , the resistivity  $\rho$  and also with the dopant:

$$d_n \sim 0.55 \sqrt{\frac{\rho}{\Omega cm}} \frac{V_{ext}}{V} \mu m \quad (2.4)$$

138

$$d_p \sim 0.32 \sqrt{\frac{\rho}{\Omega cm}} \frac{V_{ext}}{V} \mu m \quad (2.5)$$

139

140 For that reason high resistivity wafers ( $100 \Omega cm - k\Omega cm$ ) are typically preferred because they  
141 allow bigger depletion zone with smaller voltage bias. **Metto il disegno "standard" di una giunzione**

## 142 2.2 CCDs

143 **descrivi come sono fatte e come funziona il readout** Tens of ms due to the need to transfer the  
144 charge signals pixel by pixel through a single output circuit For photon imaging the need of high  
145 assorbtion efficiency, **per cui usi materiali con alto Z**

## 146 2.3 Hybrid pixels

147 **METTI IN EVIDENZAZ CHE PUOI FARE UN READOUT CON TECNOLOGIA CMOS.** Metti  
148 **in evidenza che sono più veloci** Hybrid pixels are made of two parts (fig. 2.2a), the sensor and the  
149 electronics: for each pixel these two parts are welded together through microconnection (bump  
150 bond).

151 They provide a practical system where readout and sensor can be optimized separately, although  
152 the testing is less easy-to-do since the sensor and the R/O must be connected together before.

153 In addition, the particular and sophisticated procedure to bond sensor and ASIC (application spe-  
154 cific integrated circuit) makes them difficult to produce, delicate, especially when exposed to high  
155 levels of radiation, and also expensive.

156 A critical parameter for accelerator experiments is the material budget, which represents the main  
157 limit factor for momentum measurement resolution in a magnetic field; since hybrid pixels are  
158 thicker ( $\sim$  hundreds of  $\mu m$ ) than monolithic ones (even less than  $100 \mu m$ ), using the latter the  
159 material budget can be down by a third: typical value for hybrid pixels is  $1.5 \% X_0$  per layer,  
160 while for monolithic  $0.5 \% X_0$ .

161 Among other disadvantages of hybrid pixels there is the bigger power consumption that implies,  
162 by the way, a bigger cooling system leading in turn to an increase in material too.

163 **DEPFET** are the first attempt towards the integration of the front end (FE) on the sensor bulk:  
164 they are typically mounted on a hybrid structure but they also integrate the first amplification  
166 stage.

167 Each pixel implements a MOSFET (metal-oxide-semiconductor field-effect transistor) transistor  
168 (a p-channel in fig. 2.2b): an hole current flows from source to drain which is controlled by the  
169 external gate and the internal gate together. The internal gate is made by a deep  $n+$  implant

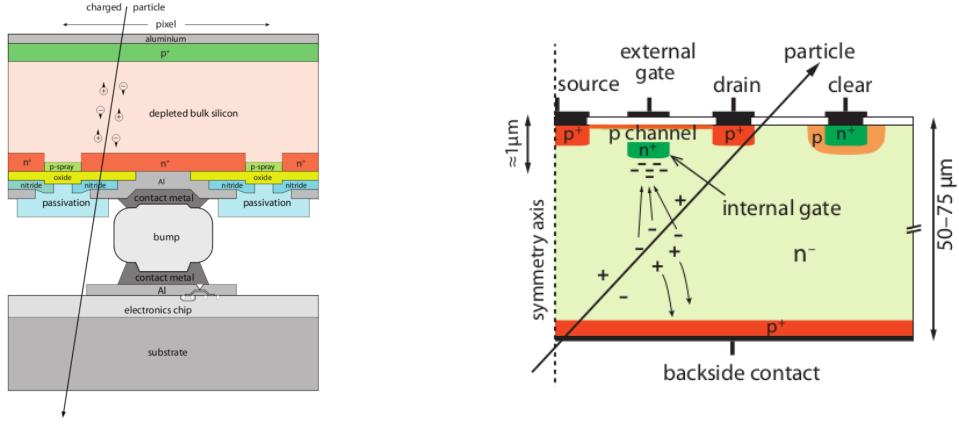


Figure 2.2: Concept cross-section of hybrid pixel (a) and of a DEPFET (b)

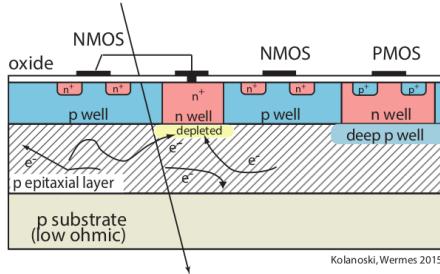


Figure 2.3: Concept cross-section of CMOS MPAS pixel

170 towards which electrons drift after being created in the depletion region (to know how the signal  
 171 is created in a pixel detector look at appendix A); the accumulation of electrons in the region  
 172 underneath the n implant changes the gate potential and controls the transistor current.  
 173 DEPFET typically have a good S/N ratio: this is principally due the amplification on-pixel and  
 174 the large depletion region. But, since they need to be connected with ASIC the limiting factor still  
 175 is the material budget.

## 176 2.4 CMOS MAPS and DMPAS

177 With respect to CCDs, the radiation tolerance could be greatly increased by sensing the signal  
 178 charge within its own pixel, instead of transporting it over thousands of pixels. The readout  
 179 speed could also be dramatically increased by in-pixel amplitude discrimination, followed by sparse  
 180 readout of only the hit pixels Monolithic active pixels accommodate on the same wafer both the  
 181 sensor and the front end electronics, with the second one implanted on top within a depth of about  
 182 1 μm below the surface.

183 MAPS have been first proposed and realized in the 1990s and their usage has been enabled by the  
 184 development of the electronic sector which guarantees the decrease in CMOS transistors dimension  
 185 at least every two years, as stated by the Moore's law<sup>2</sup>.

186 As a matter of fact the dimension of components, their organization on the pixel area and logic  
 187 density are important issues for the design and for the layout; typically different decisions are taken  
 188 for different purposes.

189 Monolithic active pixel can be distinguished between two main categories: MAPS and depleted  
 190 MAPS (DMAPS).

191 MAPS (figure a 2.3) have typically an epitaxial layer in range 1-20 μm and because they are not  
 192 depleted, the charge is mainly collected by diffusion rather than by drift. This makes the path of  
 193 charges created in the bulk longer than usual, therefore they are slow (of order of 100 ns) and the  
 194 collection could be partial especially after the irradiation of the detector (look at A for radiation  
 195 damages), when the trapping probability become higher.

<sup>2</sup>Moore's law states that logic density doubles every two years.

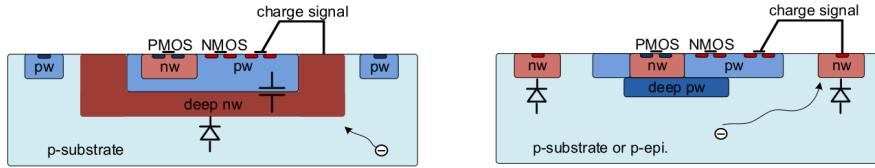


Figure 2.4: Concept cross-section with large and small fill factor

196 In figure 2.3 is shown as example of CMOS MAPS: the sensor in the scheme implements an  
 197 n well as collection diode; to avoid the others n wells (which contain PMOS transistor) of the  
 198 electronic circuit would compete in charge collection and to shield the CMOS circuit from the  
 199 substrate, additionally underlying deep p well are needed. DMAPS are instead MAPS depleted  
 200 with  $d$  typically in  $\sim 25\text{-}150 \mu\text{m}$  (eq. 2.1) which extends from the diode to the deep p-well, and  
 201 sometimes also to the backside (in this case if one wants to collect the signal also on this electrode,  
 202 additional process must be done).

#### 203 2.4.1 DMAPS: large and small fill factor

204 There are two different sensor-design approaches (figure 2.4) to DMAPS:

- 205 • large fill factor: a large collection electrode that is a large deep n-well and that host the  
 206 embedded electronics
- 207 • small fill factor: a small n-well is used as charge collection node

208 To implement a uniform and stronger electric field, DMAPS often uses large electrode design that  
 209 requires multiple wells (typically four including deep n and p wells); this layout adds on to the  
 210 standard terms of the total capacity of the sensor a new term (fig. 2.5), that contributes to the  
 211 total amplifier input capacity. In addition to the capacity between pixels ( $C_{pp}$ ) and between the  
 212 pixel and the backside ( $C_b$ ), a non-negligible contribution comes from the capacities between wells  
 213 ( $C_{WW}$  and  $C_{SW}$ ) needed to shield the embedded electronics. These capacities affect the thermal  
 214 and 1/f noise of the charge amplifier and the  $\tau_{CSA}$  too:

$$215 ENC_{thermal}^2 \propto \frac{4}{3} \frac{kT}{g_m} \frac{C_D^2}{\tau_{sh}} \quad (2.6) \qquad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_D}{C_f} \quad (2.7)$$

216 where  $g_m$  is the transconductance,  $\tau_{sh}$  is the shaping time.  
 217 Among the disadvantages coming from this large input capacity could be the coupling between  
 218 the sensor and the electronics resulting in cross talk: noise induced by a signal on neighbouring  
 219 electrodes; indeed, since digital switching in the FE electronics do a lot of oscillations, this prob-  
 lem is especially connected with the intra wells capacities. So, larger charge collection electrode

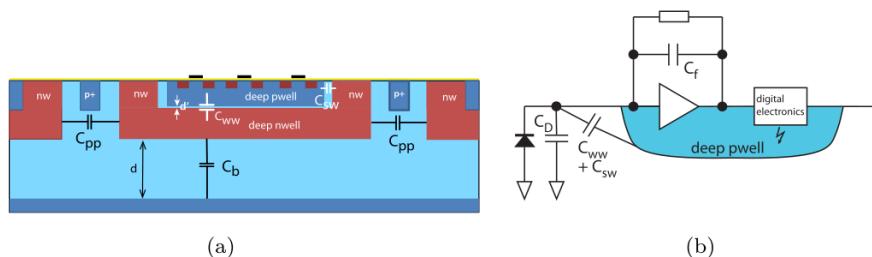


Figure 2.5:  $C_{pp}$ ,  $C_b$ ,  $C_{WW}$ ,  $C_{SW}$

220 sensors provide a uniform electric field in the bulk that results in short drift path and so in good  
 221 collection properties, especially after irradiation, when trapping probability can become an issue.  
 222 The drawback of a large fill-factor is the large capacity ( $\sim 100 \text{ fF}$ ): this contributes to the noise  
 223 and to a speed penalty and to a larger possibility of cross talk.

|                       | small fill factor | large fill factor |
|-----------------------|-------------------|-------------------|
| small sensor C        | ✓ (< 5 fF)        | ✗ (~ 100-200 fF)  |
| low noise             | ✓                 | ✗                 |
| low cross talk        | ✓                 | ✗                 |
| velocity performances | ✓                 | ✗ (~ 100 ns)      |
| short drift paths     | ✗                 | ✓                 |
| radiation hard        | ✗                 | ✓                 |

Table 2.1: Small and large fill factor DMAPS characteristics

225     The small fill-factor variant, instead, benefits from a small capacity (5-20 fF), but suffers from  
 226     a not uniform electric field and from all the issue related to that. **Ho già detto prima parlando dei  
 227     MAPS, devo ripetere qui?**

228     As we'll see these two different types of sensor require different amplifier: the large electrode one is  
 229     coupled with the charge sensitive amplifier, while the small one with voltage amplifier (sec 2.5.1).

#### 230     2.4.2 A modified sensor

231     A process modification developed by CERN in collaboration with the foundries has become the  
 232     standard solution to combine the characteristics of a small fill factor sensor (small input amplifier  
 233     capacity) and of large fill factor sensor (uniform electric field) is the one carried out for ALICE  
 234     upgrade about ten years [1].

235     A compromise between the two sensors could also be making smaller pixels, but this solution  
 236     requires reducing the electronic circuit area, so a completely new pixel layout should be though.  
 237     The modification consists in inserting a low dose implant under the electrode and one its advantage  
 238     lies in its versatility: both standard and modified sensor are often produced for testing in fact.

239     Before the process modification the depletion region extends below the diode towards the sub-  
 240     strate, and it doesn't extend laterally so much even if a high bias is applied to the sensor (fig. 2.6).  
 241     After, two distinct pn junctions are built: one between the deep p well and the  $n^-$  layer, and the  
 242     other between the  $n^-$  and the  $p^-$  epitaxial layer, extending to the all area of the sensor.

243     Since deep p well and the p-substrate are separated by the depletion region, the two p electrodes  
 244     can be biased separately<sup>3</sup> and this is beneficial to enhance the vertical electric field component.

245     The doping concentration is a trimmer parameter: it must be high enough to be greater than the  
 246     epitaxial layer to prevent the punchthrough between p-well and the substrate, but it must also be  
 247     lower enough to allow the depletion without reaching too high bias.

### 248     2.5 Analog front end

249     After the creation of a signal on the electrode, the signal enters the front end circuit (fig.2.7), ready  
 250     to be molded and transmitted out of chip. Low noise amplification, fast hit discrimination and an  
 251     efficient, high-speed readout architecture, consuming as low power as possible must be provided  
 252     by the readout integrated electronics (ROIC).

253     Let's take a look to the main steps of the analog front end chain: the preamplifier (that actually  
 254     often is the only amplification stage) with a reset to the baseline mechanism and a leakage current  
 255     compensation, a shaper (a band-pass filter) and finally a discriminator. The whole chain must be  
 256     optimized and tuned to improve the S/N ratio: it is very important both not to have a large noise  
 257     before the amplification stage in order to not multiply that noise, and chose a reasonable threshold  
 258     of the discriminator to cut noise-hits much as possible.

#### 259     2.5.1 Preamplifier

260     Even if circuits on the silicon crystal are only constructed by CMOS, a preamplifier can be modeled  
 261     as an operational amplifier (OpAmp) where the gain is determined by the input and feedback

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<sup>3</sup>This is true in general, but it can be denied if other doping characteristics are implemented, and we'll see that this is the case of TJ-Monopix1

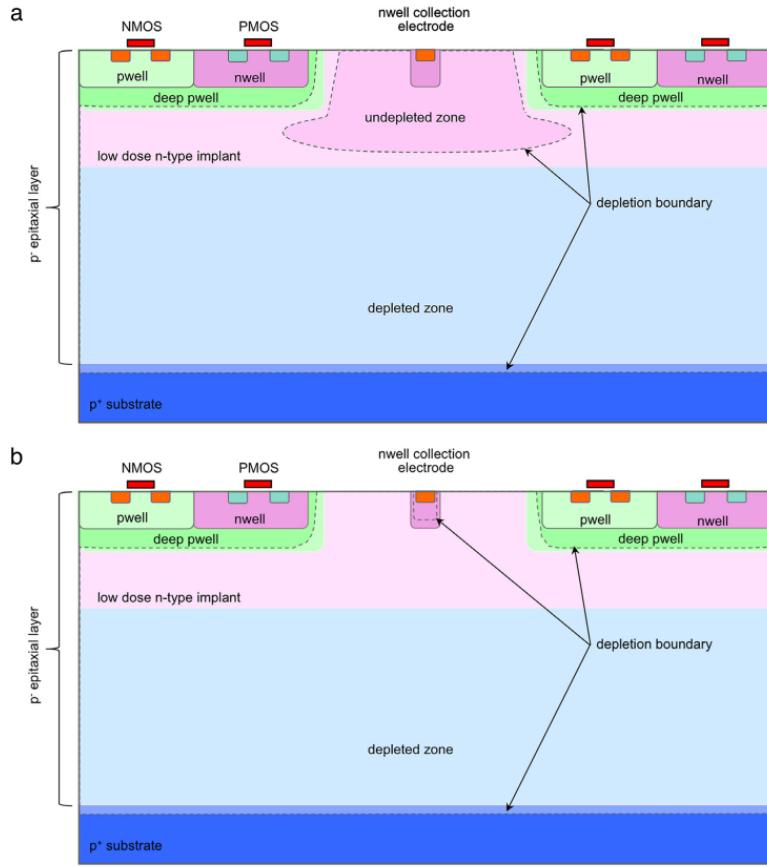


Figure 2.6: A modified process for ALICE tracker detector: a low dose n implant is used to create a planar junction. In (a) the depletion is partial, while in (b) the pixel is fully depleted.

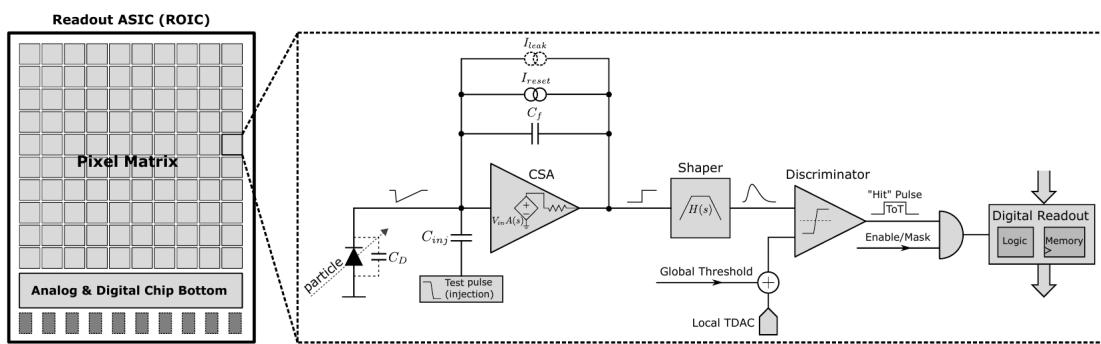


Figure 2.7: Readout FE scheme: in this example the preamplifier is a charge sensitive one (CSA) but changing the capacitive feedback into a resistive one, this can be converted in a voltage or current amplifier.

262 impedance (first step in figure 2.7):

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_f}{Z_{in}} \quad (2.8)$$

263 Depending on whether a capacity or a resistance is used as feedback, respectively a charge or a  
 264 voltage amplifier is used: if the voltage input signal is large enough and have a sharp rise time, the  
 265 voltage sensitive preamplifier is preferred. Consequently, this flavor doesn't suit to large fill factor  
 266 MAPS whose signal is already enough high:  $v_{in} = Q/C_D \approx 3\text{fC}/100\text{ pF} = 0.03\text{ mV}$ , but it's fine  
 267 for the small fill factor ones:  $v_{in} = Q/C_D \approx 3\text{fC}/3\text{ pF} = 1\text{ mV}$ .

268 In the case of a resistor feedback, if the signal duration time is longer than the discharge time  
 269 ( $\tau = R_S C_D$ ) of the detector the system works as current amplifier, as the signal is immediately  
 270 trasmit to the amplifier; in the complementary case (signal duration longer than the discharge  
 271 time) the system integrates the current on the  $C_D$  and operates as a voltage amplifier.

## 272 2.6 Readout logic

273 Readout logic includes the part of the circuit which takes the FE output signal, processes it and  
 274 then transmit it out of pixel and/or out of chip; depending on the situation of usage different  
 275 readout characteristics must be provided.

276 To store the analogical information (i.e. charge collected, evolution of signal in time, ...) big buffers  
 277 and a large bandwidth are needed; the problem that doesn't occur, or better occur only with really  
 278 high rate, if one wants record only digital data (if one pixel is hit 1 is recorded, and if not 0 is  
 279 recorded).

280 A common compromise often made is to save the time over threshold (ToT) of the pulse in clock  
 281 cycle counts; this needs of relatively coarse requirement as ToT could be trimmer to be a dozen  
 282 bits but, being correlated and hopefully being linear with the deposited charge by the impinging  
 283 particle in the detector, it provides a sufficient information. The ToT digitalization usually takes  
 284 advantage of the distribution of a clock (namely BCID, bunch crossing identification) on the pixels'  
 285 matrix. The required timing precision is at least around 25 ns, that corresponds to the period of  
 286 bunch collisions at LHC; for such reason a reasonable BCID-clock frequency for pixels detector is  
 287 40 MHz.

288 Leading and trailing edges' timestamp of the pulse are saved on pixel within a RAM until they  
 289 have been read, and then the ToT is obtained from their difference.

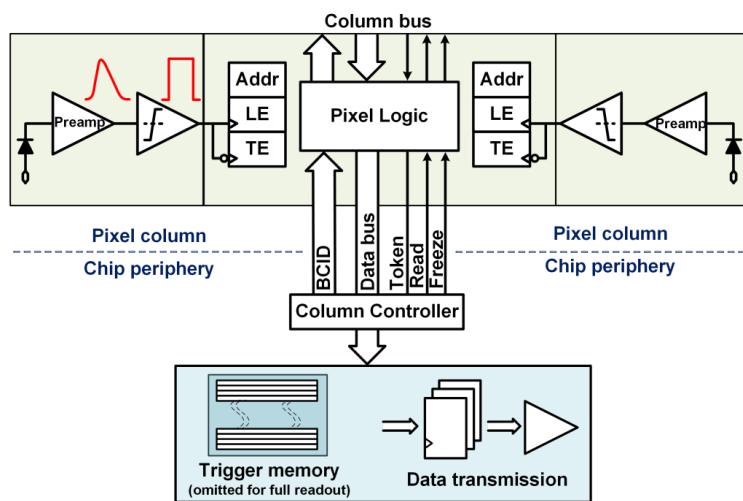


Figure 2.8: Column drain R/O scheme where ToT is saved

289 Moreover, the readout architecture can be full, if every hit is read, or triggered, if a trigger  
 290 system decides if the hit must be store or not. On one hand the triggered-readout needs buffers  
 291 and storage memories, on the other the full readout, because there is no need to store hit data on  
 292 chip, needs an high enough bandwidth.

294 A triggered readout is fundamental in accelerator experiments where the quantity of data to store  
 295 is too large to be handled, and some selections have to be applied by the trigger: to give an order

296 of growth, at LHC more than 100 TBit/s of data are produced, but the storage limit is about 100  
 297 MBit/s [2] (pag. 797).

298 Typically the trigger signal is processed in a few  $\mu s$ , so the pixel gets it only after a hundred clock  
 299 cycles from the hit arrival time: the buffer depth must then handle the higher trigger latency.

300 After having taken out the data from the pixel, it has to be transmitted to the end of column  
 301 (EoC) where a serializer deliver it out of chip, typically to an FPGA.

302 There are several ways of transmitting data from pixel to the end of column: one of the most  
 303 famous is the column-drain read out, developed for CMS and ATLAS experiments [3]. All the  
 304 pixels in a double-column share a data bus and only one pixel at a time, according to a priority  
 305 chain, can be read. The reading order circuit is implemented by shift register (SR): when a hit  
 306 arrives, the corresponding data, which can be made of timestamp and ToT, is temporarily stored  
 307 on a RAM until the SH does not allow the access to memory by data bus.

308 Even if many readout architectures are based the column-drain one, it doesn't suit for large size  
 309 matrices. The problem is that increasing the pixels on a column would also raise the number of  
 310 pixels in the priority chain and that would result in a slowdown of the readout.

311 If there isn't any storage memory, the double-column behaves as a single server queue and the  
 312 probability for a pixel of waiting a time  $T$  greater than  $t$ , with an input hit rate on the column  $\mu$   
 313 and an output bandwidth  $B_W$  is [4]:

$$P(T > t) = \frac{\mu}{B_W} e^{-(B_W - \mu)t} \quad (2.9)$$

314 To avoid hit loss (let's neglect the contribution to the inefficiency of the dead time  $\tau$  due to the  
 315 AFE), for example imposing  $P(T > t) \sim 0.001$ , one obtains  $(B_W - \mu) t_t \sim 6$ , where  $t_t$  is the time  
 316 needed to transfer the hit; since  $t_t$  is small, one must have  $B_W \gg \mu$ , that means a high bandwidth  
 [4].

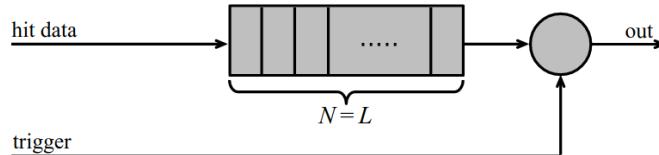


Figure 2.9: Block diagram of a pipeline buffer: N is the dimension of memory buffer and L is the trigger latency expressed in BCID cycles

317 Actually the previous one is an approximation since each pixel sees a different bandwidth de-  
 318 pending on the position on the queue: the first one sees a full bandwidth, but the next sees a  
 319 smaller one because occasionally it can be blocked by the previous pixel. Then the bandwidth seen  
 320 by the pixel  $i$  is  $B_i = B - \sum_j \mu_j$ , where  $\mu_j$  is the hit rate of the  $j$ th pixel.

321 The efficiency requirement on the bandwidth and the hit rate becomes:  $B_{W,i} > \mu_i$ , where the  
 322 index  $i$  means the constraint is for a single pixel; if all the N pixels on a column have the same  
 323 rate  $\mu = N\mu_i$ , the condition reduces to  $B_W > \mu$ . The bandwidth must be chosen such that the  
 324 mean time between hits of the last pixel in the readout chain is bigger than that.

325 In order to reduce the bandwidth a readout with zero suppression on pixel is typically employed;  
 326 this means that only information from channels where the signal exceeds the discriminator thresh-  
 327 old are stored. Qualcosa sulla zero suppression? La metto qui questa affermazione?

328 If instead there is a local storage until a trigger signal arrives, the input rate to column bus  
 329  $\mu'$  is reduced compared to the hit rate  $\mu$  as:  $\mu' = \mu \times r \times t$ , where  $r$  is the trigger rate and  $t$  is  
 330 the bunch crossing period. In this situation there is a more relaxed constraint on the bandwidth,  
 331 but the limiting factor is the buffer depth: the amount of memory designed depends both on the  
 332 expected rate  $\mu$  and on the trigger latency  $t$  as  $\propto \mu \times t$ , that means that the higher the trigger  
 333 latency and the lower the hit rate to cope with.

334 In order to have an efficient usage of memory on pixels' area it's convenient grouping pixels  
 335 into regions with shared storage. Let's compare two different situations: in the first one a buffer  
 336 is located on each pixel area, while in the second one a core of four pixels share a common buffer  
 337 (this architecture is commonly called FE-I4).

338 Consider a 50 kHz single pixel hits rate and a trigger latency of 5  $\mu s$ , the probability of losing

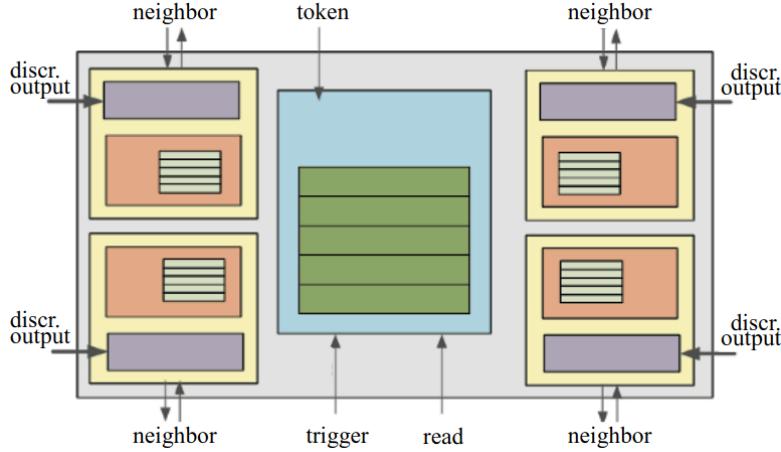


Figure 2.10: Block diagram of the FE-I4 R/O. Read and memory management section is highlighted in light blue; latency counters and trigger management section are highlighted in green; hit processing blocks are highlighted in purple; ToT counters and ToT management units are highlighted in orange

<sup>340</sup> hits is:

$$P(N > 1|\nu) = 1 - P(N = 0|\nu) - P(N = 1|\nu) = 1 - e^{-\nu}(1 + \nu) \approx 2.6\% \quad (2.10)$$

<sup>341</sup> where I have assumed a Poissonian distribution with mean  $\nu = 0.25$  to describe the counts N.

<sup>342</sup> To get an efficiency  $\epsilon$  greater than 99.9 % a 3 hit depth buffer is needed:

$$P(N > 3|\nu) = 1 - \sum_{i=0}^3 P(N = i|\nu) < 0.1\% \quad (2.11)$$

<sup>343</sup> Considering the second situation: if the average single pixel rate is still 50 kHz, grouping four  
<sup>344</sup> pixels the mean number of hits per trigger latency is  $\nu = 0.25 \times 4 = 1$ . To get an efficiency of  
<sup>345</sup> 99.9% (eq. 2.11) a buffer depth of 5 hits in the four-pixels region, instead of 3 per pixels, is needed.

<sup>346</sup> **Chapter 3**

<sup>347</sup> **Use of pixel detectors**

<sup>348</sup> There always was a tight relation between the development of cameras and pixel detectors since  
<sup>349</sup> 1969, when the idea of CCDs, thanks to whom Boyle and Smith were awarded the Nobel Prize in  
<sup>350</sup> Physics in 2009, revolutionized photography allowing light to be captured electronically instead of  
<sup>351</sup> on film. Even though the CMOS technology was already known when CCDs spread, the costs of  
<sup>352</sup> productions were too high to allow the diffusion of these sensors for which needed to wait until  
<sup>353</sup> 1990s. From that period on, the fast diffusion of CMOS was mainly due to the less cost than  
<sup>354</sup> CCD, and the less power required for supply. Nowadays CCDs are still preferred over MAPS in  
<sup>355</sup> astronomy, where the astronomical sources' rate are low enough to cope with tens of ms for the  
<sup>356</sup> readout.

<sup>357</sup> The principal use cases of pixel detectors are particle tracking and imaging: in the former case  
<sup>358</sup> individual charged particles have to be identified, in the latter instead an image is obtained by  
<sup>359</sup> the usually un-triggered accumulation of the impinging radiation. Also the demands on detectors  
<sup>360</sup> performance depends on their usage, in particular tracking requires high spatial resolution, fast  
<sup>361</sup> readout and radiation hardness.

<sup>362</sup> **3.1 Tracking in HEP**

<sup>363</sup> At first the physics world overlooked the CCDs, and all pixel in general, as against the gaseous  
<sup>364</sup> detector for tracking: there was no need to replace these ones which had a sufficient good resolution  
<sup>365</sup> ( $100\text{ }\mu\text{m}$ ). Since 1974, with the measurement of the invariant mass of the **j psi** and the affirmation  
<sup>366</sup> of the quark model, all experiments start to look for better spatial resolutions in order to achieve  
<sup>367</sup> the possibility of reconstructing short lived particle.

<sup>368</sup> Historically, the first pixel detector employed in particle physics was a CCD: it was installed in  
<sup>369</sup> the spectrometer at the CERN's Super Proton Synchrotron (SPS) by the ACCMOR Collaboration  
<sup>370</sup> (Amsterdam, CERN, Cracow, Munich, Oxford, RAL) at mid 1980s, with the purpose of studying  
<sup>371</sup> the recently-discovered charm particles. The second famous usage of CCDs took place at SLAC  
<sup>372</sup> in the Large Detector (SLD) during the two years 1996-98. **Cosa vedono di così importante da**  
<sup>373</sup> **dire che servono i pixel detector?** From that period on particle tracking in experiments have been  
<sup>374</sup> transformed radically: it was mandatory for HEP experiments to build an inner vertex detector.  
<sup>375</sup> In 1991, the more demanding environments led to the development of hybrid pixel detectors:  
<sup>376</sup> a dedicated collaboration, RD19, was established at CERN with the specific goal to define a  
<sup>377</sup> semiconductor micropattern detector with an incorporated signal processing at a microscopic level.  
<sup>378</sup> In those years a wide set of prototypes of hybrid pixel has been manufactured; among the greatest  
<sup>379</sup> productions a mention goes to the huge ATLAS and CMS vertex detectors. From the middle of  
<sup>380</sup> 2013 a second collaboration, RD 53, has been established with the new goal to find a pixel detector  
<sup>381</sup> suitable for phase II future upgrades of those experiments. Even if the collaboration is specifically  
<sup>382</sup> focused on design of hybrid pixel readout chips (aiming to 65 nm technique so that the electronics  
<sup>383</sup> fits within the pixel area), also other options have been taken in account and many test have been  
<sup>384</sup> done on MAPS for example. Requirements imposed by HL-LHC will become tighter in time: for  
<sup>385</sup> example, a dose and radiation of 5 Mrad and 1016 NIEL are expected after 5 years of operation.  
<sup>386</sup> Time resolution, material budget and power consumption are also issues for the upgrade: a time  
<sup>387</sup> resolution better than 25 ns for a bunch crossing frequency of 40 MHz, a material budget lower  
<sup>388</sup> than 2% and a power consumption lower than  $500\text{ mW/cm}^2$  are required.

389        Amidst the solutions proposed 3D silicon detector, invented by Sherwood Parker in 1995, and  
390        MAPS are the most promising. In 3D sensors the electrode is a narrow column of n-type implanted  
391        vertically across the bulk instead of being implanted on the wafer's surface. The charge produced  
392        by the impinging particle is then drifted transversally within the pixel, and, as the mean path  
393        between two electrode can be sufficient low, the trap probability is not an issue. 3D pixels have  
394        been already proved in ATLAS tracker [quando?](#). Even if 3D detector are adequately radiation hard,  
395        MAPS architecture looked very promising from the beginning: they overcome both the CCDs long  
396        reading time and the hybrid problems (I have already explained in section ?? the benefits of  
397        MAPS). Experiments such as ALICE at LHC and STAR at RHIC have already introduced the  
398        CMOS MAPS technology in their detectors. ALICE Tracking System (ITS2), upgraded during the  
399        LHC long shut down in 2019-20, was the first large-area ( $\sim 10 \text{ m}^2$  covered by 2.5 Gpixels) silicon  
400        vertex detector based on CMOS MAPS.

### 401        3.1.1 Hybrid pixels at LHC: ATLAS, CMS and LHC-b

#### 402        ATLAS

403        With CMS, ATLAS is one of two general-purpose detectors at the LHC and has the largest volume  
404        detector ever constructed for a particle collider (46 m long and 25 m in diameter). The Inner  
405        Detector consists of three different systems all immersed in a magnetic field parallel to the beam  
406        axis whose main components are: the pixel, the micro-strips and transition radiation trackers.  
407        Concerning the pixel detector, 92 million pixels are divided in 4 barrel layers and 3 disks in each  
408        end-cap region, covering a total area of  $1.9 \text{ m}^2$  and having a 15 kW of power consumption.

409        As stated by the ATLAS collaboration the pixel detector is exposed by an extreme particle  
410        flux: "By the end of Run 3<sup>1</sup>, the number of particles that will have hit the innermost pixel layers  
411        will be comparable to the number it would receive if it were placed only a few kilometres from  
412        the Sun during a solar flare". Considering that the particle density will increase even more with  
413        HL-LHC, radiation hardness is definitively target to achieve.

414        The most ambitious goal is employ a MAPS-based detector for the inner-layer barrels, and for  
415        this reason the RD53 collaboration is performing many test on MAPS prototypes, as Monopix of  
416        which I will talk about in section ??.

417        Up to now this possibility will be eventually implemented during the second phase of the HL-  
418        LHC era, as at the start of high-luminosity operation the selected option is the hybrid one. The  
419        sensor will be bonded with ITkPix, the first full-scale 65 nm hybrid pixel-readout chip developed  
420        by the RD53 collaboration. Regarding the sensor, a valuable option is using 3D pixels, which  
421        have already proved themselves in ATLAS, for the insertable B layer (IBL).[qualcosa in più sui 3d.](#)  
422        The number of pixels will be increased of a factor about 7, passing from 92 millions to 6 billion.

#### 423        CMS

#### 424        LHCb

425        LHCb is a dedicated heavy-flavour physics experiment that exploits pp interactions at 14 TeV at  
426        LHC. It was the last experiment to upgrade the vertex detector, the Vertex Locator (VELO),  
427        replacing the silicon-strip with pixels in May 2022. As the instantaneous luminosity in Run3 is  
428        increased by a factor  $\lesssim 10$ , much of the readout electronics and of the trigger system have been  
429        developed in order to cope with the large interaction rate. To place the detector as close as possible  
430        to the beampipe and reach a better track reconstruction resolution, the VELO has a surprising  
431        feature: it can be moved. During the injection of LHC protons it is parked at 3 cm from the beams  
432        and only when the stability is reached it is brought at  $\sim 5$  mm. Radiation hardness as well as readout  
433        speed are then a priority for the detectors: that's why the collaboration opted for a hybrid system.  
434        The Velopix is made bonding sensors, each measuring  $55 \times 55$  micrometers, 200  $\mu\text{m}$ -thick to a  
435        200  $\mu\text{m}$ -thick ASIC specially developed for LHCb and coming from the Medipix family (sec. ??),  
436        which can handle hit rates up to 900 MHz per chip. Since the detector is operated under vacuum  
437        near the beam pipe, the heat removal is particularly difficult and evaporative CO<sub>2</sub> microchannel  
438        cooling are used.

---

<sup>1</sup>Run 3 start in June 2022

439    **3.1.2 A DEPFET example: Belle-II**

440    **da scrivere, Depleted P-channel FET (DEPFET)**

441    Per l'upgrade LSH2 nel 2026-7 sostituzione di VXD con VTX. VXD è costituito attualmente  
442    da PXD e dalle microtips, si sostituiranno le microstrip con un rivelatore a pixel monolitico.  
443    Grande vantaggio introdotto sarà una diminuzione dell'occupancy, molto importante se si vuole  
444    raggiungere alte luminosità. Consentirà inoltre una **più grande** reiezione del fondo; inoltre verrà  
445    introdotto nel flow del trigger l'informazione del pixel detector, cosa che non è vera adesso. Con la  
446    diminuzione del material budget si avrà un miglioramento sulla ricostruzione dei vertici che è un  
447    aspetto importante soprattutto nel caso in cui si voglia studiare decadimenti di particelle a vita  
448    media breve. The OBELIX chip, selezionato per l'upgrade, is currently under design e sarà basato  
449    su TJ-Monopix2, successore di monopix1 se non he conterrà ina memoria.

450    **3.1.3 CMOS MAPS: ALICE and STAR**

451    **ALICE**

452    ALICE (A Large Ion Collider Experiment) is a detector dedicated to heavy-ion physics and to the  
453    study of the condensed phase of the chromodynamics at the LHC. The tracking detector consists of  
454    the Inner Tracking System (ITS), the gaseous Time Projection Chamber (TPC) and the Transition  
455    Radiation Detector (TRD), and all those are embedded in a magnetic field of 0.5 T. The ITS is  
456    made by six layers of detectors, two for each type, from the interaction point outwards: Silicon  
457    Pixel Detector (SPD), Silicon Drift Detector (SDD) and Silicon Strip Detector (SSD). Contrary  
458    to the others LHC experiments, ALICE tracker in placed in a quite different environments: the  
459    expected dose is smaller by two order of magnitude and the rate of interactions is few MHz instead  
460    of 40 MHz, but the number of particles comes out of each interaction is higher (the SPS is invested  
461    by a density of particles of  $\sim 100 \text{ cm}^{-2}$ ). The reconstruction of very complicated events whit a  
462    large number of particle is a challenge, hence to segment and to minimize the amount of material,  
463    which may cause secondary interaction complicating futher the event topology, is considered a  
464    viable strategy. Thanks to the reduction of the material budget, ITS2, which uses the ALPIDE  
465    chip developed by ALICE collaboration, obtained an amazing improvement both in the position  
466    measurement and in the momentum resolution, improving the efficiency of track reconstruction  
467    for particle with very low transverse momentum (by a factor 6 at  $pT \sim 0.1 \text{ GeV}/c$ ). Further  
468    advancements in CMOS MAPS technology are being aggressively pursued for the ALICE ITS3  
469    vertex detector upgrades (foreseen around 2026-27), with the goals of further reducing the sensor  
470    thickness and improving the readout speed of the devices, while keeping power consumption at a  
471    minimum.

472

473    **STAR**

474    MIMOSA-28 devices for the first MAPS-based vertex detector: a 356 Mpixel two-layer barrel  
475    system for the STAR experiment at Brookhaven's Relativistic Heavy Ion Collide **da scrivere**

476    **3.2 Applications in imaging**

477    Historically for imaging pourpose the CCDs were the favoured device: they can be used as single  
478    photon counter or integrating and collecting the charge released by more impinging particles. The  
479    utilisation in the first case is similar to the tracking one, except that the requirements are less  
480    tight, so much that two noteworthy of microchips originally meant for detectors in particle physics  
481    at the LHC, and later employed in other fields are Medipix and Timepix. They are read-out chips  
482    developed by the Medipix Collaborations since early 1990s. For two decades, different Medipix  
483    generations have been produced, having a rough correlation with the feature size used: Medipix2  
484    (1999) used 250 nm feature size CMOS while Medipix3 (2005) 130 nm. The aim of the fourth col-  
485    laboration (2016), instead, is designing pixel read-out chips that prepared for **TSV processing and**  
486    **may be tiled on all four sides. DOVREI METTERE DUE RIGHE SU TSV OPPURE TAGLIARE.**

487    For photons imaging other materials with higher atomic charge than silicon could be prefered,  
488    as a high photon absorption efficiency is needed: it was for this reason that Medipix2 was bump  
489    bonded to identically segmented sensors of both silicon and GaAs.

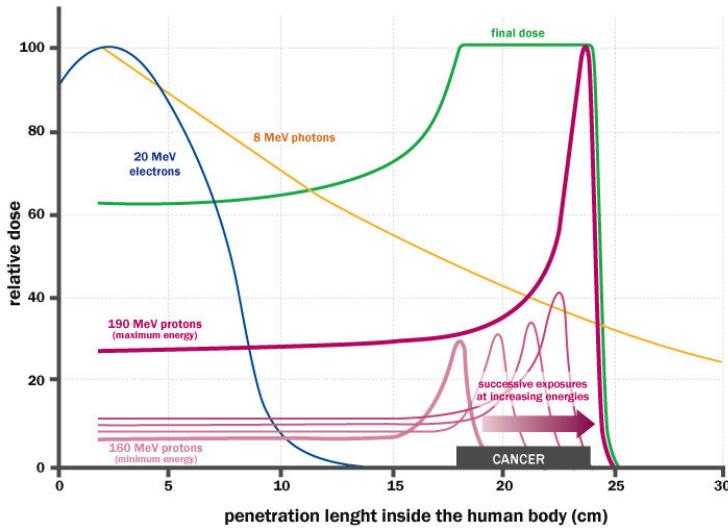


Figure 3.1: The Spread Out Bragg Peak (SOBP) curve (green), which is a constant dose distribution, is obtained from the superposition of many Bragg peak of hadrons with different energy.

The applications in scientific imaging vary from astrophysics and medical imaging to more exotic domains as studies of protein dynamics, art authentication and dosimetry. The most important employment of Medipix is as X-ray single photon counting in industrial and medical radiography and in 3D computed tomography. Thanks to a New-Zealand company, the MARS Bioimaging detector has been fabricated, which is capable of resolving the photons energy and produce 3D coloured images. Besides tracking in HEP (I have already cited the use of Timepix3 is in the beam telescope of the LHCb VELO), an important use of Timepix is in dosimetry [Timepix Detector for Imaging in Ion Beam Radiotherapy- aggiungi qualche info](#) A small-Timepix detector with the dimension of a USB can also be found at the International Space Station, where it is exploited for radiation, principally made of heavy-ion, monitoring.

### 3.2.1 Applicability to FLASH radiotherapy

The radiological treatment is a common method used in 60% of tumors both as palliative care and as treatment. It can be given before, after or during a surgery, [per cosa sta iort](#) IORT and many different types of radiations (photons, electrons, protons and ions, which mainly are hydrogen and carbon) can be used to irradiate the affected tissues. Exploiting the ionizing energy loss a biological damage can be delivered to the tissue. [nomina il LET](#). If x-ray photons, with energy in  $\sim 4\text{-}25\text{MeV}$ , are used, the ionization is caused by the Compton electrons and is more in the superficial layers of the tissue due to the exponential attenuation of the beam. The hadrons energy loss, instead, is strongly localized in the last region of the track, that is the Bragg peak. Ion beam enables better focusing of the radiation thereby improves the sparing of the surrounding healthy tissues; on the other hand the delivered dose distribution depends more on the patient's density tissues (e.g. bones, swelling, fat). [Questo significa che per non creare un danno là dove non necessario serve una buona conoscenza del percorso fatto dalle particelle](#).

The Tumor Control Probability (TCP) and the Normal Tissue Complication (NTC) functions parametrize the efficiency of damaging on the tumor after having released a certain dose and the probability of not affecting the healthy tissues respectively: the [il caso migliore è quello in cui le problematiche sorgono ad alti dosi mentre il danno è efficace subito. La zona intermedia in cui la NTC è bassa e TC è alta si chiama therapeutic window](#). Una scelta bilanciata si applica guardando a questi due fattori; si usa il therapeutic index definito come TCP/NTCP.

[Curva di efficacia del trattamento in funzione della dose: The surviving fraction probability is de](#)

$$\frac{S(D)}{S(0)} = e^{-F(D)} \quad (3.1)$$

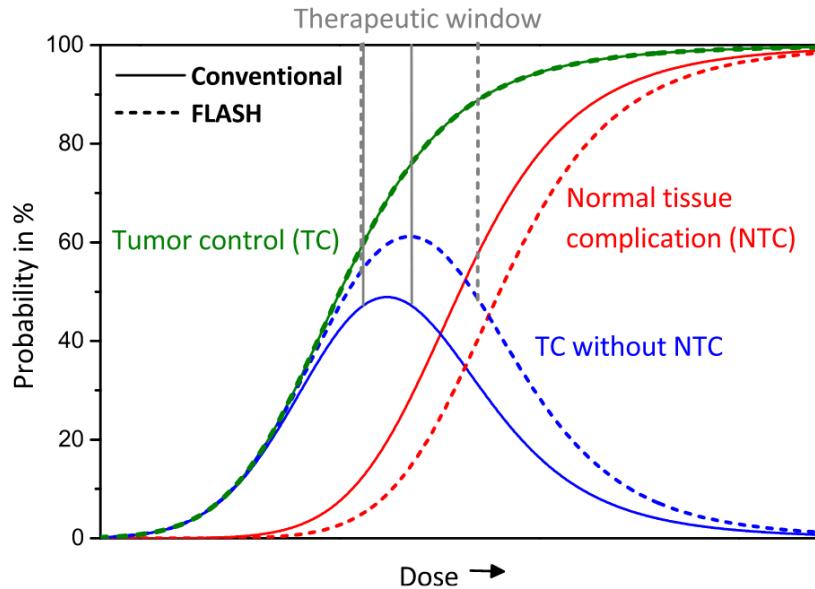


Figure 3.2: Illustration of dependence of TCP, NTCP and therapeutic window on dose, for CONV-RT ad FLASH-RT.

|           | CONV-RT | FLASH   |
|-----------|---------|---------|
| Dose rate |         | 40 Gy/s |

Table 3.1

dove  $F(D)$  è una funzione che rappresenta il danno alle cellule. Si ottiene una curva di sopravvivenza dove si vede la possibilità delle cellule di autoripararsi. A basse dosi infatti le cellule possono ripararsi.

Si è visto che in modalità flash la finestra si apre. In figure c'è per la conventional r FLASH.

CONV-RT 0.01-5 Gy/min. A typical RT regime today consists of daily fractions of 1.5 to 3 Gy given over several weeks.

Nell Intra operative radiation therapy (IORT), where they reach values respectively about 20 and 100 times greater than those of conventional radiation therapy.

FLASH vuole ultrahigh mean dose-rate (maggione di 40 Gy/s) in modo da ridurere anche il trattamento a meno di un secondo.

Ci sono due effetti che affect the flsh effect and la sua applicabilità: Dose rate effect e oxygen

- 535 • dose rate effect
- 536 • oxygen effect

Cellule che esibiscono hypoxia (cioè cellule che non hanno ossigeno sono radioresistenti); al contrario normoxia e phyoxia non lo sono. la presenza di ossigeno rende la curva steeper indicando che lo stesso danno si raggiunge a livelli di dose più bassi rispetto al caso senza ossigeno.

Typically, the OER is in the order of 2.5-3.5 for most cellular systems Quindi si vogliono sfruttare questi effetti per diminuire la tossicità sui tessuti sani

543 **Dosimetric problems**

544 I dosimetri standard finora hanno esibito problemi di saturazione: in particolare i dosimetri di  
545 riferimento per una misura di dose assoluta, cioè le camere a ionizzazione, ad alti campi elettrici  
546 mostrano sia problemi di saturazione sia di scariche. Questo doppio effetto è dato dal fatto che,  
547 creandosi tante cariche nella camera, che va ad annullare il campo elettrico di drift. Questo  
548 ovviamente paralizza le cariche che non driftano più, ma che anzi si ricombinano ed inoltre facilita  
549 la formazione di scariche.

550 Un altro grande limite delle camere a ionizzazione è la risoluzione spaziale dato ch non posson  
551 essere fatte più piccole di circa un centimetro. Questo limite è principalmente dovuto a problemi  
552 meccanici per cui non si può fare una camera con P bassa e con materiali sottili, perchè le pareti  
553 si incurvano.

554 Oltre al problema della dose assoluta (la cui misura finora viene fatta con camere a ionizzazione  
555 per legge) nell'ambito della radioterapia ad alta intensità esistono altri problemi sperimentali, quali  
556 un detector che sia in grado di monitorare la posizione e direzionalità del fascio, quindi detto in  
557 altre parole un beam monitor. Questo detector deve essere abbastanza veloce da poter fornire una  
558 risposta in real time e avere anche una buona risoluzione temporale.

559    **Chapter 4**

560    **TJ-Monopix1**

561    TJ-Monopix1 is a small electrode DMAPS with fast R/O capability, fabricated by TowerJazz  
 562    foundry in 180 nm CMOS imaging process. It is part, together with prototypes from other series  
 563    such as TJ-MALTA, of the ongoing R&D efforts aimed at developing DMAPS in commercial CMOS  
 564    processes, that could cope with the requirements at accelerator experiments. Both TJ-Monopix  
 565    and TJ-MALTA series [5], produced with the same technology by TowerJazz (the timeline of the  
 566    foundry products is shown in figure 4.1), are small electrode demonstrators and principally differ in  
 567    the readout design: while Monopix implements a column-drain R/O, an asynchronous R/O without  
 568    any distribution of BCID has been used by TJ-Malta in order to reduce power consumption.



Figure 4.1: Timeline in TowerJazz productions in 180 nm CMOS imaging process

569    Another Monopix series, but in 150 nm CMOS technology, has been produced by LFoundry [6].  
 570    The main differences between the LF-Monopix1 and the TJ-Monopix1 (summarized in table 4.2),  
 571    lay in the sensor rather than in the readout architecture, as both chips implements a fast col-  
 572    umn drain R/O with ToT capability [7][8]. Concerning the sensors, either are based on a p-type  
 573    substrate, but with slightly different resistivities; in addition LFoundry pixels are larger, thicker  
 574    and have a large fill factor (the very deep n-well covers ~55% of the pixel area). The primary  
 575    consequence is that LF-Monopix1 pixels have a higher capacity resulting in higher consumption  
 576    and noise. As I discussed in section 2.4.1, the fact that LF-Monopix has a large fill factor electrode  
 577    is expected to improve its radiation hardness. Indeed, a comparison of the performance of the  
 578    two chips showed that TJ-Monopix suffers a comparatively larger degradation of efficiency after  
 579    irradiation, due to the low electric field in the pixel corner; on the other hand, a drawback of the  
 580    large fill factor in LF-Monopix is a significant cross-talk.

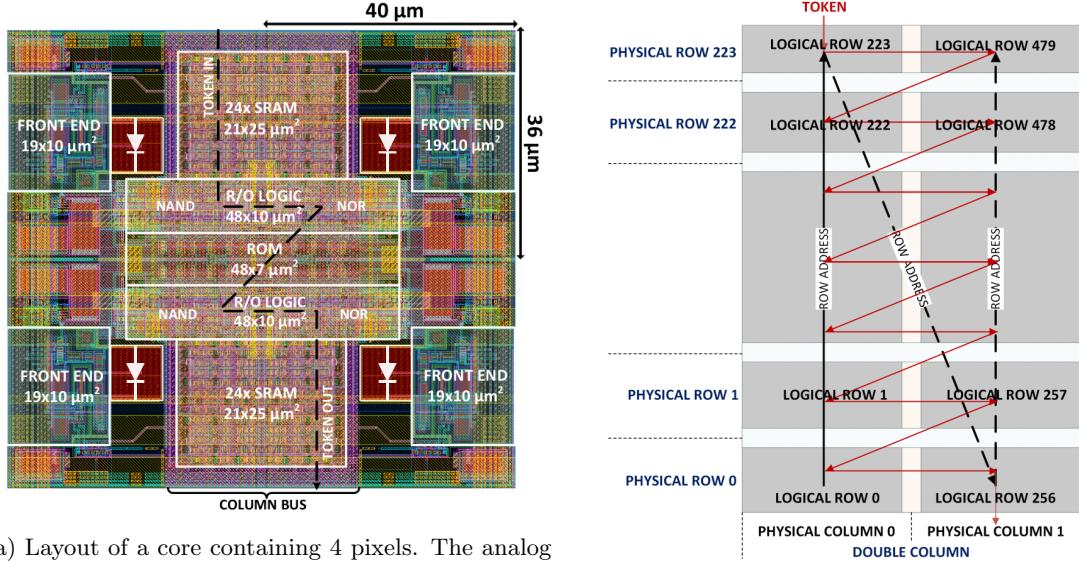
581    The TJ-Monopix1 chip contains, apart from the pixels matrix, all the required support blocks  
 582    used for configuration and testing:

- 583    • the whole matrix contains  $224 \times 448$  pixels, yielding a total active area approximately equal  
 584    to  $145 \text{ mm}^2$  over a total area of  $1 \times 2 \text{ cm}^2$ ;
- 585    • at the chip periphery are placed some 7-bit Digital to Analog Converter (DAC), used to  
 586    generate the analog bias voltage and current levels and to configure the FE;

|                    | LF-Monopix1                  | TJ-Monopix1                  |
|--------------------|------------------------------|------------------------------|
| Resistivity        | $>2\text{ k}\Omega\text{cm}$ | $>1\text{ k}\Omega\text{cm}$ |
| Pixel size         | $50 \times 250\mu\text{m}^2$ | $36 \times 40\mu\text{m}^2$  |
| Depth              | $100\text{-}750\mu\text{m}$  | $25\mu\text{m}$              |
| Capacity           | $\sim 400\text{ fF}$         | $\sim 3\text{ fF}$           |
| Preamplifier       | charge                       | voltage                      |
| Threshold trimming | on pixel (4-bit DAC)         | global threshold             |
| ToT                | 8 bits                       | 6 bits                       |
| Consumption        | $\sim 300\text{ mW/cm}^2$    | $\sim 120\text{ mW/cm}^2$    |
| Threshold          | $1500 e^-$                   | $\sim 270 e^-$               |
| ENC                | $100 e^-$                    | $\sim 30 e^-$                |

Table 4.1: Main characteristics of Monopix1 produced by TowerJazz and LFoundry [7][8]

- 587 • at the EoC is placed a serializer to transferred datas immediately, indeed no trigger memory  
 588 is implemented in this prototypes;
- 589 • the matrix power pads are distributed at the sides
- 590 • four pixels which have analog output and which can be monitored with an oscilloscope, and  
 591 therefore used for testing
- 592 Pixels are grouped in  $2 \times 2$  cores (fig. 4.2a): this layout allows to separate the analog and the  
 593 digital electronics area in order to reduce the possible interference between the two parts. In  
 594 addition it simplifies the routing of data as pixels on double column share the same column-bus to  
 595 EoC. Therefore pixels can be addressed through the physical column/row or through the logical  
 596 column/row, as shown in fig. 4.2b: in figure is also highlighted the token propagation path, whose  
 597 I will discuss later.



(a) Layout of a core containing 4 pixels. The analog FE and the digital part are separated in order to reduce cross-talk be

(b)

## 598 4.1 The sensor

599 As already anticipated, TJ-Monopix1 has a p-type epitaxial layer and a n doped small collection  
 600 electrode ( $2\mu\text{m}$  in diameter); to avoid the n-wells housing the PMOS transistors competing for the  
 601 charge collection, a deep p-well substrate, common to all the pixel FE area, is used. TJ-Monopix1  
 602 adopts the modification described in section 2.4.2 that allows to achieve a planar depletion region

| Parameter         | Value                        |
|-------------------|------------------------------|
| Matrix size       | $1 \times 2 \text{ cm}^2$    |
| Pixel size        | $36 \times 40 \mu\text{m}^2$ |
| Depth             | $25 \mu\text{m}$             |
| Electrode size    | $2 \mu\text{m}$              |
| BCID              | 40 MHz                       |
| ToT-bit           | 6                            |
| Power consumption | $\sim 120 \text{ mW/cm}^2$   |

Table 4.2

near the electrode applying a relatively small reverse bias voltage. This modification improves the efficiency of the detector, especially after irradiation, however a simulation of the electric field in the sensor, made with the software TCAD (Technology Computer Aided Design), shows that a nonuniform field is still produced in the lateral regions of the pixel compromising the efficiency at the corner. Two variations to the process have been proposed in order to further enhance the transversal component of electric field at the pixel borders: on a sample of chip, which includes the one in Pisa, a portion of low dose implant has been removed, creating a step discontinuity in the deep p-well corner (fig. 4.3); the second solution proposed[MOUSTAKAS THESYS, PAG 58] consists in adding an extra deep p-well near the pixel edge. A side effect of the alteration in the low dose implant is that the separation between the deep p-well and the p-substrate becomes weak to the point that they cannot be biased separately to prevent the punchthrough.

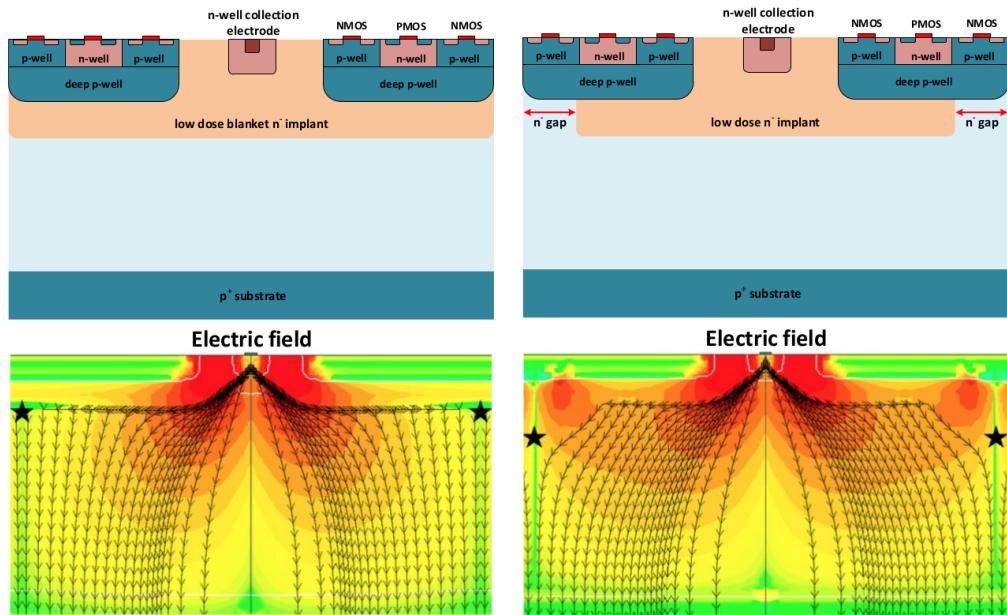


Figure 4.3: (a) The cross-section of a monolithic pixel in the TJ-Monopix with modified process; additionally in (b) a gap in the low dose implant is created to improve the collection of charge due to a bigger lateral component of the electric field. this point in figure is indicated by a star . transversal component of the electric field drops at the pixel corner

Moreover, to investigate the charge collection properties, pixels within the matrix are split between bottom top half and bottom half and feature a variation in the coverage of the deep p-well: the electronics area can be fully covered or not. In particular the pixels belonging to rows from 0 to 111 are fully covered (FDPW) and pixels belonging to rows from 112 to 223 have a reduced p-well (RDPW), resulting in a enhancement of the lateral component of the electric field.

## 619 4.2 Front end

620 The matrix is split in four sections, each one corresponding to a different flavor of the FE. The  
 621 four variation have been implemented in order to test the data-bus readout circuits and the input  
 reset modes.

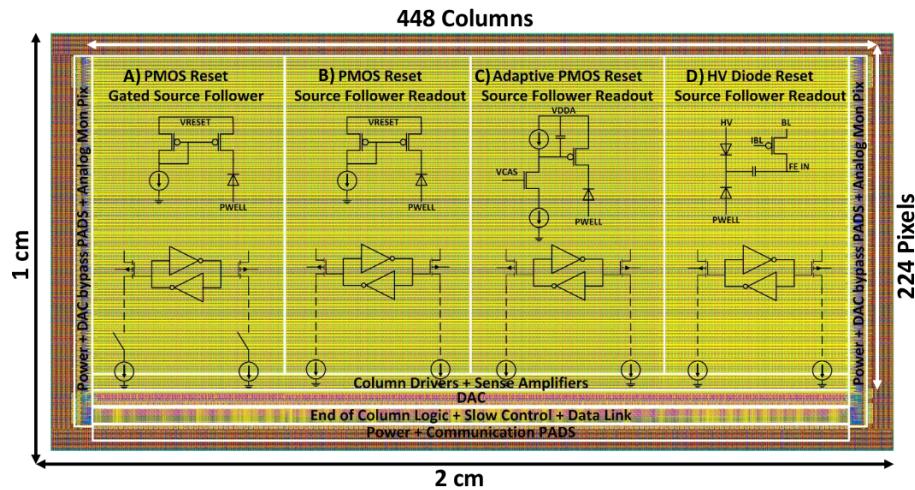


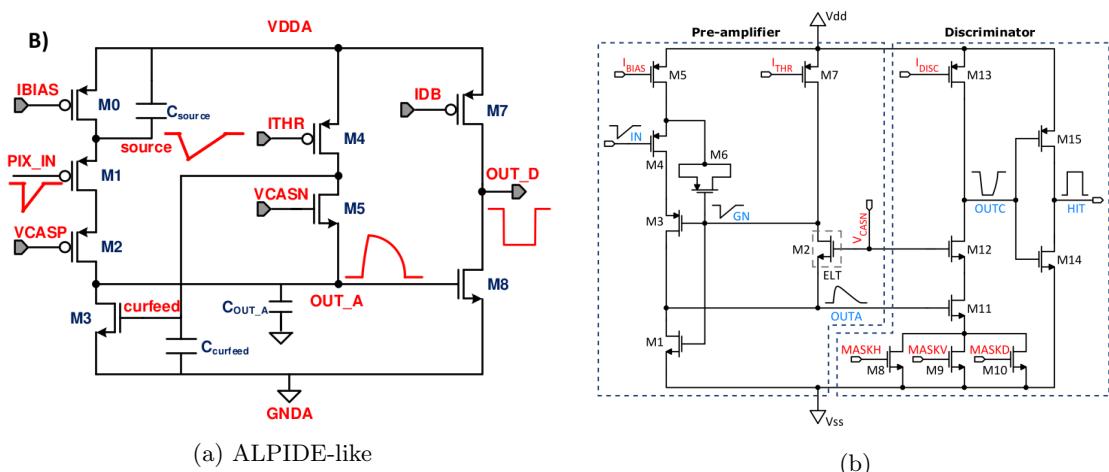
Figure 4.4

622 All the flavors implement a source-follower double-column bus readout: the standard variation  
 623 is the flavor B, that features a PMOS input reset (referred as "PMOS reset"). Flavor A is identical  
 624 to flavor B except for the realization of the source follower (it is a gated one) that aim to reduce  
 625 the power consumption. cosa significa? C instead implements a novel leakage compensation circuit.  
 626 Moreover the collection electrode in flavors A, B, C is DC-coupled to the front-end input, while  
 627 in D is AC-coupled, providing to apply a high bias voltage; for this reason flavor D is called "HV  
 628 flavor".

630 Principio generale: R resistenza di reset deve essere abbastanza grande in modo da far sì che  
 631 il ritorno allo zero è abbastanza lento (non devi "interferire" con la tot slope e non deve essere  
 632 più corto del tempo del preamplificatore, sennò hai perdita di segnale). Baseline reset: all'input  
 633 solitamente hai un PMOSS o un diodo; R reset

### 634 4.2.1 ALPIDE-like

635 ALPIDE chips, developed by the ALICE collaboration, implemented a standard FE to the point  
 636 that many CMOS MAPS detectors used a similar FE and are called "ALPIDE-like". Considering  
 637 that both TJ-Monopix1 and ARCADIA-MD1 have an ALPIDE-like FE, I am going to explain the  
 broad principles of the early FE stage. The general idea is of the amplification to transfer the



| Parameter | Meaning   |            |
|-----------|---|------------|
| IBIAS     | mainly controls the rise time                   | yes? check |
| IDB       | sets the discriminator threshold                | yes        |
| ITHR      | sets the velocity of the return to the baseline | yes        |
| ICASN     | sets the baseline of the signal                 | yes        |
| VRESET    | sets the gain of the preamplifier               | yes        |
| IRESET    | sets the gain of the preamplifier               | no         |

Table 4.3: FE parameters which must be setted through the DAQ. "Function" means that higher parameter implies higher value

639 charge from a bigger capacity[9],  $C_{source}$ , to a smaller one,  $C_{out}$ : the input transistor M1 with  
 640 current source IBIAS acts as a source follower and this forces the source of M1 to be equal to the  
 641 gate input  $\Delta V_{PIX\_IN} = Q_{IN}/C_{IN}$ .

$$Q_{source} = C_{source} \Delta V_{PIX\_IN} \quad (4.1)$$

642 The current in M2 and the charge accumulates on  $C_{out}$  is fixed by the one on  $C_{source}$ :

$$\Delta V_{OUT\_A} = \frac{Q_{source}}{C_{OUT\_A}} = \frac{C_{source} \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_{source}}{C_{OUT\_A}} \frac{Q_{IN}}{C_{IN}} \quad (4.2)$$

643 A second branch (M4, M5) is used to generate a low frequency feedback, where VCASN and ITHR  
 644 set the baseline value of the signal on  $C_{OUT\_A}$  and the velocity to goes down to the baseline.

#### IL RUOLO DI CURVFEED NON L'HO CAPITO.

645 Finally IDB defines the charge threshold with which the signal  $OUT\_A$  must be compared: de-  
 646 pending on if the signal is higher than the threshold or not, the  $OUT\_D$  is high or low respectively.

647 The actual circuit implemented in TJ-Monopix1 is shown in figure 4.5b: the principal difference  
 648 lays in the addition of disableing pixels' readout. This possibility is uttermost important in order to  
 649 reduce the hit rate and to avoid saturating the bandwidth due to the noisy pixels, which typically  
 650 are those with manufacturing defects. In the circuit transistors M8, M9 and M10 have the function  
 651 of disabling registers with coordinates MASKH, MASKV and MASKD (respectively vertical, ori-  
 652 ental and diagonal) from readout: if all three transistors-signals are low, the pixel's discriminator  
 653 is disabled. Compared with a configurable masking register which would allow disableing pixels  
 654 individually, to use a triple redundancy reduces the sensistivity to SEU but also gives amount of  
 655 intentionally masked ("ghost") pixels. This approach is suitable only for extremely small number  
 656 N of pixel has to be masked: if two coordinate projection scheme had been implemented, the  
 657 N's number of ghost pixels would have scale with  $N^2$ , if instead three coordinates are used, the N's  
 658 exponential is lower than 2 (fig. 4.6)

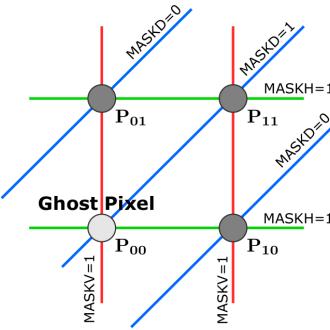


Figure 4.6

659

### 4.3 Readout logic

660 TJ-Monopix1 has a triggerless, fast and with ToT capability R/O which is based on a column-drain  
 661 architecture. On the pixel are located two Random Access Memory (RAM) cells to store the 6-bit

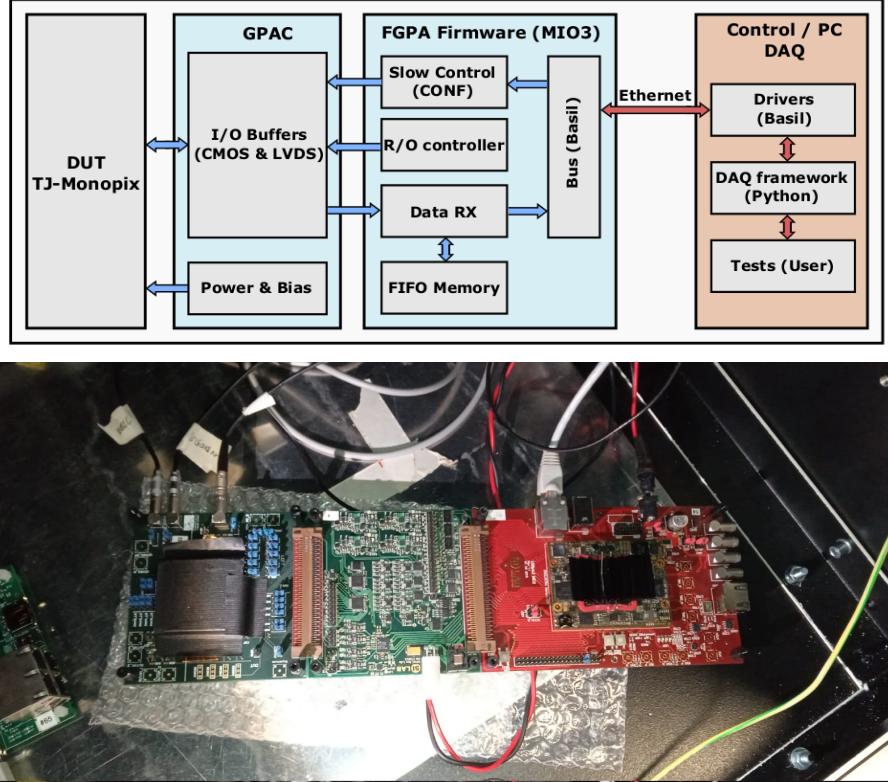


Figure 4.7: Main caption

663 LE and 6-bit TE of the pulse, and a Read-Only Memory (ROM) containing the 9-bit pixel address.  
 664 Excluded these memories, TJ-Monopix1 hasn't any other buffer: if a hit arrives while the pixel is  
 665 already storing a previous one, the new data get lost. After being read, the data packet is sent to  
 666 the EoC periphery of the matrix, where a serializer transfers it off-chip to an FPGA (4.7). There  
 667 a FIFO is used to temporarily stored the data, which is transmitted to a computer through an  
 668 ethernet cable in a later time.

669 The access to the pixels' memory and the transmission of the data to the EoC, following  
 670 a priority chain, is managed by control signals and is based on a Finite State Machine (FSM)  
 671 composed by four state: no-operation (NOP), freeze (FRZ), read (RD) and data transfer (DTA).  
 672 The readout sequence (??) starts with the TE of a pulse: the pixel immediately tries to grab the  
 673 column-bus turning up a hit flag signal called *token*. The token is used to control the priority chain  
 674 and propagates across the column indicating what pixel that must be read. To start the readout  
 675 and avoid that the arrival of new hits disrupt the priority logic, a *freeze* signal is activated, and  
 676 then a *read* signal controls the readout and the access to memory. During the freeze, the state of  
 677 the token for all pixels on the matrix remains settled: this does not forbid new hits on other pixels  
 678 from being recorded, but forbids pixels hit from turning on the token until the freeze is ended. The  
 679 freeze stays on until the token covers the whole priority chain and gets the EoC: during that time  
 680 new token cannot be turned on, and all hits arrived during a freeze will turn on their token at the  
 681 end of the previous freeze. Since the start of the token is used to assign a timestamp to the hit,  
 682 the token time has a direct impact on the time resolution measurement; this could be a problem  
 683 coping with high hits rate.

684 The analog FE circuit and the pixel control logic are connected by an edge detector which is  
 685 used to determine the LE and the TE of the hit pulse(fig. 4.9): when the TE is stored in the first  
 686 latch the edge detector is disabled and, if the **FREEZE** signal is not set yet, the readout starts. At  
 687 this point the HIT flag is set in a second latch and a token signal is produced and depending on  
 688 the value of **Token in** the pixel can be read or must wait until the **Token in** is off. In figure an OR  
 689 is used to manage the token propagation, but since a native OR logic port cannot be implemented  
 690 with CMOS logic, a sum of a NOR and of an inverter is actually used; this construct significantly  
 691 increases the propagation delay (the timing dispersion along a column of 0.1-0.2 ns) of the token

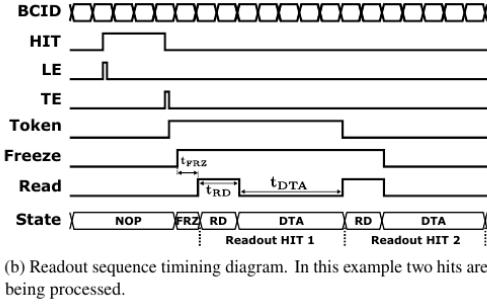


Figure 4.8: Readout timing diagram: in this example two hits are being processed

and to speed up the circuit optimized solution are often implemented. When the pixel become the next to be read in the queue, and at the rising edge of the **READ** signal, the state of the pixel is stored in a D-latch and the pixel is allowed to use the data bus; the TE and the HIT flag latches are reset and a **READINT** signal that enable access of the RAM and ROM cells is produced.

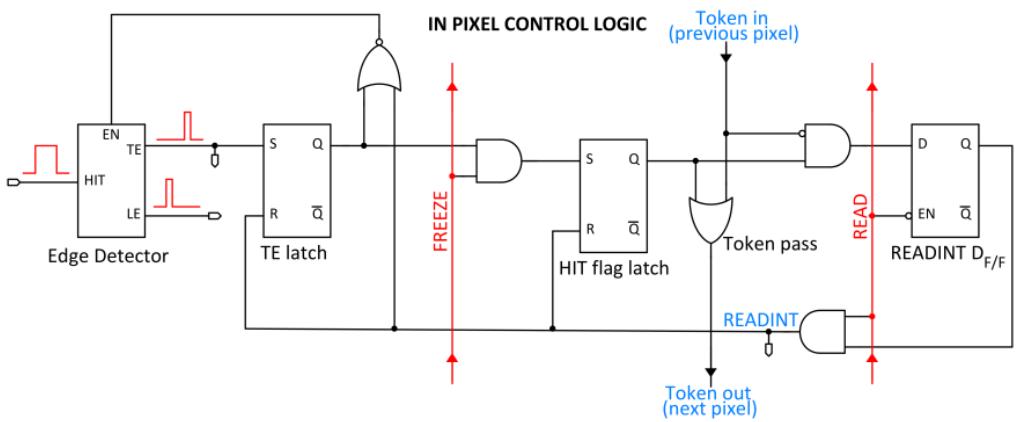


Figure 4.9

The final data must provide all the hits' information: the pixel address, the ToT and the timestamp. All those parts are assigned and appended at different time during the R/O chain:

- **Pixel address:** while the double column address (6-bit) is appended by the EoC circuit, the row address (8-bits for each flavor) and the physical column in the doublet (1-bit) are assigned by the in-pixel logic
- **ToT:** is obtained offline from the difference of 6-bits TE and 6-bits LE, stored by the edge detector in-pixel; since a 40 MHz BCID is distributed across the matrix, the ToT value is range 0-64 clock cycle which corresponds to 0-1.6  $\mu$ s
- **Timestamp:** The timestamp of the hit correspond to the time when the pixel set up the token; it is assigned by the FPGA, that uses the LE, TE and a 640 MHz clock to derive it. For all those hits which arrived while the matrix is frozen, the timestamp is no more correlated with the time of arrival of the particle

When the bits are joined up together the complete hit data packet is 27-bit.

### 4.3.1 Dead time measurements

The hit loss is due to analog and digital pile up: the first one occurs when a new hit arrives during the pre-amplifier response, the second instead, which is the more relevant contribution with high rate, while the information of the previous hit has not yet been transferred to the periphery. As only one hit at a time can be stored on the pixel's RAM, until the data have completed the path to get out, the pixel is paralyzed and the dead time  $\tau$  almost corresponds with the time needed

| Parameter    | Value [DAC] | Value [ $\mu\text{s}$ ] |
|--------------|-------------|-------------------------|
| START_FREEZE | 64          | 1.6                     |
| STOP_FREEZE  | 100         | 2.5                     |
| START_READ   | 66          | 1.65                    |
| STOP_READ    | 68          | 1.7                     |

Table 4.4: Default configuration of the R/O parameters

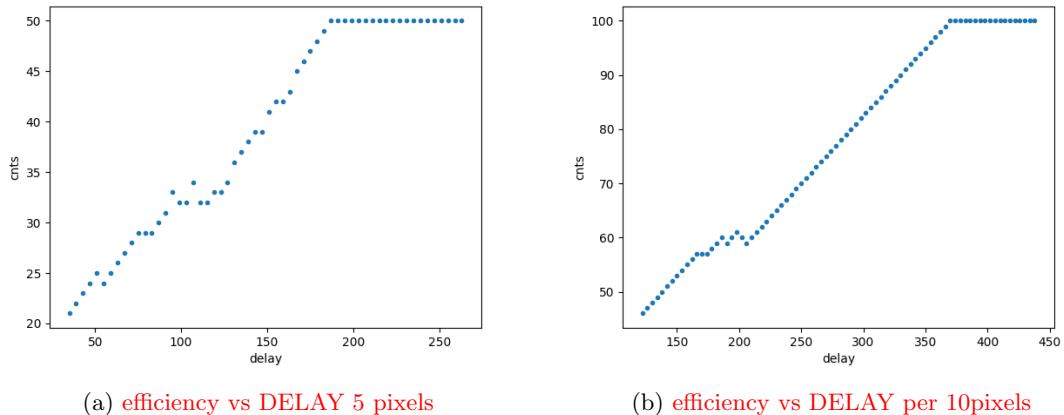
716 to trasmit the data-packets off-chip. Since the exportation of data from pixel to the EoC occurs  
 717 via a 21-bits data bus, only one clock cycle is need to transfer the data to the end of column and  
 718 the dead time bottleneck is given by the bandwidth of the serializer at the EoC. In our setup the  
 719 serializer operates at 40 MHz, thus to transmit a data packet (27-bit considering the addition at  
 720 the EoC) at least 675 ns are needed. For what we have said so far, the R/O is completely sequential  
 721 and therefore is expected a linear dependence of the reading time on the number of pixels to read:

$$\tau = 25 \text{ ns} \times (\alpha N + \beta) \quad (4.3)$$

722 where  $\alpha$  and  $\beta$  are parameters dependent on the readout chain setting.

723 To measure and test the linearity of the reading time with the number of pixels firing, I have  
 724 used the injection mode available on the chip. Indeed, the injection mode allows fixing not only  
 725 the amplitude of the pulse, which corresponds to the charge in DAC units, but also the period and  
 726 the width. I have injected a fix number of pulses (100) and looked for the rate when the efficiency  
 727 decreases. Moreover to test that there is no dependece of the digital readout time from the charge  
 728 of the pulse, I have try to change the amplitude of the pulse injected, but the parameters found  
 729 were consistent with the default configuration ones.

730 Al posto degli esempi con 5 e 10 pixels metterei un esempio dell'efficienza vs il periodo quando  
 731 leggo un singolo pixel. Una cosa che volevo fare era anche provare a fissare la slope con cui  
 l'efficienza scende: se la slope è uguale per tutti il readout diventa completamente predittivo.



(a) efficiency vs DELAY 5 pixels

(b) efficiency vs DELAY per 10pixels

732 While the single pixel reading time and the dead time do not depend on the position on the  
 733 pixel matrix and are equal to 106 (46+60) clock counts within 1 clock count, on the other hand the  
 734  $\tau$  depends on the pixel position on the matrix when more than one pixel are firing. In particular  
 735 the priority chain goes from row 224 to row 0, and from col 0 to 112, that means the last pixels to  
 736 be read is the one on le bottom right corner of the matrix.

737 In figure 4.12 is reported the reading time versus the number of pixels injected; the R/O  
 738 parameters that control the reading time and their default values are reported on table ??.

739 The factor  $\alpha$ , referring to eq. 4.3 is proportional to the difference (STOP\_FREEZE - START\_READ),  
 740 while the offset  $\beta$  lies between 5 and 15 clock counts. Since through the injection a random hit rate  
 741 on the matrix can't be simulated, as the coordinates of the pixels to inject must be specified, for  
 742 convenience I used the pixels on the same column/row. No difference in the  $\alpha$  and  $\beta$  coefficients  
 743 has been observed between the two case.

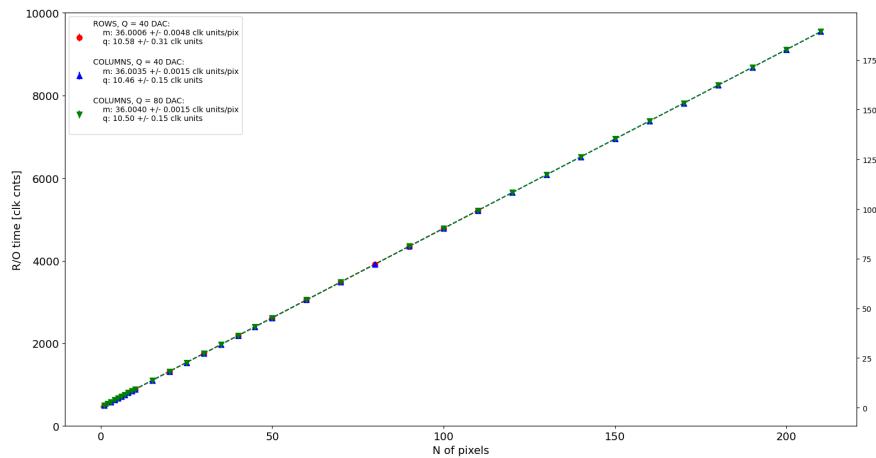


Figure 4.11

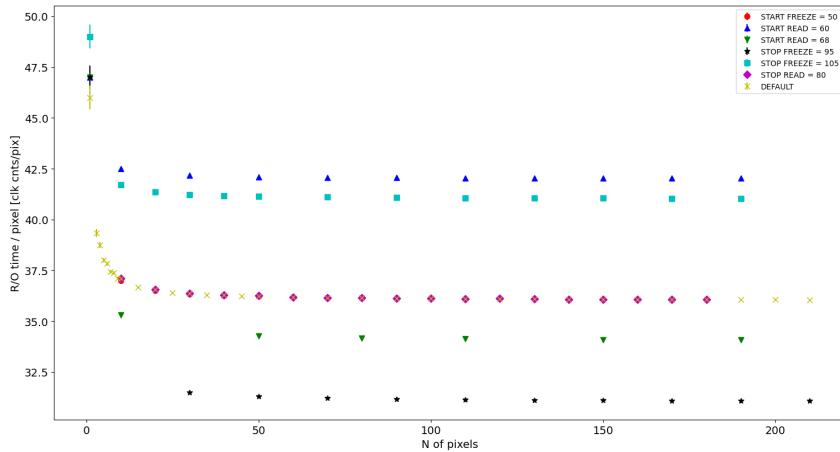


Figure 4.12

745 Ci sarebbe da spiegare perchè i parametri che usiamo noi come default non sono quelli che  
 746 minimizzano il tempo di lettura. La spiegazione è che "Abbiamo copiato i valori dal repository  
 747 di quelli di Bonn". Un'altra domanda potrebbe essere: come mai non ho esplorato una zona più  
 748 vasta per i parametri del R/O. Cambiando molto i parametri del R/O la lettura non funzionava  
 749 per niente: ad esempio CONF\_STOP\_FREEZE non può essere impostato nè sopra 105 nè sotto 95

## 750 4.4 Measurements with radioactive sources

751 CI metterei i plot con ferro, stronzio e cosmici Istogrammi, cluster distribution e definizione di  
 752 cluster, coincidenze casuali con rumore.

# 753 Chapter 5

## 754 Arcadia-MD1

755 [10] [11]

756 Breve introduzione analoga a Monopix1 in cui descrivo brevemente la "timeline" da SEED  
757 Matisse a Md1 e Md2

### 758 5.1 The sensor

759 ARCADIA-MD1 is an LFoundry chip which implements the technology 110 nm CMOSS node  
760 with six metal layer ???. The standard p-type substrate was replaced with an n-type floating zone  
761 material, that is a tecnique to produce purified silicon crystal. (pag 299 K.W.).

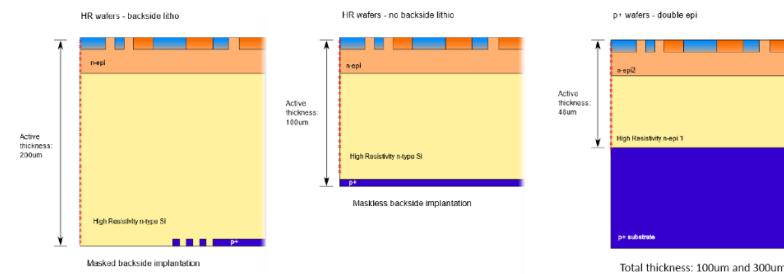


Figure 5.1

762  
763 Wafer thinning and backside litography were necessary to introduce a junction at the bottom  
764 surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side.  
765 C'è un deep pwell per - priority chainseparare l'elettronica dal sensore; per controllare il punchthrough  
766 è stato aggiunto un n doped epitaxial layer having a resistivity lower than the substrate.

767 RILEGGI SUL KOLANOSKY COS'È IL PUNCHTHROUGHT, FLOAT ZONE MATERIAL,  
768 COME VENGONO FATTI I MAPS COME FAI LE GIUNZIONI

769 It is part of the cathegory of DMAPS Small electrode to enhance the signal to noise ratio.  
770 It is operated in full depletion with fast charge collection by drift.

771 Prima SEED si occupa di studiare le prestazioni: oncept study with small-scale test struc-  
772 ture (SEED), dopo arcadia: technology demonstration with large area sensors Small scale demo  
773 SEED(sensor with embedded electronic developement) Quanto spazio dato all'elettronica sopra il  
774 pwell e quanto al diodo. ..

### 775 5.2 Readout logic and data structure

#### 776 5.2.1 Matrix division and data-packets

777 The matrix is divided into an internal physical and logical hierarchy: The 512 columns are divided  
778 in 16 section: each section has different voltage-bias + serializzatori. Each section is devided in

779 cores () in modo che in ogni doppia colonna ci siano 1Pacchetto dei dati 6 cores. ricordati dei serializzaatori: sono 16 ma possono essere ridotti ad uno in modalità spazio

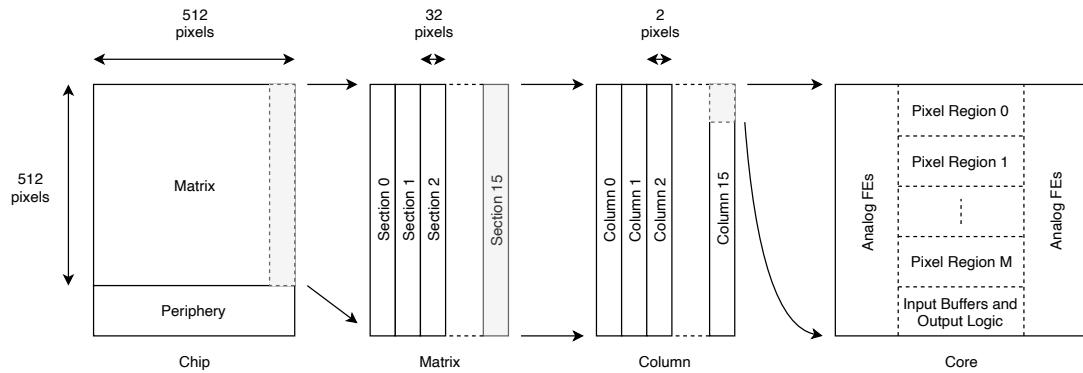


Figure 5.2

780

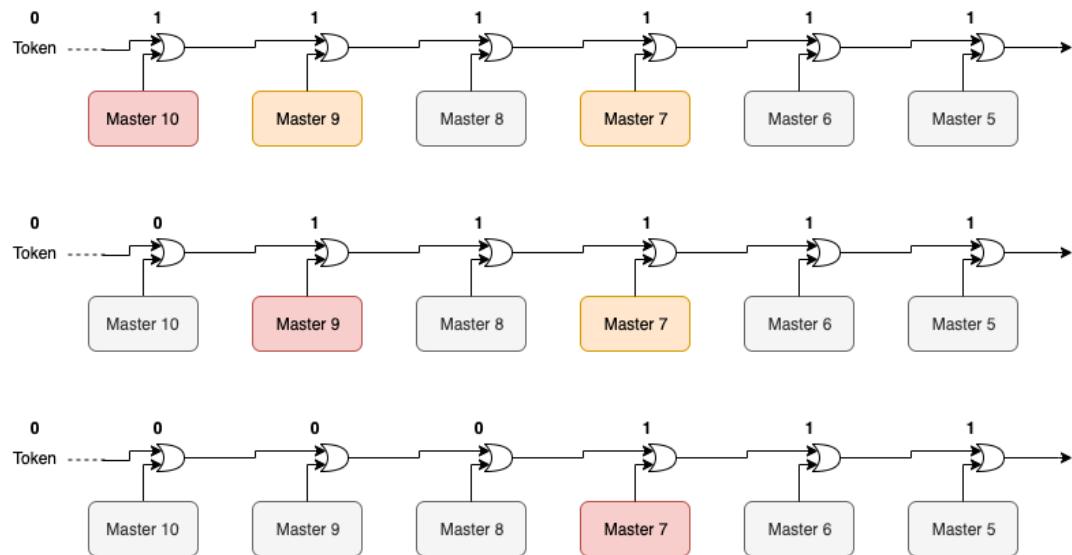


Figure 5.3

781 Questa divisione si rispecchia in come sono fatti i dati: scrivi da quanti bit un dato è fatto e le  
782 varie coordinate che ci si trovano dentro; devi dire che c'è un pixel hot e spieghi dopo a cosa serve,  
783 e devi accennare al timestamp

784 "A core is simply the smallest stepped and repeated instance of digital circuitry. A relatively  
785 large core allows one to take full advantage of digital synthesis tools to implement complex func-  
786 tionality in the pixel matrix, sharing resources among many pixels as needed.". pagina 28 della  
787 review.

788

789 TABELLA: con la gerarchia del chip Matrix (512x512 pixels) Section (512x32 pixels) Column  
790 (512x2) Core (32x2) Region (4x2)

791 Nel chip trovi diverse padframe: cosa c'è nelle padframe e End of section.

792 "DC-balance avoids low frequencies by guaranteeing at least one transition every n bits; for  
793 example 8b10b encoding n =5"

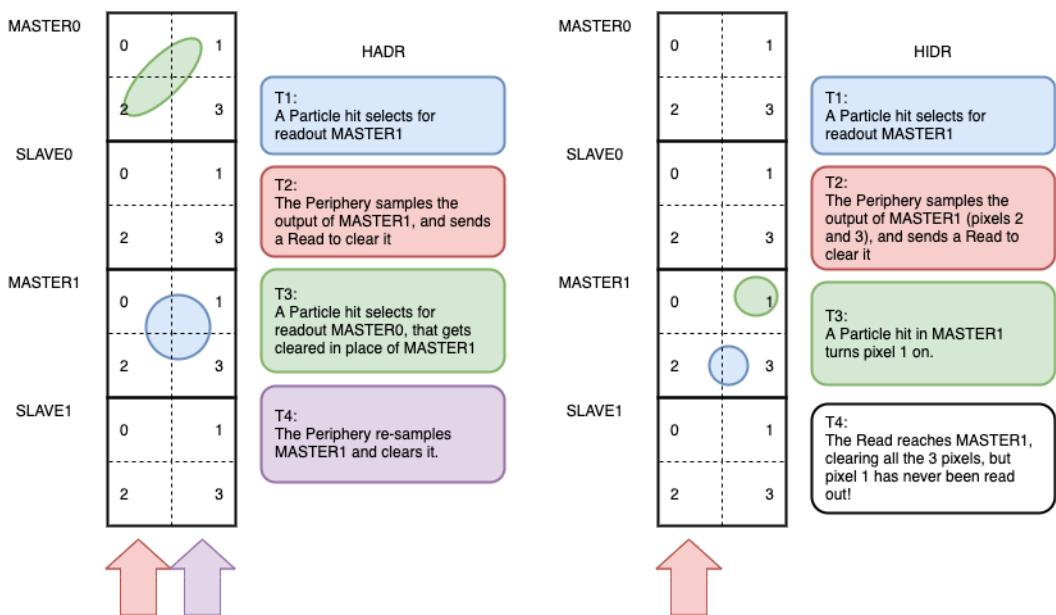


Figure 5.4

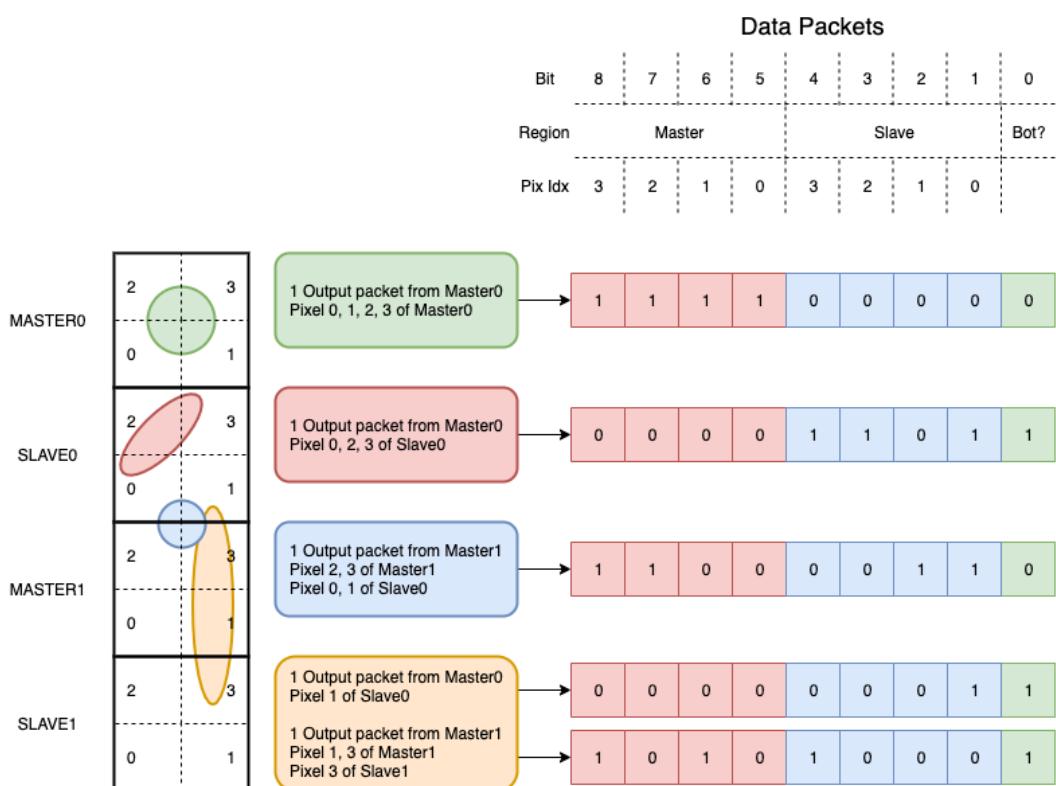


Figure 5.5

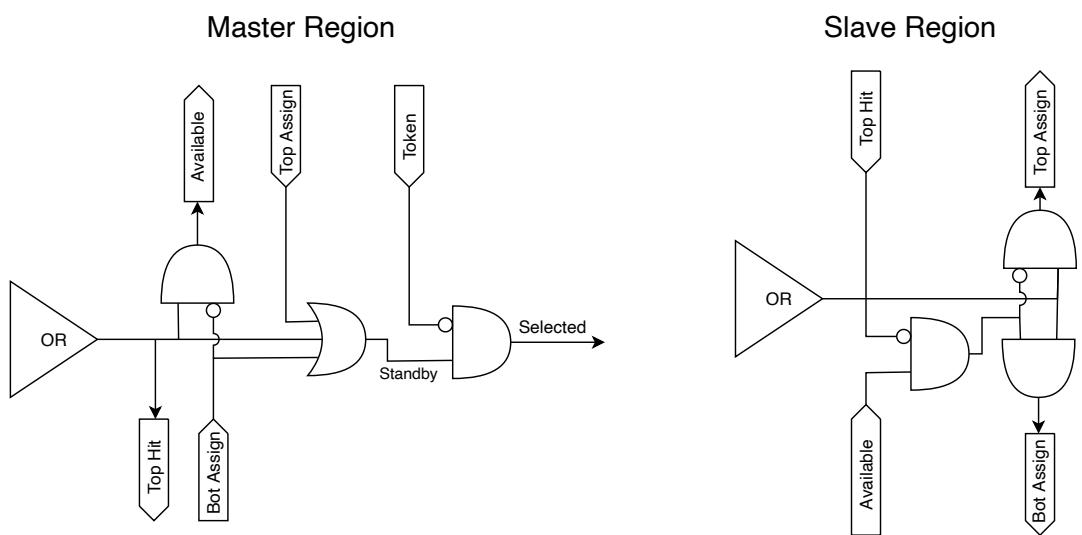


Figure 5.6

794 **Chapter 6**

795 **Threshold and noise  
characterization**

797 **6.1 Threshold and noise: figure of merit for pixel detectors**

798 IN QUESTO CAPITOLO HO MESSO SOLO APPUNTI SPARSI DA RIORGANIZZARE, E  
799 DEVO AGGIUNGERE POI I PLOT DI MONOPIX1

800 The signal to threshold ratio is the figure of merit for pixel detectors.

801  
802 la soglia deve essere abb alta da tagliare il rumore ma abb bassa da non perdere efficienza.  
803 Invece di prendere il rapporto segnale rumore prendi il rapporto segnale soglia. Perchè? la soglia  
804 è collegato al rumore, nel senso che: supponiamo di volere un occupancy di 10-4 allora sceglierò la  
805 soglia in base a questo. (plot su quaderno) Da questo conto trovo la minima soglia mettibile  
806 In realtà quello che faccio è mettere una soglia un po' più grande perchè il rate di rumore dipende  
807 da molti fattori quali la temperatura, l annealing ecc, e non voglio che cambiando leggermente uno  
808 di questi parametri vedo alzarsi molto il rate di rumore. In realtà non è solo il rumore sensibile a  
809 diversi fattori, ma anche la soglia: ad esempio la cosa classica è la variabilità della soglia da pixel  
810 a pixel.

811 In questo modo rumore e soglia diventano parenti.

812 Review pag 26.

813 Questo implica tra le altre cose che voglio poter assegnare delle soglie diverse a diversi pixel:  
814 Drawback è dare spazio per registri e quantaltro.  
815 Questo lascia però ancora aperto il problema temporale delle variazioni del rumore: problema per  
816 cui diventano necessarie le misure dei sensori dopo l'irraggiamento.

817  
818 Non fare trimming sulla soglia è uno dei problemi che si sono sempre incontrati: a casusa dei  
819 mismatch dei transistor le soglie efficaci pixel per pixel cambiano tanto. La larghezza della s curve  
820 è il noise se assumi che il noise è gaussiano

821 Il trimming della soglia avviene con dei DAC: la dispersione della soglia dopo al tuning e dovuta  
822 al dac è:

$$\sigma_{THR,tuned} = \frac{\sigma_{THR}}{2^{nbit}} \quad (6.1)$$

823 dove il numero di bit cambia varia tra 3-7 tipicamente. Monopix è 7 Arcadia 6

824  
825 Each ROIC is different in this respect, but in general the minimum stable threshold was around  
826 2500 electrons (e) in 1st generation ROICs, whereas it will be around 500 e for the 3rd generation.  
827 This reduction has been deliberate: required by decreasing input signal values. Large pixels (2 104  
828 um<sup>2</sup>), thick sensors (maggiore di 200 um), and moderate sensor radiation damage for 1st generation  
829 detectors translated into expected signals of order 10 ke, while small pixels (0.25 104 um<sup>2</sup>), thinner  
830 sensors (100 um), and heavier sensor radiation damage will lead to signals as low as 2 ke at the  
831 HL-LHC

832 The ENC can be directly calculated by the Cumulative Distribution Function (CDF) (scurve)  
833 obtained from the discriminator "hit" pulse response to multiple charge injections

834 **6.2 TJ-Monopix1 characterization**

835 **6.2.1 Threshold and noise dispersion**

836 Un plot con s curve e residui (perchè dovrebbe essere migliore il modello con doppia retta? sul  
837 RD53 c'era scritto, trovalo e leggilo) Istogrammi e colormap

838

839 **6.2.2 Absolute calibration of ToT**

840 Misure con il ferro. Metti un plot di singolo pixel dello spettro del ferro fittato con CB. Perchè  
841 CB? rimuovere i cluster comunque lasciava una coda abbastanza grande a sx e fissare con una  
842 gaussiana comunque non dava risultati migliori.

843 **6.3 ARCADIA-MD1 characterization**

844 **Chapter 7**

845 **Test beam measurements**

846 **7.1 Testbeam motivation**

847 Possibilità di integrare carica sul pixel: due elettroni consecutivi su un pixel ogni quanto arrivano?

848 Vogliamo sfruttare l'analog pile up, per fare questo dobbiamo fare attenzione a non finire nel  
849 digital pile up Devi avere che il tot dell'elettrone (cioè MIP) è maggiore del deltat medio; in questo  
850 caso potresti riuscire ad integrare carica.

851 **7.2 Apparatus description**

852 L'acceleratore utilizzato è un acceleratore per ricerca sulla flash di fisica medica. È l'unico al mondo  
853 che permette di raggiungere alti dosaggi mantenendo l'indipendenza dei parametri del fascio. La  
854 struttura del fascio e le varie quantità che si usano per descriverlo sono riportate in figure 7.1.

$$R[\text{Hz}/\text{cm}^2] = \frac{DPP[\text{Gy}]}{1.6 \cdot 10^{10} S[\text{g}/\text{cm}^2]} \quad (7.1)$$

855 where S is the stopping power in water,  $2.17 \text{ g/cm}^2$

**Table 1.** Terminology used throughout the text.

| Term                       | Symbol      | Description   |
|----------------------------|-------------|---|
| intra-pulse dose-rate      | —           | The duration of a single pulse. <sup>a</sup>  |
|                            | $\bar{D}$   | Mean dose-rate for a multi-pulse delivery.  |
| pulse repetition frequency | $\dot{D}_p$ | Dose-rate in a single pulse. <sup>a</sup>   |
|                            | DPP         | Dose in a single pulse. <sup>a</sup>  |
|                            | PRF         | Number of pulses delivered per unit time. <sup>a</sup>  |
|                            | $t_i$       | Total irradiation time from the beginning of the first delivered pulse to the end of the last delivered pulse.  |
| ultrahigh dose-rate        | —           | Radiation delivered with mean dose-rate of $> \sim 40 \text{ Gy s}^{-1}$ .  |
|                            | —           | Ultrahigh dose-rate RT that presents decreased damage to normal tissues compared to RT delivered with conventional dose-rate of $\sim 0.04 \text{ Gy s}^{-1}$ . |

<sup>a</sup>Pulses are considered to be macro-pulses unless otherwise stated (see also figure 1).

<sup>b</sup>In literature sometimes referred to as the instantaneous dose-rate.

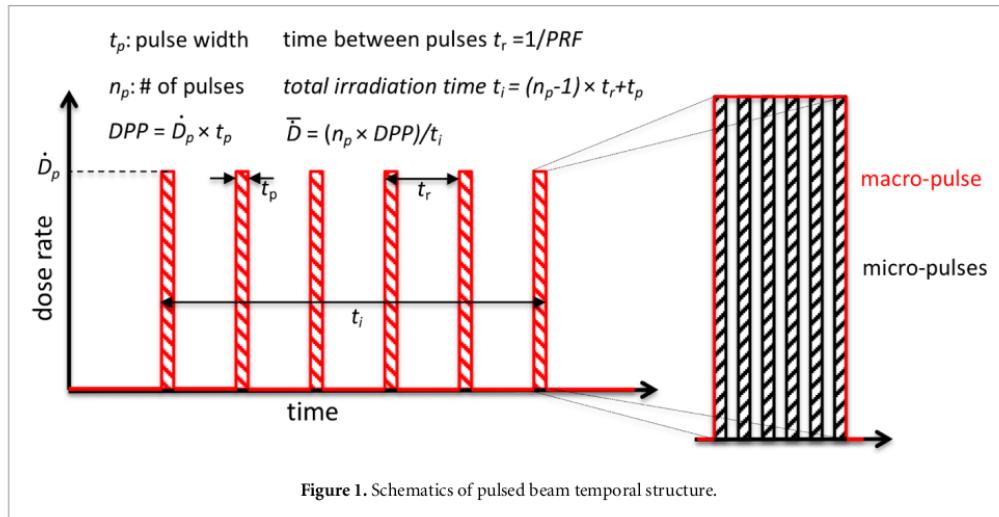


Figure 7.1

## 856 Appendix A

# 857 Pixels detector: a brief overview

### 858 A.1 Radiation damages

859 Radiation hardness is a fundamental requirement for pixels detector especially in HEP since they  
 860 are almost always installed near the interaction point where there is a high energy level of radiation.  
 861 At LHC the  $\phi_{eq}$  per year in the innermost pixel detector is  $10^{14} n_{eq}/cm^2$ ; this number reduces by  
 862 an order passing to the outer tracker layer [2] pag 341 Wermes. Here the high fluence of particles  
 863 can cause a damage both in the substrate of the detector and in the superficial electronics.

864 The first one has a principal non ionizing nature, due to a non ionizing energy loss (NIEL), but  
 865 it is related with the dislocation of the lattice caused by the collision with nuclei; by this fact the  
 866 NIEL hypothesis states that the substrate damage is normalized to the damage caused by 1 MeV  
 867 neutrons. Differently, surface damages are principally due to ionizing energy loss.

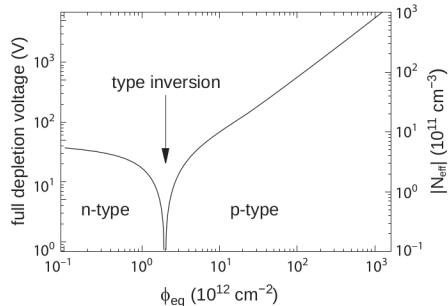
868 **DUE PAROLE IN PIÙ SUL SURFACE DAMAGE** A charge accumulation in oxide ( $SiO_2$ ) can  
 869 cause the generation of parasitic current with an obvious increase of the 1/f noise. Surface damages  
 870 are mostly less relevant than the previous one, since with the development of microelectronics and  
 871 with the miniaturization of components (in electronic industry 6-7 nm transistors are already used,  
 872 while for MAPS the dimensions of components is around 180 nm) the quantity of oxide in circuit  
 873 is reduced.

874 Let's spend instead two more other words on the more-relevant substrate damages: the general  
 875 result of high radiation level is the creation of new energy levels within the silicon band gap and  
 876 depending on their energy-location their effect can be different, as described in the Shockley-Read-  
 877 Hall (SRH) statistical model. The three main consequence of radiation damages are the changing  
 878 of the effect doping concentration, the leakage current and the increasing of trapping probability.

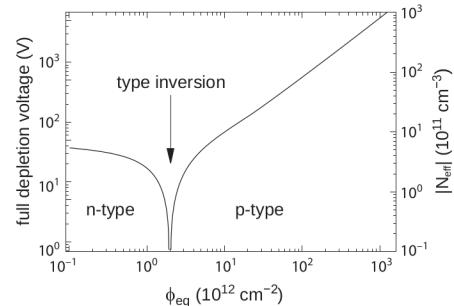
879 **Changing of the effective doping concentration:** is associated with the creation/removal  
 880 of donors and acceptors center which trap respectively electrons/holes from the conduction band  
 881 and cause a change in effective space charge density. Even an inversion (p-type becomes n-type<sup>1</sup>)  
 882 can happen: indeed it is quite common at not too high fluences ( $\phi_{eq} 10^{12-13} n_{eq} cm^{-2}$ ). A changing  
 883 in the doping concentration requires an adjustment of the biasing of the sensor during its lifetime  
 884 (eq.2.1) and sometimes can be difficult keeping to fully deplete the bulk.

---

<sup>1</sup>L'INVERSIONE OPPOSTA NON CE L'HA PERCHÈ?



(a) 1a



(b) 1b

885       **Leakage current:** is associated with the generation-recombination centers. It has a strong  
886 dependence with the temperature ( $I_{leak} \propto T^2$ ), whose solution is therefore to operate at lower  
887 temperature.

888       **Increase of trapping probability:** since the trapping probability is constant in the depleted  
889 region, the collected charge decreases exponentially with the drift path. The exponential coefficient,  
890 that is the mean trapping path, decreases after irradiation and typical values are 125-250  $\mu m$  and  
891 must be compared with the thickness of the depleted region which () corresponds to the mean drift  
892 path.

893       Different choices for substrate resistivity, for junctions type and for detector design are typically  
894 made to fight radiation issues. Some material with high oxygen concentration (as crystal produced  
895 using Czochralki (Cz) or float-zone (Fz) process (**CONTROLLA LA DIFFERENZA TRA I DUE**))  
896 for example, show a compensation effect for radiation damage; another example is the usage of  
897 n+ -in-p/n sensors (even if p+ -in-n sensors are easier and cheaper to obtain) to get advantage  
898 of inversion/to have not the inversion (since they are already p-type). After inversion the n+p  
899 boundary, coming from n+ in-n, but to keep using the sensor the depletion zone still must be  
900 placed near the diode.

901       Single Event Upset, in sostanza è quando un bit ti cambia valore (da 0 a 1 o viceversa) perché  
902 una particella deposita carica nell'elettronica che fa da memoria registro/RAM/.... Questo tipo  
903 di elettronica ha bisogno di un sacco di carica prima che il bit si "flippi" (cambi valore), infatti  
904 tipicamente per avere un SEU non basta una MIP che attraversa esattamente quel pezzo di chip  
905 in cui è implementata la memoria, ma un adrone che faccia interazione nucleare producendo più  
906 carica di quanto farebbe una MIP. Questo metodo pur essendo più comodo richiede less amount of  
907 area ha però come drawback che il registro può essere soggetto a SEU problema non trascurabile  
908 in acceleratori come HL-LHC adronici

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