Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, May 23, 14:00

Student ID:

Student Name:

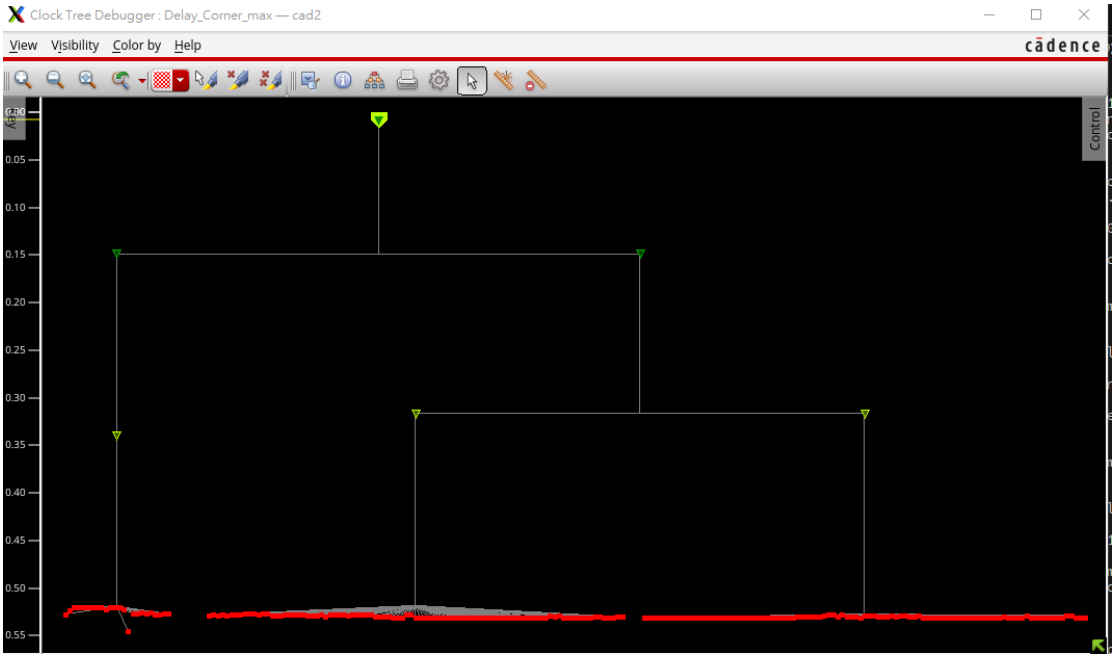
APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	400980.20
	Core Area (um^2)	223567.95
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	10ns
Follow your design in HW3? (If not, write down the student ID of the designer)		YES

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (10%).



2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
*** Starting Verify DRC (MEM: 1968.4) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 160.480 160.480} 1 of 16
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 0.000 320.960 160.480} 2 of 16
 VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 0.000 481.440 160.480} 3 of 16
 VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 0.000 633.420 160.480} 4 of 16
 VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 160.480 160.480 320.960} 5 of 16
 VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 160.480 320.960 320.960} 6 of 16
 VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 160.480 481.440 320.960} 7 of 16
 VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 160.480 633.420 320.960} 8 of 16
 VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 320.960 160.480 481.440} 9 of 16
 VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 320.960 320.960 481.440} 10 of 16
 VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 320.960 481.440 481.440} 11 of 16
 VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 320.960 633.420 481.440} 12 of 16
 VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 481.440 160.480 633.040} 13 of 16
 VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 481.440 320.960 633.040} 14 of 16
 VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 481.440 481.440 633.040} 15 of 16
 VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 481.440 633.420 633.040} 16 of 16
 VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.7  ELAPSED TIME: 0.00  MEM: 260.1M) ***
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed Apr 26 17:29:43 2023

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (633.4200, 633.0400)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Apr 26 17:29:43 2023
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.2  MEM: 0.000M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

```
------------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------------

Setup views included:
 av_func_mode_max
Hold views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.050  |  0.050  |  0.503  |  1.045  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   467   |   228   |   265   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.482  |  0.482  |  2.493  |  3.381  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   467   |   228   |   265   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+
```

4. Show the critical path after post-route optimization. What is the path type? (5%) (The slack of the critical path should match the smallest slack in the timing report)

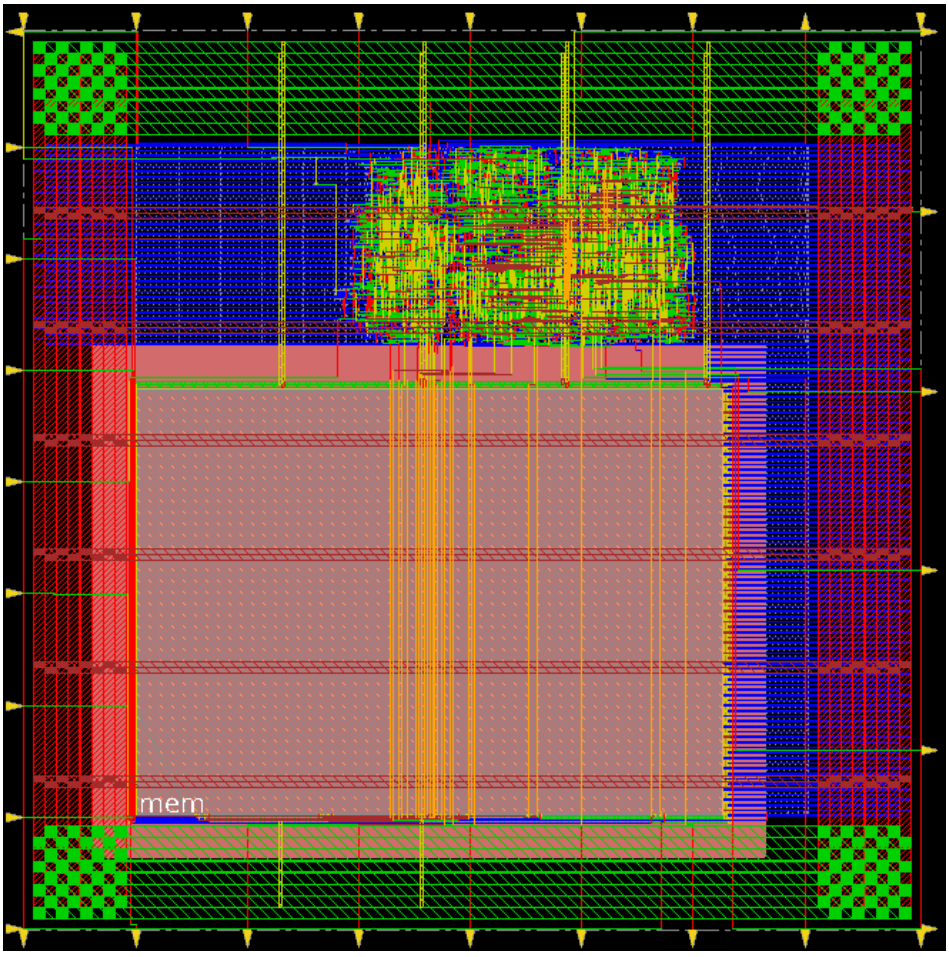
```
Path 1: MET Setup Check with Pin psum_r_reg_9_/CK
Endpoint:   psum_r_reg_9_/D (^) checked with  leading edge of 'i_clk'
Beginpoint: mem/Q[2]        (^) triggered by  leading edge of 'i_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.512
- Setup                         0.209
+ Phase Shift                   5.000
+ CPPR Adjustment               0.000
= Required Time                 5.304
- Arrival Time                  5.254
= Slack Time                    0.050
     Clock Rise Edge                     0.000
     + Source Insertion Delay           -0.022
     = Beginpoint Arrival Time          -0.022
     Timing Path:
     +-------------------------------------------------------------------------------------+
     |          Pin          | Edge |    Net     |    Cell     | Delay | Arrival | Required |
     |                       |      |            |             |       |  Time   |   Time   |
     |-----------------------+------+------------+-------------+-------+---------+----------|
     | i_clk                 |  ^   | i_clk      |             |       | -0.022  |    0.028 |
     | CTS_cdb_buf_00016/A   |  ^   | i_clk      | CLKBUFX3    | 0.001 | -0.020  |    0.030 |
     | CTS_cdb_buf_00016/Y   |  ^   | CTS_6      | CLKBUFX3    | 0.138 |  0.118  |    0.168 |
     | CTS_cdb_buf_00018/A   |  ^   | CTS_6      | CLKBUFX3    | 0.000 |  0.118  |    0.168 |
     | CTS_cdb_buf_00018/Y   |  ^   | CTS_2      | CLKBUFX3    | 0.188 |  0.306  |    0.356 |
     | CTS_ccl_a_buf_00003/A |  ^   | CTS_2      | CLKBUFX16   | 0.001 |  0.307  |    0.357 |
     | CTS_ccl_a_buf_00003/Y |  ^   | CTS_3      | CLKBUFX16   | 0.178 |  0.485  |    0.535 |
     | mem/CLK               |  ^   | CTS_3      | sram_4096x8 | 0.024 |  0.509  |    0.559 |
     | mem/Q[2]              |  ^   | D_rdata[2] | sram_4096x8 | 2.719 |  3.227  |    3.277 |
     | U1038/A               |  ^   | D_rdata[2] | CLKINVX1    | 0.009 |  3.237  |    3.287 |
     | U1038/Y               |  v   | n1989      | CLKINVX1    | 0.137 |  3.374  |    3.424 |
     | U1037/B               |  v   | n1989      | AND2X2      | 0.000 |  3.374  |    3.424 |
     | U1037/Y               |  v   | n1980      | AND2X2      | 0.204 |  3.578  |    3.628 |
     | FE_RC_7_0/A0          |  v   | n1980      | OAI31XL     | 0.000 |  3.578  |    3.628 |
     | FE_RC_7_0/Y           |  ^   | n1982      | OAI31XL     | 0.217 |  3.795  |    3.845 |
     | U1200/B               |  ^   | n1982      | NOR2X1      | 0.000 |  3.795  |    3.845 |
     | U1200/Y               |  v   | n1463      | NOR2X1      | 0.163 |  3.959  |    4.009 |
     | U2130/C               |  v   | n1463      | OR3X2       | 0.000 |  3.959  |    4.009 |
     | U2130/Y               |  v   | n2111      | OR3X2       | 0.318 |  4.277  |    4.327 |
     | U1866/B               |  v   | n2111      | NAND2X1     | 0.000 |  4.277  |    4.327 |
     | U1866/Y               |  ^   | n2012      | NAND2X1     | 0.151 |  4.428  |    4.478 |
     | FE_RC_10_0/A0         |  ^   | n2012      | AOI21X1     | 0.000 |  4.428  |    4.478 |
     | FE_RC_10_0/Y          |  v   | n1482      | AOI21X1     | 0.143 |  4.570  |    4.621 |
     | U3044/B0              |  v   | n1482      | AO21X4      | 0.000 |  4.571  |    4.621 |
     | U3044/Y               |  v   | n2028      | AO21X4      | 0.186 |  4.757  |    4.807 |
     | U1263/C               |  v   | n2028      | AND3X2      | 0.000 |  4.757  |    4.807 |
     | U1263/Y               |  v   | n2048      | AND3X2      | 0.218 |  4.975  |    5.025 |
     | U1434/B               |  v   | n2048      | OR3X4       | 0.000 |  4.975  |    5.025 |
     | U1434/Y               |  v   | n1329      | OR3X4       | 0.220 |  5.195  |    5.245 |
     | U1002/A               |  v   | n1329      | NAND2X1     | 0.000 |  5.195  |    5.245 |
     | U1002/Y               |  ^   | n955       | NAND2X1     | 0.059 |  5.254  |    5.304 |
     | psum_r_reg_9_/D       |  ^   | n955       | DFFRX1      | 0.000 |  5.254  |    5.304 |
     +-------------------------------------------------------------------------------------+
```

5. Attach the snapshot of GDS stream out messages. (10%)

```
Trim Metal                          0

Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file library/gds/tpz013g3_v1.1.gds to register cell name ......
Scanning GDS file sram_lib/sram_4096x8.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file library/gds/tpz013g3_v1.1.gds ......
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has version number: 5.
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file sram_lib/sram_4096x8.gds ......
        ****** Merge file: sram_lib/sram_4096x8.gds has version number: 5.
        ****** Merge file: sram_lib/sram_4096x8.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```

6. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



7. Attach the snapshot of the final area result. (5%)

```
************************ Analyze Floorplan ************************
    Die Area(um^2)              : 400980.20
    Core Area(um^2)             : 223567.95
    Chip Density (Counting Std Cells and MACROs and IOs): 50.007%
    Core Density (Counting Std Cells and MACROs): 89.690%
    Average utilization         : 100.000%
    Number of instance(s)       : 5048
    Number of Macro(s)          : 1
    Number of IO Pin(s)         : 33
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
```

8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)