Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, May 23, 14:00

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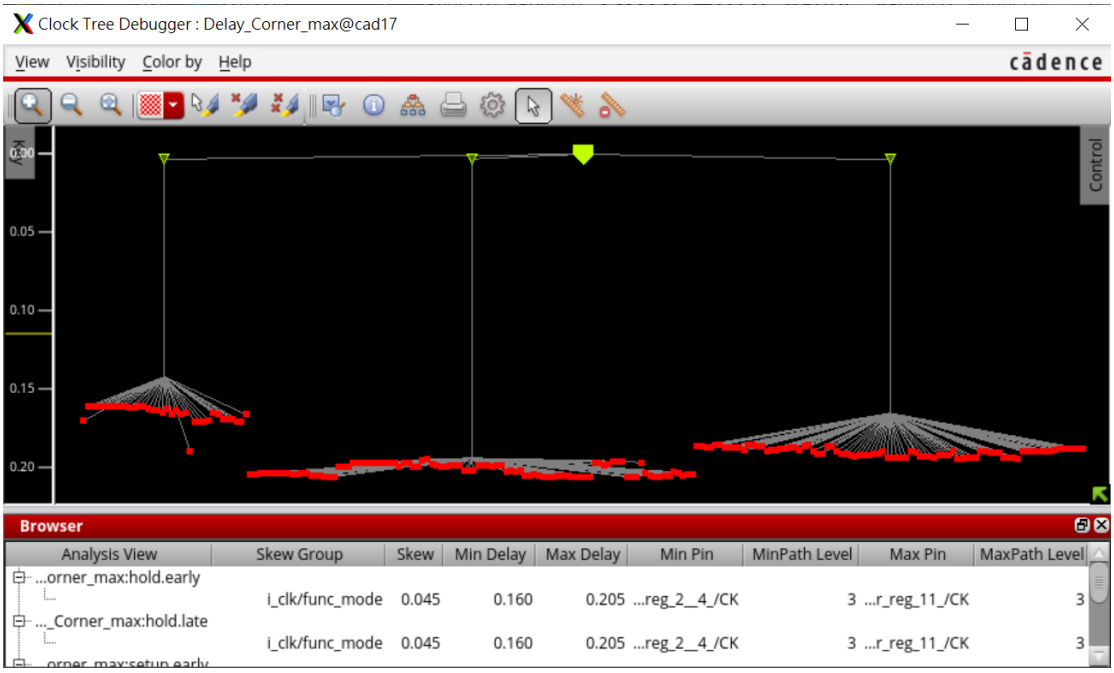
APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	400980.20
	Core Area (um^2)	223567.95
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	10ns
Follow your design in HW3? (If not, write down the student ID of the designer)		Ref_design

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result, and show the routing result in the layout (10%).



2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
*** Starting Verify DRC (MEM: 1500.6) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 160.480 160.480} 1 of 16
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 0.000 320.960 160.480} 2 of 16
 VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 0.000 481.440 160.480} 3 of 16
 VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 0.000 633.420 160.480} 4 of 16
 VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 160.480 160.480 320.960} 5 of 16
 VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 160.480 320.960 320.960} 6 of 16
 VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 160.480 481.440 320.960} 7 of 16
 VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 160.480 633.420 320.960} 8 of 16
 VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 320.960 160.480 481.440} 9 of 16
 VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 320.960 320.960 481.440} 10 of 16
 VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 320.960 481.440 481.440} 11 of 16
 VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 320.960 633.420 481.440} 12 of 16
 VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {0.000 481.440 160.480 633.040} 13 of 16
 VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {160.480 481.440 320.960 633.040} 14 of 16
 VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {320.960 481.440 481.440 633.040} 15 of 16
 VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
 VERIFY DRC ..... Sub-Area: {481.440 481.440 633.420 633.040} 16 of 16
 VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

 Verification Complete : 0 Viols.
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Mon May 22 21:29:59 2023

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (633.4200, 633.0400)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Mon May 22 21:29:59 2023
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.3  MEM: 6.750M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.285  |  0.285  |  0.368  |  1.344  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   467   |   228   |   265   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)       |     0       |      0 (0)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 35.398%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.656  |  0.656  |  2.510  |  3.437  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   467   |   228   |   265   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+
```

4. Show the critical path after post-route optimization. What is the path type? (5%)
   (The slack of the critical path should match the smallest slack in the timing report)

```
Path 1: MET Setup Check with Pin psum_r_reg_9_/CK
Endpoint:   psum_r_reg_9_/D (^) checked with  leading edge of 'i_clk'
Beginpoint: mem/Q[2]        (^) triggered by  leading edge of 'i_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.162
- Setup                         0.212
+ Phase Shift                   5.000
+ CPPR Adjustment               0.000
= Required Time                 4.949
- Arrival Time                  4.665
= Slack Time                    0.285
     Clock Rise Edge                     0.000
     + Source Insertion Delay           -0.191
     = Beginpoint Arrival Time          -0.191
     Timing Path:
     +-------------------------------------------------------------------------------------------+
     |             Pin              | Edge |    Net     |    Cell     | Delay | Arrival | Required |
     |                              |      |            |             |       |  Time   |   Time   |
     |------------------------------+------+------------+-------------+-------+---------+----------|
     | i_clk                        |  ^   | i_clk      |             |       | -0.191  |    0.094 |
     | CTS_ccl_a_BUF_i_clk_G0_L1_1/A |  ^   | i_clk      | CLKBUFX20   | 0.003 | -0.188  |    0.097 |
     | CTS_ccl_a_BUF_i_clk_G0_L1_1/Y |  ^   | CTS_12     | CLKBUFX20   | 0.138 | -0.050  |    0.235 |
     | mem/CLK                      |  ^   | CTS_12     | sram_4096x8 | 0.042 | -0.008  |    0.276 |
     | mem/Q[2]                     |  ^   | D_rdata[2] | sram_4096x8 | 2.726 |  2.717  |    3.002 |
     | U1038/A                      |  ^   | D_rdata[2] | CLKINVX1    | 0.011 |  2.729  |    3.013 |
     | U1038/Y                      |  v   | n1989      | CLKINVX1    | 0.173 |  2.902  |    3.186 |
     | U1037/B                      |  v   | n1989      | AND2X2      | 0.000 |  2.902  |    3.187 |
     | U1037/Y                      |  v   | n1980      | AND2X2      | 0.224 |  3.126  |    3.411 |
     | FE_RC_1_0/A0                 |  v   | n1980      | OAI31X1     | 0.000 |  3.126  |    3.411 |
     | FE_RC_1_0/Y                  |  ^   | n1981      | OAI31X1     | 0.151 |  3.277  |    3.562 |
     | U1200/A                      |  ^   | n1981      | NOR2X1      | 0.000 |  3.277  |    3.562 |
     | U1200/Y                      |  v   | n1463      | NOR2X1      | 0.079 |  3.356  |    3.641 |
     | U2130/C                      |  v   | n1463      | OR3X2       | 0.000 |  3.356  |    3.641 |
     | U2130/Y                      |  v   | n2111      | OR3X2       | 0.310 |  3.666  |    3.951 |
     | U1866/B                      |  v   | n2111      | NAND2X1     | 0.000 |  3.666  |    3.951 |
     | U1866/Y                      |  ^   | n2012      | NAND2X1     | 0.149 |  3.816  |    4.100 |
     | U1901/A1                     |  ^   | n2012      | AOI21X1     | 0.000 |  3.816  |    4.100 |
     | U1901/Y                      |  v   | n1482      | AOI21X1     | 0.120 |  3.936  |    4.221 |
     | U3044/B0                     |  v   | n1482      | AO21X2      | 0.000 |  3.936  |    4.221 |
     | U3044/Y                      |  v   | n2028      | AO21X2      | 0.254 |  4.190  |    4.475 |
     | U1263/C                      |  v   | n2028      | AND3X4      | 0.000 |  4.190  |    4.475 |
     | U1263/Y                      |  v   | n2048      | AND3X4      | 0.154 |  4.344  |    4.629 |
     | U1434/B                      |  v   | n2048      | OR3X2       | 0.000 |  4.344  |    4.629 |
     | U1434/Y                      |  v   | n1329      | OR3X2       | 0.251 |  4.596  |    4.880 |
     | U1002/A                      |  v   | n1329      | NAND2X1     | 0.000 |  4.596  |    4.880 |
     | U1002/Y                      |  ^   | n955       | NAND2X1     | 0.069 |  4.665  |    4.949 |
     | psum_r_reg_9_/D              |  ^   | n955       | DFFRX1      | 0.000 |  4.665  |    4.949 |
     +-------------------------------------------------------------------------------------------+
     Clock Rise Edge                     0.000
     = Beginpoint Arrival Time           0.000
     Other End Path:
     +-------------------------------------------------------------------------------------------+
```

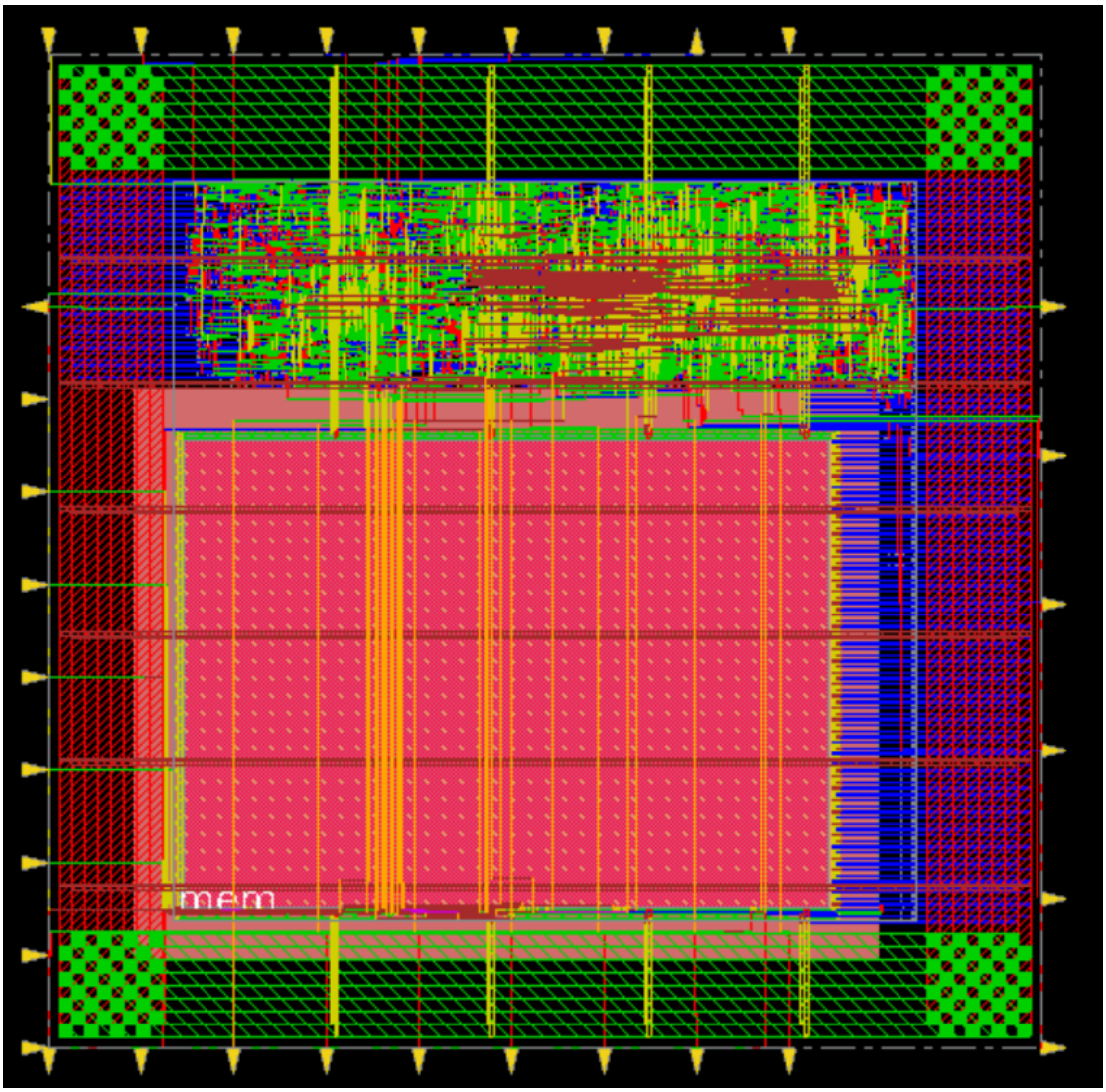
5. Attach the snapshot of GDS stream out messages. (10%)

```
    Via Instances                    0

Text                                35
    metal layer METAL2              20
    metal layer METAL3              15


Blockages                            0


Custom Text                          0


Custom Box                           0

Trim Metal                           0

Merging with GDS libraries
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file library/gds/tpz013g3_v1.1.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file library/gds/tpz013g3_v1.1.gds ......
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has version number: 5.
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
**WARN: (IMPOGDS-217):  Master cell: sram_4096x8 not found in merged file(s) and will therefore not be inclu
ded in the resulting streamOut file. Verify the file names specified with the -merge option are correct and
that they contain a definition of this cell.
**WARN: (IMPOGDS-218):  Number of master cells not found after merging: 1

######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)

```
innovus 19>  analyzeFloorplan
**WARN: (IMPAFPU-9006): Command 'analyzeFloorplan' is obsolete. Please use commands 'placeDesign + trialRout
e + create_ps_per_micron_model + timeDesign -proto + load_timing_debug_report -proto' to analyze congestion
and timing for the floorplan.
Start to collect the design information.
Build netlist information for Cell core.
Finished collecting the design information.
Average module density = 1.000.
Density for the design = 1.000.
       = stdcell_area 41920 sites (71155 um^2) / alloc_area 41920 sites (71155 um^2).
Pin Density = 0.07051.
            = total # of pins 9287 / total area 131712.
************************ Analyze Floorplan *************************
    Die Area(um^2)             : 400980.20
    Core Area(um^2)            : 223567.95
    Chip Density (Counting Std Cells and MACROs and IOs): 48.762%
    Core Density (Counting Std Cells and MACROs): 87.456%
    Average utilization        : 100.000%
    Number of instance(s)      : 7930
    Number of Macro(s)         : 1
    Number of IO Pin(s)        : 33
    Number of Power Domain(s) : 0
************************ Estimation Results ************************
********************************************************************
```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)
   Since there is only one SRAM in this design, I simply place it around chip periphery to prevent detour routing.