Politecnico di Milano

Facoltà di ingegneria
Dipartimento di elettronica e informazione

OTA Design Lab

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Group:
Matteo Baldo - matteo.baldo@mail.polimi.it
Edoardo Contini - edoardo.contini@mail.polimi.it
Piergiulio Mannocci - piegiulio.mannocci@mail.polimi.it
Michele Mastella - michele.mastella@mail.polimi.it
Francesco Tesolin - francesco.tesolin@mail.polimi.it

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Chapter 1

Part 1

As first step, we choose the tail current of the first stage of XXX uA, in order to comply with CMRR requirement. Then, we choose the overdrive voltage of the NMOS of the second stage, in order to have a 1 kHz noise corner frequency, using the following equation:

Finally, we choose the W/L of the tail transistor to be 10u/25u, so that the slew rate was higher than the requested one. According to our knowledge, output transistor are too narrow, but we couldn't find a better solution. At the end, we were able to build an amplifier with a GBWP of 40 MHz, with a 60 deg phase margin, that consumes XXX uA.

Chapter 2

Part 2

Since we were asked to reduce the power consumption, we needed to use a different compensation technique. As the supply voltage of the OTA is 3 V, the more suitable compensation technique is the feedforward one, as, given a fixed bandwidth, it allows a lower input current noise of the OTA. We managed to re-design whose frequency response is the same one as the Miller one, with half the current consumption.

Bibliography