LPM Registers Definition

Requirements

#	Requirement	Design Input	Design Output	Validation
	The firmware should be updatable through I2C supporting a dual bank mechanism			
	During an update, the firmware should ensure the bank B is valid before to jump the code and should fallback if anything abnormal occurs			
	The power mode should be implemented following the state diagram in the SkyHawk Hardware Platform v2.0 (page 15)			
	The LPM should allow to configure VIN threshold			
	The LPM should manage the battery charging	If Vin is present, the charge should be enable		
	The LPM should do the GPS external antenna auto-detection			
	All the configuration registers should be saved in flash so when the device reboots the CPU do not need to reconfigure the settings			

Registers

[0x00-0x0E] - Firmware Version

Register to read firmware version (String). When you issue a read command, simply read 30 bytes directly to get the whole firmware version. Calls to any other register between 0x01 and 0x0E will result in fault.

Firmware Version																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	FWVER															
permission	RO															
default value	0															

FWVER: Firmware Version
String : 15 chararacters max
Keyword : This register has no Keyword, use grpc call GetFWVersion()

0x0F - Hardware Version

Register to read hardware version

Hardware Version																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description											HWVER					
permission											RO					
default value											0					

HWVER: Hardware Version
0-63
Keyword : This register has no Keyword, use grpc call GetHWVersion()

0x10 - CPU Wake Event Mask

Register to configure what will enable CPU and move the state machine from Low Power to Normal mode.
If at least one event is writing on bit 01 to 06 and VIN is present, the LPM will wake-up the CPU.
Otherwise, the LPM will wake-up CPU only when VIN is present (default).

CPU Wake Event Mask																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description										CAN	ACC	DI2	DI1	RTC	IGN	VIN
permission										RW	RW	RW	RW	RW	RW	RO
default value										0	0	0	0	0	0	1

VIN: VIN condition
Keyword : CPU_WAKE_VIN

IGN: Ignition Event
Keyword : CPU_WAKE_IGN

RTC: RTC Timeout
Keyword : CPU_WAKE_RTC

DI1: Digital Input Event
Keyword : CPU_WAKE_DI1

DI2: Digital Input Event
Keyword : CPU_WAKE_DI2

ACC: Accelerometer Event
Keyword : CPU_WAKE_ACC

CAN: CAN Activity Event
Keyword : CPU_WAKE_CAN

0x11 - CPU Wake Event Delay

Register to configure the delay before enabling the CPU following the Wake Event. This configuration can help to prevent the CPU to restart to fast if a shutdown was issued and the wake up condition are meet before the board was correctly shutdown.

CPU Wake Event Delay																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Delay (msec)															
permission	RW															
default value	0															

Keyword : CPU_WAKE_DELAY

0x20 - Digital Inputs Polarity

Register to configure the digital inputs polarity.

Digital Inputs Polarity															
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description													DI2		DI1	
permission													RW		RW	
default value													00		00	

DI1
00: Disable
01: Rising edge
10: Falling edge
11: Both edge
Keyword : DIG1_POLARITY

DI2
00: Disable
01: Rising edge
10: Falling edge
11: Both edge
Keyword : DIG2_POLARITY

0x21 - Power Control

Register to control the Power Mode and power to the external interfaces.

Power Control																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description						CANLPEN	CANEN	BPLPEN	BPEN	GPSLPEN	GPSEN	VREFLPEN	VREFSEL	VREFEN	RSM	RLP
permission						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
default value						0	0	0	0	0	0	0	0	0	0	0

RLP: Request Low Power
Keyword : POWER_CTRL_RLP

RSM: Request Shelf Mode
Keyword : POWER_CTRL_RSM

VREFEN: VREF Enable
Keyword : POWER_CTRL_VREFEN

VRESEL:VREF Selector
0: 5V
1: Vin
Keyword : POWER_CTRL_VRESEL

VREFLPEN: VREF Low Power Enable
Keyword : POWER_CTRL_VREFLPEN

GPSEN: GPS Enable
Keyword : POWER_CTRL_GPSEN

GPSLPEN: GPS Low Power Mode Enable
Keyword : POWER_CTRL_GPSLPEN

BPEN: BitPipe Enable
Keyword : POWER_CTRL_BPEN

BPLPEN: BitPipe Low Power Mode Enable
Keyword : POWER_CTRL_BPLPEN

CANEN: CAN Bus Enable
Keyword : POWER_CTRL_CANEN

CANLPEN: CAN Bus Low Power Mode Enable
Keyword : POWER_CTRL_CANLPEN

0x22 - GPS External Antenna Control

Register to control the external antennas of the GPS.

GPS External Antenna Control																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description																GPSEXTANTE
permission																RW
default value																1

GPSEXTANTE: GPS External Antenna Enable
Keyword : GPS_EXT_ANT_CTRL

0x30 - VBAT Low Threshold

Register to configure the battery voltage (VBAT) threshold to trigger VBATLOW IRQ.

VBAT Low Threshold																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Voltage (mV)															
permission	RW															
default value	3000															

Keyword : VBAT_LOW_THRESHOLD

0x31 - VBAT Shelf Mode

Register to configure the battery voltage (VBAT) threshold for VBAT Shelf Mode.
If VBAT falls below THRESHOLD - HYSTERESIS, LPM transitions to Shelf Mode.
If VBAT rises above THRESHOLD + HYSTERESIS, LPM transitions to RTC Only.
Even if this value is set to 0, the minimum value is 2700mV

VBAT Shelf Mode																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Voltage (mV)															
permission	RW															
default value	2700															

Keyword : VBAT_SHELF_MODE

0x32 - VIN RTC Mode (VIN Lost)

Register to configure the input voltage (VIN) threshold for VIN RTC Mode.
If VIN falls below THRESHOLD - HYSTERESIS, LPM transitions to RTC Mode.
If VIN rises above THRESHOLD + HYSTERESIS, LPM transitions to Low Power Mode.

VIN RTC Mode (VIN Lost)																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Voltage (mV)															
permission	RW															
default value	6000															

Keyword : VIN_RTC_MODE

0x33 - VIN Normal (Low Voltage) Mode

Register to configure the input voltage (VIN) threshold for VIN Normal (Low Voltage) Mode.
If VIN falls below THRESHOLD - HYSTERESIS, LPM transitions to Normal (Low Voltage) Mode.
If VIN rises above THRESHOLD + HYSTERESIS, LPM transitions to Normal Mode.

VIN Normal (Low voltage) Mode																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Voltage (mV)															

permission	RW
default value	12000

Keyword : VIN_NORM_LV_MODE

0x40 - VIN Hysteresis

Register to configure the VIN hysteresis before to change the power mode.

VIN Hysteresis															
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Voltage (mV)															
permission	RW															
default value	200															

Keyword : VIN_HYSTERESIS

0x41 - VBAT Hysteresis

Register to configure the VBAT hysteresis before to change the power mode.

VBAT Hysteresis															
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Voltage (mV)															
permission	RW															
default value	100															

Keyword : VBAT_HYSTERESIS

0x50 - IRQ Enable

Register to configure IRQ Enable.

VIN Alarm																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description													KAWARN	VINLOST	VBATLOWE	MODECHGE
permission													RO	RW	RW	RW
default value													1	1	1	1

MODECHGEN: Mode Change Enable
Keyword : IRQ_MODECHGEN

VBATLOWEN: VBAT Low Alarm Enable
Keyword : IRQ_VBATTLOWEN

VINLOST: VIN Lost Alarm Enable
Keyword : IRQ_VINLOWEN

KAWARN: Keep Alive Warning
Keyword : IRQ_KAWARN

0x51 - Low Power Mode Request Timeout

Register to configure the timeout after which the CPU will be powered off even if it's not correctly shutdown.
The timeout will start after the CPU launch a Low Power Mode Request.

Low Power Mode Request Timeout																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Timeout (sec)															
permission	RW															
default value	15															

0-65535: Timeout in sec
Keyword : LP_MODE_REQ_TIMEOUT

0x52 - CPU Cold Boot Keep Alive Timeout

Register to configure the grace period before requiring the first kick from the CPU.

CPU Cold Boot Keep Alive Timeout																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Timeout (sec)															
permission	RW															
default value	60															

0: Disable
1-65535: Timeout in sec
Keyword : CPU_COLD_KA_TIMEOUT

0x53 - CPU Keep Alive Timeout

Register to configure the time after which the LPM will need to be "kicked" by the CPU to keep the power on.

CPU Keep Alive Timeout																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Timeout (sec)															
permission	RW															
default value	30															

0: Disable
1-65535: Timeout in sec
Keyword : CPU_KA_TIMEOUT

0x54 - Power Loss Warning Delay

Register to configure the delay before the LPM will warn the CPU that the VIN is lost (**VINLOST** IRQ).
This delay will start after the VIN RTC Mode threshold is met.

Power Loss Warning Delay																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Delay (sec)															
permission	RW															
default value	5															

0-65535: Delay in sec
Keyword : POWER_LOSS_WARNING_DELAY

0x55 - Power Loss Shutdown Timeout

Register to configure the timeout after which the CPU will be powered off even if it's not correctly shutdown.
Time timeout will start after the **VINLOST** IRQ.

Power Loss Shutdown Timeout																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	Timeout (sec)															
permission	RW															
default value	5															

0: Disable
1-65535: Timeout in sec
Keyword : POWER_LOSS_SHUTDOWN_TIMEOUT

0x60 - Last Wake Event Status

Register to read the last wake event that powered the CPU

Last Wake Event Status																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description										CAN	ACC	DI2	DI1	RTC	IGN	VIN
permission										RO	RO	RO	RO	RO	RO	RO
default value										0	0	0	0	0	0	0

VIN: VIN condition
Keyword : LAST_WAKE_VIN

IGN: Ignition Event
Keyword : LAST_WAKE_IGN

RTC: RTC Timeout
Keyword : LAST_WAKE_RTC

DI1: Digital Input Event
Keyword : LAST_WAKE_DI1

DI2: Digital Input Event
Keyword : LAST_WAKE_DI2

ACC: Accelerometer Event
Keyword : LAST_WAKE_ACC

CAN: CAN Activity Event
Keyword : LAST_WAKE_CAN

0x61 - VIN Voltage Status

Register to read the current VIN voltage.

VIN Voltage Status																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	VIN (mV)															
permission	RO															
default value	0															

Keyword : VIN_STATUS

0x62 - VBAT Voltage Status

Register to read the current VBAT voltage.

VBAT Voltage Status																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	VBAT (mV)															
permission	RO															
default value	0															

Keyword : VBAT_STATUS

0x63 - Power Status

Register to read the current power mode, the battery voltage and the charge status.

Power Status																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description				VBAT								CHGSTS		PM		
permission				RO								RO		RO		
default value				0								00		000		

PM: Power Mode
000: Shutdown / Shelf Mode (not used)
001: RTC Only (Not used)
010: Low power mode
011: Normal (Low voltage)
100: Normal
Keyword : POWER_STATUS_PM

CHGSTS: Charge Status
00: Charge complete
01: Charging
10: Safety timer fault or cell temperature invalid
11: Reserved
Keyword : POWER_STATUS_CHGSTS

VBATT: Battery voltage in pourcentage
Keyword : POWER_STATUS_VBATT

0x64 - GPS External Antenna Status

Register to read GPS External Antenna Status.

GPS External Antenna Status																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description															GPSANTSHRT	GPSANTDET
permission															RO	RO
default value															0	0

GPSANTDET: GPS External Antenna Detected
Keyword : GPS_ANT_DET

GPSANTSHRT: GPS External Antenna Short
Keyword : GPS_ANT_SHRT

0x65 - IRQ Status

Register to read IRQ status. This register is cleared on read.

IRQ Status																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description													KAWARN	VINLOST	VBATLOW	MODECHG
permission													RO	RO	RO	RO
default value													0	0	0	0

MODECHG: Power Mode Change
Keyword : IRQ_STATUS_MODECHG

VBATLOW: VBAT is under VBATLOW threshold
Keyword : IRQ_STATUS_VBATLOW

VINLOST: VIN is under VIN RTC Mode threshold
Keyword : IRQ_STATUS_VINLOST

KAWARN: Keep Alive Warning occurs when CPU forgot to kick the LPM for a keep alive timeout cycle. The LPM will trigger the CPU reset after the second keep alive timeout cycle.
Keyword : IRQ_STATUS_KAWARN

0x70 - Firmware Update Commands

Register to control the firmware update process. The firmware update status will be automatically clear when a new command is received. Following the command, a buffer of 128 bytes is available to add a payload.

Firmware Update Request																	
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description											REBOOT	VALIDATE	WRITEADR	WRITECRC	WRITE	ERASE
permission											WO	WO	WO	WO	WO	WO
default value											0	0	0	0	0	0

ERASE: Erase the inactive bank
Keyword : FW_UPDT_CMD_ERASE

WRITE: Write data to flash. This command will fill a buffer (Write Buffer) waiting for CRC confirmation before to write the data to the flash. A minimum of 2 bytes is required in the payload.
Keyword : FW_UPDT_CMD_WRITE

WRITECRC: Validate CRC of the last command. On CRC match, the data from the last WRITE operation will be write to the flash. A 4 bytes CRC value is required in the payload.
Keyword : FW_UPDT_CMD_WRITECRC

WRITEADR: Modify the current write address. This command can be used to skip blank space in application. A 4 bytes address value is required in the payload and the address should be a multiple of 4.
Keyword : FW_UPDT_CMD_WRITEADR

VALIDATE: Validate request command. This command will check the CRC of the whole application. The CRC value is already include in the transferred file.
Keyword : FW_UPDT_CMD_VALIDATE

REBOOT: Reboot the Low Power Manager. This command will do the exact same thing as CPU shutdown request, but in addition it will reboot

the LPM.
Keyword : FW_UPDT_CMD_REBOOT

[0x71-0x72] - Firmware Update Start Address

Register to get the starting address of the currently inactive bank. Sends 32 bits of data containing the starting address.
When you issue a read command, simply read 4 bytes directly to get the whole firmware update start address.
Calls to register 0x72 will result in fault.

Firmware Update Start Address																
bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
description	FWSTARTADR															
permission	RO															
default value	0															

Value between 0 and 2,147,483,647.

[0x73-0x74] - Firmware Update End Address

Register to get the ending address of the currently inactive bank. Sends 32 bits of data containing the ending address.
When you issue a read command, simply read 4 bytes directly to get the whole firmware update end address.
Calls to register 0x74 will result in fault.

Firmware Update Start Address																
bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
description	FWENDADR															
permission	RO															
default value	0															

Value between 0 and 2,147,483,647.

0x75 - Firmware Update Status

Register to read firmware update status. This register is cleared on read.

Firmware Update Status																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description					REBOOTSTS		VALIDATESTS		WRITEADRSTS		WRITECRCSTS		WRITESTS		ERASESTS	
permission					RO		RO		RO		RO		RO		RO	
default value					00		00		00		00		00		00	

00: Idle
01: Command in progress
10: Command failed
11: Command succeed

ERASESTS: Erase command status. Fail reason: Cannot erase flash.
Keyword : FW_UPDT_STS_ERASE

WRITESTS: Write command status. Fail reason: Cannot write data from "Write Buffer" to flash.
Keyword : FW_UPDT_STS_WRITE

WRITECRCSTS: Write CRC command status. Fail reason: "Write buffer" CRC doesn't match with the WRITECRC command payload.
Keyword : FW_UPDT_STS_WRITECRC

WRITEADRSTS: Write ADR command status. Fail reason: The address from WRITEADR payload is out of range.
Keyword : FW_UPDT_STS_WRITEADR

VALIDATESTS: Validate command status. Fail reason: Application CRC doesn't match with the VALIDATE command payload.
Keyword : FW_UPDT_STS_VALIDATE

REBOOTSTS: Reboot command status. Fail reason: ?
Keyword : FW_UPDT_STS_REBOOT

[0x80-0x84] - RTC Time

Register to read and write the RTC time. (EPOCH format)

RTC Time																
bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
description	RTCTIME															
permission	RW															
default value	0															