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ELECTRONICS AND INFORMATION TECHNOLOGY

Institute of Electronic Systems

Master's diploma thesis

in the field of study Electronics
and specialisation Microsystem and electronic systems

Synchronisation implementation in FPGA for scientific grade cameras

Piotr Zdunek
student record book number 229417

Dr inż. Grzegorz Kasprowicz

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Politechnika Warszawska
Warsaw University of Technology

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miejscowość i data
place and date

Piotr Zdunek
imię i nazwisko studenta
name and surname of the student

229417
numer albumu
student record book number

Elektronika
kierunek studiów
field of study

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Abstract

Text of the Abstract.

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Chapter 1

Introduction

In the scientific embedded camera systems time synchronisation is often necessary to control precisely the exposure time of the sensor. In this master thesis, a timestamping unit implementation for Xilinx Zynq SoC based scientific camera is presented. The implementation consists of the digital system part implemented in FPGA logic as well as firmware side developed on Cortex A9 embedded inside the Zynq. The provided unit allows for more precise timing between the cameras in the multichannel scenario, than what is available by using standard features provided by the manufacturer.

In this chapter a definition of PTP timestamping unit is presented, as well as the basics of time synchronisation in embedded systems. The chapter introduces basic terms and concepts which are used throughout the thesis.

1.1 Motivation and Objectives

In order to provide time synchronisation capability for a scientific grade camera based on Zynq SoC a Timestamping Synchronisation Unit was designed, developed and deployed.

1.2 Time synchronisation

1.2.1 Basic terms

1.2.2 GPS synchronisation

1.2.3 Ethernet network synchronistaion

NTP - Network Time Protocol

PTP - Precision Time Protocol

White Rabbit

1.2.4 Local clock sources

1.3 Scientific camera systems

1.4 Thesis statement

The built in PTP mechanism in Xilinx Zynq SoC does not allow to read the UTC PTP Time defined by IEEE1588 standard (TODO - reference). What is more, the time synchronisation capability is poor (TODO XIL APP NOTE), due to the use of CPU Clock as PTP counter clock and also poor design of the hardware MAC (REFERENCE). The goal of this master thesis is to solve this problem by implementing a PTP Timestamping Unit (TSU) in the FPGA fabric and modifying the Xilinx Ethernet Driver so that it supports the custom TSU. This will allow to achieve time synchronisation between embedded systems using Zynq SoC, based on PTP, which was one of the requirements for the scientific camera system.

1.5 Publications

Chapter 2

Genesis

In this master thesis an implementation of Precision-Time-Protocol Timestamping Unit in FPGA fabric for scientific camera systems is presented. The project was completed at Photonics and Web Engineering Group at the Institute of Electronics Systems which has a significant contribution to X-ray measurement research (TODO publikacje). Having a scientific cooperation with another Polish university, there was a need to develop hardware and firmware for novel extremely high-speed, multichannel, X-ray silicon based camera. This project is undergoing a patent application, and for this reason the detailed description of the project cannot be included in this thesis.

Specifically, a time synchronisation system providing an accurate UTC time was required in order to correctly control the exposure time between the systems' channels. This master thesis focuses on that aspect of the project.

2.1 Problem statement

Providing an accurate timestamping for modern scientific grade camera system is a **complicated engineering problem**. The designed hardware for the camera system used Xilinx Zynq SoC[**?**] which has built in timestamping capability in the Media Access Controller (MAC). Nevertheless, the timestamping register is not available for to be read by the operating system and

programmable logic [**?**, 16.4.2] and the provided functionality of timestamping from Xilinx is limited and provides low accuracy [**?**, 16.2.7] and significant jitter [**?**]. Xilinx User Guide Number 585 - Technical Rerence Manual explicitly mentions the fact that the Timestamping Unit can be implemented in hardware (programmable logic) in order to achieve better accuracy. This has not been done before and this thesis provides the solution to the mentioned problem.

2.2 Solution

The solution for the problem is to design a Timestamping Unit (TSU) in digital system in FPGA fabric for the Zynq SoC and use the MAC's built in PTP filtering capability to use this IP Core as a replacement for the internal built in TSU. What is more, an Ethernet driver modification is required to exchange the TSU and an external oscillator has to be added to the system in order to precisely run the counters in the TSU.

2.3 Statement of Originality

This solution provides a way to perform PTP based time synchronisation using Zynq SoC. There are other methods which provide time synchronisation of different precision such as:

- GPS
- NTP - precision of up to
- PTP (by standard) - sub-milisecond precision
- White Rabbit - sub-nanosecond precision

Nevertheless, the solution provided in this master thesis is **original**. Standard PTP in the Zynq SoC does not function properly and in order to be able to use PTP on Zynq with high precision and low jitter, TSU needs to be implemented in digital fabric.

Chapter 3

Concept

In this chapter a thorough analysis of the problem is shown and a solution for the problem is presented.

3.1 Analysis of PTP on Zynq SoC

3.2 Possible solution presentation - timestamping in FPGA

3.2.1 General idea

3.2.2 Technical implementation

Digital system design

Petalinux configuration

MAC driver modification

Chapter 4

Requirements

- provide timestamping capability with accuracy in ns range, better than built-in solution provided by Xilinx
- timestamping register value should be available by operating system and programmable logic

Chapter 5

Realisation

5.1 Digital system design

5.1.1 Zynq MAC PTP filter

Xilinx Zynq SoC has an integrated Media Access Controller for 10/100/1000 Mbps Ethernet. MAC supports IEEE1588[**?**, 16.2.7], but it's Timestamping Unit is limitted as mentioned before. Nevertheless, the MAC PTP packet filter can be used to implement custom TSU.

Zynq MAC PTP signal test

In order to validate the signals coming out from the PTP a simple test was performed

5.1.2 Zynq Processing System Configuration

5.1.3 Timestamping Unit Implementation

5.2 Firmware implementation

5.2.1 MAC driver

5.2.2 MAC driver

5.2.3 Linux PTP driver

5.2.4 PTP driver

5.2.5 PTPd program

Done - basic digital system with ptp signals connected to chipscope - added register connected to axi to test whether it can be added through uio to xemacps - run qemu on host for zc706 - modified the petalinux device tree to support phy

Chapter 6

Summary