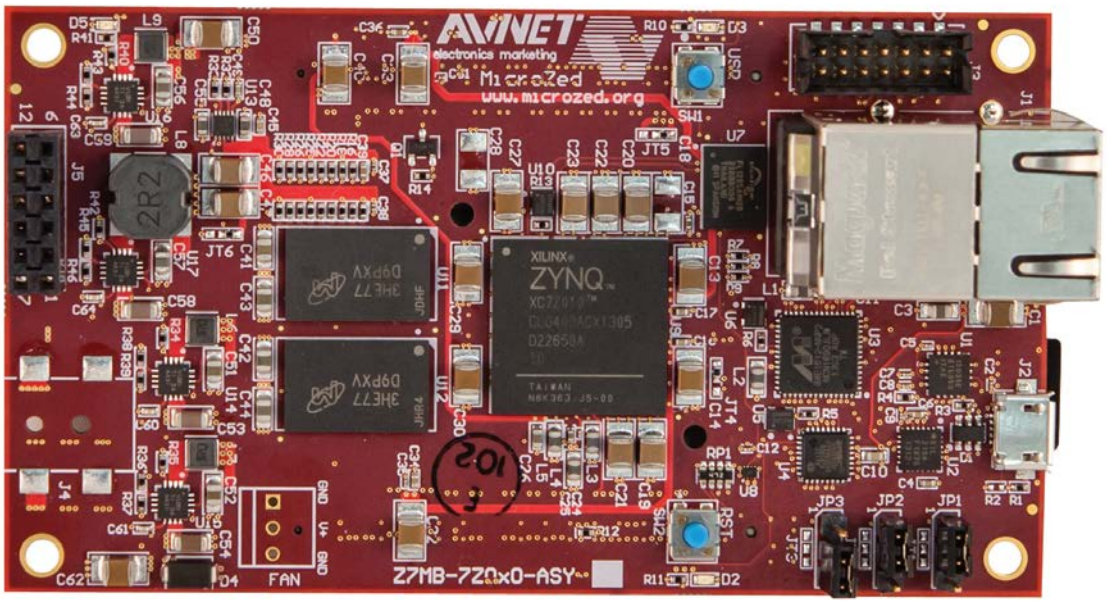
MicroZed

Zynq™ Evaluation and Development
and
System on Module

Hardware User Guide



Version 1.4
28 Jan 2014

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1 Introduction

The MicroZed is a low cost evaluation board and system on module (SOM) targeted for broad use in many applications. The features provided by the MicroZed consist of:

- Xilinx XC7Z010-1CLG400C AP SOC
  - Primary configuration = QSPI Flash
  - Auxiliary configuration options
    - JTAG (through PL via Xilinx PC4 Header)
    - microSD Card
- Memory
  - 1 GB DDR3 (x32)
  - 128 Mb QSPI Flash
  - 4 GB microSD Card
- Interfaces
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  - Three potential powering methods
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    - Optional carrier card
- Software
  - Vivado Design Suite
    - Download from www.xilinx.com/support/download.html
    - Request a free DVD from www.xilinx.com/onlinestore/dvd_fulfillment_request.htm
  - Vivado Design Suite: Design Edition license voucher (node-locked, device-locked to the XC7Z010)

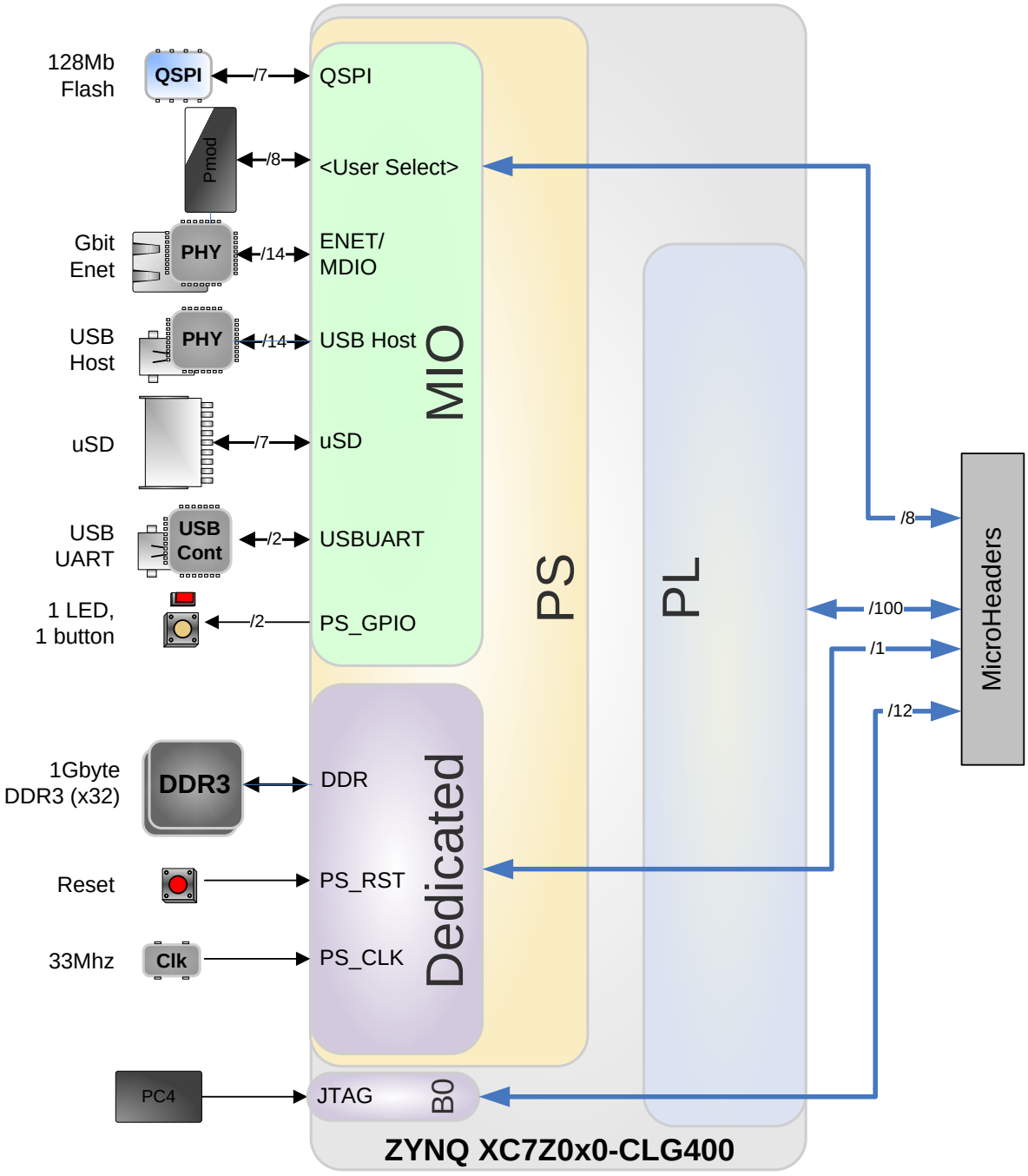


Figure 1 – MicroZed Block Diagram

1.1 Zynq Bank Pin Assignments

The following figure shows the Zynq bank pin assignments on the MicroZed followed by a table that shows the detailed I/O connections.

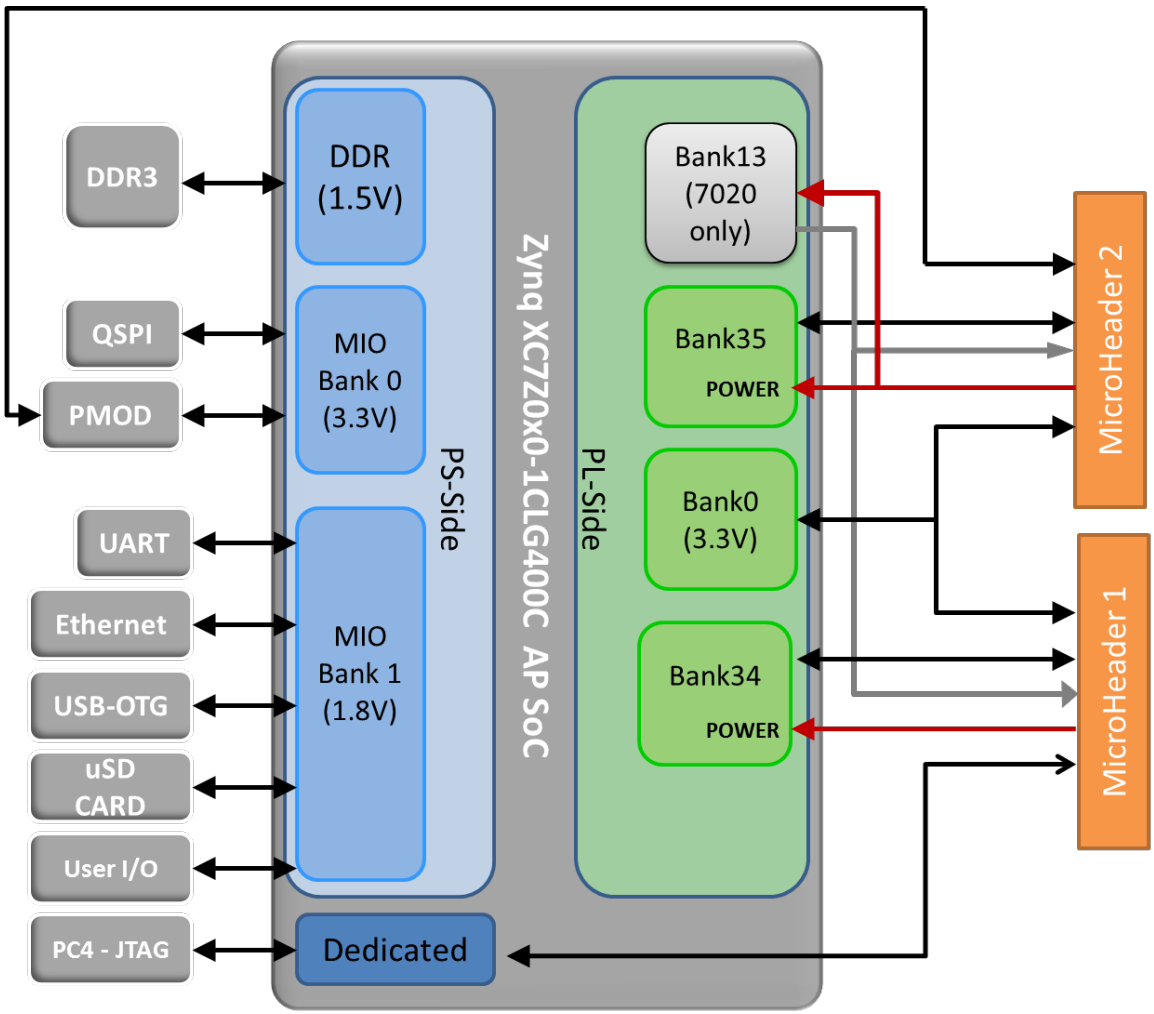


Figure 2 – Zynq CLG400 Bank Assignments

2 Functional Description

2.1 All Programmable SoC

MicroZed includes a Xilinx Zynq XC7Z010-1CLG400C or Zynq XC7Z020-1CLG400C AP SoC. Other temperature or speed grades are available as a custom order through Avnet Engineering Services.

2.2 Memory

Zynq contains a hardened PS memory interface unit. The memory interface unit includes a dynamic memory controller and static memory interface modules. MicroZed takes advantage of these interfaces to provide system RAM as well as two different bootable, non-volatile memory sources.

2.2.1 DDR3

MicroZed includes two Micron MT41K256M16HA-125:E DDR3 memory components creating a 256M x 32-bit interface, totaling 1 GB of random access memory. The DDR3 memory is connected to the hard memory controller in the PS of the Zynq AP SoC. The PS incorporates both the DDR controller and the associated PHY, including its own set of dedicated I/Os. Speed of up to 1,066 MT/s for DDR3 is supported.

The DDR3 interface uses 1.5V SSTL-compatible inputs. DDR3 Termination is utilized on the MicroZed and configured for fly-by routing topology, as recommended in AR55820. Additionally the board trace lengths are matched, compensating for the XC7Z010-CLG400 internal package flight times, to meet the requirements listed in the Zynq-7000 AP SoC PCB Design and Pin Planning Guide (UG933).

All single-ended signals are routed with 40 ohm trace impedance. DCI resistors (VRP/VRN), as well as differential clocks, are set to 80 ohms. DDR3-CKE0 is terminated through 40 ohms to VTT as described in AR51778. DDR3-ODT has the same 40 ohm to VTT termination. At the time of the MicroZed design, there was a discrepancy in the Xilinx documentation regarding whether DDR3-RESET# should have 40 ohms to VTT or 4.7K ohm to GND, which is why JT6 was designed in to give both options. Xilinx has since clarified that 4.7K-ohm to GND is the correct configuration for DDR3-RESET#. See AR55616.

Each DDR3 chip has its own 240-ohm pull-down on ZQ. Note DDR-VREF is not the same as DDR-VTT.

Table 1 – DDR3 Connections

Signal Name	Description	Zynq AP SOC pin	DDR3 pin
DDR_CK_P	Differential clock output	L2	J7
DDR_CK_N	Differential clock output	M2	K7
DDR_CKE	Clock enable	N3	K9
DDR_CS_B	Chip select	N1	L2
DDR_RAS_B	RAS row address select	P4	J3
DDR_CAS_B	RAS column address select	P5	K3
DDR_WE_B	Write enable	M5	L3
DDR_BA[2:0]	Bank address	PS_DDR_BA[2:0]	BA[2:0]
DDR_A[14:0]	Address	PS_DDR_A[14:0]	A[14:0]
DDR_ODT	Output dynamic termination	N5	K1
DDR_RESET_B	Reset	B4	T2
DDR_DQ[31:0]	I/O Data	PS_DDR_[31:0]	DDR3_DQ pins
DDR_DM[3:0]	Data mask	PS_DDR_DM[3:0]	LDM/UDM x2
DDR_DQS_P[3:0]	I/O Differential data strobe	PS_DDR_DQS_P[3:0]	UDQS/LDQS
DDR_DQS_N[3:0]	I/O Differential data strobe	PS_DDR_DQS_N[3:0]	UDQS#/LDQS#
DDR_VRP	I/O Used to calibrate input termination	H5	N/A
DDR_VRN	I/O Used to calibrate input termination	G5	N/A
DDR_VREF[1:0]	I/O Reference voltage	H6, P6	DDR_VREF

2.2.2 SPI Flash

MicroZed features a 4-bit SPI (quad-SPI) serial NOR flash. The Spansion S25FL128S (S25FL128SAGBHI200) is used on this board. The Multi-I/O SPI Flash memory is used to provide non-volatile boot, application code, and data storage. It can be used to initialize the PS subsystem as well as configure the PL subsystem (bitstream). Spansion provides Spansion Flash File System (FFS) for use after booting the Zynq-7000 AP SoC.

The relevant device attributes are:

- 128Mbit
- x1, x2, and x4 support
- Speeds up to 104 MHz, supporting Zynq configuration rates @ 100 MHz
  - In Quad-SPI mode, this translates to 400Mbs
- Powered from 3.3V

The SPI Flash connects to the Zynq PS QSPI interface. This requires connection to specific pins in MIO Bank 0/500, specifically MIO[1:6,8] as outlined in the Zynq TRM. Quad-SPI feedback mode is used, thus qspi_sclk_fb_out/MIO[8] is connected to a 20K pull-up resistor to 3.3V and nothing else. This allows a QSPI clock frequency greater than FQSPICLK2. The 20K pull-up straps vmode[1], setting the Bank 1 Voltage to 1.8V.

Table 2 – QSPI Flash Pin Assignment and Definitions

Signal Name	Description	Zynq Pin	MIO	QSPI Pin
CS	Chip Select	A7 (MIO Bank 0/500)	1	1
DQ0	Data0	B8 (Bank MIO0/500)	2	5
DQ1	Data1	D6 (MIO Bank 0/500)	3	2
DQ2	Data2	B7 (MIO Bank 0/500)	4	3
DQ3	Data3	A6 (MIO Bank 0/500)	5	7
SCK	Serial Data Clock	A5 (MIO Bank 0/500)	6	6
FB Clock	QSPI Feedback	D5 (MIO Bank 0/500)	8	N/A

Note: The QSPI data and clock pins are shared with the vmode and BOOT_MODE jumpers.

2.2.3 microSD Card Interface

The Zynq PS SD/SDIO peripheral controls communication with the MicroZed microSD Card. A 4GB card is included in the MicroZed kit. The microSD card can be used for non-volatile external memory storage as well as booting the Zynq-7000 AP SoC. PS peripheral sd0 is connected through Bank 1/501 MIO[40-46], including Card Detect. microSD cards do not include a Write Protect signal, but the Linux driver expects to have one. Therefore, MicroZed connects MIO[50] as a SD_WP pin that simply goes to a pull-down. This signal is not connected to the microSD card in any way; it was added only for increased Linux compatibility.

The microSD Card is a 3.3V interface but is connected through MIO Bank 1/501 which is set to 1.8V. Therefore, a Maxim MAX13035EETE+ level shifter performs this voltage translation. The MAX13035 is 6-channel, bidirectional level translator that provides the level shifting necessary for 100Mbps data transfer in multi-voltage systems. The MAX13035E is ideally suited for memory-card level translation, as well as generic level translation in systems with six channels.

As stated in the Zynq TRM, host mode is the only mode supported.

The MicroZed microSD Card is connected through a 8-pin micro SD card connector, J6, Molex 502570-0893. A Class 4 card or better is recommended. Up to 32 GB is supported.

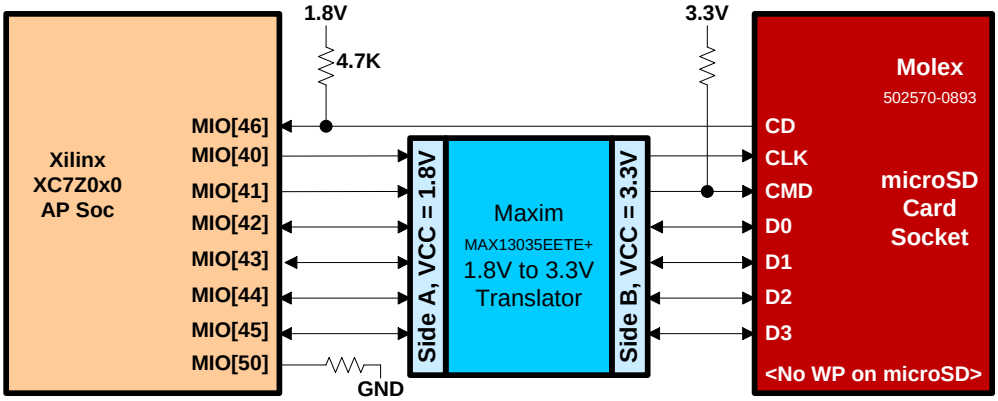


Figure 3 – microSD Card Interface

Table 3 – microSD Card Pin Assignment and Definitions

Signal Name	Description	Zynq Pin	MIO	Level Shift Pin	SD Card Pin
CLK	Clock	D14 (MIO Bank 1/501)	40	Pass-Thru	5
CMD	Command	C17 ((MIO Bank 1/501)	41	Pass-Thru	3
Data[3:0]	Data	MIO Bank 1/501 D0: E12 D1: A9 D2: F13 D3: B15	42:45	Pass-Thru	Data Pins 7 8 1 2
CD	Card Detect	D16 (MIO Bank 1/501)	46	Pass-Thru	CD
WP	Write Protect	B13 MIO Bank 1/501	50	N/C	N/C

2.3 USB

2.3.1 USB Host 2.0

MicroZed implements one of the two available PS USB 2.0 interfaces. An external PHY with an 8-bit ULPI interface is required. A SMSC USB3320 Standalone USB Transceiver Chip is used as the PHY. The PHY features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbs. VDDio for this device can be 1.8V or 3.3V, and on MicroZed it is powered at 1.8V. The PHY is connected to MIO Bank 1/501, which is also powered at 1.8V. This is critical since a level translator cannot be used as it would impact the tight ULPI timing.

Additionally the USB chip must clock the ULPI interface which requires a 24 MHz crystal or oscillator (configured as ULPI Output Clock Mode). On MicroZed, the 24 MHz oscillator is a Discera DSC1001 CMOS oscillator.

The USB connector is Type A and is combined with the Ethernet RJ45. This combination connector is J1, Bel-Fuse 0821-1X1T-43-F.

The usb0 peripheral is used on the PS, connected through MIO[28-39] in MIO Bank 1/501. With the USB Reset signal connected to MIO[7]. Signal PS_MIO7 is a 3.3V signal. It is AND-ed with the power-on reset (PG_MODULE) signal and then level shifted to 1.8V through U8, TI TXS0102 before connecting to the USB3320 Pin 27 RESET.

MicroZed is preconfigured for USB Host mode by default. The mode can be changed to Device mode by changing the following components:
To put MicroZed in Device Mode:

- Remove C1 (100uF)
- Remove C3 (22uF)
- Remove R50
- Remove L10 (not populated by default)
- Replace R56 with a 10KΩ resistor.

Note that MicroZed does not support OTG mode since a 5-pin USB connector is not used, therefore the ID pin is not available to detect role change. Zynq and the SMSC PHY both support OTG mode with a USB connector that supports it.

In the default Host mode, MicroZed provides the Vbus supply. In the default standalone mode where the MicroZed is powered from the USB-UART port, the amount of power available to the MicroZed is limited. Therefore, care should be taken in this USB-UART powered mode to only attach devices to the USB Host that consume less than 100 mA.

When MicroZed is powered via a carrier board or through the on-board DC barrel jack with 5V, MicroZed can deliver up to 500mA of 5V on Vbus via a pass-through resistor, R50. MicroZed also has a non-default option of being driven by a 12V input. In this case, a 12V-to-5V power supply must be populated when in Host mode. When the 12V-to-5V circuit is populated, R50 must be removed. See schematic for details.

Table 4 – USB Host Pin Assignment and Definitions

Signal Name	Description	Zynq Bank	MIO	SMSC 3320 Pin	USB Conn Pin
Data[7:0]	USB Data lines	MIO Bank 1/501	28:39	Data[7:0]	N/C
REFCLOCK	USB Clock	MIO Bank 1/501		26	N/C
DIR	ULPI DIR output signal	MIO Bank 1/501		31	N/C
STP	ULPI STP input signal	MIO Bank 1/501		29	N/C
NXT	ULPI NXT output signal	MIO Bank 1/501		2	N/C
REFSEL[2:0]	USB Chip Select	N/C	N/C	8,11,14	N/C
DP	DP pin of USB Connector			18	2
DM	DM pin of USB Connector			19	3
ID	Identification pin of the USB connector			23	4
RESET_B	Reset	MIO Bank 1/501	7**	27**	N/C

** Connected through AND-gate with PG_MODULE through level translator (TI TXS0102DQE).

2.3.2 USB-to-UART Bridge

MicroZed implements a USB-to-UART bridge connected to a PS UART peripheral. A Silicon Labs CP2104 USB-to-UART Bridge device allows connection to a host computer. The USB/UART device connects to the USB Micro AB connector, J2, (FCI 10104111-0001LF). Only basic TXD/RXD connection is implemented.

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers which permit the CP210x USB-to-UART bridge to appear as a COM port to host computer communications application software (for example, HyperTerm or Tera Term). Please refer to the Silicon Lab's website for detailed instructions for installing the driver. Note that each CP2104 ships with a unique ID and appears as a unique device when connected to a PC. Windows will enumerate multiple MicroZed boards with a unique COM port for each one. This means that multiple MicroZeds can be connected to a single PC without issue.

The uart1 Zynq PS peripheral is accessed through MIO[48:49] in MIO Bank 1/501 (1.8V). The CP2104 features adjustable I/O voltage, so it is connected directly to Zynq.

This USB port can power the board. By USB specification, a single USB port can only supply a maximum of 500 mA @ 5V. For simply PS experimentation, this is enough.

However, when powered from this port, it is recommended that less than 100mA @ 5V be consumed on the USB-Host interface. Also, if the PL fabric is exercised in the design, the 2.5W available on a single USB port may not be enough.

Additional power could be obtained by switching over to a USB Y-cable (with two connections to the Host for 1A) or connecting to a USB 3.0 port. MicroZed is also designed to get power from the carrier card or by populating a DC barrel jack (J4).

Table 5 – CP2104 Connections

UART Function in Zynq	Zynq Pin	MIO	Schematic Net Name	CP2104 Pin	UART Function in CP2104
TX, data out	B12 (MIO Bank 1/501)	48	USB_1_RXD	23	RXD, data in
RX, data in	C12 (MIO Bank 1/501)	49	USB_1_TXD	4	TXD, data out

2.3.3 USB circuit protection

All USB data lines, D+/-, are protected with Bourns Steering Diodes, CDSOT23-SR208.

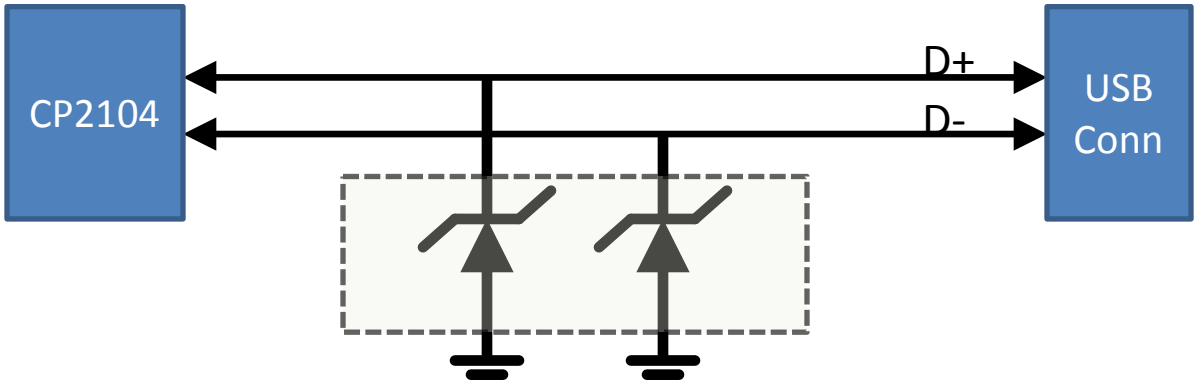


Figure 4 – ESD Protection

2.4 Clock source

The MicroZed connects a dedicated 33.3333 MHz clock source to the Zynq-7000 AP SoC's PS. A Discera DSC1001DI1-033.3300 with 40-ohm series termination is used. The PS infrastructure can generate up to four PLL-based clocks for the PL system. An attached carrier card can also supply clocks to the PL subsystem.

2.5 Reset Sources

2.5.1 Power-on Reset (PS_POR_B)

The Zynq PS supports an external power-on reset signal. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. On MicroZed this signal, labeled PG_MODULE, is connected to the power good output of the final stage of the power regulation circuitry. These power supplies have open drain outputs that pull this signal low until the output voltage is valid. If a carrier card is connected to MicroZed, the carrier card should also wire-OR to this net and not release it until the carrier card power is also good. Other IC's on MicroZed are reset by this signal as well.

To stall Zynq boot-up, this signal should be held low. No other signal (SRST, PROGRAM_B, INIT_B) is capable of doing this as in other FPGA architectures.

2.5.2 Program_B, DONE, PUDC_B, INIT_B

INIT_B, Program_B_0 and PUDC_B all have 4.7K-ohm pull-ups to 3.3V. INIT_B, PUDC_B and DONE signals are routed to the carrier card via the MicroHeaders, JX1 and JX2.

When PL configuration is complete, a blue LED D2, labeled DONE, will light.

2.5.3 Processor Subsystem Reset

System reset, labeled PS_SRST#, resets the processor as well as erases all debug configurations. The external system reset allows the user to reset all of the functional logic within the device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. System reset does not re-sample the boot mode strapping pins.

This active-low signal can be asserted by a pushbutton, SW2. Through an open-drain buffer, this signal also connects to the carrier card via the MicroHeader and the PC4 JTAG interface.

Note: This signal cannot be asserted while the boot ROM is executing following a POR reset. If PS_SRST_B is asserted while the boot ROM is running through a POR reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or PS_POR_B needs to be asserted.

2.6 User I/O

2.6.1 User Push Button

MicroZed provides 1 user GPIO push button to the Zynq-7000 AP SoC; interfacing to the PS. A pull-down resistor provides a known default state. Pushing the button connects the I/O to Vcco.

Table 6 – Push Button Connections

Signal Name	Subsection	MIO Pin	Zynq pin
PB1	PS (MIO Bank 500)	MIO[51]	B9

2.6.2 User LED

The MicroZed has one user LED. A logic high from the Zynq-7000 AP SoC I/O causes the LED to turn on.

Table 7 – LED Connections

REFDES	Subsection	MIO Pin	Zynq pin
D3	PS (MIO Bank 501)	MIO[47]	B14

2.7 10/100/1000 Ethernet PHY

MicroZed implements a 10/100/1000 Ethernet port for network connection using a Marvell 88E1512 PHY. This part operates at 1.8V. The PHY connects to MIO Bank 1/501 (1.8V) and interfaces to the Zynq-7000 AP SoC via RGMII.

The RJ-45 connector, J1 (BEL 0821-1X1T-43-F), is shared with the USB-Host interface. The RJ-45 integrates two status indicator LEDs that indicate traffic and valid link state.

A high-level block diagram the 10/100/1000 Ethernet interface is shown in the following figure.

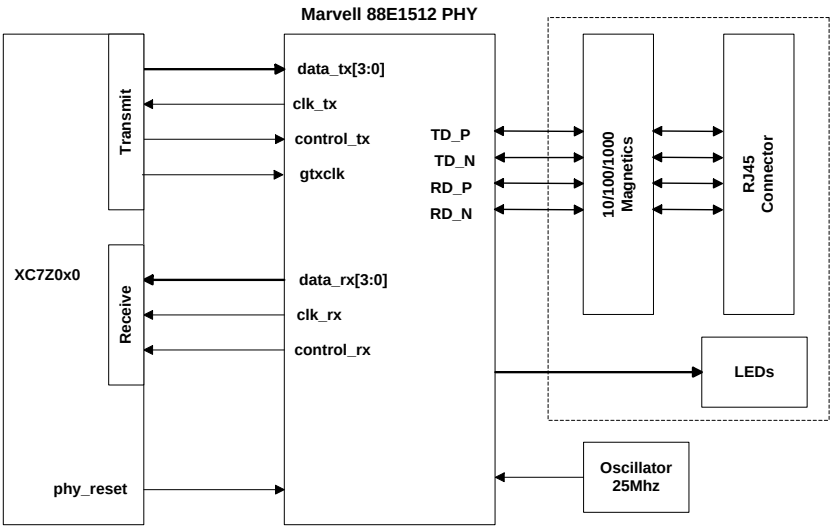


Figure 5 – 10/100/1000 Ethernet Interface

Zynq requires a voltage reference for RGMII interfaces. Thus PS_MIO_VREF, E11, is tied to 0.9V, half the bank voltage of MIO Bank 1/501. The 0.9V is generated through a resistor divider.

The 88E1512 also requires a 25 MHz input clock. A Discera DSC1001DI1-025.0000 is used as this reference.

Table 8 – Ethernet PHY Pin Assignment and Definitions

Signal Name	Description	Zynq pin	MIO	88E1512 pin
RX_CLK	Receive Clock	B17	16:27	46
RX_CTRL	Receive Control	D13		43
RXD[3:0]	Receive Data	RXD0: D11 RXD1: A16 RXD2: F15 RXD3: A15		44 45 47 48
TX_CLK	Transmit Clock	A19		53
TX_CTRL	Transmit Control	F14		56
TXD[3:0]	Transmit Data	TXD0: E14 TXD1: B18 TXD2: D10 TXD3: A17		50 51 54 55
MDIO	Management Data	C11	53	8
MDC	Management Clock	C10	52	7
ETH_RST_N	PHY Reset	--	--	16**

****** Controlled via level translator U8 and can be held low using PG_MODULE signal.

The datasheet for the Marvell 88E1512 is not available publicly. An NDA is required for this information. Please contact your local Avnet Memec or Marvell representative for assistance.

2.8 Expansion Headers

2.8.1 Digilent Pmod™ Compatible Header (2x6)

MicroZed has one Digilent Pmod™ compatible header (2x6), J5. This is a right-angle, 0.1" female header (Bourns BCS-106-L-D-TE) that includes eight user I/O plus 3.3V and ground signals as shown in the figure below.

The Digilent Pmod compatible interface connects to the PS-side on MIO pins [0, 9-15] in MIO Bank 0/500 (3.3V). Uses for this Digilent Pmod compatible interface include PJTAG access (MIO[10-13]) as well as nine other hardened MIO peripherals (SPI, GPIO, CAN, I2C, UART, SD, QSPI, Trace, Watchdog).

These 8 MIO pins are also routed to the MicroHeader so they can be utilized on an expansion carrier card. NOTE: These MIO pins should not be simultaneously used by both the MicroZed and MicroHeader interfaces.

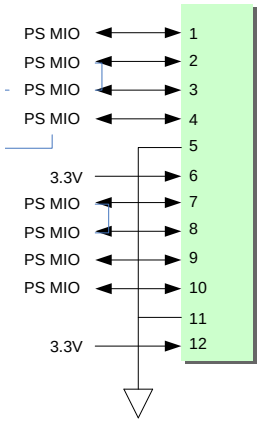


Figure 6 – Digilent Pmod™ Compatible Interface Connections

Table 9 – Digilent Pmod™ Compatible Interface Connections

Pmod	Signal Name	PS MIO Pin	Zynq pin
J5 MIO Pmod	PMOD_D0	MIO 13	E8
	PMOD_D1	MIO 10	E9
	PMOD_D2	MIO 11	C6
	PMOD_D3	MIO 12	D9
	PMOD_D4	MIO 0	E6
	PMOD_D5	MIO 9	B5
	PMOD_D6	MIO 14	C5
	PMOD_D7	MIO 15	C8

2.8.2 MicroHeaders

MicroZed features two 100-pin MicroHeaders (FCI, 61082-101400LF) for connection to expansion carrier cards. Each connector interfaces PL I/O to the carrier card as well as eight PS-MIO, two dedicated analog inputs, the four dedicated JTAG signals, power and control signals.

NOTE: The eight PS-GPIO and four JTAG signals are shared on MicroZed, thus for each interface, it can only be used on either MicroZed or the carrier card, not simultaneously.

The connectors are FCI 0.8mm Bergstak®, 100 Position, Dual Row, BTB Vertical Receptacles. These have variable stack heights from 5mm to 16mm, making it easy to connect to a variety of expansion or system boards. The carrier card can power MicroZed as an alternative to the on-board USB-UART port or DC jack. Each pin can carry 500mA of current and support I/O speeds in excess of what Zynq can achieve.

MicroZed does not power the PL VCC_{IO} banks. This is required by the carrier card. This gives the carrier card the flexibility to control the I/O bank voltages. Separate routes/planes are used for Vcco_34 and Vcco_35 such that the carrier card could potentially power these independently. The 7Z010 has two PL I/O banks, banks 34 and 35, each containing 50 I/O. If populated with a 7Z020, the 7Z020 has a third I/O bank, bank 13, which is partially connected on MicroZed. Bank 13's power has an independent rail, Vcco_13, which is powered from the Carrier.

NOTE: When used without a carrier card, the PL I/O banks are unpowered on MicroZed. However, the PL fabric is still available for custom HDL logic, without access to PL I/O.

Within a PL I/O bank, there are 50 I/O capable of up to 24 differential pairs. Differential LVDS pairs on a -1 speed grade device are capable of 950Mbps of DDR data. Each differential pair is isolated by a power or ground pin. Additionally, eight of these I/O can be connected as clock inputs (four MRCC and four SRCC inputs). Each PL bank can also be configured to be a memory interface with up to four dedicated DQS data strobes and data byte groups. Bank 35 adds the capability to use the I/O to interface up to 16 differential analog inputs. One of the differential pairs (JX1_LVDS_2) in Bank 34 is shared with PUDC_B.

MicroZed was designed with MIG DDR3 memory DQ byte groups*. The existing byte groups are defined in the table below:

Table 10 – DQ Byte Groups

Byte Group	Zynq Pins	Byte Group	Zynq Pins	Byte Group	Zynq Pins	Byte Group	Zynq Pins
DQ[7:0]	B20 B19 A20 D19 D20 E18 E19 F16	DQ[15:8]	M20 M17 M18 K19 J19 L16 L17 K17	DQ[23:16]	H16 H17 J18 H18 G18 J20 H20 G19	DQ[31:24]	G15 K14 J14 L14 L15 M14 M15 K16

**As chosen by MIG 14.4 for a 7Z010-CLG400 package.*

The diagram below illustrates the connections on the MicroHeader.

Table 11 – MicroHeader Pinout

MicroHeader #1 (JX1)				MicroHeader #2 (JX2)			
Signal Name		**Source**	**Pin Count**	**Signal Name**		**Source**	**Pin Count**
PL	Bank 34 I/Os (except for PUDC_B)	Zynq Bank 34	49	PL	Bank 35 I/Os	Zynq Bank 35	50
JTAG	TMS_0	Zynq Bank 0	5	PS	PS Pmod MIO[0,9-15]	Zynq Bank 500	8
	TDI_0	Zynq Bank 0					
	TCK_0	Zynq Bank 0		C	Init_B_0	Zynq Bank 0	2
	TDO_0	Zynq Bank 0		Power	Vccio_EN	Module/Carrier	1
	Carrier_SRST#	Carrier			PG_MODULE	Module/Carrier	1
Analog	VP_0	Zynq Bank 0	4		Vin	Carrier	5
	VN_0	Zynq Bank 0			GND	Carrier	23
	DXP_0	Zynq Bank 0			VCCO_35	Carrier	3
	DXN_0	Zynq Bank 0			Bank 13 pins	Bank 13 **	7
C	PUDC_B / IO	Zynq Bank 34	2	**Total**			100
	DONE	Zynq Bank 0					
Power	PWR_Enable	Carrier	1				
	Vin	Carrier	4				
	GND	Carrier	23				
	VCCO_34	Carrier	3				
	VBATT	Carrier	1				
	Bank 13 pins	Bank 13 **	8				
TOTAL			100				

** 7020 device only

Table 12 – JX1 Connections

SoC Pin #	MicroZed Net	JX1 Pin #	JX1 Pin #	MicroZed Net	SoC Pin #
Bank 0, F9	JTAG_TCK	1	2	JTAG_TMS	Bank 0, J6
Bank 0, F6	JTAG_TDO	3	4	JTAG_TDI	Bank 0, G6
N/A	PWR_ENABLE	5	6	CARRIER_SRST#	N/A
N/A	FPGA_VBATT	7	8	FPGA_DONE	Bank 0, R11
Bank 34, R19	JX1_SE_0	9	10	JX1_SE_1	Bank 34, T19
Bank 34, T11	JX1_LVDS_0_P	11	12	JX1_LVDS_1_P	Bank 34, T12
Bank 34, T10	JX1_LVDS_0_N	13	14	JX1_LVDS_1_N	Bank 34, U12
N/A	**GND**	15	16	**GND**	N/A
Bank 34, U13	JX1_LVDS_2_P	17	18	JX1_LVDS_3_P	Bank 34, V12
Bank 34, V13	JX1_LVDS_2_N	19	20	JX1_LVDS_3_N	Bank 34, W13
N/A	**GND**	21	22	**GND**	N/A
Bank 34, T14	JX1_LVDS_4_P	23	24	JX1_LVDS_5_P	Bank 34, P14
Bank 34, T15	JX1_LVDS_4_N	25	26	JX1_LVDS_5_N	Bank 34, R14
N/A	**GND**	27	28	**GND**	N/A
Bank 34, Y16	JX1_LVDS_6_P	29	30	JX1_LVDS_7_P	Bank 34, W14
Bank 34, Y17	JX1_LVDS_6_N	31	32	JX1_LVDS_7_N	Bank 34, Y14
N/A	**GND**	33	34	**GND**	N/A
Bank 34, T16	JX1_LVDS_8_P	35	36	JX1_LVDS_9_P	Bank 34, V15
Bank 34, U17	JX1_LVDS_8_N	37	38	JX1_LVDS_9_N	Bank 34, W15
N/A	**GND**	39	40	**GND**	N/A
Bank 34, U14	JX1_LVDS_10_P	41	42	JX1_LVDS_11_P	Bank 34, U18
Bank 34, U15	JX1_LVDS_10_N	43	44	JX1_LVDS_11_N	Bank 34, U19
N/A	**GND**	45	46	**GND**	N/A
Bank 34, N18	JX1_LVDS_12_P	47	48	JX1_LVDS_13_P	Bank 34, N20
Bank 34, P19	JX1_LVDS_12_N	49	50	JX1_LVDS_13_N	Bank 34, P20
N/A	**GND**	51	52	**GND**	N/A
Bank 34, T20	JX1_LVDS_14_P	53	54	JX1_LVDS_15_P	Bank 34, V20
Bank 34, U20	JX1_LVDS_14_N	55	56	JX1_LVDS_15_N	Bank 34, W20
N/A	**VIN_HDR**	57	58	**VIN_HDR**	N/A
N/A	**VIN_HDR**	59	60	**VIN_HDR**	N/A
Bank 34, Y18	JX1_LVDS_16_P	61	62	JX1_LVDS_17_P	Bank 34, V16
Bank 34, Y19	JX1_LVDS_16_N	63	64	JX1_LVDS_17_N	Bank 34, W16
N/A	**GND**	65	66	**GND**	N/A
Bank 34, R16	JX1_LVDS_18_P	67	68	JX1_LVDS_19_P	Bank 34, T17
Bank 34,R17	JX1_LVDS_18_N	69	70	JX1_LVDS_19_N	Bank 34, R18
N/A	**GND**	71	72	**GND**	N/A
Bank 34, V17	JX1_LVDS_20_P	73	74	JX1_LVDS_21_P	Bank 34, W18
Bank 34, V18	JX1_LVDS_20_N	75	76	JX1_LVDS_21_N	Bank 34, W19
N/A	**GND**	77	78	**VCCO_34**	N/A
N/A	**VCCO_34**	79	80	**VCCO_34**	N/A
Bank 34, N17	JX1_LVDS_22_P	81	82	JX1_LVDS_23_P	Bank 34, P15
Bank 34, P18	JX1_LVDS_22_N	83	84	JX1_LVDS_23_N	Bank 34, P16
N/A	**GND**	85	86	**GND**	N/A
Bank 13, U7	BANK13_LVDS_0_P	87	88	BANK13_LVDS_1_P	Bank 13, T9
Bank 13, V7	BANK13_LVDS_0_N	89	90	BANK13_LVDS_1_N	Bank 13, U10
Bank 13, V8	BANK13_LVDS_2_P	91	92	BANK13_LVDS_3_P	Bank 13, T5
Bank 13, W8	BANK13_LVDS_2_N	93	94	BANK13_LVDS_3_N	Bank 13, U5
N/A	**GND**	95	96	**GND**	N/A
Bank 0, L10	VP_0_P	97	98	DXP_0_P	Bank 0, M9
Bank 0, K9	VN_0_N	99	100	DXN_0_N	Bank 0, M10

Table 13 – JX2 Connections

SoC Pin #	MicroZed Net	JX2 Pin #	JX2 Pin #	MicroZed Net	SoC Pin #
Bank 500, E8	PMOD_D0	1	2	PMOD_D1	Bank 500, E9
Bank 500, C6	PMOD_D2	3	4	PMOD_D3	Bank 500, D9
Bank 500, E6	PMOD_D4	5	6	PMOD_D5	Bank 500, B5
Bank 500, C5	PMOD_D6	7	8	PMOD_D7	Bank 500, C8
Bank 0, R10	INIT#	9	10	VCCIO_EN	N/A
Bank 500, C7	PG_MODULE	11	12	**VIN_HDR**	N/A
Bank 35, G14	JX2_SE_0	13	14	JX2_SE_1	Bank 35, J15
N/A	**GND**	15	16	**GND**	N/A
Bank 35, C20	JX2_LVDS_0_P	17	18	JX2_LVDS_1_P	Bank 35, B19
Bank 35, B20	JX2_LVDS_0_N	19	20	JX2_LVDS_1_N	Bank 35, A20
N/A	**GND**	21	22	**GND**	N/A
Bank 35, E17	JX2_LVDS_2_P	23	24	JX2_LVDS_3_P	Bank 35, D19
Bank 35, D18	JX2_LVDS_2_N	25	26	JX2_LVDS_3_N	Bank 35, D20
N/A	**GND**	27	28	**GND**	N/A
Bank 35, E18	JX2_LVDS_4_P	29	30	JX2_LVDS_5_P	Bank 35, F16
Bank 35, E19	JX2_LVDS_4_N	31	32	JX2_LVDS_5_N	Bank 35, F17
N/A	**GND**	33	34	**GND**	N/A
Bank 35, L19	JX2_LVDS_6_P	35	36	JX2_LVDS_7_P	Bank 35, M19
Bank 35, L20	JX2_LVDS_6_N	37	38	JX2_LVDS_7_N	Bank 35, M20
N/A	**GND**	39	40	**GND**	N/A
Bank 35, M17	JX2_LVDS_8_P	41	42	JX2_LVDS_9_P	Bank 35, K19
Bank 35, M18	JX2_LVDS_8_N	43	44	JX2_LVDS_9_N	Bank 35, J19
N/A	**GND**	45	46	**GND**	N/A
Bank 35, L16	JX2_LVDS_10_P	47	48	JX2_LVDS_11_P	Bank 35, K17
Bank 35, L17	JX2_LVDS_10_N	49	50	JX2_LVDS_11_N	Bank 35, K18
N/A	**GND**	51	52	**GND**	N/A
Bank 35, H16	JX2_LVDS_12_P	53	54	JX2_LVDS_13_P	Bank 35, J18
Bank 35, H17	JX2_LVDS_12_N	55	56	JX2_LVDS_13_N	Bank 35, H18
N/A	**VIN_HDR**	57	58	**VIN_HDR**	N/A
N/A	**VIN_HDR**	59	60	**VIN_HDR**	N/A
Bank 35, G17	JX2_LVDS_14_P	61	62	JX2_LVDS_15_P	Bank 35, F19
Bank 35, G18	JX2_LVDS_14_N	63	64	JX2_LVDS_15_N	Bank 35, F20
N/A	**GND**	65	66	**GND**	N/A
Bank 35, G19	JX2_LVDS_16_P	67	68	JX2_LVDS_17_P	Bank 35, J20
Bank 35, G20	JX2_LVDS_16_N	69	70	JX2_LVDS_17_N	Bank 35, H20
N/A	**GND**	71	72	**GND**	N/A
Bank 35, K14	JX2_LVDS_18_P	73	74	JX2_LVDS_19_P	Bank 35, H15
Bank 35, J14	JX2_LVDS_18_N	75	76	JX2_LVDS_19_N	Bank 35, G15
N/A	**GND**	77	78	**VCCO_35**	N/A
N/A	**VCCO_35**	79	80	**VCCO_35**	N/A
Bank 35, N15	JX2_LVDS_20_P	81	82	JX2_LVDS_21_P	Bank 35,L14
Bank 35, N16	JX2_LVDS_20_N	83	84	JX2_LVDS_21_N	Bank 35,L15
N/A	**GND**	85	86	**GND**	N/A
Bank 35, M14	JX2_LVDS_22_P	87	88	JX2_LVDS_23_P	Bank 35, K16
Bank 35, M15	JX2_LVDS_22_N	89	90	JX2_LVDS_23_N	Bank 35, J16
N/A	**GND**	91	92	**GND**	N/A
Bank 13, Y12	BANK13_LVDS_4_P	93	94	BANK13_LVDS_5_P	Bank 13, V11
Bank 13, Y13	BANK13_LVDS_4_N	95	96	BANK13_LVDS_5_N	Bank 13, V10
Bank 13, V6	BANK13_LVDS_6_P	97	98	**VCCO_13**	N/A
Bank 13, W6	BANK13_LVDS_6_N	99	100	BANK13_SE_0	Bank 13, V5

** Pmod_JZ has only 7 connections thus cannot connect to QSPI or SD interfaces.

2.9 Configuration Modes

Zynq-7000 AP SoC devices use a multi-stage boot process that supports both non-secure and secure boot. The PS is the master of the boot and configuration process. Upon reset, the device mode pins are read to determine the primary boot device to be used: NOR, NAND, Quad-SPI, SD Card or JTAG. MicroZed allows 3 of those boot devices: QSPI is the default, while SD Card and JTAG boot are easily accessible by changing jumpers.

Additionally, Zynq has Voltage Mode pins, which are fixed on MicroZed

The boot mode pins are shared with MIO[8:2]. The usage of these mode pins can be and are used as follows:

- MIO[2] / Boot_Mode[3]
  - sets the JTAG mode
- MIO[5:3] / Boot_Mode[2:0]
  - select the boot mode
  - Boot_Mode[1] is fixed since it is only required for NOR boot, which is not supported on MicroZed
- MIO[6] / Boot_Mode[4]
  - enables the internal PLL
  - fixed to 'enabled' on MicroZed
- MIO[8:7] / Vmode[1:0]
  - configures the I/O bank voltages
  - fixed on MicroZed
  - MIO Bank 0 / 500 (MIO[7] / Vmode[0]) set to '0' for 3.3V
  - MIO Bank 1 / 501 (MIO[8] / Vmode[1]) set to '1' for 1.8V

All mode pins have resistor footprints such that any could be pulled either high or low through a 20 KΩ resistor if a designer chooses to experiment. By default, four mode signals are not jumper-adjustable and are populated as follows:

- MIO[3] / Boot_Mode[1] is pulled low via 20 KΩ resistor.
- MIO[6] / Boot_Mode[4] is pulled low via 20 KΩ resistor.
- MIO[7] / Vmode[0] is pulled low via 20 KΩ resistor.
- MIO[8] / Vmode[1] is pulled high via 20 KΩ resistor.

By default, the other three mode signals do not populate either resistor. Instead MicroZed provides jumpers for MIO[2], MIO[4] and MIO[5]. For a production development using MicroZed as a SOM, the jumpers can be replaced with the appropriate resistor population options exist to fix these permanently. A diagram for these three mode signals is shown below, with the pull-up option tied to Vcco for MIO Bank 0.

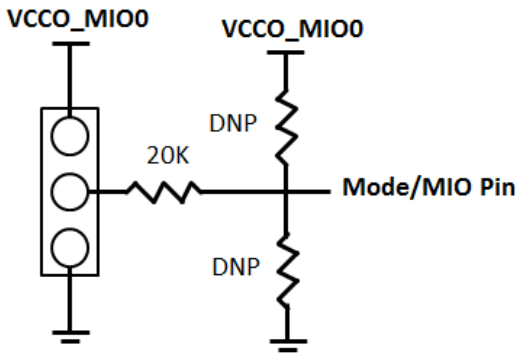


Figure 7 – Configuration Mode Jumpers

The 1x3 jumper options with default positions highlighted are shown below. The default position is Cascaded JTAG Chain, QSPI Boot.

Table 14 – MicroZed Configuration Modes

	JP3	JP2	JP1
Xilinx TRM→	Boot_Mode[0]	Boot_Mode[2]	Boot_Mode[3]
MIO→	MIO[5]	MIO[4]	MIO[2]
JTAG Mode			
Cascaded JTAG Chain			1-2 (0)
Independent JTAG Chain			2-3 (1)
Boot Devices			
JTAG	1-2 (0)	1-2 (0)	
Quad-SPI	2-3 (1)	1-2 (0)	
SD Card	2-3 (1)	2-3 (1)	

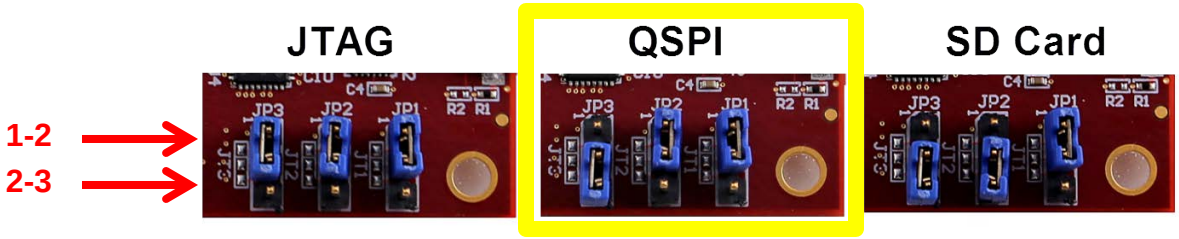


Figure 8– Boot Mode Jumper Settings with Cascaded JTAG Chain

Expected configuration time using a 50MB/s QSPI flash is 250ms.

Zynq has many other configuration options, MicroZed uses this configuration:

- V_{CCO_0} is tied to 3.3V on MicroZed.
- PUDC_B can be pulled high or low on MicroZed via a resistor (JT4). This active-low input enables internal pull-ups during configuration on all SelectIO pins. By default, JT4 is populated with a 1K resistor in the 1-2 position, which pulls up PUDC_B and disables the pull-ups during configuration. PUDC_B is shared with Bank 34 I/O IO_L3P and is connected to the MicroHeader.
- Init_B is pulled high via a 4.7KΩ resistor (RP2.2-7), but also connected to the MicroHeader.
- Program_B is pulled high via a 4.7KΩ resistor (RP2.4-5).
- CFGBVS is pulled high via a 4.7KΩ resistor (RP2.1-8).

The PS is responsible for reconfiguring the PL. Zynq will not automatically reconfigure the PL as in standard FPGAs by toggling PROG. Likewise, it is not possible to hold off Zynq boot up with INIT_B as this is now done with POR. If the application needs to reconfigure the PL, the software design must do this, or you can toggle POR to restart everything. When PL configuration is complete, a blue LED, D2, will light.

2.9.1 JTAG

MicroZed requires an external JTAG cable for JTAG operations. MicroZed is designed with the Platform Cable JTAG connector, Molex 87832-1420 which is a 2.0mm 2x7 shrouded, polarized header. On MicroZed, this is J3 and is compatible with Xilinx Platform Cables and Digilent JTAG HS1 or HS2 Programming Cables. The JTAG Reset signal is connected to PS_SRST_B through an open-drain buffer.

2.10 Power

2.10.1 Primary Power Input

MicroZed is designed to be used either as a Standalone evaluation kit or as a SOM connected to a Carrier Card. Supporting these multiple use cases required the board to be designed with multiple power input sources.

The board's default primary input in standalone mode is through the USB-UART connector, J2. Alternatively, a DC barrel jack footprint is provided that is compatible with CUI PJ-002B-SMT. This allows you to power MicroZed from a compatible AC/DC 5V converter with 2.5mm inner diameter, 5.5mm outer diameter, center positive connection.

One such compatible AC/DC supply from Emerson Network Power is:

- DA12-050MP-M – requires addition of plug
- Plugs
  - DA-US
  - DA-UK
  - DA-EU
  - DA-AU
  - DA-ALL

Additionally, in SOM mode, MicroZed is powered by a carrier card via the MicroHeader.

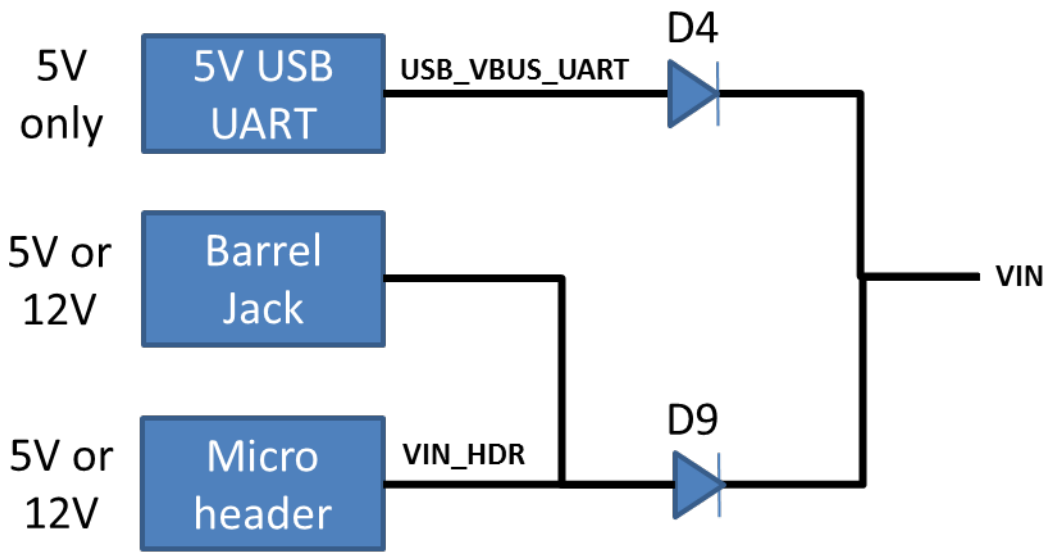


Figure 9 – Power Input Options

As shown in Figure 9, protection diodes were put in place to prevent one supply from back-powering another one. These diodes are Diodes Inc. B330A-13-F. It is expected that the voltage will drop ~0.5V over these diodes. At 4.5V for Vin, all regulators will continue to regulate properly.

When used as a production SOM, it is recommended that D4 be de-populated and D9 be replaced with a shunt. This can be done by special request through Avnet.

When powering from the USB-UART, be aware that the USB specification allows a maximum of 500mA for USB 2.0. With only 2.5W of power, the MicroZed will be able to operate in the default, out-of-box mode. During testing, the measured current of the MicroZed was 300-400mA while running a PS-only application exercising one cpu and RAM at maximum speeds. If you want to fill the PL fabric with logic, get more power on the PS Pmod or get more power on the USB-host Vbus, several options exist for standalone operation:

- Use a PC USB port that is capable of sourcing more than 500mA (or won't alert about supplying more than 500mA).

- Use a USB Y-Cable that connects to 2 ports on the PC for power. This will provide at a minimum twice the current capacity to the board (1.0 Amperes if following the USB specification, more if the PC port is not following the specification).

- Populate J4 barrel jack and use a 5V AC/DC supply rated for the projected current demand AND install the capacitors C212, C217, and C218.

*** Please note Vcco 13, 34 and 35 will NOT be powered in the above MicroZed stand-alone power modes. These banks are only powered when a suitable I/O Carrier Card is used.**

- Use an I/O Carrier Card, either from Avnet or one designed in-house. The Avnet Carrier Cards (IOCC, FMC) provide power to banks 13, 34 and 35.

If you intend to plug in a USB device to the USB-Host port while powered from USB-UART, it is recommended that this be a low-power device or a powered USB hub.

2.10.2 Regulators

The following power solution provides the power rails of the MicroZed. Sequencing of the supplies is implemented by cascading the POWER GOOD outputs of each supply to the ENABLE input for the next supply in the sequence. 3.3V is the last supply to come up, therefore the PG for the 3.3V supply is used to drive the PG_MODULE net and is used as the power-on reset control for Zynq(U9.pinC7), Ethernet PHY (U3.pin16), USB-Host PHY (U4.pin27) and USB_UART (U2.pin9).

This net is also connected to the MicroHeaders so power supplies on the carrier card can also control this signal.

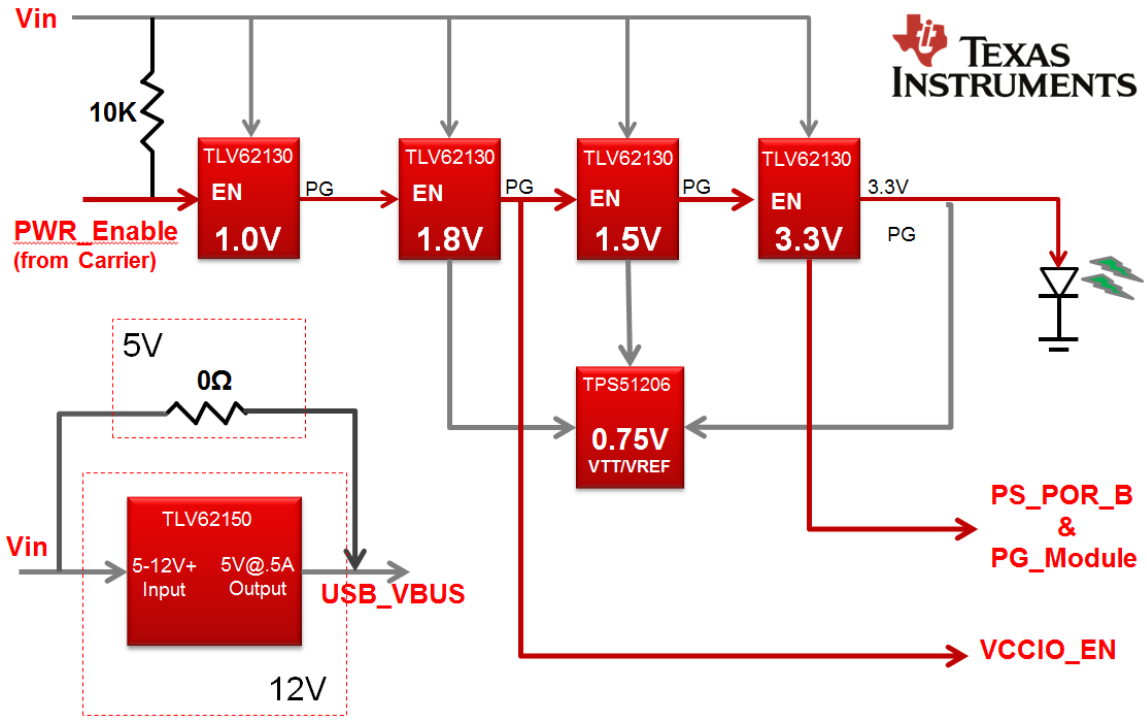


Figure 10 – Regulation Circuitry (VCCIO_EN specific to Rev C)

This circuit sequences power-up of MicroZed. 1.0V comes up first, then 1.8V, then 1.5V and then 3.3V. When 3.3V is valid in standalone mode, the Power Good (Module) LED, D5, is illuminated. PG_MODULE is connected to PS_POR_B on Zynq, thus when the power supplies are valid, PS_POR_B is released.

When plugged into a carrier card, the power good outputs of the carrier card should also be tied to the PG_MODULE net on JX2.pin11. If the carrier card power supplies do not have power good outputs, a voltage supervisor or open-drain buffer should be used to complement this circuit.

MicroZed also provides an Enable signal to the Carrier Card to signal that Vccint and Vccaux are both up and the Carrier is free to bring up the Vcco supplies. This signal is called VCCIO_EN and is tied to JX2.pin10.

- Rev B
  - VCCIO_EN is provided by 3.3V pull-up RP2.4-5, which is also used for PROGRAM#
- Rev C
  - VCCIO_EN is provided by the power good output of the 1.8V regulator.

The table below shows the minimum required voltage rails, currents, and tolerances.

Table 15 – Voltage Rails w/ Current Estimates

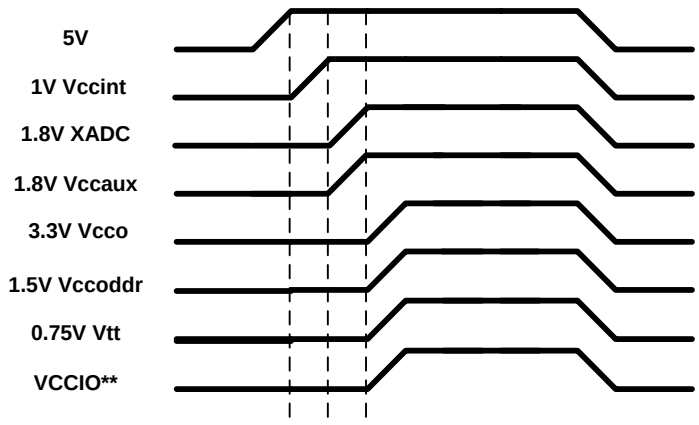
Voltage (V)	7010 Current (A)	7020 Current (A)	Tolerance	TI Part Number
1.0 (Vccint)	1.0	1.9	5.00%	TLV62130
1.5 (Vccoddr)	1.0	1.0	5.00%	TLV62130
1.8 (Vccaux)	0.8	0.9	5.00%	TLV62130
3.3 (Vcco/Pmod)	0.7	0.7	5.00%	TLV62150
1.8 (analog) (Vccadc)	0.15	0.15	5.00%	Filtered from 1.8V
0.75 (DDR3 Vtt)	0.400	0.400	5.00%	TPS51206
5.0 (USB-Host Vbus)*	0.5	0.5	5.00%	TLV62150

* Not populated by default

2.10.3 Sequencing

When attached to a carrier card, the carrier card must provide an active-high, power enable signal, PWR_ENABLE. This controls the first MicroZed regulator (U17, 1.0V) turning on. This should be an open drain design such that when MicroZed is in standalone mode, this signal will float high (pulled high to 5V on MicroZed via R87). This allows for the carrier card to control powering MicroZed. Thus it can be powered down in low power applications.

Sequencing for the power supplies follows the recommendations for the Zynq device. PS and PL INT and AUX supplies are tied together on the MicroZed platform to create a low cost design. The following diagram illustrates the supply sequencing:



** VCCIO driven from carrier card.

Figure 11 – Power Sequencing

As noted above, if connected to a carrier card, the 1.8V power supply's power good output should be used to enable the VCCIO regulators.

The following diagram illustrates sequencing with a carrier card:

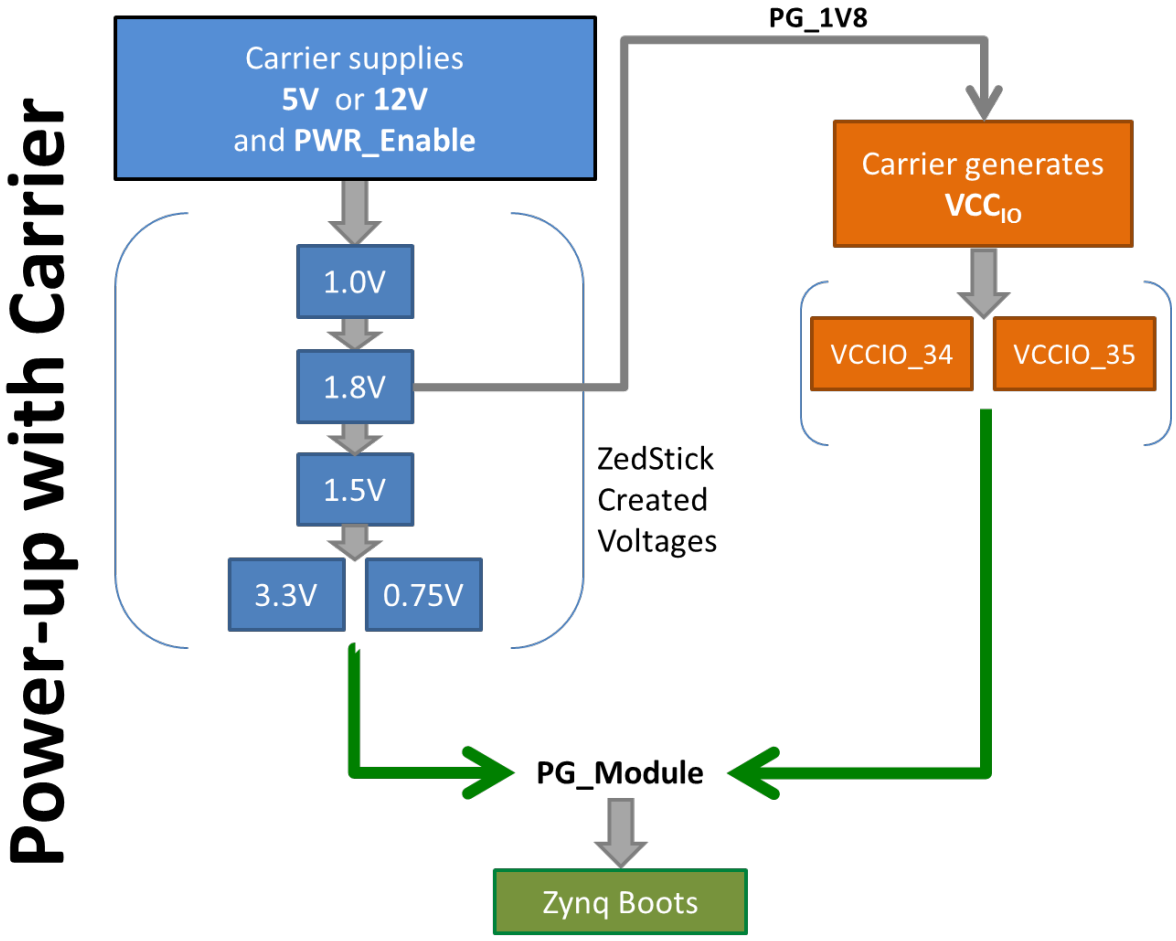


Figure 12 – Power Sequencing with Carrier Card

2.10.4 Bypassing/Decoupling

The MicroZed design follows the PCB decoupling strategy as outlined in UG933 for the 7Z020, CLG400 package. The 7Z010 MicroZed depopulates a few of these capacitors while maintaining the listed 7Z010 requirements.

Package	Device	V_{CCINT}					V_{CCBRAM}				V_{CCAUX}			V_{CCAUX_IO}			V_{CCO} per Bank			Bank 0
		680 µF	330 µF	100 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	47 µF
CLG400	7Z010	0	0	1	2	3	0	1	1	2	1	1	2	NA	NA	NA	1	3	5	1
CLG400	7Z020	0	1	0	5	7	1	0	2	3	1	1	2	NA	NA	NA	1	3	5	1

Figure 13 – CLG400 PL Decoupling

Package	Device	V_{CCPINT}			V_{CCPAUX}(2)			V_{CCO_DDR}			V_{CCO_MIO0}			V_{CCO_MIO1}			V_{CCPLL}(1)(3)	
		100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	10 µF	0.47 µF
CLG400	7Z010	1	3	5	1	2	3	2	3	7	1	1	2	1	2	3	1	1
CLG400	7Z020	1	3	5	1	2	3	2	3	7	1	1	2	1	2	3	1	1

Figure 14 – CLG400 PS Decoupling

2.10.5 Power Good LED

A green status LED, D5, illuminates with the U16 3.3V power rail. Since this regulator is the last one in the sequence to come up, it is an effective indication that all regulators are on.

2.10.6 Power Estimation

The total input power budget for the 7010 MicroZed consists of two components. The first is the power required for the module components. The calculation for the 7010 MicroZed is 4.8W for the circuits themselves, including the PL fabric utilized to 85% capacity and the PS Pmod consuming 100mA. See Table 16. To be conservative, the regulation efficiency is assumed to be 80%, although we expect it is much better than that. With a 5V input supply, this results in 1.2A (4.8W / 80% / 5V).

Table 16 – Current Usage Calculation for 7010 MicroZed

Feature	Est. Power (A)				W
	1.0V	1.5V	1.8V	3.3V	
7010-400*	0.89	0.33	0.28	0.15	2.2
1G DDR3		.600			1.0
DDR3 Term				.100	.3
USB Host ǂ			.03	0.03	.15
GIGE	.07		.09	0.05	.4
QSPI FLASH				0.10	.34
USB UART				0.03	.10
PMOD				0.1	.33
TOTAL	**.96**	**1.0**	**.4**	**.56**	**4.8**

ǂ *USB interface requires 500mA on 5V rail.*

* *Based on XPE 14.4, ~85% Utilization*

The second component is the USB-Host Vbus supply, which is required to be 500mA @ 5V.

Combining the two, the recommended, full-capacity 5V input supply is 1.7A (8.5W).

If using Vin = 12V, then 0.8A (9.6W) is recommended. ((4.8W + 2.5W) / 80% / 12V)

2.10.7 XADC Power Configuration

The XADC component is powered from the filtered 1.8V VCCaux supply utilizing the on-chip reference as shown below.

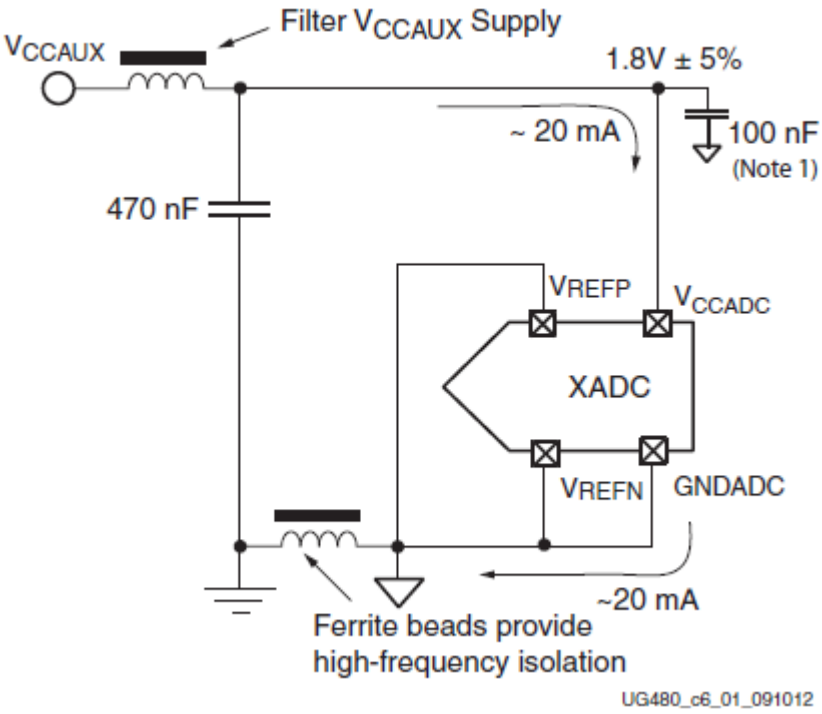


Figure 15 – XADC Power Configuration

2.10.8 Battery Backup for Device Secure Boot Encryption Key

Zynq power rail V_{CCBATT} is a 1.0V to 1.89V voltage typically supplied by a battery. This supply is used to maintain an encryption key in battery-backed RAM for device secure boot. The encryption key can alternatively be stored in eFuse.

As specified in the Zynq TRM, if the battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}. On MicroZed, V_{CCBATT} is connected to net FPGA_VBATT and is tied through a 0 Ω resistor (R12) to the MicroZed V_{CCAUX} supply, which is 1.8V. However, FPGA_VBATT is also extended to the carrier card. To apply an external battery to Zynq on the Carrier Card, remove R12.

2.10.9 Cooling Fan

An unpopulated-header JP4, labeled FAN, is available in the event a fan is needed for high performance designs. This header provides two ground connections and one connection to the Vin voltage, which is 5V by default. MicroZed also provides two mounting holes (MTG[3:4]) near the Zynq device where a fansink might be secured.

3 Zynq-7000 AP SoC I/O Bank Allocation

3.1 PS MIO Allocation

There are 54 I/O available in the PS MIO. The table below lists the required I/O per peripheral:

Table 17 – PS MIO Interface Requirements

Interface	I/O Required
SD	7
QSPI FLASH	7
USB Host	14
ENET	14
UART	2
uHeader/Digilent Pmod compatible interface	8
Button, LED	2
TOTAL	**54**

The specific MIO assignments are shown in Table 19. Since the GPIO assignments aren't specific those are supplemented in the table below.

Table 18 – PS GPIO Assignments

MIO	Voltage	Function
7 (output only)	3.3V	USB Reset
0, 9-15	3.3V	PS Pmod
47	1.8V	PS LED
51	1.8V	PS Pushbutton

Table 19 – PS MIO Allocation

IO	Peripheral	Signal	IO Type	Speed	Pullup	Direction
MIO 0	GPIO	gpio[0]	LVCMOS 3.3V	slow	disabled	inout
MIO 1	Quad SPI Flash	qspi0_ss_b	LVCMOS 3.3V	slow	enabled	out
MIO 2	Quad SPI Flash	qspi0_io[0]	LVCMOS 3.3V	slow	disabled	inout
MIO 3	Quad SPI Flash	qspi0_io[1]	LVCMOS 3.3V	slow	disabled	inout
MIO 4	Quad SPI Flash	qspi0_io[2]	LVCMOS 3.3V	slow	disabled	inout
MIO 5	Quad SPI Flash	qspi0_io[3]	LVCMOS 3.3V	slow	disabled	inout
MIO 6	Quad SPI Flash	qspi0_sclk	LVCMOS 3.3V	slow	disabled	out
MIO 7	USB 0	reset	LVCMOS 3.3V	slow	disabled	inout
MIO 8	Quad SPI Flash	qspi_fbclk	LVCMOS 3.3V	slow	disabled	out
MIO 9	GPIO	gpio[9]	LVCMOS 3.3V	slow	disabled	inout
MIO 10	GPIO	gpio[10]	LVCMOS 3.3V	slow	disabled	inout
MIO 11	GPIO	gpio[11]	LVCMOS 3.3V	slow	disabled	inout
MIO 12	GPIO	gpio[12]	LVCMOS 3.3V	slow	disabled	inout
MIO 13	GPIO	gpio[13]	LVCMOS 3.3V	slow	disabled	inout
MIO 14	GPIO	gpio[14]	LVCMOS 3.3V	slow	disabled	inout
MIO 15	GPIO	gpio[15]	LVCMOS 3.3V	slow	disabled	inout
MIO 16	Enet 0	tx_clk	LVCMOS 1.8V	slow	enabled	out
MIO 17	Enet 0	txd[0]	LVCMOS 1.8V	slow	enabled	out
MIO 18	Enet 0	txd[1]	LVCMOS 1.8V	slow	enabled	out
MIO 19	Enet 0	txd[2]	LVCMOS 1.8V	slow	enabled	out
MIO 20	Enet 0	txd[3]	LVCMOS 1.8V	slow	enabled	out
MIO 21	Enet 0	tx_ctl	LVCMOS 1.8V	slow	enabled	out
MIO 22	Enet 0	rx_clk	LVCMOS 1.8V	slow	enabled	in
MIO 23	Enet 0	rxd[0]	LVCMOS 1.8V	slow	enabled	in
MIO 24	Enet 0	rxd[1]	LVCMOS 1.8V	slow	enabled	in
MIO 25	Enet 0	rxd[2]	LVCMOS 1.8V	slow	enabled	in
MIO 26	Enet 0	rxd[3]	LVCMOS 1.8V	slow	enabled	in
MIO 27	Enet 0	rx_ctl	LVCMOS 1.8V	slow	enabled	in
MIO 28	USB 0	data[4]	LVCMOS 1.8V	slow	enabled	inout
MIO 29	USB 0	dir	LVCMOS 1.8V	slow	enabled	in
MIO 30	USB 0	stp	LVCMOS 1.8V	slow	enabled	out
MIO 31	USB 0	nxt	LVCMOS 1.8V	slow	enabled	in
MIO 32	USB 0	data[0]	LVCMOS 1.8V	slow	enabled	inout
MIO 33	USB 0	data[1]	LVCMOS 1.8V	slow	enabled	inout
MIO 34	USB 0	data[2]	LVCMOS 1.8V	slow	enabled	inout
MIO 35	USB 0	data[3]	LVCMOS 1.8V	slow	enabled	inout
MIO 36	USB 0	clk	LVCMOS 1.8V	slow	enabled	in
MIO 37	USB 0	data[5]	LVCMOS 1.8V	slow	enabled	inout
MIO 38	USB 0	data[6]	LVCMOS 1.8V	slow	enabled	inout
MIO 39	USB 0	data[7]	LVCMOS 1.8V	slow	enabled	inout
MIO 40	SD 0	clk	LVCMOS 1.8V	slow	enabled	inout
MIO 41	SD 0	cmd	LVCMOS 1.8V	slow	enabled	inout
MIO 42	SD 0	data[0]	LVCMOS 1.8V	slow	enabled	inout
MIO 43	SD 0	data[1]	LVCMOS 1.8V	slow	enabled	inout
MIO 44	SD 0	data[2]	LVCMOS 1.8V	slow	enabled	inout
MIO 45	SD 0	data[3]	LVCMOS 1.8V	slow	enabled	inout
MIO 46	SD 0	cd	LVCMOS 1.8V	slow	enabled	in
MIO 47	GPIO	gpio[47]	LVCMOS 1.8V	slow	disabled	inout
MIO 48	UART 1	tx	LVCMOS 1.8V	slow	enabled	out
MIO 49	UART 1	rx	LVCMOS 1.8V	slow	enabled	in
MIO 50	SD 0	wp	LVCMOS 1.8V	slow	disabled	in
MIO 51	GPIO	gpio[51]	LVCMOS 1.8V	slow	disabled	inout
MIO 52	Enet 0	mdc	LVCMOS 1.8V	slow	enabled	out
MIO 53	Enet 0	mdio	LVCMOS 1.8V	slow	enabled	inout

3.2 Zynq-7000 AP SoC Bank Voltages

The I/O bank voltage assignments are shown in the table below.

Table 20 – Zynq Bank Voltage Assignments

PS-Side	
Bank	**Voltage (default)**
MIO Bank 0/500	3.3V
MIO Bank 1/501	1.8V
DDR	1.5V
PL-Side	
Bank0	3.3V
Bank 34	Carrier card – Vcco_34
Bank 35	Carrier card – Vcco_35
Bank 13 (7Z020 Only)	Carrier card – Vcco_13

PL I/O Banks 34, 35, and 13 are powered from the carrier card. These bank supplies are designed to be independent on the MicroZed. Maximum flexibility is allowed to the designer for these banks as the voltage level and standard are left to the Carrier Card design, as well as whether the banks use the same shared voltage supply or independent ones.

4 Jumper Settings

This section is intended to show all of the user-adjustable jumpers and their default settings on MicroZed. However, MicroZed only has three jumpers, which are all related to the boot_mode.

Table 21 – Jumper Settings

Ref Designator	Connection	Default Setting	Function
JP1	PS_MIO[2]	1-2 (GND)	PS-PL JTAG Cascaded
JP2	PS_MIO[4]	1-2 (GND)	QSPI Boot Mode
JP3	PS_MIO[5]	2-3 (VCC)	

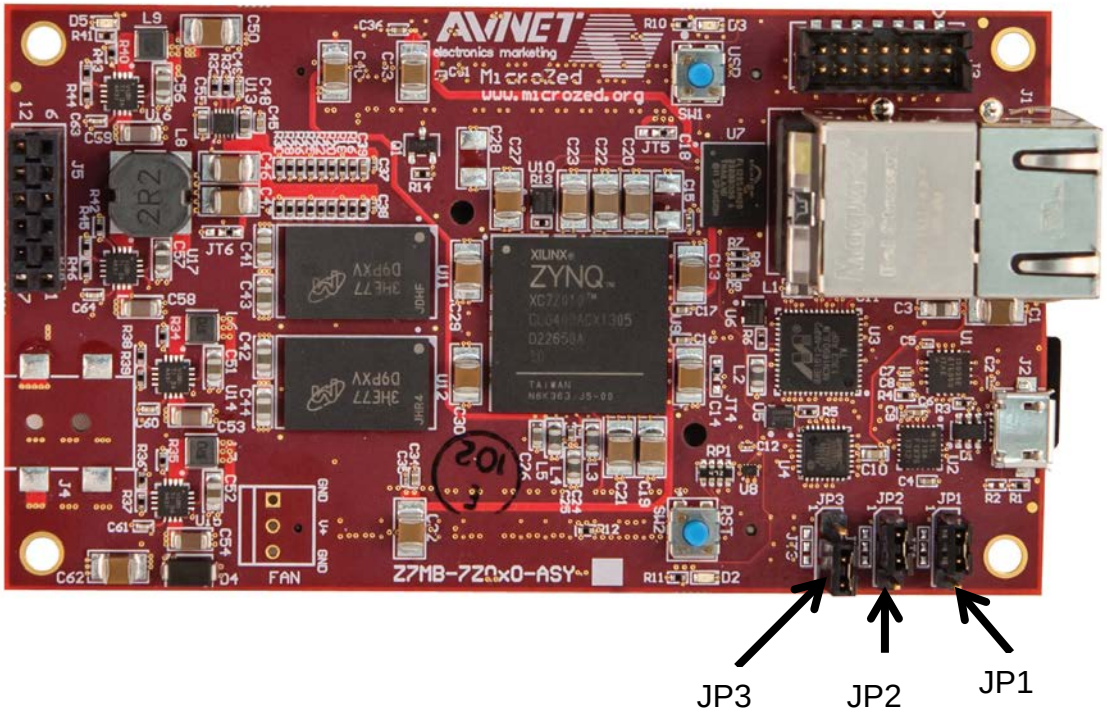


Figure 16 – MicroZed Jumper Locations

5 Mechanical

MicroZed measures 2.25” x 4.00” (57.15 mm x 101.6 mm)

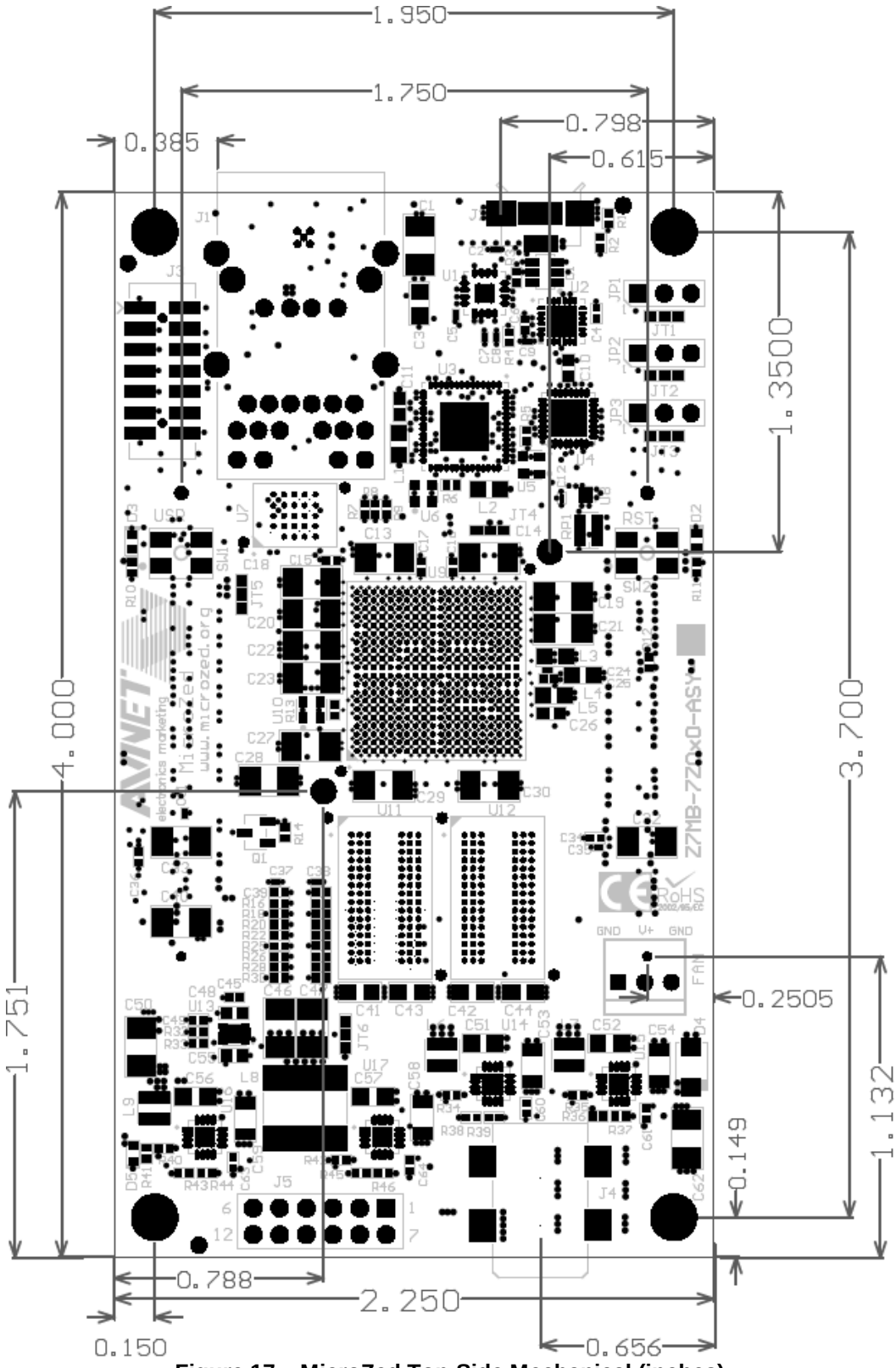


Figure 17 – MicroZed Top-Side Mechanical (inches)

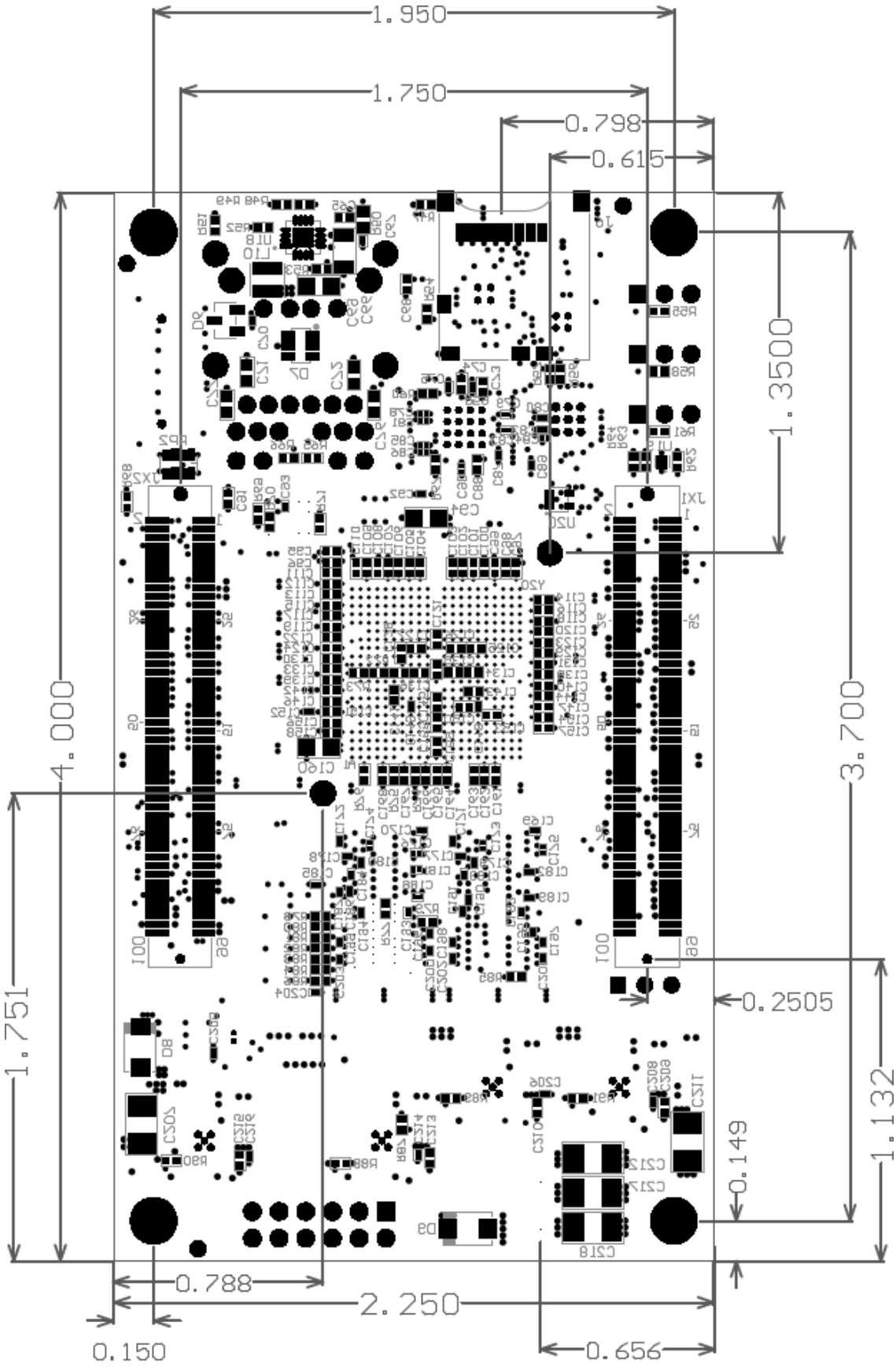


Figure 18 – MicroZed Bottom-side Mechanical (inches)

Figure 19 – MicroZed Side Vertical Dimensions

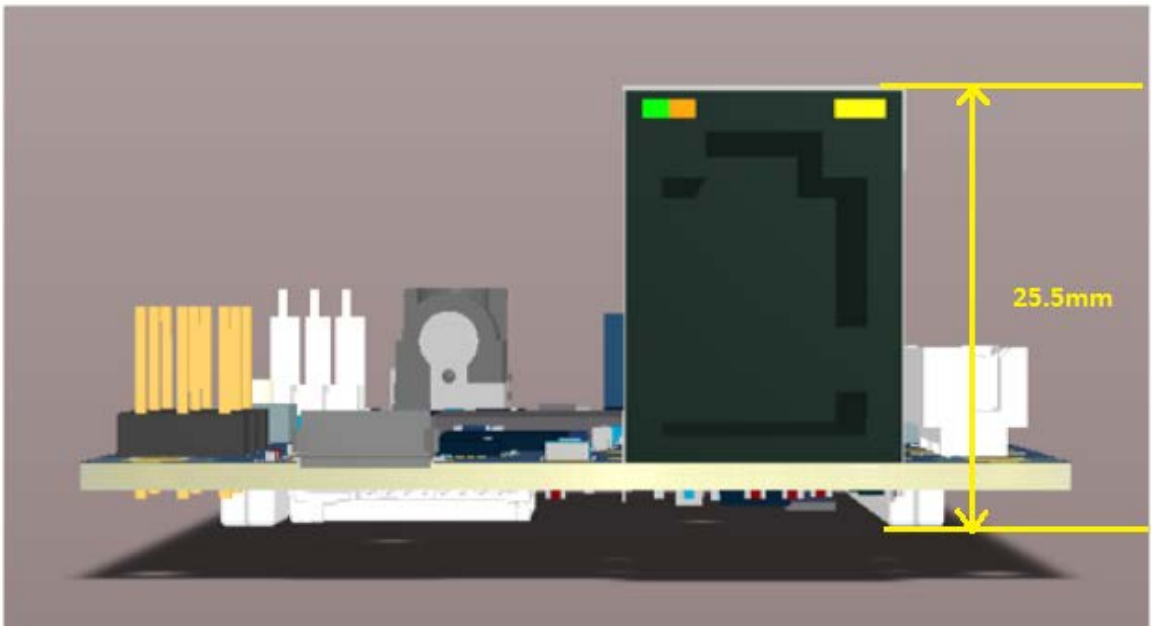


Figure 20 – MicroZed Max vertical dimensions (front)

6 Revision History

Rev date	Rev #	Reason for change
02 Aug 13	1.0	Initial MicroZed Hardware User Guide
09 Aug 13	1.1	microSD 32 GB support noted; USB OTG not supported due to USB connector; DDR3 uses 1.5V SSTL; Added GND and Vcc connections to JX1 and JX2 connections, re-ordered numerically by JX1/JX2 pin numbers; Updated 1.8V current estimate since it is the DDR Termination LDO input; updated mechanical drawings with all measurements in inches; Corrected independence of Bank 13 voltage rail.
26 Nov 13	1.2	Updated Table 12 & 13 SOC Pin numbers & names. Added vertical dimensions to Mechanical section.
18 Dec 13	1.3	Updated table 13, PMOD header to FPGA pin numbers.
28 Jan 14	1.4	Updated based on feedback: Pgs: 11, 16, 21.