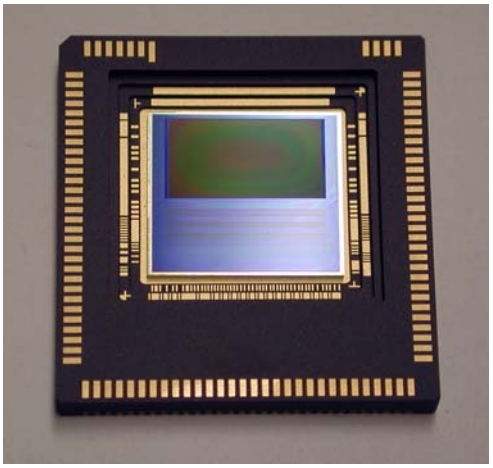
Fairchild Imaging CIS 1910F

Standard and Scientific Package Datasheet

2.1 Megapixel CMOS Image Sensor

PRODUCT DESCRIPTION



The CIS1910F is a medium resolution, ultra low-noise CMOS image sensor intended for scientific and industrial applications requiring high quality imaging under extremely low light levels. The device features an array of 5T pixels on a 6.5µm pitch with an active imaging area of 1920(H) x 1080(V) pixels. The sensor supports both rolling shutter and global shutter (snapshot) readout modes. The sensor has two ADC channels per row with one optimized for very low light levels and the other optimized for high light levels, allowing high dynamic range data collection in a single image. The sensor supports user-programmable row start/stop control for region of interest (ROI) readout mode. The CIS1910F delivers extreme low-light sensitivity with a read noise approaching one electron (rms), quantum efficiency (QE) above 55%, and very low dark current. This, combined with megapixel resolution and 100 fps readout, makes the CIS1910F an ideal imaging device for a variety of low-light-level imaging applications.

The CIS1910F sensor is available as an unpackaged die (CIS1910Fx001), in a 101 pin scientific package (CIS1910Fx121), or in a 105 pad standard package (CIS1910Fx221). For this datasheet, the two packaged options are specified. The Scientific package is shown above. The unpackaged die is specified in a separate datasheet.

FEATURES	BENEFITS
1920 (H) x 1080 (V) pixel CMOS Image Sensor	2.1 Megapixels of data
6.5 µm x 6.5 µm pixel area	Ideal pixel size for optical microscopy
Maximum frame rates: -100 fps in Rolling Shutter readout mode - 50 fps in Global Shutter readout mode	Capture dynamic events and kinetics
< 1.2 e- noise	Enables ultra-low-light imaging
Programmable ROI readout	Flexible windowing to allow faster frame rates
< 35 e-/pixel/second dark current @ 20°C	Low dark current so deep cooling not needed
≥ 55% peak quantum efficiency (QE)	High sensitivity visible through NIR
> 88 dB intra-scene dynamic range	Record intense & faint features simultaneously
On-chip column parallel 11-bit A/D converters Dual gain 11-bit output channels per pixel	Digital sensor for more compact designs

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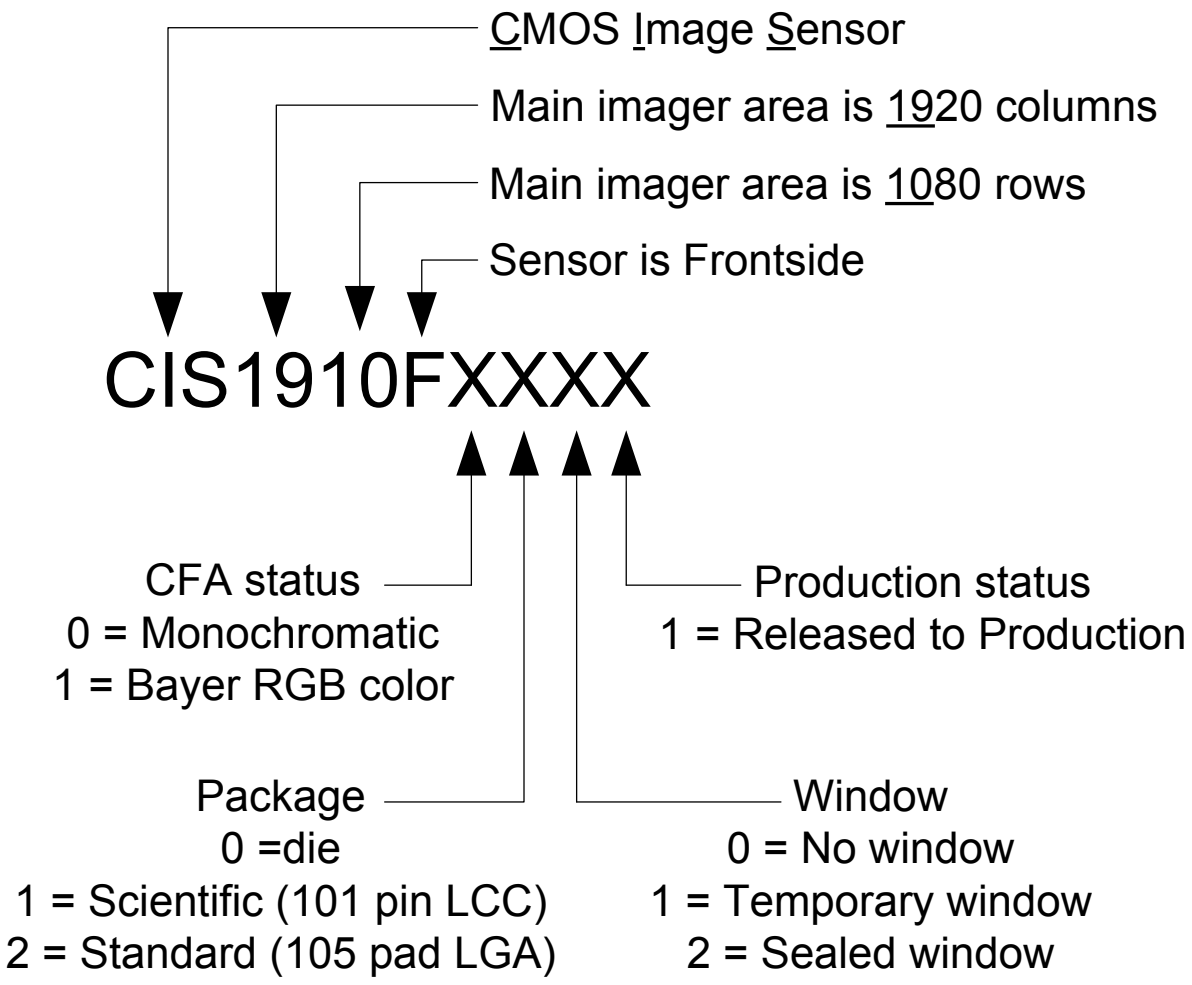
Sensor naming convention



This datasheet will describe the monochromatic and color options for the Scientific and Standard packages. Drawings will assume that the Sealed window option is always used. So, effectively this datasheet covers the four parts CIS1910F0121, CIS1910F1121, CIS1910F0221, and CIS19101221.

For the monochromatic and color unpackaged die (with no window), see the datasheet “MAN 0127 CIS1910F Die Datasheet”.

At the time of this datasheet revision (December 2012) there is no Backside CIS1910. Therefore this datasheet will sometimes use “CIS1910” and “CIS1910F” interchangeably.

General Specifications

Parameter	Typical value
Active array size	1920 (H) x 1080 (V), main imager area 2048 (H) x 1144 (V), all pixels (including border and dark)
Pixel size	6.5 µm x 6.5 µm
Dimensions of active area	12480 microns (H) x 7020 microns (V), main imager area 13311.6 microns (H) x 7435.6 microns (V), all pixels
Dimensions of die (Note 1)	15675 microns (H) x 14829.8 microns (V), die circuit only 15715 microns (H) x 14869.8 microns (V), including seal ring 16035 microns (H) x 15389.8 microns (V), including saw street (estimate)
Distance from die center to center of active area	3187.68 microns
Shutter type	Rolling Shutter, Global Shutter (snapshot). ROI readout capabilities for both shutter types.
Maximum frame rate	100 fps (Rolling Shutter) (@ 283MHz clock rate) 50 fps (Global Shutter)
Number of readout ports	1
Maximum line rate (Note 2)	114kHz (8.7 µs/line)
Maximum pixel rate (Note 3)	234 MHz (3.5ns/pixel, and 2048 pixels/line, + ADC dead time)
ADC resolution	2 x 11-bit
Column level amplifier gain	1x or 2x (low gain output) 10x or 30x (high gain output)
Power consumption	0.8W dual channel @100fps, 0.3W in Low-Gain only @50fps
I/O interface	1.8V LVCMOS and 1.8V HSTL
Package type	Wirebondable 101-pin CLCC (for Scientific package) Wirebondable 105 pad LGA (for Standard package)

Note 1: The dimensions for the die circuit area and the seal ring around it are defined by lithography and are accurate to sub-micron tolerances. When the die is cut from the wafer, there may be greater variations depending on the wafer cut process.

Note 2: Maximum line rate calculation is based on the assumption of 1144 lines being read out at 100 frames per second. (1144 lines)/(0.01 second to read out 1144 lines) = 114.4 kHz line rate.

Note that this is a calculated number. In actuality, each line is read out according to the number of SCLKs in a line (set by both the default and BAE-recommended wavetables to be 2464 SCLKs) divided by the SCLK frequency. Therefore the minimum line time is 2464/283,000,000 = 8.71 µsec. This corresponds to a maximum line rate of 114.854 kHz.

Note 3: Maximum pixel rate calculation is based on the assumption of 1144 lines being read out at 100 frames per second, with each line consisting of 2048 pixels. (2048 pixels/line)(1144 lines/frame)(100 frames/second) = 234,291,290 pixels/second = 234 MHz maximum pixel rate. Note that this is a calculated number. At 100 fps, the system clock is 283 MHz, not 234 MHz. This means that pixels are actually read out at 283 MHz, not 234 MHz. However, because there is a dead time associated with each row, the average rate at which pixels are captured is less

than the 283 MHz clock rate. For the assumptions that were made above, the maximum pixel rate would be 234 MHz, even though the clock would be clocking at 283 MHz while this was happening. New pixel data appears on the DOUT and DOUT_LG pins at the SCLK frequency, not the calculated frequency above.

Electrical-optical specifications

Parameter	Specification	Notes
Intra-frame dynamic range	30000:1.2 => 25000:1	
PRNU	< 3% RMS	at 75% of max output
Dark current	< 35 e-/pixel/sec	at 20ºC
Dark current non-uniformity	< 65 e-/pixel/sec RMS	at 20ºC
Fixed pattern noise (FPN)	< 2% RMS uncorrected	of the max output
Conversion gain (DN/e-)	High gain output − 1.7 at 30x − 0.55 at 10x Low gain output − 0.12 at 2x − 0.055 at 1x	w/1.4V ADC input range (ADC input range is user programmable from 0.8V to 2V) (30x: 1.3DN/e- w/1.85V ADC default input range)
Full well capacity (FWC)	≥ 30,000 e-	
Lag	< 0.1%	of maximum output
Non-linearity	< 1%	
Fill factor with microlens	> 0.9	
Microlens F-number	1.5 for monochromatic sensor 1.6 for color sensor	
Peak QE	≥ 0.55	at 600nm
MTF	≥ 0.4	at 600nm
Temporal read noise	< 1.2 e- RMS @ 50 fps Rolling Shutter readout, @T=30ºC	Median value of read noise distribution from high gain output (30x gain)
Spectral sensitivity range	400 – 700nm	See QE plots (Figure 32 and Figure 34) for spectral sensitivity in the Near IR out to 1100 nm

The above specifications are from CIS1910F devices running in Rolling Shutter mode. Although the CIS1910F runs in Global Shutter mode, BAE does not guarantee any performance specifications for Global Shutter mode. However, the functionality of all sensors to operate in Global Shutter mode is verified at wafer test.

For sensor performance specifications in photometric units, contact Technical Support at cams.techsupport@baesystems.com.

Recommended Operating Conditions

Parameter	Definition	Min	Nom	Max	Units
AVDD	Analog circuits power supply (avg 90 mA, Peak at 170mA on 5% duty cycle) Note 1.	3.135	3.3	3.465	V
AVDD_PIX	Pixel source follower power supply (10 mA avg)	3.135	3.3	3.465	V
AVDD_RST1	Pixel reset power supply1 (1mA)	2.50	3.00 (RS) or 2.77 (GS) (Note 2)	3.3	V
AVDD_RST2	Pixel reset power supply2 (1mA)	2.50	3.0	3.3	V
DVDD	Digital circuits power supply (160mA)	1.71	1.8	1.89	V
DVDD_IO	I/O circuits power supply (65 mA) (with no terminations on outputs) Note 3.	1.71	1.8	1.89	V
VTX1_POS	TX1 Transfer gate positive power supply (80 mA/ 1µsec pulse in GS, <1mA in RS) Note 4.	3.135	3.3	3.465	V
VTX2_POS	TX2 Transfer gate positive power supply (80 mA/ 1µsec pulse in GS, <1mA in RS) Note 4.	3.135	3.3	3.465	V
VTX1_NEG	TX1 Transfer gate negative power supply (80 mA/ 1µsec pulse in GS, < 1mA in RS) Note 4.	-1.5	-0.4	+0.3	V
VTX2_NEG	TX2 Transfer gate negative power supply (80 mA/ 1µsec pulse in GS, < 1mA in RS) Note 4.	-1.5	-0.4 or +0.8 (Note 5)	+0.85	V
$T_{operation}$	Sensor junction temperature	-40	30	+55	°C
RTRIM	Bias resistor for bandgap based internal bias generator (current through resistor is approximately 100µA; for low noise, place resistor close to sensor)	11K	12.2K (Note 6)	13.5K	Ω
PTAT R_{OUT}	Output resistance of PTAT temperature sensor (@ pin VPTAT)		100K (Note 7)		Ω

Note 1: The relevant period for this duty cycle is the row readout time, which is 2464 SCLKs for both the default and BAE-recommended wavetables. The 5% number comes from the percentage of clock cycles that buff_en (wavetable bit 9) is high during the 2464 SCLK row readout time. (115/2464 =4.67% for the default wavetables, 122/2464 = 4.95% for the BAE-recommended wavetables.)

Note 2: The recommended voltage for AVDD_RST1 is 3.00 Volts when running in Rolling Shutter and 2.77 Volts when running in Global Shutter. If the user plans on switching between Rolling and Global Shutter, the power to AVDD_RST1 must be switchable between these two voltages. For Global Shutter operation, it is critical for there to be a tightly controlled differential between AVDD_RST1 and AVDD_RST2 – a 230 mV differential in the case of AVDD_RST1 =

2.770 V and AVDD_RST2 = 3.000 V. This is particularly critical for high gain Global Shutter operations. This differential voltage controls the DN level of the Reset frame, with a target of about 300 DN for the Reset frame being the goal. At 10x gain, each 10mV of differential voltage changes the Reset level by 100 DN. At 30x gain, each 10mV of differential voltage changes the Reset level by 300 DN.

Note 3: Normally the DOUT and DOUT_LG pins send their outputs to another chip (typically an FPGA) to be decoded from Gray Code to binary. If the traces connecting the imager to this external chip are too long, the user may wish to add termination at the inputs to this other chip to prevent signal reflection. Adding such termination will increase the current requirement on DVDD_IO. (In practice, no BAE-designed cameras have required such termination.)

Note 4: In Rolling Shutter, the TX2 gate is not typically pulsed and the TX1 gate only gets pulsed for one row of pixels at a time. The current requirements of VTX1_POS, VTX2_POS, VTX1_NEG, and VTX2_NEG are therefore minimal (<1mA) in typical Rolling Shutter applications. In Global Shutter, the both the TX1 and TX2 gates pulse globally (i.e. every pixel in the sensor pulsing simultaneously). In Global Shutter therefore, VTX1_POS, VTX2_POS, VTX1_NEG, and VTX2_NEG all must have enough current capacity to source or sink the necessary currents. For a Global TX2 pulse, the VTX2_POS must supply 80 mA on the rising edge of that pulse and the VTX2_NEG must sink 80 mA on the falling edge of that pulse. Similarly, for a Global TX1 pulse, the VTX1_POS must supply 80 mA on the rising edge of that pulse and the VTX1_NEG must sink 80 mA on the falling edge of that pulse. At a minimum, Global Shutter operation typically requires a single Global TX2 pulse and a single Global TX1 pulse. But sometimes (see Figures 15, 16, 18, and 21) there are Global TX2 pulse trains where these 80 mA source/sink current requirements are needed each line time. While this is an issue for Global Shutter, there may be some special modes in which Global TX2 pulses occur in Rolling Shutter (see Figure 20).

Note 5: VTX2_NEG is recommended to be -0.4 V in Global Shutter or in Rolling Shutter, low light. But in Rolling Shutter, high light, +0.8 V is recommended for VTX2_NEG. This voltage on VTX2_NEG will give the pixel an anti-blooming capability.

Note 6: On the RTRIM pin, a 12.2 KΩ resistor should be attached with one end to the RTRIM pin and with the other end at analog ground. This resistor is important to power the column amplifier circuits and insure functioning DOUT and DOUT_LG outputs.

Note 7: The 100KΩ resistance is an internal resistance inside the chip (i.e. it is the PTAT voltage source output resistance). The user does not need to add any external resistor. The 100KΩ number is given so that when the user measures the PTAT voltage, the user will choose a voltmeter with an internal impedance much greater than 100KΩ so as not to load the PTAT pin and get an inaccurate voltage reading. PTAT stands for Proportional To Absolute Temperature.

Timing Specifications

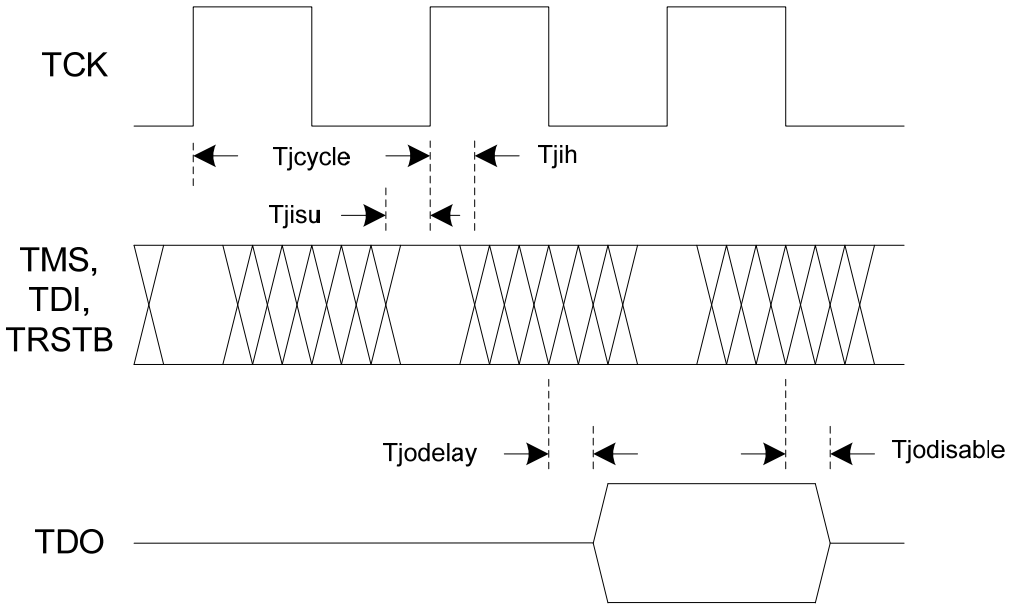
SPI Interface

For the unpackaged die, there is a choice of communicating with the registers in the CIS1910's Digital Control Block by either the JTAG or the SPI protocol. This choice is determined by the voltage on the die pad JTAG_SPI_B. If JTAG_SPI_B = 1, communication occurs using the JTAG protocol. If JTAG_SPI_B = 0, communication occurs using the SPI protocol.

In the packaged part (Standard or Scientific), the user does not have this choice because JTAG_SPI_B is not available as an external pin on the packaged part. Internal to the package, JTAG_SPI_B is tied to logic 0, so that the SPI protocol is always selected. However, even though the packaged part uses SPI, the names for the register programming pins (clock, mode select, input, output, and reset) are given with JTAG-style names. The SPI interface shares the same pins (TCK, TMS, TDI, TDO, TRSTB) with the JTAG tap controller. The following table lists the mapping of SPI functionality to the JTAG-style-named pins of the packaged part:

Pin name	Scientific Package Pin number	Standard Package Pad number	SPI functionality
TCK_PAD	79	F16	clk (SPI clock)
TMS_PAD	73	K16	ceb (Chip enable, active low)
TDI_PAD	78	G16	si (Serial input)
TDO_PAD	80	G15	so (Serial output)
TRSTB_PAD	74	J16	rstb (Optional, though if rstb = 0, this puts the SPI controller in a reset state and disables the other SPI pins. The voltage on this pin must be logic 1 for SPI communication to work.)

Figure 1. SPI Interface I/O Timing

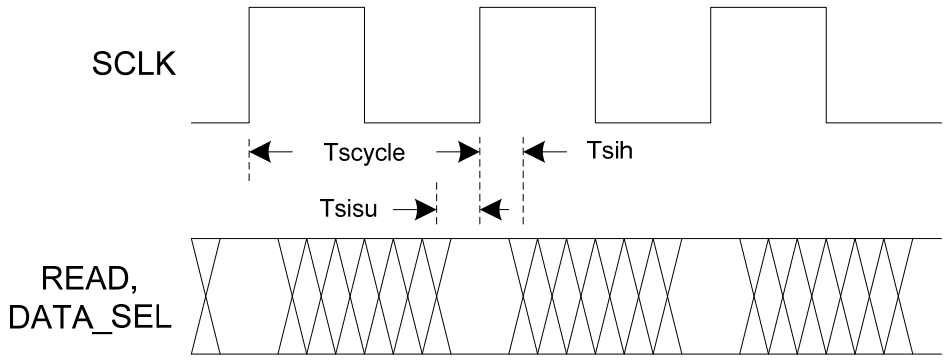


Parameter	Definition	Unit	Min	Max	Note
Tjcycle	TCK clock cycle time	ns.	40		
Tjdc	TCK clock duty cycle	%	45	55	
Tjisu	TMS, TDI, TRSTB input setup time	ns.	2.0		
Tjih	TMS, TDI, TRSTB input hold time	ns.	1.0		
Tjodelay	TDO output delay time from falling edge of TCK	ns.		8.0	
Tjodisable	TDO output disable time from falling edge of TCK	ns		6.0	

Note: The above table is valid for both JTAG and SPI interfaces (even though the Standard and Scientific packaged parts only use the SPI interface).

Functional Control Inputs

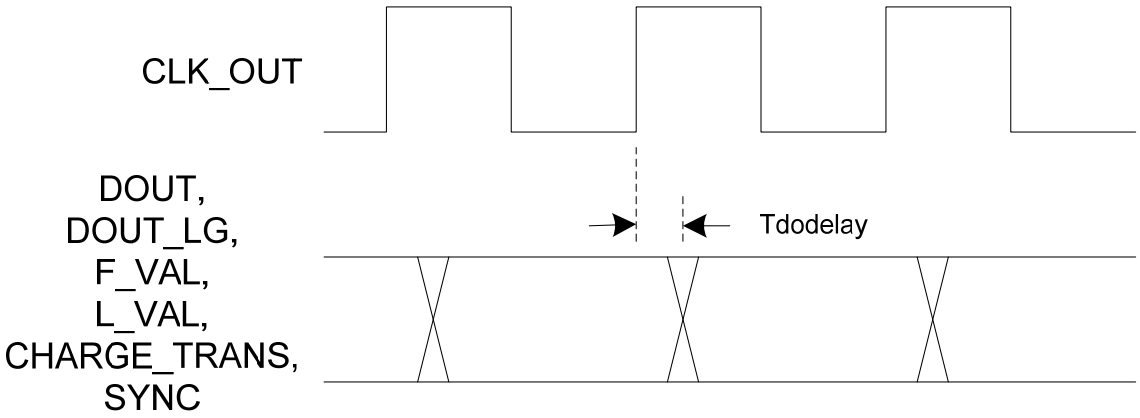
Figure 2. Functional Control Inputs Timing



Parameter	Definition	Unit	Min	Max	Note
Tscycle	SCLK clock cycle time	ns.	3.53		
Tsdc	SCLK clock duty cycle	%	48	52	
Tsjitter	SCLK peak to peak cycle jitter	ps.		150	
Tsisu	READ, DATA_SEL input setup time	ns.	1.0		
Tsih	READ, DATA_SEL input hold time	ns.	0.5		

Data and Status Outputs

Figure 3. Data and Status Output Timing

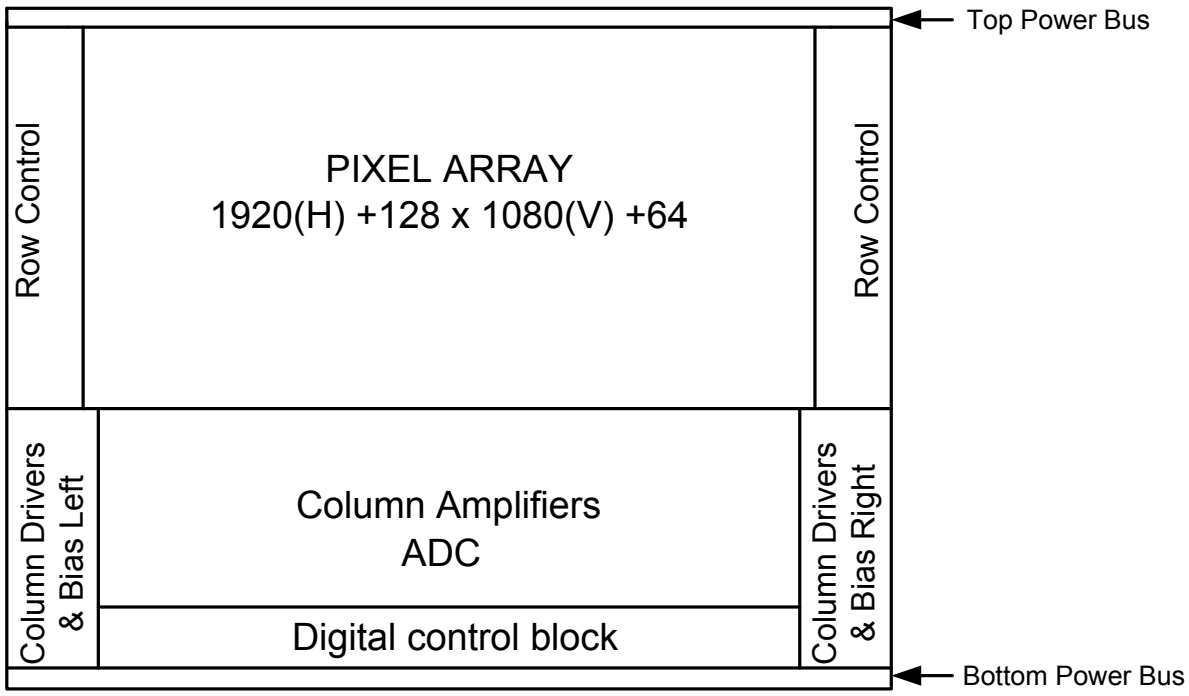


Parameter	Definition	Unit	Min	Max	Note
Tdodelay	DOUT, DOUT_LG, F_VALID, L_VALID CHARGE_TRANS, SYNC output delay time	ns		1.5	Source Synchronous

Device Architecture

Sensor Floor plan

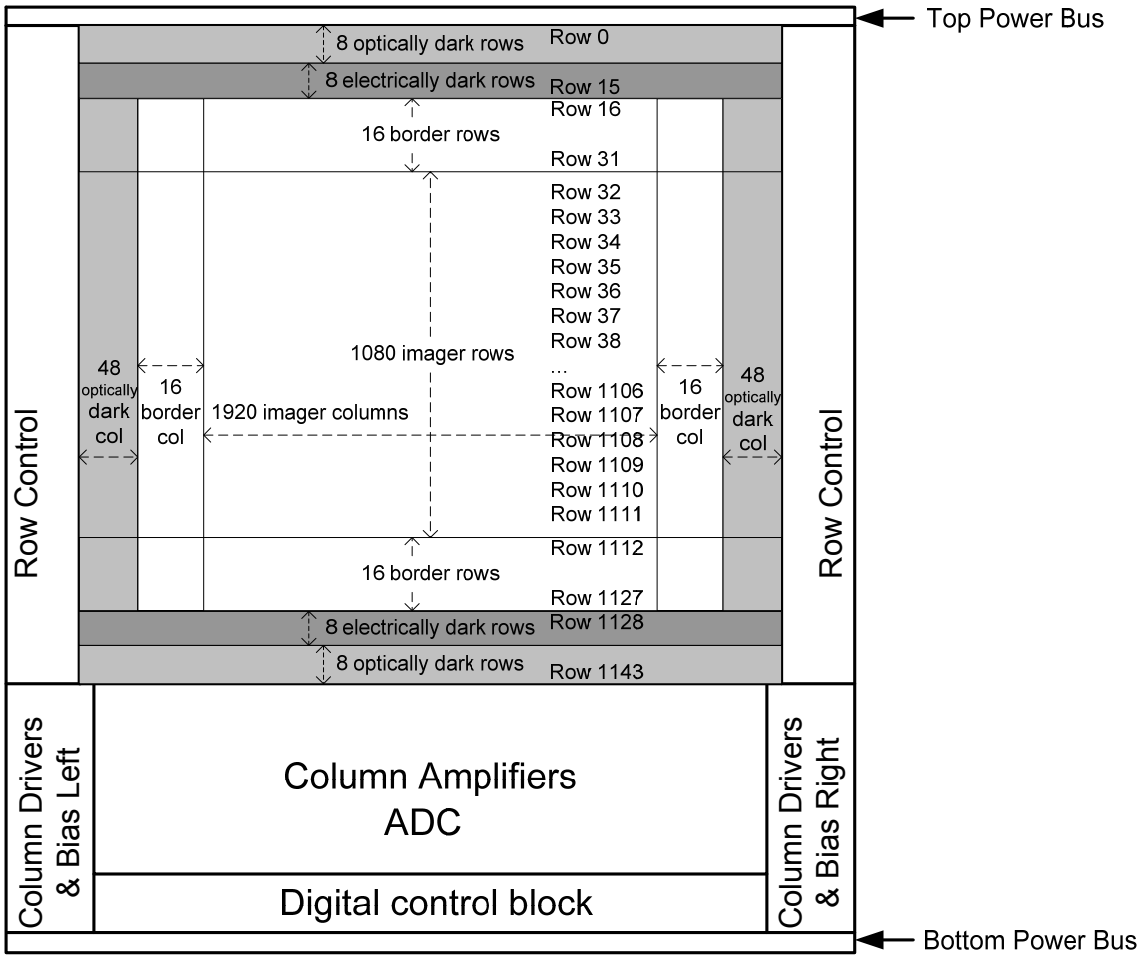
Figure 4. Floor Plan of the CIS1910 Image Sensor



The CIS1910 floor plan is shown in Figure 4. The column amplifier circuits, ADCs and the digital control block (DCB) are located at the bottom of the array. The row control circuits are located on both sides of the pixel array.

The active image area of the pixel array is 1920 pixels wide and 1080 pixels high, but there is also a 16 pixel wide border that is light sensitive and surrounds the active image area on all sides. 48 dark columns are on the far left and far right of the array, and 16 dark rows are on the upper and lower most edge of the array. The sensor floor plan can therefore be redrawn as:

Figure 5. CIS1910 sensor floor plan with row numbering



The optically dark rows are covered with metal so light cannot enter. The electrically dark rows are also covered with metal so light cannot enter, but in addition, all the pixels of these rows have the gates of their TX2 transistors permanently tied to AVDD. This makes them “electrically dark” as well as “optically dark”, because any charge in these dark rows (from dark current, for example) is removed via the TX2 charge dump, which is permanently active for these rows.

Note that the border rows and columns are not fixed in place as being specific physical rows and columns. When the 1920 (H) x 1080 (V) dimensions are reduced, the 16 pixel wide border rows and columns will move as necessary to remain contiguous with the active imager ROI.

Sensor Architecture

Figure 6. Architecture of the CIS1910

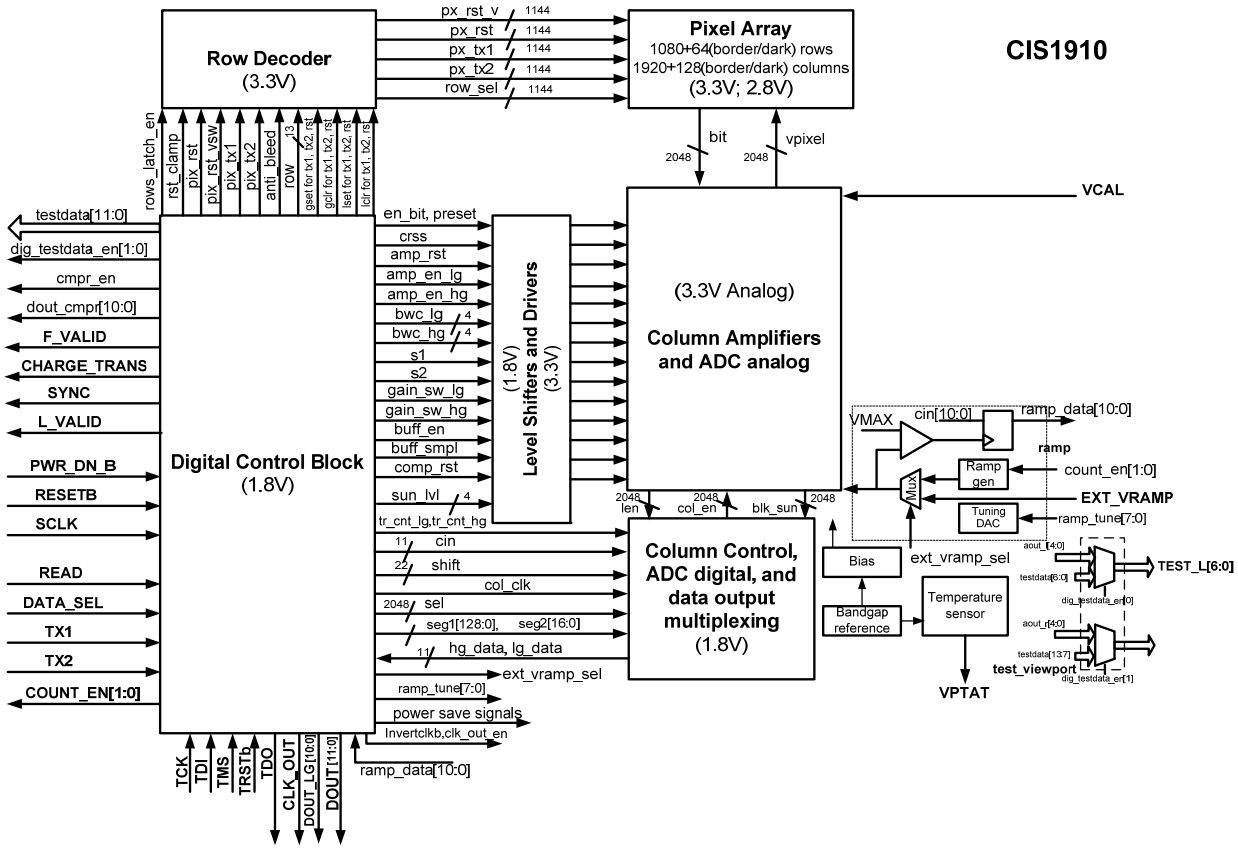


Figure 6 illustrates the architecture of the sensor. The DCB includes all of the digital circuits required for programming and controlling the device. The DCB contains six major sub-sections: the SPI/JTAG register programming controller, the registers, the Gray code ramp counter, the row controller, the waveform generator, and the output data multiplexing control.

The row decoder consists of a 13-bit decoder and 1144 row-driver circuits that control each row of pixels. There are five output signals for each pixel row: PX_TX1, PX_TX2, PX_RST, PX_RST_V, and ROW_SEL.

Column control signals are generated in the DCB and routed to the “Level Shifters and Drivers” on both sides of the column circuitry. The “Level Shifter and Drivers” convert incoming 1.8V LVCMOS signals into 3.3V LVCMOS signals for controlling the column level amplifiers and ADCs. This block also contains the bias generator circuitry. There are two bias references that can be selected via a register. The first bias reference, based on the internal bandgap reference voltage, allows the bias point to be changed via an external resistor RTRIM. It achieves the minimum bias variation as a function of temperature. It is selected when Register 9 bit 25 is 0 (the default). The second bias reference, based on an internal resistor, achieves the lowest readout noise. It is selected when Register 9 bit 25 is 1. Even if the internal resistor is used by setting Register 9 bit 25 to 1, the external RTRIM resistor at the RTRIM pin should still be added.

Separate power supplies are used for the pixel core, analog amplifiers and ADCs, the pad ring, and the digital circuitry. A voltage ramp generator is integrated on the sensor to drive the single slope ADCs in each column. The offset and swing of the ramp generator can be programmed via the SPI interface.

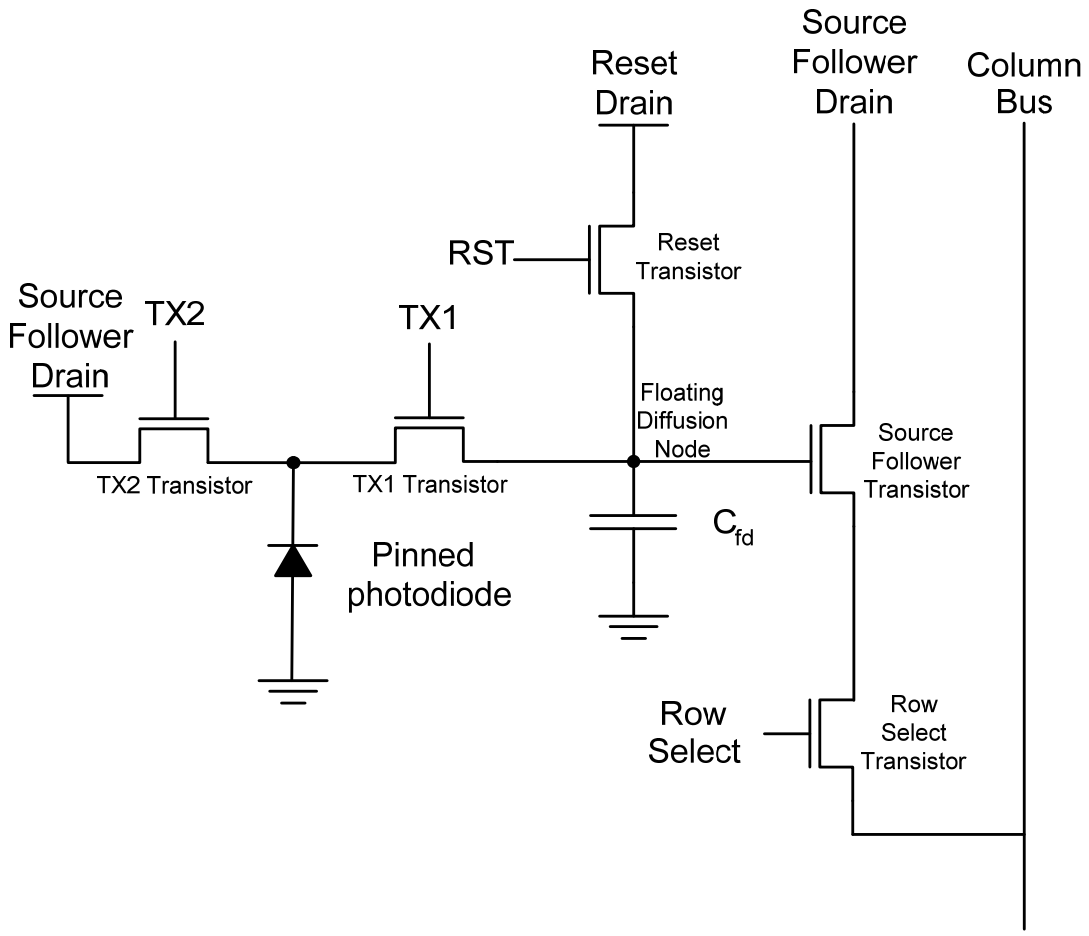
The user must provide a system clock which synchronizes all the operations in the chip. The row and column control clocks, and the built-in Gray code counter for the single slope ADCs are all derived from the system clock.

The user has the ability to change the timing of the internal control signals by reprogramming the registers.

An on-chip PTAT temperature sensor provides a continuous analog output voltage for monitoring the die temperature.

Pixel architecture

Figure 7. 5T pixel schematic



A schematic diagram of the 5T pinned photodiode pixel is shown in Figure 7. The pinned photodiode inside of each pixel starts to integrate charge as soon as the transfer gate TX1 is turned off, then when the transfer gate TX1 is turned on, the integrated charge in the photodiode is dumped onto the floating diffusion node and read out as a voltage signal by the source follower. The TX2 gate serves both as a global reset gate and a lateral anti-blooming protection gate.

Column readout circuitry

Figure 8. Column readout circuitry

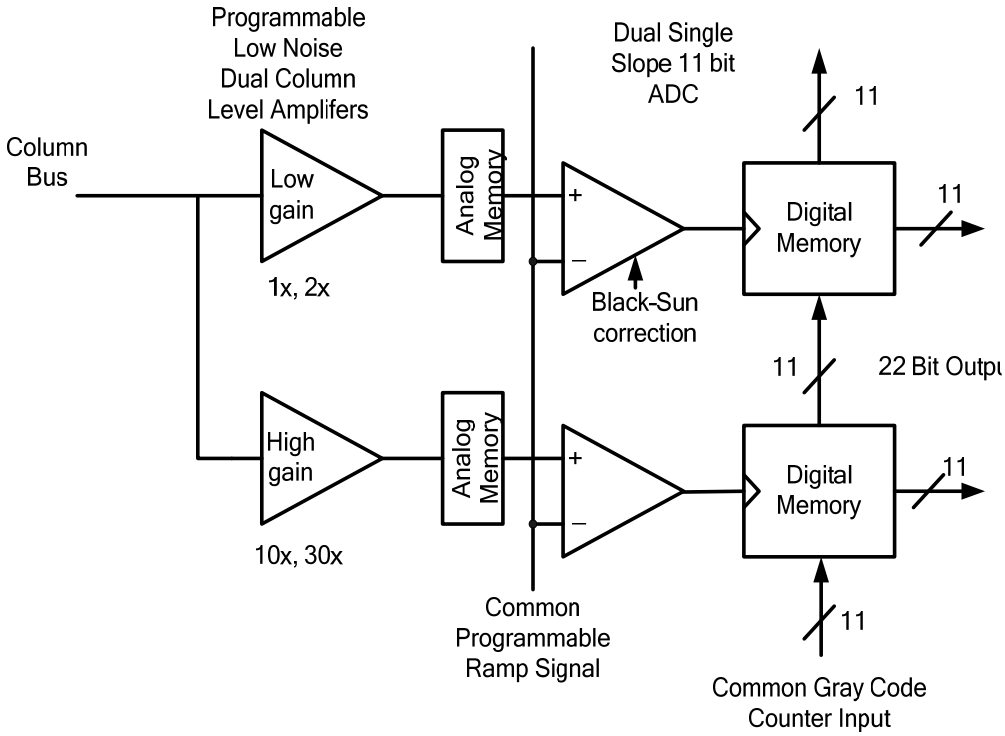


Figure 8 shows the amplifier and ADC structure used in each column of the sensor. This architecture was selected to minimize the sensor read noise while maximizing dynamic range.

There are two amplifiers per column simultaneously generating low gain and high gain output signals. The data output bus is 22 bits wide with 11 bits of low gain data, DOUT_LG[10:0] and 11 bits of multiplexed data, DOUT[10:0]. By default, the DOUT[10:0] data is high gain, but the DOUT pins can be set to output either low gain or high gain data by the action of a comparator circuit (see next section). An extra bit, DOUT[11], indicates the status of the multiplexed data, with DOUT[11] = 1 indicating that the DOUT[10:0] data came from the low gain channel and DOUT[11] = 0 indicating that the DOUT[10:0] data came from the high gain channel. The gain of each amplifier is selected to either maximize the full well capacity, i.e. 1x gain, or to minimize the read noise, i.e. 30x gain. The amplifier output gain is further controlled by the settings of the gain_sw_lg and gain_sw_hg signals (via the SPI registers). When gain_sw_lg is set to 1, the low gain output is 1x, if gain_sw_lg is set to 0, then the low gain output is 2x. On the other hand, when gain_sw_hg is set to 1, the high gain output is 10x and when gain_sw_hg is set to 0, the high gain output is 30x.

In addition to gain, the bandwidth of the column level amplifiers is also programmable via SPI Register 2 bits 8 to 15. Each column also contains two 11-bit single slope ADCs. The outputs of the amplifiers and the outputs of the ADCs are double buffered to maximize the line rate of the sensor. A check for “black-sun”, a failure mode where a signal from very bright light appears dark, is made on the low gain data (Rolling Shutter mode only, and only if this function is enabled by setting Register 2 bit 26 to1). If the ‘black sun” failure mode is detected the low gain output is set to the maximum value, ensuring the extremely bright light signal results in a saturated value.

Sensor Data

After the analog pixel data is digitized, the 22 bit pixel data is sent through a multiplexer and clocked through two registers to the output pads. The low gain data path has a dedicated 11 bit output port DOUT_LG[10:0], while the data at the other output port DOUT[10:0] can be multiplexed between high and low gain data. Multiplexing is enabled via a register bit (setting register 2 bit 20 to 1). If the high gain data is smaller than a reference value (stored in an SPI register), the high gain data is sent to DOUT[10:0] and DOUT[11] = 0. When the high gain data exceeds the reference value, the low gain data is sent to DOUT[10:0] and DOUT[11] = 1. If multiplexing is disabled only high gain data is sent to DOUT[10:0]. When multiplexing is enabled, DOUT_LG[10:0] is forced to 0.

A source synchronous output clock CLK_OUT is provided with the output data. CLK_OUT is used to register DOUT_LG[10:0] and DOUT[10:0]. CLK_OUT can be inverted or disabled via a register bit.

Sensor Interface

Programming Interface

Name	Direction	SPI Description
TCK_PAD	Input	Clk, SPI clock
TDI_PAD	Input	Si, SPI serial data input
TMS_PAD	Input	Ceb, SPI chip enable (active low)
TRSTB_PAD	Input	Rstb, SPI reset (active low) This must be set high for other SPI pins to function
TDO_PAD	Output	So, SPI serial data output

Control Signals

Name	Direction	Description
DATA_SEL	Input	When DATA_SEL = 0, wavetable A is used for sensor output. Wavetable A can be read and wavetable B can be written to. When DATA_SEL = 1, wavetable B is used for sensor output. Wavetable B can be read and wavetable A can be written to. In Rolling Shutter, wavetable A is typically used exclusively for sensor readout, so DATA_SEL is always 0 unless you want to write to wavetable A. In Global Shutter, both wavetables are used for sensor readout. Wavetable A is the Global Shutter Reset frame and Wavetable B is the Global Shutter Data frame. In order to create a sequence of Reset and Data frames, the user typically inputs both logic 0 (Reset frame) and logic 1 (Data frame), alternating between frames.
READ	Input	READ has multiple functions depending on the sensor's mode of operation. It controls external start/pause of the row counter and readout activities in internally triggered readout modes. It is also used for external triggering in external triggered readout mode. It can also be used to synchronously reset the sensor operation.

Name	Direction	Description
RESETB	Input	Active low reset input (asynchronous). RESETB = 0 resets the sensor and loads the JTAG registers with default values (as does a power cycle to the chip).
SCLK	Input	System clock input.
SCAN_MODE	Input	Activates scan mode testing when set to 1 (This is for BAE internal use – all external users should set this pin to 0).
PWR_DN_B	Input	Logic 0 on this pin activates power-reduction functions of Register 12. (These can also be activated by setting Register 2, bit 25 to 1).
CHARGE_TRANS	Output	Marker pulse indicating when data sampling is occurring for the selected row. This signal comes directly from the wavetable without any modification.
F_VALID	Output	Frame valid output, high from beginning of the first physical row to end of the last physical row (i.e. physical rows = active rows and dark rows but not pre-scan rows). The timing of rising and falling edge is processed from multiple register and wavetable settings. There is a pipeline delay latency associated with this signal, with the default delay being equal to 2 row times.
L_VALID	Output	Line valid output indicates valid line data. This signal pulses for all lines, including pre-scan lines. It goes high shortly after the col_in signal (wavetable bit 6) pulses, and stays high for the duration of time necessary to read out the Horizontal ROI pixels. Thus, this signal is a processed signal arising from multiple register and wavetable settings. There is a pipeline delay latency associated with this signal, with the default delay being equal to 2 row times.
SYNC	Output	Unprocessed line synchronization (“l_sync”) or frame synchronization (‘f_sync”) output. If Register 11 bit 14 = 0, SYNC is l_sync and SYNC will pulse exactly as defined by wavetable bit 4. If Register 11 bit 14 = 1, SYNC is f_sync and SYNC will pulse as defined by wavetable bit 4, but only for the first physical row of a frame. There is no pipeline delay associated with the SYNC signal.

Global Shutter Readout Mode Pixel Control

Name	Direction	Description
TX1	Input	Global Shutter readout mode charge transfer pulse.
TX2	Input	Exposure control / charge dump signal. Although not generally used for Rolling Shutter (see Figures 13, 14, and 19), this signal can have the same exposure control function in Rolling Shutter mode (see Figure 20).

Power up sequence

To prevent excessive AVDD current drain at power-on startup, the following sequence is recommended:

1. DVDD and DVDD_IO should be powered-up with all the analog supplies held low and with both RESETB and READ held low.
2. Then SCLK should be activated for a minimum of 8 cycles before proceeding.
3. Then, the sensor should be taken out of reset with both RESETB and READ going high. SCLK should be clocked for at least 8 cycles before proceeding to next step.
4. Taking the sensor back into reset is optional at this point. (For example, setting the READ pin to 0 while leaving RESETB at 1 at this point would make it possible to program the registers with non-default values. When this task is done, READ should be set high again.)
5. Finally, AVDD and all other analog power supplies can be brought up.

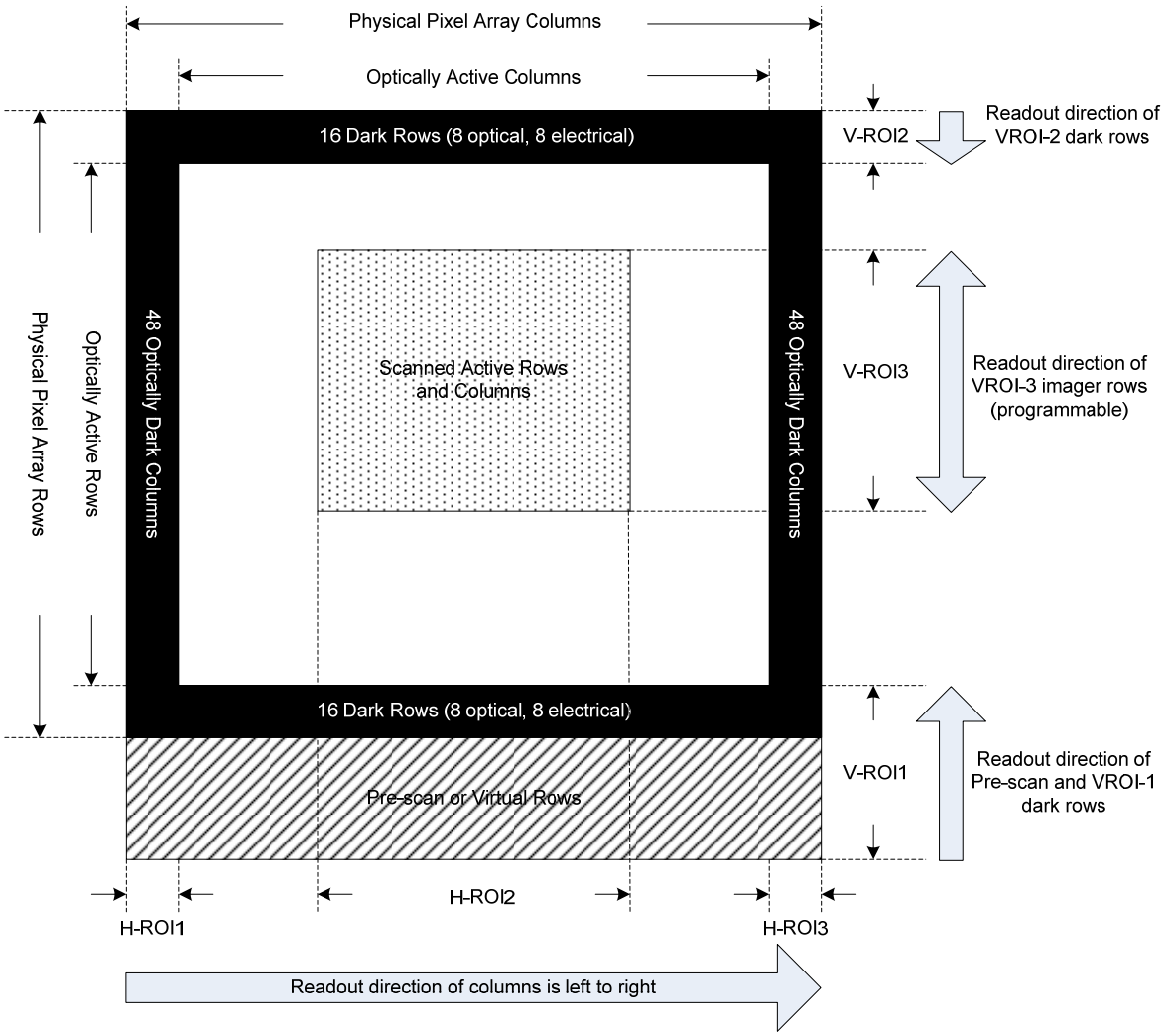
Power down sequence

All the power supplies can be brought down simultaneously.

Readout Modes

Region of Interest

Figure 9. Programmable Regions of Interest



There are three Vertical Regions of Interest (V-ROI) along the vertical dimension and three Horizontal Regions of Interest (H-ROI) along the horizontal dimension.

The first Vertical Region of Interest (V-ROI1) is composed of virtual rows and the 16 dark rows at the bottom of the physical array. The maximum size of V-ROI1 is 261015 and the minimum allowable size is 0 meaning no row data will be accessed. The scanning direction is always from a high virtual row address down to physical row address 1128. If the row address is greater than the physical array rows (i.e. greater than 1143), no actual row is selected and the chip output data would correspond to background noise of the column circuits. These rows are termed “pre-scan rows” or “virtual rows”. When enabled, this region is always at the beginning of frame data. The signal F_VALID will be asserted only for rows within the physical array.

The second Vertical Region of Interest (V-ROI2) is composed of a number of the 16 dark rows at the top of the physical array. The maximum size of V-ROI2 is 16 and the minimum allowable size is 0 meaning no row data will be accessed. The scanning direction is always from the low

physical row address up to physical row address 15 with the total row count corresponding to the programmed size. The default register setting for V-ROI2 is 16, meaning the first row of V-ROI2 to be read out is physical row 0 (the uppermost row in the imager, a dark row) and the last row of V-ROI2 to be read out is physical row 15 (the last dark row of the upper border of dark rows).

The third Vertical Region of Interest (V-ROI3) is composed of the programmable size of active rows in between the two dark regions with physical row address from 32 (at the top) to 1111 (at the bottom). This region can be programmed with a starting address (Register 6) and an ending address (Register 7). If the starting address is less than the ending address, the scanning direction is down. If the starting address is greater than the ending address, the scanning direction is up. For ease of programming, the starting and ending addresses are in terms of logical row, not physical row, resulting in addresses from 0 (top) to 1079 (bottom). A logical to physical row address will be computed automatically (logical row address = physical row address – 32). The maximum V-ROI3 size is 1080, not including the V-ROI3 Border.

The V-ROI3 Border consists of 16 active rows immediately adjacent to the top edge of the VROI3 region and 16 active rows immediately adjacent to the bottom edge of the VROI3 region. The V-ROI3 Border is activated by setting Register 8 bit 23 to 1.

For example, in the case where VROI3 is its maximum size (i.e. 1080 rows), the VROI3 Border consists of active rows with physical row addresses from 16 to 31 (the upper V-ROI3 Border) and physical row addresses 1112 to 1127 (the lower V-ROI3 Border). The order of row readout depends on the V-ROI3 start and end addresses – these define whether the direction for row readout is up or down. If the V-ROI3 readout direction is up, V-ROI3 begins in the lower V-ROI3 Border with physical row 1127, continues to physical row 1112, continues to the row set by Register 6 (V-ROI3 Start), continues to the row set by Register 7 (V-ROI3 End), continues to the bottom of the upper V-ROI3 Border (physical row 31), and ends at the top of the upper V-ROI3 Border (physical row 16). If the V-ROI3 readout direction is down, the readout order of these elements is reversed.

In the case where VROI3 is not at its maximum size, the VROI3 Border (upper and lower region) will move as necessary so that the VROI3 Border is contiguous with the VROI3 region defined by Registers 6 and 7.

The first Horizontal Region of Interest (H-ROI1) is composed of the 48 dark columns on the left side of the physical array. This region can be turned on or off with a register setting (Register 3 bit 15).

The second Horizontal Region of Interest (H-ROI2) is composed of the programmable size of the active columns in between the two dark regions. The beginning and end of this region can be programmed in 16-column segment resolution in logical segment address. The maximum H-ROI2 size is 120 segments (= 1920 columns). The beginning and end of H-ROI2 is set by Register 3, bits 0 to 13. H-ROI2 is also bordered by a left and right H-ROI2 Border (16 columns to the left and 16 columns to the right, contiguous with H-ROI2), which can be turned on or off with a register setting (Register 3 bit16).

The third Horizontal Region of Interest (H-ROI3) is composed of the 48 dark columns on the right side of the physical array. This region can be turned on or off with a register setting (Register 3 bit 14).

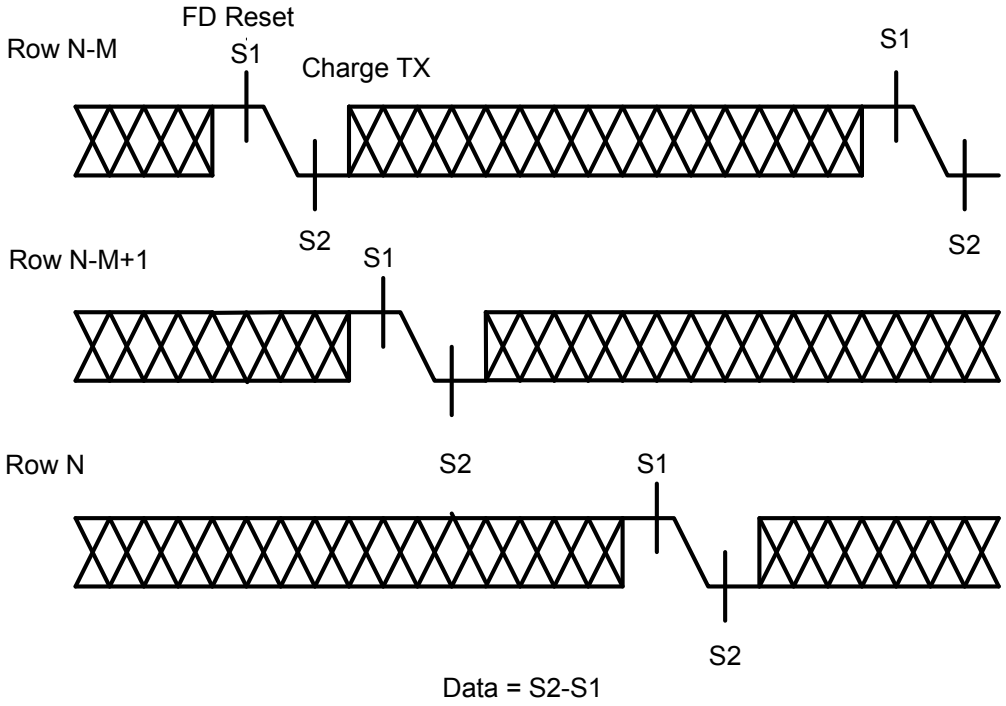
The readout direction in the H-ROI is always from left to right: H-ROI1 => left H-ROI2 Border => H-ROI2 => right H-ROI2 Border => H-ROI3.

Rolling Shutter readout

Rolling Shutter is the standard readout method for CMOS image sensors. When READ is asserted in Rolling Shutter mode, one row at a time is sequentially processed until the frame is completely read out. In video readout mode, i.e. when READ is always asserted, frames are continuously read out, separated only by a programmable frame blanking time. Note that the frame blanking time is determined by the number of pre-scan lines in each image. Readout of each row consists of four separate operations. The first operation is resetting the floating diffusion nodes in each pixel. The second operation is reading the reset voltage out via the source follower transistor in each pixel. The third operation is transferring charge from the pinned photodiode to the floating diffusion node, via TX1, and the last operation is reading out the signal voltage. At the edge of the array, column parallel circuitry amplifies, subtracts, and digitizes the row data. The difference between the reset voltage and the signal voltage is a form of correlated double sampling (CDS). CDS removes kTC, i.e. reset noise on the floating diffusion node, and suppresses the source follower 1/f noise. This readout mode achieves the lowest read noise available for the CIS1910.

The CDS operation in Rolling Shutter mode is illustrated in Figure 10. The floating diffusion voltages of rows N-M, N-M+1, and N are shown. The reset sample for each row is S1 and the data sample for each row is S2. The final pixel value is the difference between S2 and S1.

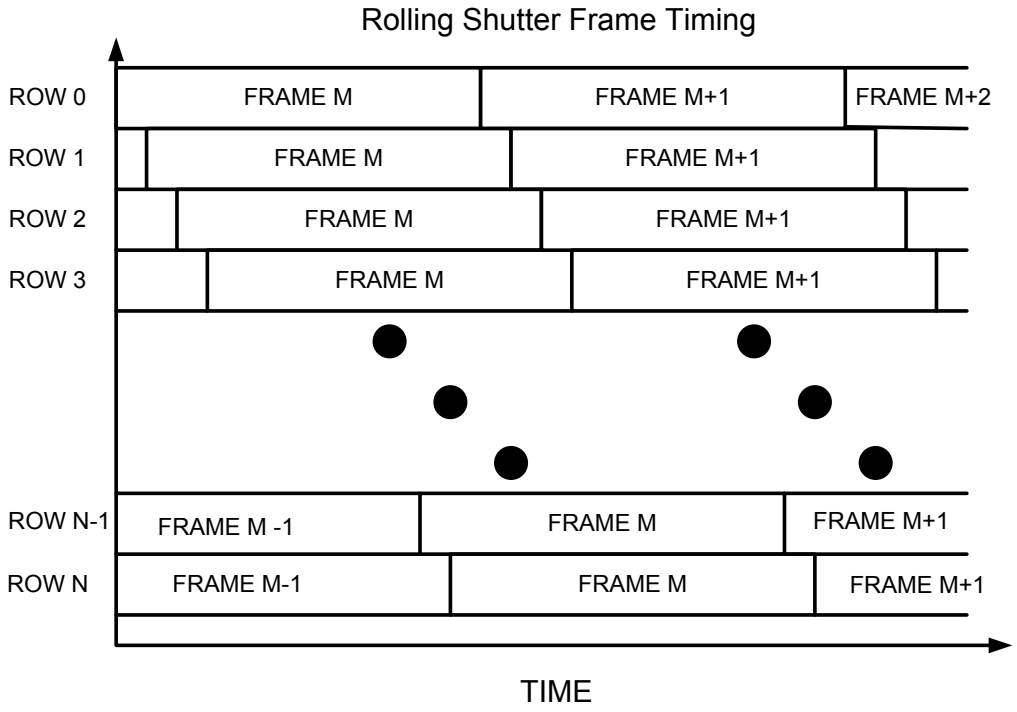
Figure 10. CDS Operation in Rolling Shutter Mode



In Rolling Shutter readout each row in the sensor integrates photo-charge for the same amount of time, but the exact time interval (i.e. integration start and stop points) is different. Moreover, the integration interval for row N+1 is shifted by one line time in comparison to row N.

Figure 11 illustrates this effect.

Figure 11. Integration during Rolling Shutter Mode



Seamless change of integration time in Rolling Shutter readout

Seamless change of integration time in Rolling Shutter readout mode is implemented on this sensor to allow standard auto exposure algorithms to be implemented in a camera. This operation is always active in Rolling Shutter readout mode. Seamless change of integration time is implemented in the sensor by forcing the integration time of each row in each frame to be the same. This enables smooth video output when integration time is used as an electronic shutter.

Global Shutter

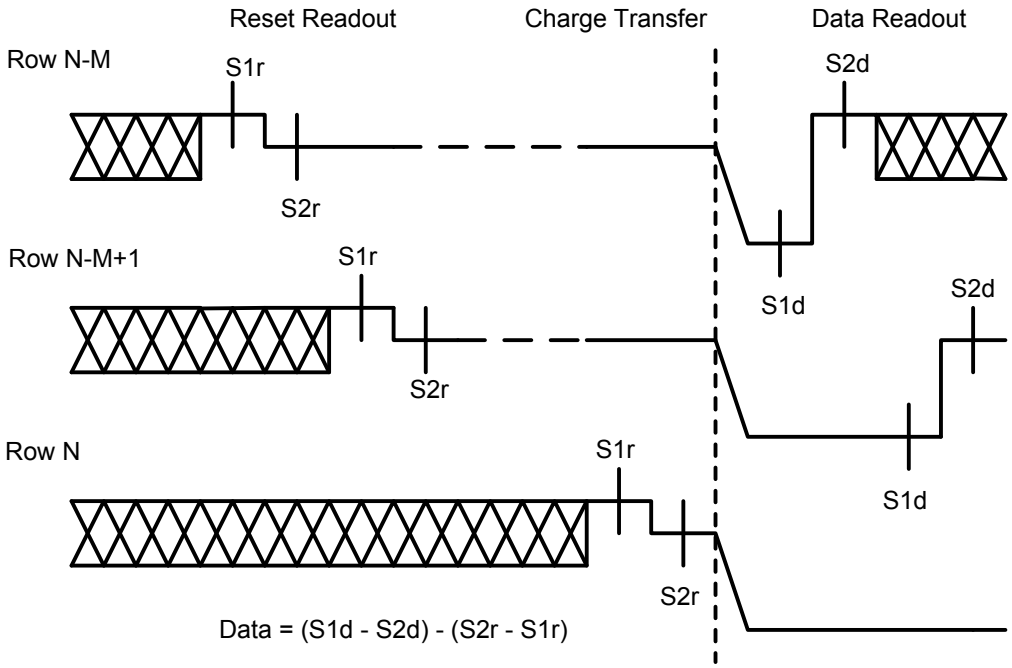
Global Shutter operation allows every pixel in the sensor to integrate charge during the same time period. This minimizes motion artifacts when compared with Rolling Shutter operation. The CIS1910 performs Global Shutter using TX1 (transfer charge from pinned photodiode to floating diffusion) and TX2 (dump charge from pinned photodiode) to simultaneously control the end and start of integration respectively. Both TX1 and TX2 are active high, i.e. they transfer or dump charge when high.

In order to achieve low noise readout, correlated double sampling (CDS) must be performed to mitigate the affects of reset and 1/f noise in each pixel. Due to the global operation of TX1, the typical Rolling Shutter-type readout method (scrolling reset and then readout of each line) cannot be used to perform CDS. Therefore correlated quadruple sampling (CQS) is used to minimize read noise. CQS requires that the sensor be read out twice to construct each image frame. Moreover, a Reset frame and a Data frame are required for each image and the final image is created by subtracting the Reset frame from the Data frame. The first readout, i.e. the Reset frame, is a measurement of the kTC noise charge on the floating diffusion in each pixel, and the second readout, i.e. the Data frame, is a measurement of the charge transferred from the pinned photodiode onto the floating diffusion.

Figure 12 illustrates the operation of CQS. S1r and S2r are reset samples collected during a Reset frame, and S1d and S2d are data samples collected during a Data frame. During a Reset frame each row within the ROI is read out sequentially. When a given row is selected all of the floating diffusion capacitances in that row first receive a hard reset to RD via the reset transistor in each pixel. Then while the reset transistor is on, S1r samples the pixel voltage. The reset gate is then turned off and S2r samples the floating diffusion, i.e. the noise charge. After all of the rows in the Reset frame are read out, charge can be transferred from the pinned photodiode to the floating diffusion capacitance in each pixel. After charge is transferred to the floating diffusion capacitance, a Data frame can be collected. Similar to the readout of a Reset frame, a Data frame is read out sequentially row by row. While a given row is selected, all of the floating diffusion capacitances in that row are first sampled via S1d. Then the reset transistor in each pixel is turned on and S2d samples the pixel voltage. Finally the Reset frame is subtracted from the Data frame, external to the sensor, forming the image S1d-S2r. Note that this assumes that S1r and S2d are the same value, which is only true if RD is noiseless. Therefore the noise voltage on RD is critical to the final read noise of the sensor in Global Shutter operation.

To prevent banding artifacts, use of the TX2 should be limited to pulses within the CHARGE_TRANS low period. Even though the TX2 pulse could be used at any time during the frame blanking period (when pre-scan rows are being read out) with no banding artifacts being generated, it is better to consistently put the TX2 pulse in the CHARGE_TRANS low period of each line just to be safe, since the location of the TX2 pulse(s) in Global Shutter varies with the integration period. Multiple TX2 pulses (one per line) during the time when integration is not desired will prevent excess charge buildup in high-light applications. Integration begins with the falling edge of the last TX2 pulse before the Data frame.

Figure 12. Correlated quadruple sampling operation



The following sections discuss Global Shutter operation in more detail and explain Reset frame and Data frame readout.

Reset frame readout

In Global Shutter mode, reset readout occurs when the DATA_SEL is low and the READ is high. Each Reset frame begins at the first row of V-ROI$_1$ and ends with the last row of V-ROI$_3$. For example, if V-ROI$_1$ size=967 then 951 virtual lines and 16 optically dark lines are sequentially read out from V-ROI$_1$. If V-ROI$_2$ is 16, then the 16 dark rows at the top of the array are read out. If V-ROI$_3$ start=11 and V-ROI$_3$ end=1070 then the row counter counts up, and 1060 active rows are read out of the sensor in V-ROI$_3$. Note that after the last row (row 15) is read out of V-ROI$_2$ then the next row, i.e. the first row of V-ROI$_3$, is physical row 43 (logical row 11 of V-ROI$_3$). If DATA_SEL is held low and READ is held high, Reset frames will continue to be generated by the sensor and the row counter will continuously cycle through the row values in the current V-ROIs. When selecting a Reset-frame/Data-frame pair to create the final image, the Reset frame read out just before the Data frame should be used.

In video mode every Reset frame needs to be followed by a Data frame. Note that just like with Rolling Shutter mode, the frame blanking time is determined by the number of pre-scan lines in each image. When switching between a Reset frame and a Data frame, DATA_SEL should be toggled during the frame blanking period.

Data frame readout

In Global Shutter mode, data readout occurs when the DATA_SEL is high and the READ is high. The V-ROI readout sequence is exactly the same as that for Reset frame readout as described above. To perform correlated quadruple sampling (CQS) a Reset frame must be read out before each Data frame. When performing long integrations (greater than one frame time), multiple Reset frames may occur before a Data frame. For correct CQS sampling, the pair of frames chosen for CQS should be the Data frame and the Reset frame that occurs just before it.

Selective power down

An SPI register (Register 12) is provided to selectively power down individual circuits in order to reduce noise and power dissipation of the sensor under some modes of operation. This register is activated by setting register 2 (the mode register) bit 25 (low power activation) to 1, or by bringing the PWR_DN_B pin low.

Pause/Resume using READ pin

The READ pin switching to 0 will stop SCLK without glitches when SPI register 2 (mode register) bit 21 is 0 resulting in a “zero activity” pause operation. All sensor activities other than SPI operation or reset will be frozen. The assertion of the READ pin to 1 will cause SCLK to resume normal sensor operation. While the clock is stopped, it is possible that the internal voltage ramp generator will lose synchronization. The voltage ramp generator will take up to 65 row periods to stabilize.

Reset using READ pin

When SPI register 2 (mode register) bit 21 is 1 (and this is the default), READ = 0 resets the sensor state (except the SPI register values will not be forced back to their default values). This behavior is necessary to start operation from a controlled start point.

External trigger using READ pin

When SPI register 2 (mode register) bit 23 is 1, it overrides the setting of bit 21 as described above and modifies the behavior of the READ pin. This is called external trigger mode. In this mode, the READ pin is sampled near the falling edge of CHARGE_TRANS. A change in the value of READ before and after the sample qualifies as a transition on READ.

Global Shutter external trigger

In this mode, each transition of the READ pin causes one and only one frame of either reset or data operation (depending on the value of DATA_SEL) before the sensor goes into an “idling” state where only one virtual row is continuously being accessed. In the “idling” state, the sensor is waiting for the next transition on READ. While the sensor is “idling”, external control signals TX1 and TX2 can be applied to precisely control the start and duration of the frame exposure. The response time of the sensor to a READ transition is one row time, i.e. the amount of time required to switch from the virtual row to a valid row.

Rolling Shutter external trigger

In this mode, each transition of the READ pin causes one and only one frame of either rolling reset or rolling read operation before the sensor goes into an “idling” state where only one virtual row is continuously accessed. This is controlled by Register 2 bit 19.
If bit 19 is set to 0, when READ goes from 0 to 1 the complete vertical regions of interest go through a rolling reset (no data is read). When READ goes to 0, the complete vertical regions of interest go through a rolling data readout. The exposure is the amount of time that READ is 1.
If bit 19 is set to 1, when READ has a transition, the complete regions of interest (V-ROI1 and V-ROI2 if enabled and V-ROI3) go through a rolling readout with an immediate reset on the same row. The amount of exposure is therefore approximately the duration of the READ pulse. Even though all rows have the same exposure time, the start of exposure differs from row to row. The last row of the frame starts exposure almost a frame time after the rising transition of READ.
TX2 can be used to address the exposure issue described in previous paragraph. When TX2 is asserted, the exposure is held off until the fall of TX2. This means all rows will have the same exposure start time but different exposure end time. This difference may not matter if the light source is pulsed.

Timing diagrams

Frame and line timing diagrams of the CIS1910 sensor in various operating modes are shown next.

Figure 13. Basic Rolling Shutter Mode

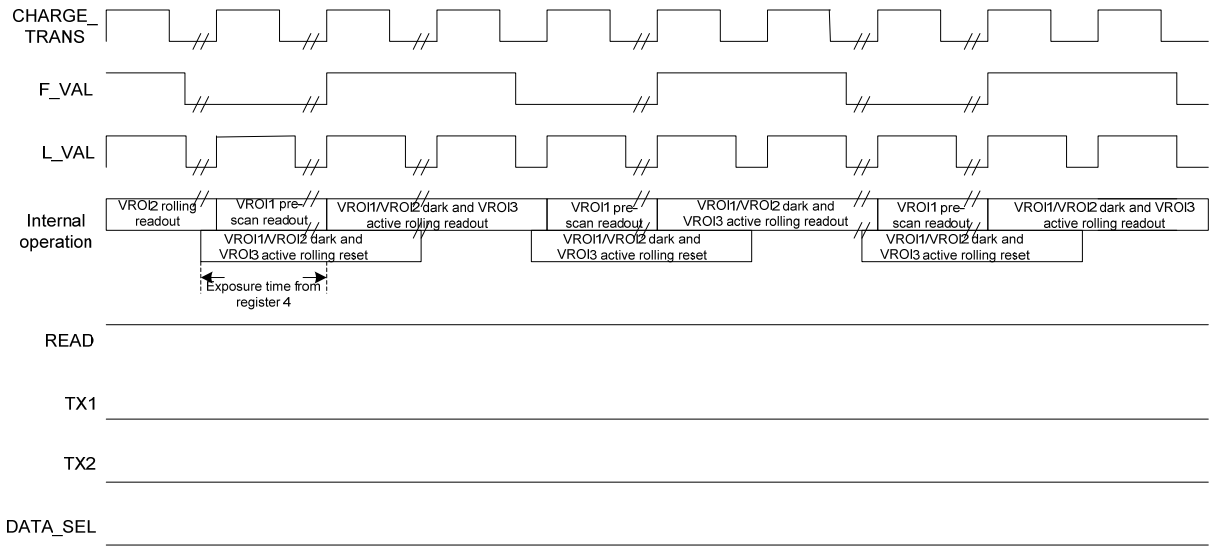


Figure 14. Rolling Shutter Mode using READ pin to extend exposure time. (Reg 2, bit 21=0)

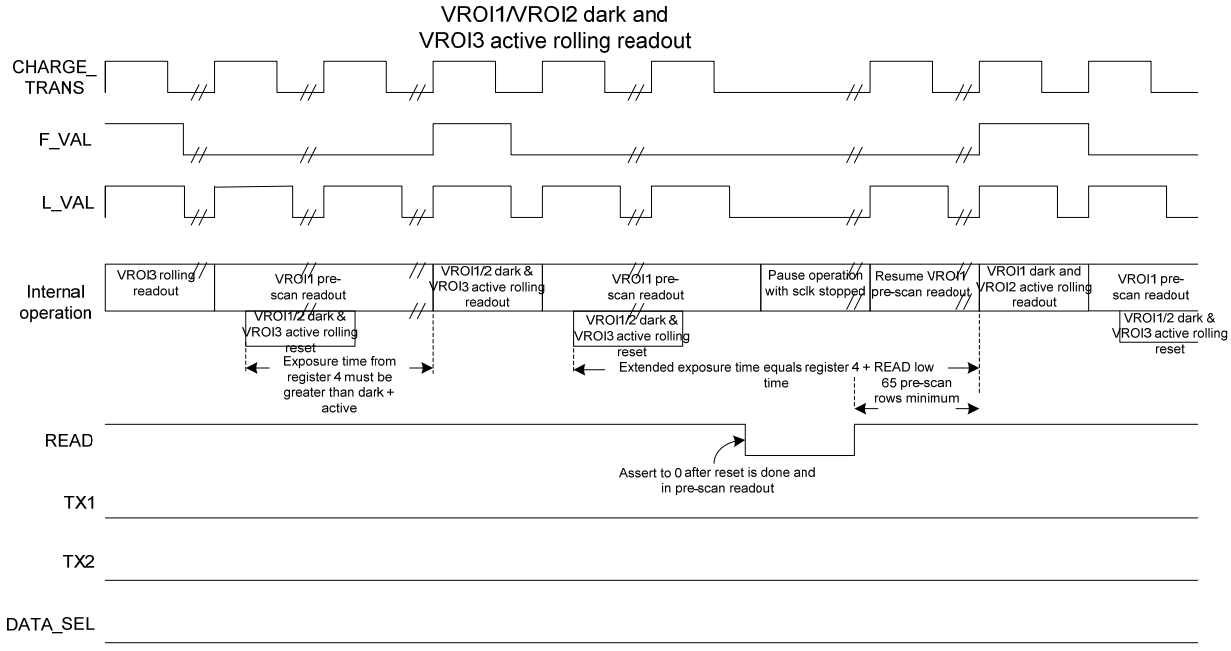


Figure 15. Basic Global Shutter Mode (Register 2, bit 17=1)

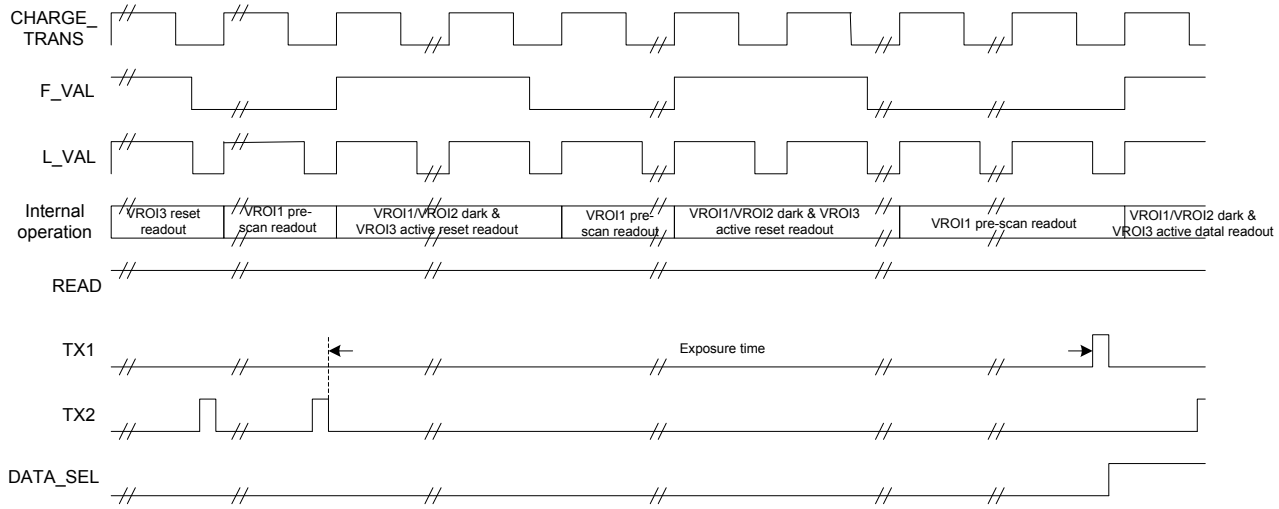
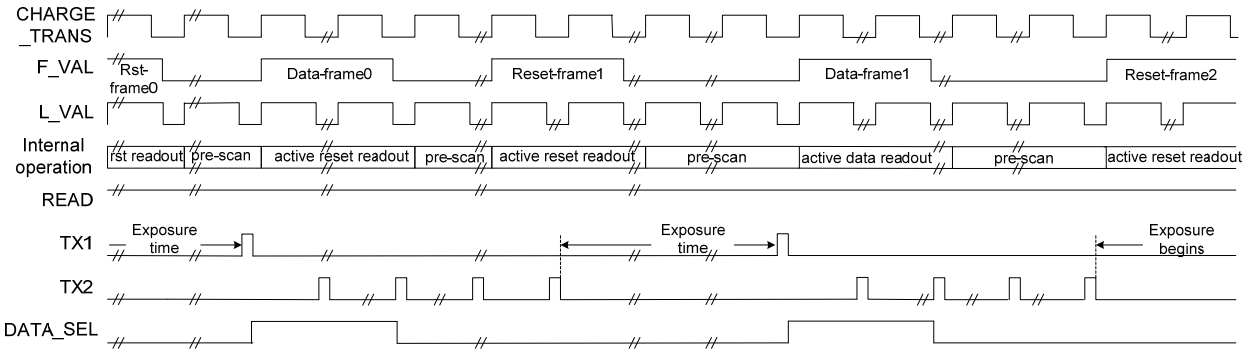


Figure 16. Basic Global Shutter Mode, Short Exposure (Similar to Fig 15, but with more details)



Note: Figures 16 and 17 show an identical readout mode (Basic Global Shutter Mode) with the only difference being that Figure 16 gives the example of a short exposure time and Figure 17 has a long exposure time.

The signals that are different are F_VAL (Figure 16 has one Reset frame preceding the Data frame, Figure 17 has two) and TX2 (Figure 16 has TX2 pulsed during the CHARGE_TRANS low period in each row readout, and Figure 17 has TX2 continuously on or continuously off).

Previously it has been stated that TX2 should be pulsed during the CHARGE_TRANS low time to avoid banding artifacts in the image. Since the Global Shutter final image is constructed from the Data frame and the immediately preceding Reset frame, any TX2 activity during this immediately preceding Reset frame must be pulsed, and this is shown in Figure 16.

In Figure 17, however, the last falling edge of TX2 is not in the immediately preceding Reset frame (Reset frame 1), but rather in the Reset frame before that (Reset frame 0). TX2 activity in this region cannot induce any banding artifacts in the final Global Shutter image, since only data in the immediately preceding Reset frame (Reset frame 1) is used to create the final image.

Therefore, pulsing TX2 in Global Shutter is not necessary as long as there is no TX2 activity when active imager rows are being read out for a Data frame or its immediately preceding Reset frame. Having TX2 continuously on during either of these periods would produce banding artifacts. A time period when active imager rows are being read out roughly corresponds to when F_VAL is high, though F_VAL is high for both dark rows and active imager rows (= “physical rows”), and F_VAL (by default) has a 2 row time delay in its rise and fall times from when the physical rows begin and end their frame readout.

Of course, all complications can be avoided by pulsing TX2 during the CHARGE_TRANS low time regardless of the exposure time. But pulsing TX2 incurs a cost in current consumption. In Low power applications, TX2 may therefore avoid pulsing for long exposure times, as is shown in Figure 17 below.

Figure 17. Basic Global Shutter Mode, Long Exposure (Similar to Fig 15, but with more details)

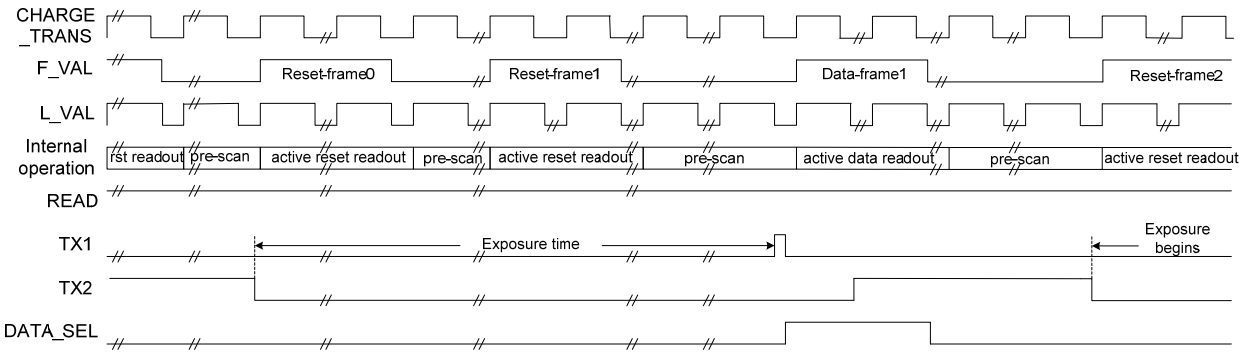


Figure 18. Global Shutter Mode using READ pin to extend exposure time. (Register 2, bit 17=1 and bit 21=0)

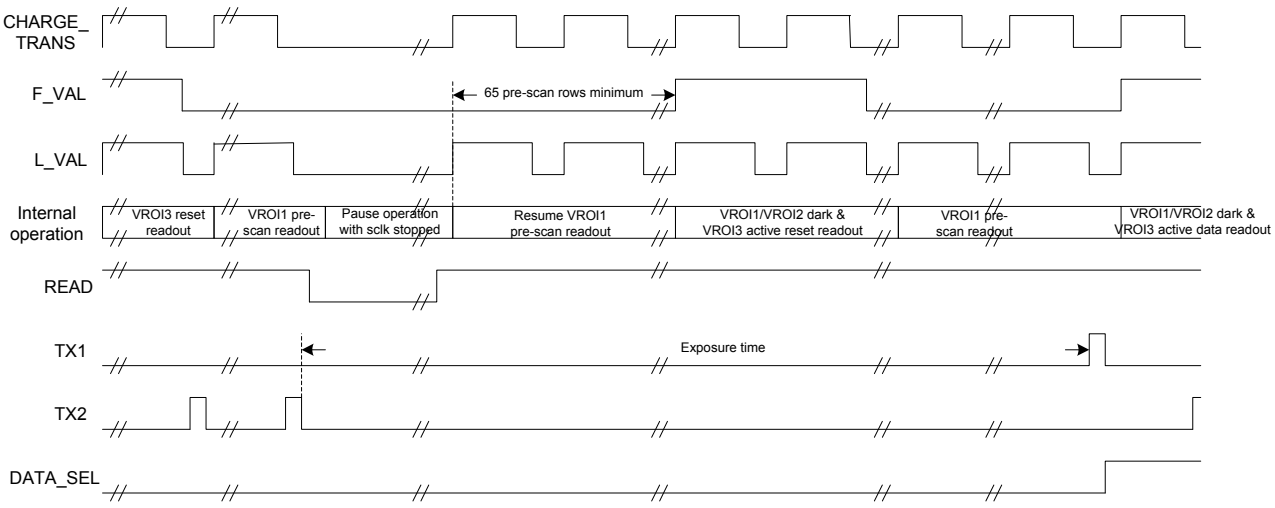


Figure 19. Rolling Shutter Mode with External Trigger. (Register 2, bit 19=0, bit 23=1)

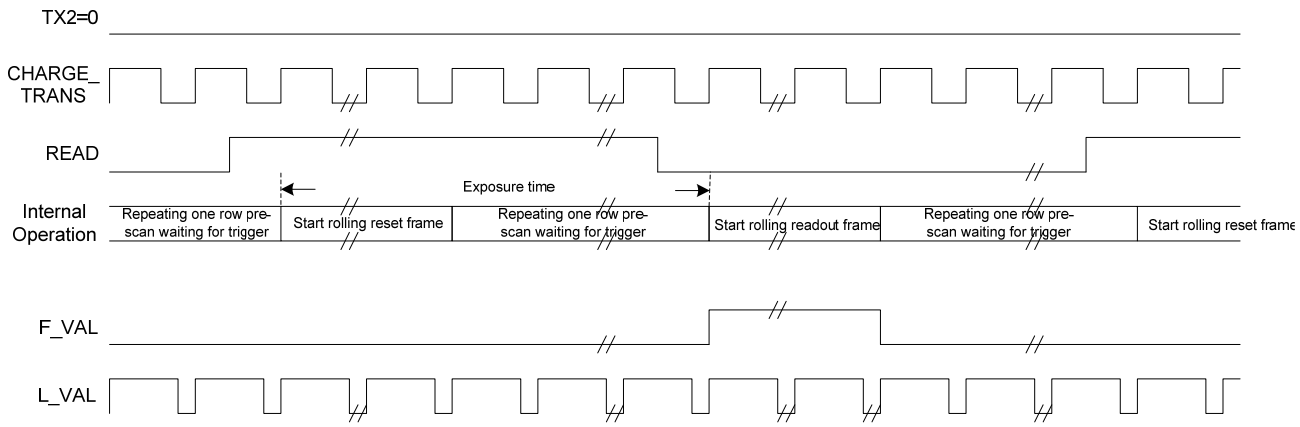


Figure 20. Rolling Shutter Mode with External Trigger. (Register 2, bit 19=1, bit 23=1)

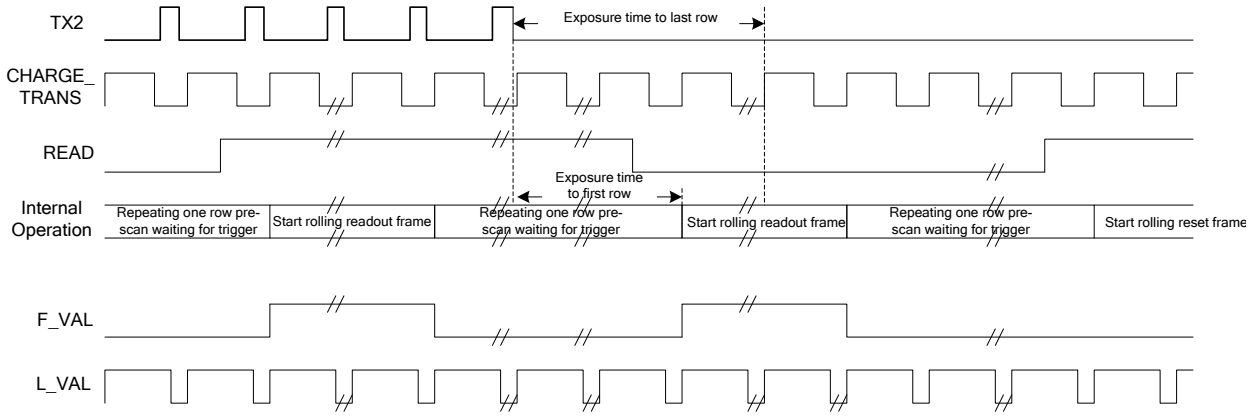
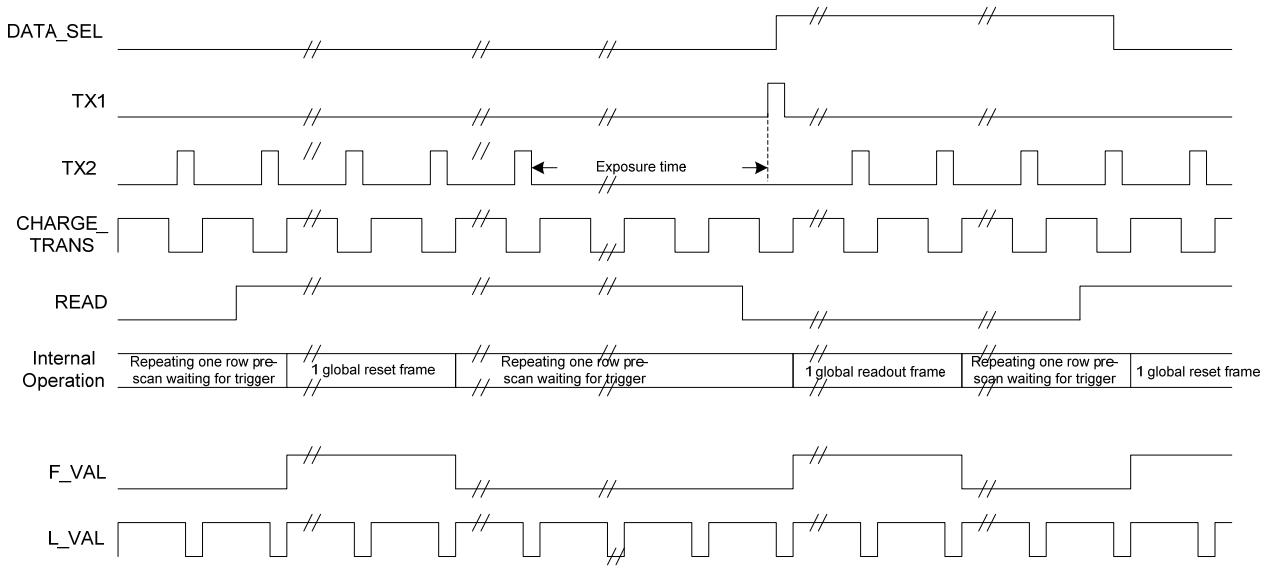


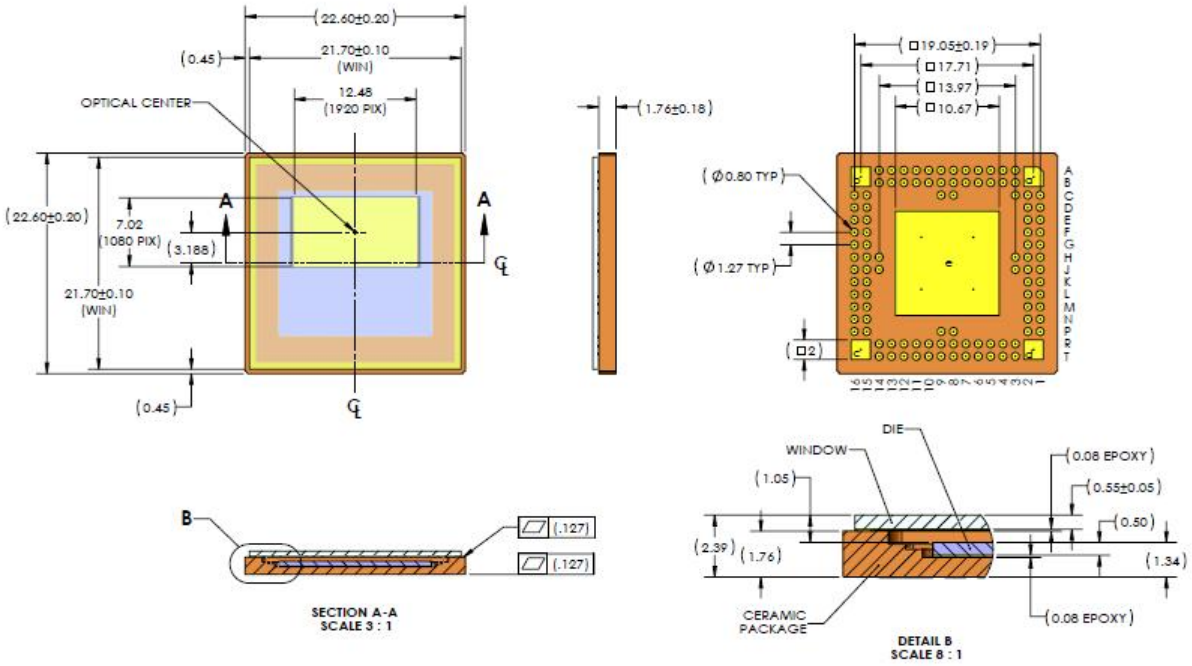
Figure 21. Global Shutter Mode with External Trigger. (Register 2, bit 17=1, bit 23=1)



Packaging information

Standard Package drawings

Figure 22. Standard package overview



All dimensions are in mm.

For soldering the part, the temperature should not exceed 225°C for more than 60 seconds. Follow temperature ramp guidelines in JEDEC/IPC standard J-STD-020, current revision, for the IR/Convection oven reflow profile.

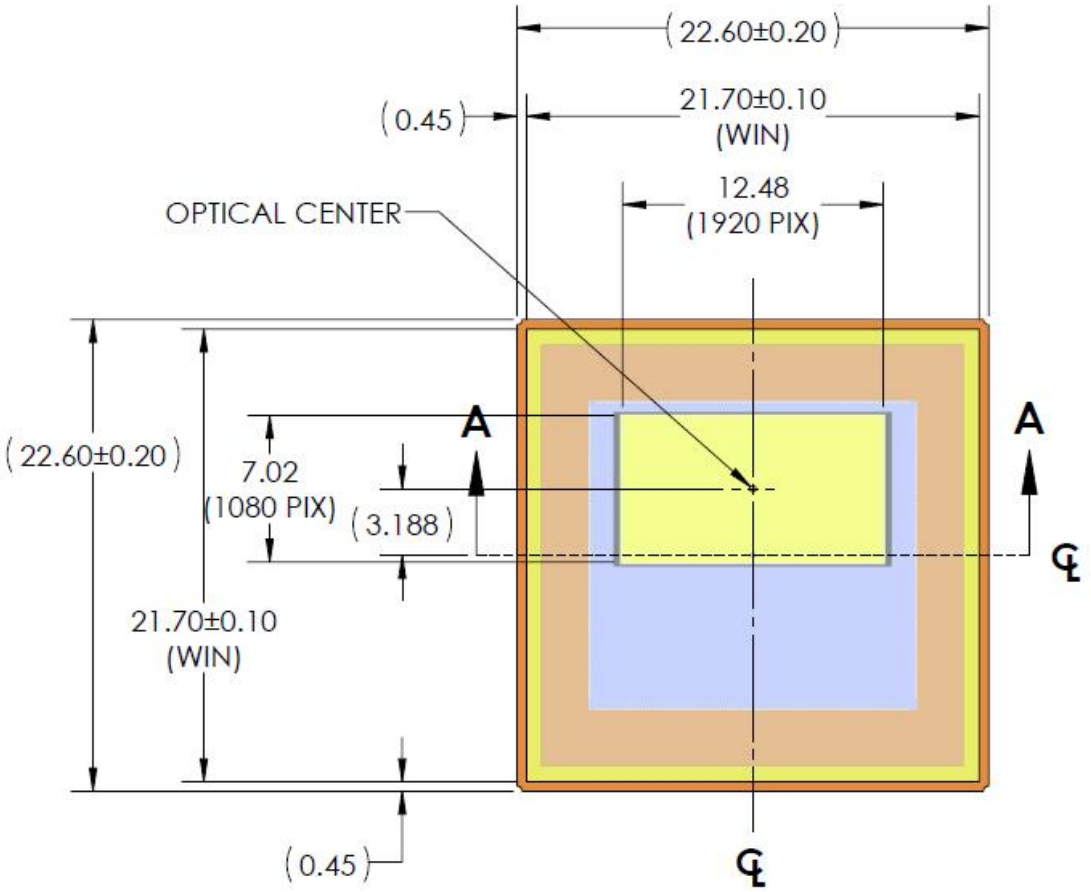
The Moisture Sensitivity Level (MSL) of the package is MSL 2, which means the package can resist moisture ingress under conditions of 30°C and 60% relative humidity for a year or more.

For cleaning the window, first recognize the active area of the sensor. The active area of the sensor is the gray/silver area which is surrounded by the inactive blue area. Only the window surface above the active area needs to be cleaned. Do not pour solvent or any liquid directly on to the window surface. Use a clean, lint-free swab. Dip the swab in methanol or isopropyl alcohol and carefully wipe the surface of the window. Clean, dry air can also be used to blow particle contamination off the window.

Cleaning the sensor active area surface itself is not possible since the CIS1910x221 is always shipped with an epoxy-sealed window that covers the sensor active area.

For cleaning the sensor package, use a clean, lint-free swab, dipping the swab in methanol or isopropyl alcohol and carefully wiping the sensor package. Acetone can also be used to clean the sensor package, but only if it can be kept away from the window seal epoxy. Clean, dry air can also be used to blow particle contamination off the window.

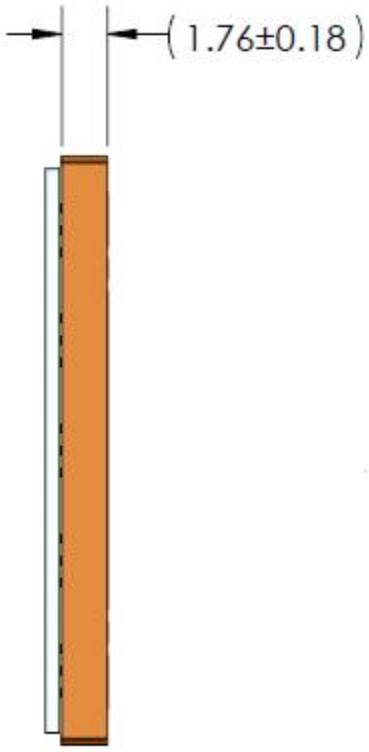
Figure 23. Standard package top view



The tolerance for positioning the die center to the cavity center is +/- 4 mils.
The tolerance for the rotation of the die relative to the package is < 1°.
The tolerance for the die tilt relative to the package bottom is < 1°.

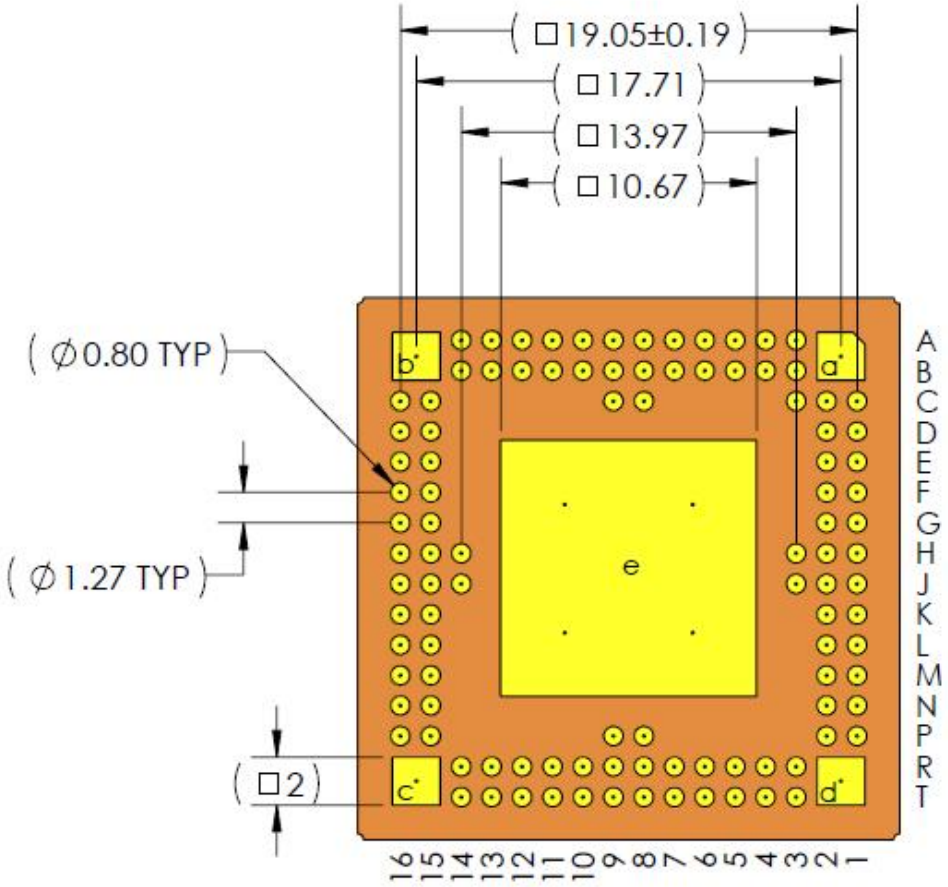
All the dimensions in the above drawing are in mm.

Figure 24. Standard package side view



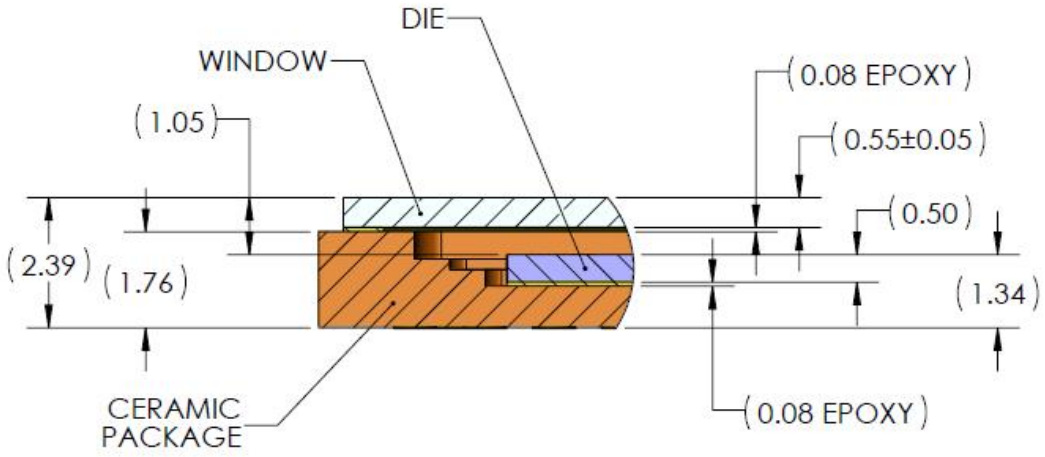
The above dimensions are in mm. The dimensions of the figures on the next page are also in mm.

Figure 25. Standard package bottom view



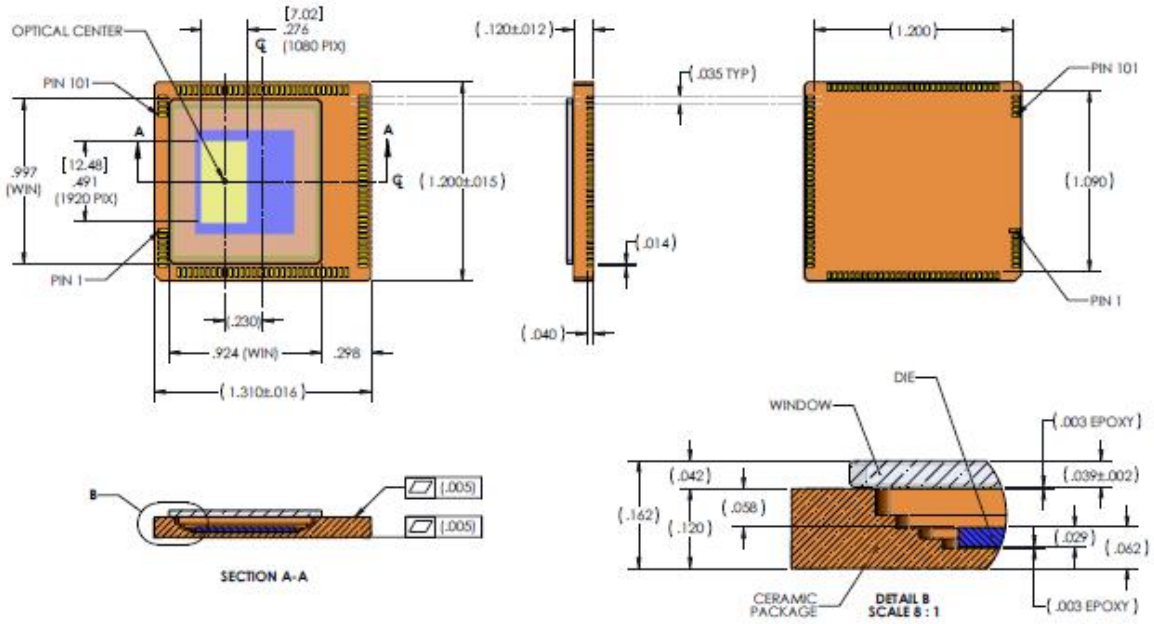
The central thermal pad (“e”, in the above diagram) and the corner pads (“a”, “b”, “c”, and “d”) should all be electrically grounded.

Figure 26. Standard package cross section



Scientific Package drawings

Figure 27. Scientific package overview



All dimensions in the above diagram are in inches except the sensor active area which has dimensions in inches and mm – the dimensions in mm are in brackets.

For soldering the part, the temperature should not exceed 225°C for more than 60 seconds. Follow temperature ramp guidelines in JEDEC/IPC standard J-STD-020, current revision, for the IR/Convection oven reflow profile.

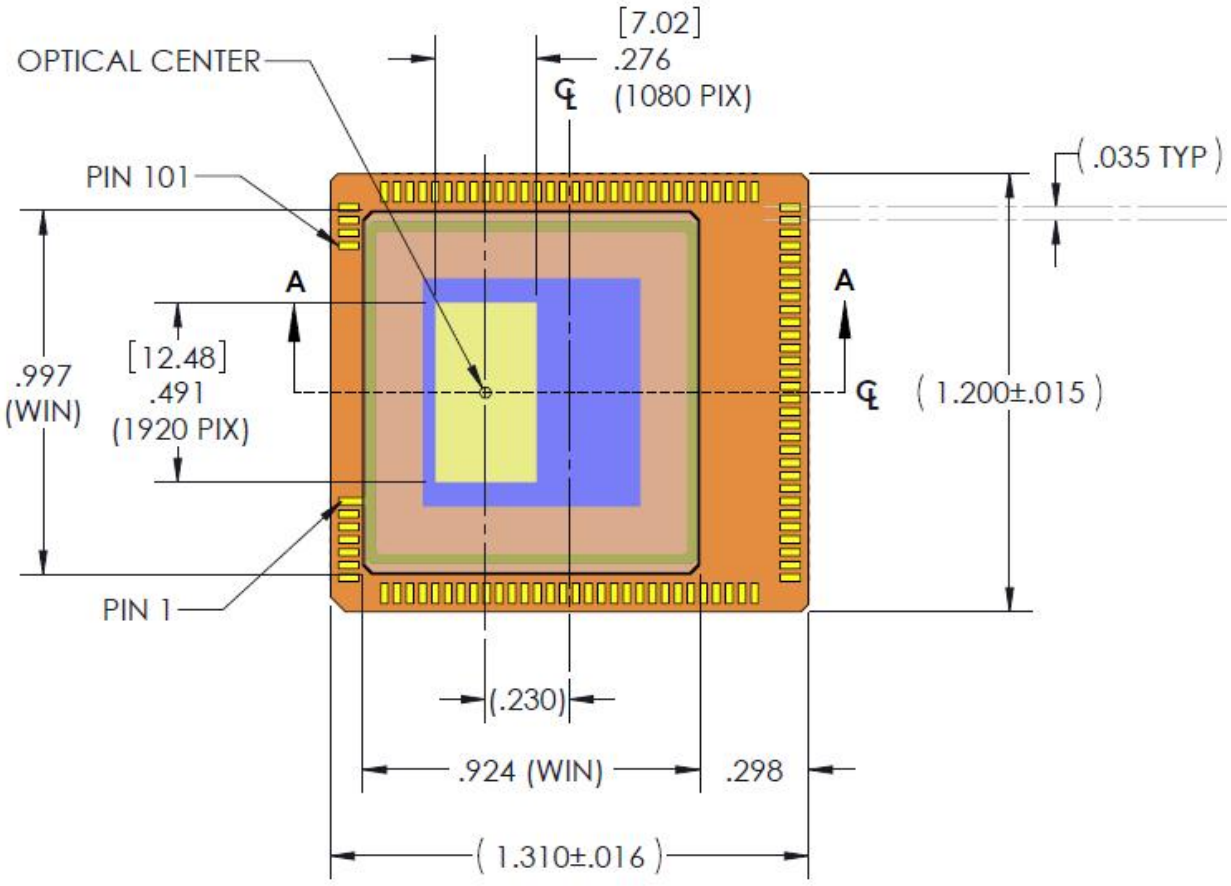
The Moisture Sensitivity Level (MSL) of the package is MSL 2, which means the package can resist moisture ingress under conditions of 30°C and 60% relative humidity for a year or more.

For cleaning the window, first recognize the active area of the sensor. The active area of the sensor is the gray/silver area which is surrounded by the inactive blue area. Only the window surface above the active area needs to be cleaned. Do not pour solvent or any liquid directly on to the window surface. Use a clean, lint-free swab. Dip the swab in methanol or isopropyl alcohol and carefully wipe the surface of the window. Clean, dry air can also be used to blow particle contamination off the window.

Cleaning the sensor active area surface itself is not possible since the CIS1910x121 is always shipped with an epoxy-sealed window that covers the sensor active area. For the CIS1910x101 or CIS1910x111, accessing the die may be possible, but cleaning is not recommended.

For cleaning the sensor package, use a clean, lint-free swab, dipping the swab in methanol or isopropyl alcohol and carefully wiping the sensor package. Acetone can also be used to clean the sensor package, but only if it can be kept away from the window seal epoxy. Clean, dry air can also be used to blow particle contamination off the window.

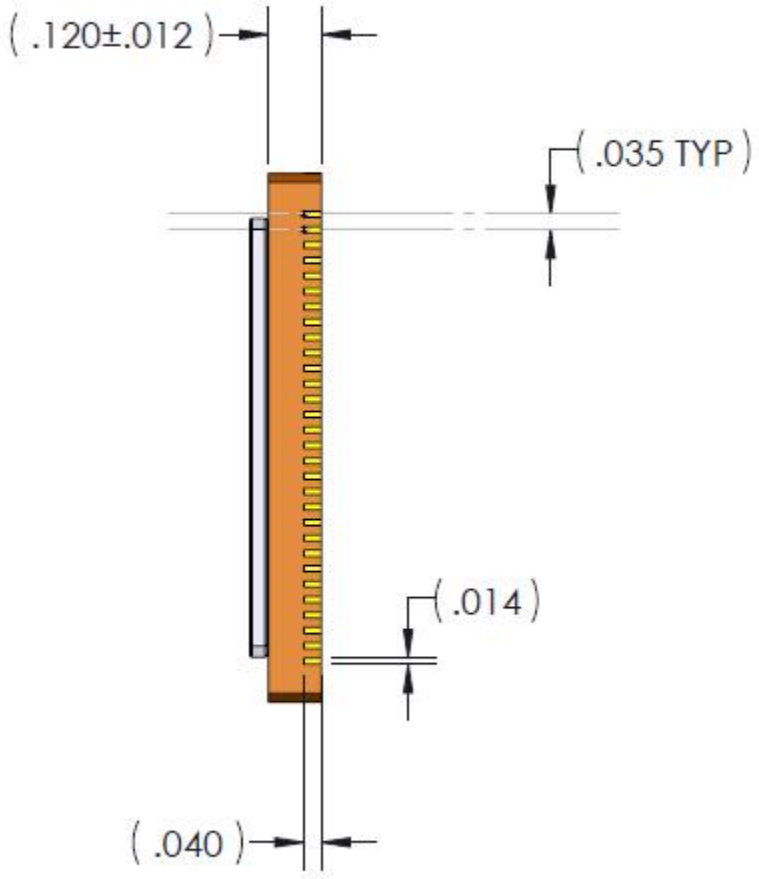
Figure 28. Scientific package top view



The tolerance for positioning the die corners to the package corner fiducials +/- 2.5 mils.
The tolerance for the rotation of the die relative to the package is < 125 microns.
The tolerance for the die tilt relative to the package top and bottom is < 125 microns.

All dimensions in the above diagram are in inches except the sensor active area which has dimensions in inches and mm – the dimensions in mm are in brackets.

Figure 29. Scientific package side view



All dimensions for the figure on this page and the figures on the next page are in inches.

Figure 30. Scientific package bottom view

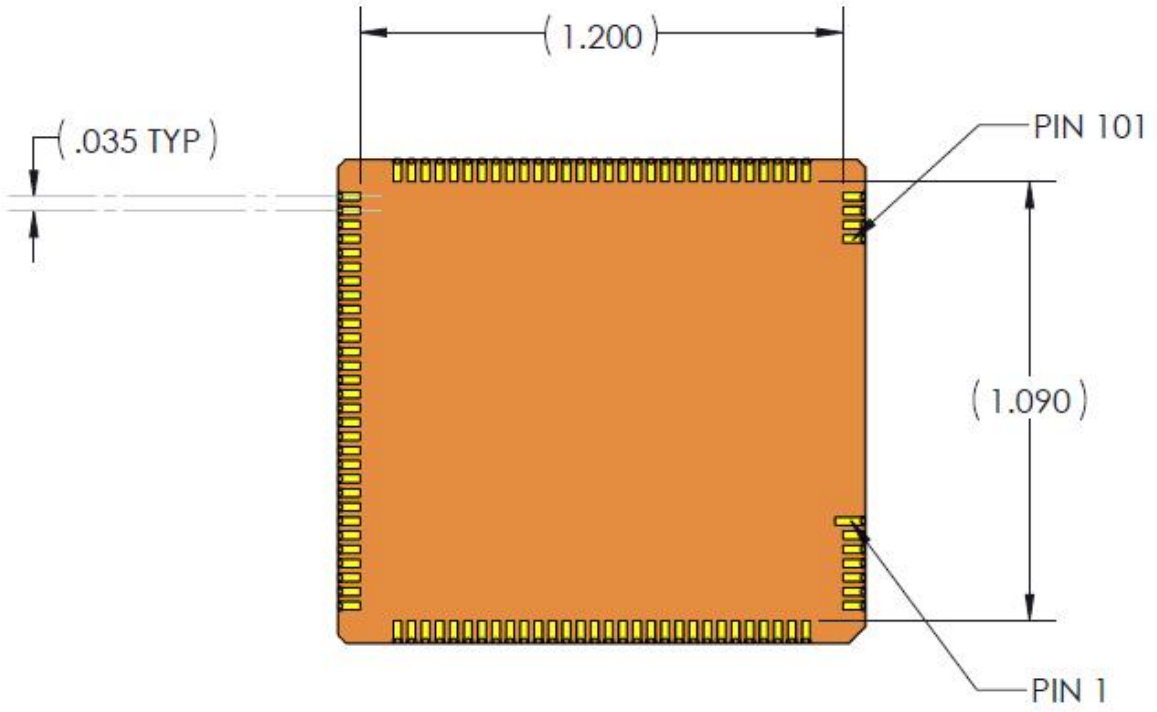
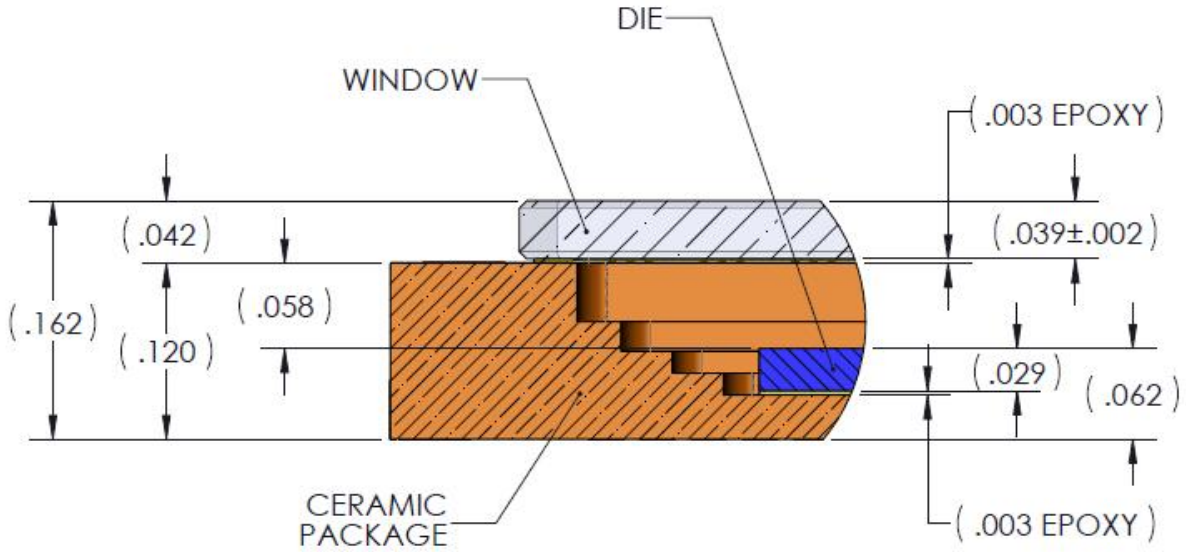
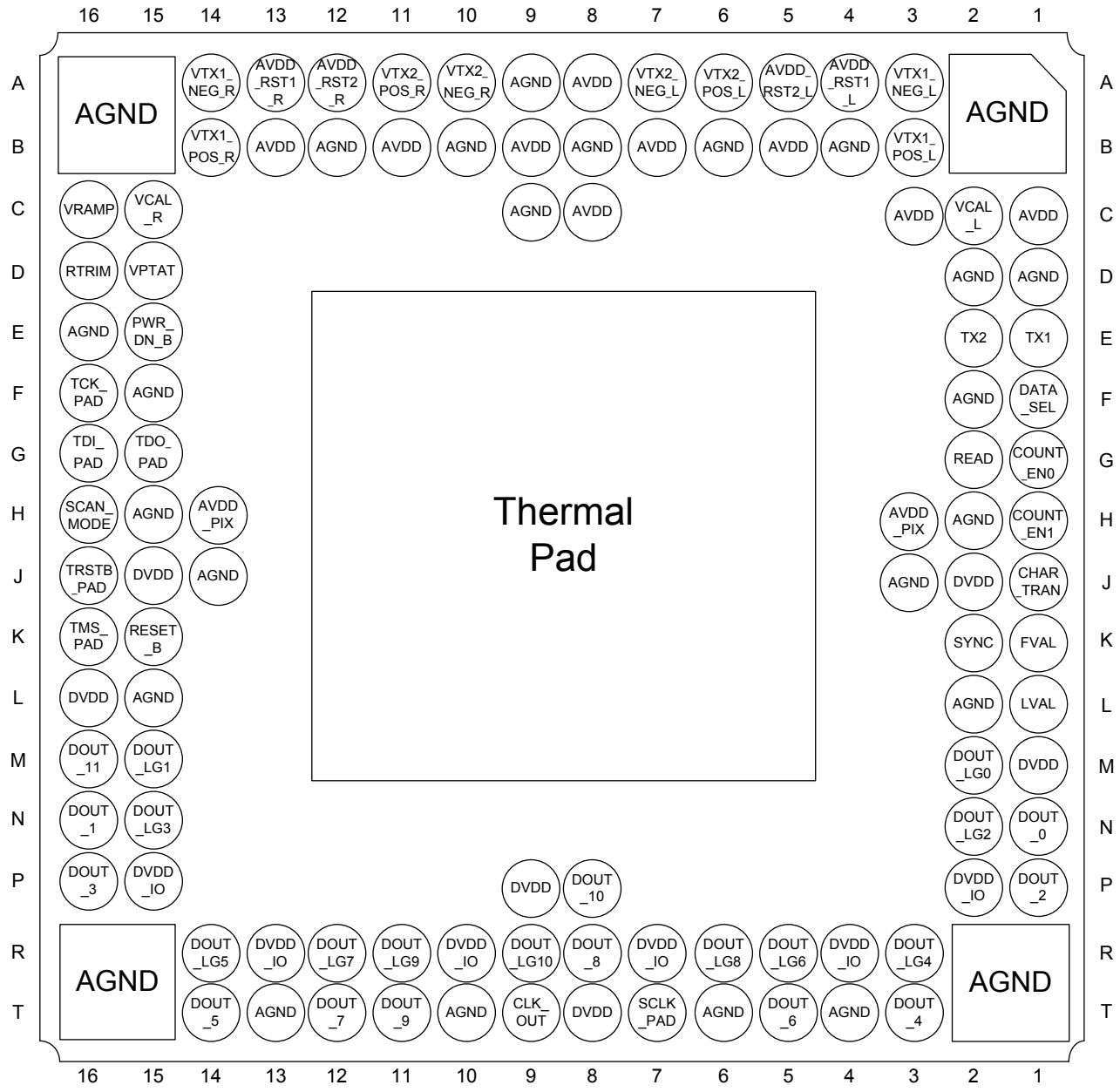


Figure 31. Scientific package cross section



Standard Package Pad Diagram and Pad List

Standard Package Pad Diagram



This diagram shows the pad layout as viewed from the bottom. The orientation of the chip may be found by noting that the pad layout is mostly symmetrical except for the upper right corner. The AGND corner pad is not a perfect square for the upper right corner. Also, the upper right corner has an extra pad (Pad C3).

Standard Package Pad List

The CIS1910 Standard package image sensor has 105 pads in a LGA (Land Grid Array) package. The list shown below provides a complete description of the pad names, their functions and electrical requirements. Note the suffix L is appended to pads on left side of the sensor, and the suffix R is appended to pads on right side of the sensor.

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
A3	VTX1_NEG_L	Power		0~-1.5v/80mA max, Ripple < 100µV RMS	TX1 negative supply
A4	AVDD_RST1_L	Power		2.7-3.0v/1 mA, Ripple < 10 µV RMS	AVDD_RST1 reset supply
A5	AVDD_RST2_L	Power		3.0v/1 mA, Ripple < 10 µV RMS	AVDD_RST2 reset supply
A6	VTX2_POS_L	Power		3.3v/80mA max, Ripple < 1 mV RMS	TX2 positive supply
A7	VTX2_NEG_L	Power		+0.8v to -1.5v/80mA max, Ripple < 1 mV RMS	TX2 negative supply
A8	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
A9	AGND	Ground			AGND common ground 0V
A10	VTX2_NEG_R	Power		+0.8v to -1.5v/80mA max, Ripple < 1 mV RMS	TX2 negative supply
A11	VTX2_POS_R	Power		3.3v/80mA max, Ripple < 1 mV RMS	TX2 positive supply
A12	AVDD_RST2_R	Power		3.0v/1 mA, Ripple < 10 µV RMS	AVDD_RST2 reset supply
A13	AVDD_RST1_R	Power		2.7-3.0v/1 mA, Ripple < 10 µV RMS	AVDD_RST1 reset supply
A14	VTX1_NEG_R	Power		0~-1.5v/80mA max, Ripple < 100µV RMS	TX1 negative supply
B3	VTX1_POS_L	Power		3.3v/80mA max, Ripple < 1 mV RMS	TX1 positive supply
B4	AGND	Ground			AGND common ground 0V
B5	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
B6	AGND	Ground			AGND common ground 0V
B7	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
B8	AGND	Ground			AGND common ground 0V
B9	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
B10	AGND	Ground			AGND common ground 0V
B11	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
B12	AGND	Ground			AGND common ground 0V
B13	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
B14	VTX1_POS_R	Power		3.3v/80mA max, Ripple < 1 mV RMS	TX1 positive supply
C1	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
C2	VCAL_L	Input	Analog		Optional column calibration reference voltage. Normally not used and so this pad is left as no connection or tied to ground. When it is used, the user inputs a fixed voltage (2.5V-1.0V, 1mA), when Register 2 bit 18 = 0 (not the default). With this Register setting, VCAL is connected to the column amplifier inputs (instead of the pixel floating diffusion voltages being connected to the column amplifier inputs).
C3	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
C8	AVDD	Power		3.3v/90mA average, 170mA peak on 5%	AVDD analog supply

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
				duty cycle for each line time, Ripple < 1mV RMS	
C9	AGND	Ground			AGND common ground 0V
C15	VCAL_R	Input	Analog		Optional column calibration reference voltage. Normally not used and so this pad is left as no connection or tied to ground. When it is used, the user inputs a fixed voltage (2.5V-1.0V, 1mA), when Register 2 bit 18 = 0 (not the default). With this Register setting, VCAL is connected to the column amplifier inputs (instead of the pixel floating diffusion voltages being connected to the column amplifier inputs).
C16	VRAMP	Input	Analog		Optional external VRAMP voltage that can be used in place of the internally provided VRAMP. Normally this pad is not used and can be left as a no connection or tied to ground. If it is used, the user inputs the ADC ramp voltage (from 1.0V to 2.5V, 20mA) using timing signals from COUNT_EN[1:0].
D1	AGND	Ground			AGND common ground 0V
D2	AGND	Ground			AGND common ground 0V
D15	VPTAT	Output	Analog		Temperature sensor Output. This pad will output a voltage of slightly over 2 Volts at room temperature that will change linearly with temperature with a slope of 5 to 7 mV per degree Celsius. The exact calibration of offset and slope for VPTAT must be performed by the user with a reference temperature sensor (e.g. a thermocouple).
D16	RTRIM	Output	Analog		External current reference resistor pad. This pad must have a 12.2 kΩ resistor attached to this pad at one end and tied to ground at the other end. Providing this pad with a path to ground through a 12.2 kΩ resistor is necessary for the functioning of the column amplifiers.
E1	TX1	Input	1.8v lvcmos		Global TX1 Charge transfer control, rise/fall time < 500ns, Skew < 100ns, Ripple < 100µV RMS
E2	TX2	Input	1.8v		Global TX2 Charge dump control,

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
			lvcmos		rise/fall time < 500ns, Skew < 100ns, Ripple < 1mV RMS
E15	PWR_DN_B	Input	1.8v lvcmos		Power Down Input (active low). Setting this pad to logic 0 has the same effect as setting Register 2 bit 25 to 1. It enables the low power control register, Register 12.
E16	AGND	Ground			AGND common ground 0V
F1	DATA_SEL	Input	1.8v lvcmos		DATA_SEL = 0 selects wavetable A for sensor readout and wavetable B for read/write access. DATA_SEL = 1 selects wavetable B for sensor readout and wavetable A for read/write access. Typically, for Rolling Shutter operation, wavetable A is always used fro sensor readout, so DATA_SEL = 0 (fixed). For Global Shutter operation, DATA_SEL = 0 selects wavetable A (the GS Reset frame) and DATA_SEL = 1 selects wavetable B (the GS Data frame) so DATA_SEL is constantly switching between 0 and 1.
F2	AGND	Ground			AGND common ground 0V
F15	AGND	Ground			AGND common ground 0V
F16	TCK_PAD	Input	1.8v lvcmos		SPI clock (clk) This clock must be 25 MHz or less.
G1	COUNT_EN0	Output	1.8v hstl		External count and external VRAMP synchronization Output, bit 0. Normally ignored unless the external VRAMP (pad C16) is being used (which it typically is not).
G2	READ	Input	1.8v lvcmos		External start/pause row counter and readout activities control Input from pad
G15	TDO_PAD	Output	1.8v hstl		SPI serial data Output (so)
G16	TDI_PAD	Input	1.8v lvcmos		SPI serial data Input (si)
H1	COUNT_EN1	Output	1.8v hstl		External count and external VRAMP synchronization Output, bit 1. Normally ignored unless the external VRAMP (pad C16) is being used (which it typically is not).
H2	AGND	Ground			AGND common ground 0V
H3	AVDD_PIX	Power		3.3v/10mA avg, Ripple < 100 µV RMS	Pixel source follower supply

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
H14	AVDD_PIX	Power		3.3v/10mA avg, Ripple < 100 µV RMS	Pixel source follower supply
H15	AGND	Ground			AGND common ground 0V
H16	SCAN_MODE	Input	1.8v lvcmos		Input switch to put the sensor into “Scan Mode” when logic 1 is input. SCAN_MODE is an internal BAE test so the customer should always tie this pad to ground.
J1	CHARGE_TRANS	Output	1.8v hstl		Marker pulse indicating when data sampling of the floating node voltage is occurring for the selected row. This signal comes directly from the wavetable without any modification. In Global Shutter, the user must supply TX1, TX2, and DATA_SEL inputs on external pads, and the timing of these signals should (usually) be correlated with CHARGE_TRANS.
J2	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
J3	AGND	Ground			AGND common ground 0V
J14	AGND	Ground			AGND common ground 0V
J15	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
J16	TRSTB_PAD	Input	1.8v lvcmos		Optional SPI Reset This pad is optional but it is still functional in that a logic 0 on this pad will put the SPI controller in a reset state that prevents the other SPI pads from working. Therefore, in SPI mode, this pad should be tied to logic 1.
K1	FVAL	Output	1.8v hstl		Frame valid Output, also called F_VALID. Will be high when data from the physical array (i.e. active imager rows and dark rows, but not pre-scan rows) is being output on the DOUT/DOUT_LG pads.
K2	SYNC	Output	1.8v hstl		Marker pulse for line or frame. This signal comes from the wavetable and will pulse once at the beginning of each line (if Register 11 bit 14 = 0, the default) or once at the beginning of each frame (if Register 11 bit 14 = 1).
K15	RESET_B	Input	1.8v lvcmos		Active low reset to the chip. RESET_B = 0 will reset all state machines and reload default values to the registers. The effect of a RESETB = 0 on the

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
					chip is equivalent to power cycling the chip.
K16	TMS_PAD	Input	1.8v lvcmos		SPI active low chip enable (ceb)
L1	LVAL	Output	1.8v hstl		Line valid Output, also called L_VALID. Will be high once each line during the period each line time when data is appearing on the DOUT/DOUT_LG pads.
L2	AGND	Ground			AGND common ground 0V
L15	AGND	Ground			AGND common ground 0V
L16	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
M1	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
M2	DOUT_LG0	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 0. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
M15	DOUT_LG1	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 1. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
M16	DOUT_11	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is always 0 because the DOUT[10:0] pads will only output data from the High gain channel. If Register 2 bit 20 = 1, data multiplexing for the DOUT pads is enabled, and this Output will be logic 0 when DOUT[10:0] is High gain data and this Output will be logic 1 when DOUT[10:0] is Low gain data.
N1	DOUT_0	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 0. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
					multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 0. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
N2	DOUT_LG2	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 2. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
N15	DOUT_LG3	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 3. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
N16	DOUT_1	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 1. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 1. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
P1	DOUT_2	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 2. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip.

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
					If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 2. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
P2	DVDD_IO	Power		1.8v/65 mA max, Ripple < 1 mV RMS	DVDD digital core supply
P8	DOUT_10	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 10. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 10. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
P9	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
P15	DVDD_IO	Power		1.8v/65 mA max, Ripple < 1 mV RMS	DVDD digital core supply
P16	DOUT_3	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 3. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 3. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0],

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
					including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
R3	DOUT_LG4	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 4. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
R4	DVDD_IO	Power		1.8v/65 mA max, Ripple < 1 mV RMS	DVDD digital core supply
R5	DOUT_LG6	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 6. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
R6	DOUT_LG8	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 8. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
R7	DVDD_IO	Power		1.8v/65 mA max, Ripple < 1 mV RMS	DVDD digital core supply
R8	DOUT_8	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 8. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 8. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.

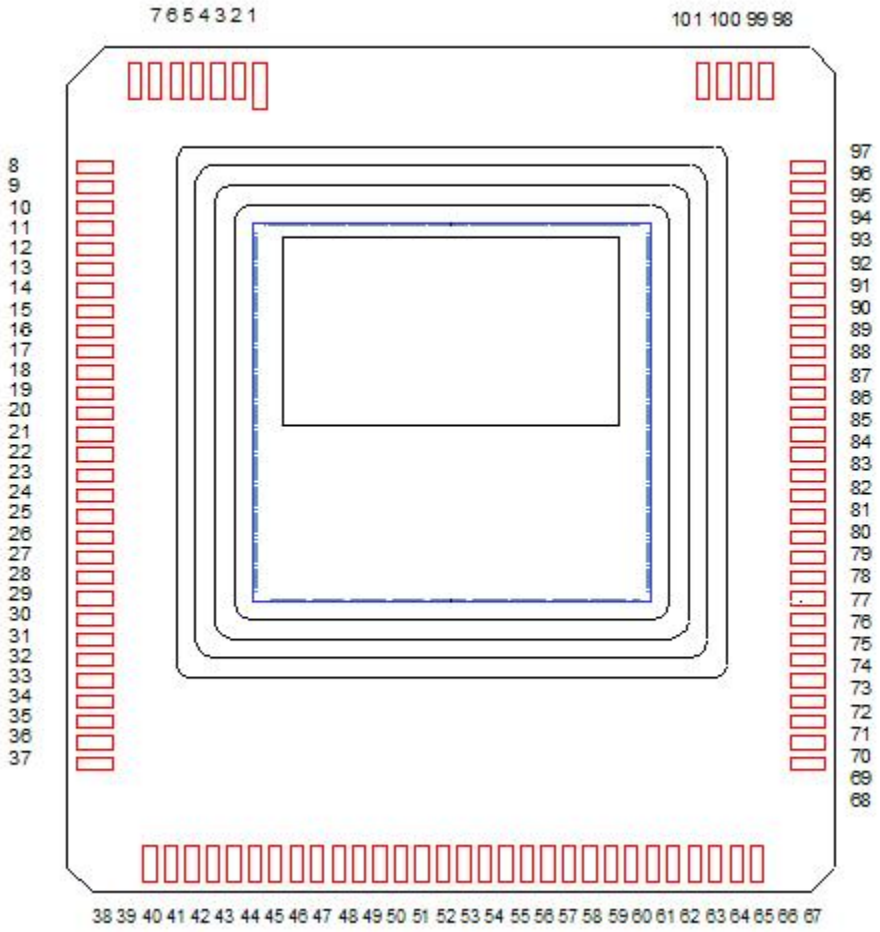
Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
R9	DOUT_LG10	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 10. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
R10	DVDD_IO	Power		1.8v/65 mA max, Ripple < 1 mV RMS	DVDD digital core supply
R11	DOUT_LG9	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 9. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
R12	DOUT_LG7	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 7. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
R13	DVDD_IO	Power		1.8v/65 mA max, Ripple < 1 mV RMS	DVDD digital core supply
R14	DOUT_LG5	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is Low gain ADC Output bit 5. The DOUT_LG[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pad is forced to 0.
T3	DOUT_4	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 4. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 4. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case,

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
					DOUT[10:0] is in Gray code and must be converted to binary off-chip.
T4	AGND	Ground			AGND common ground 0V
T5	DOUT_6	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 6. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 6. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
T6	AGND	Ground			AGND common ground 0V
T7	SCLK_PAD	Input	1.8v hstl		System clock. Input frequency should be between 30 MHz and 283 MHz.
T8	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
T9	CLK_OUT	Output	1.8v hstl		Clock to synchronize the data Output. This output clock is from the user-supplied input clock SCLK. CLK_OUT may have some phase shift relative to SCLK but it will be of the same frequency. The phase of the data on the DOUT and DOUT_LG pads is aligned to the phase of CLK_OUT.
T10	AGND	Ground			AGND common ground 0V
T11	DOUT_9	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 9. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 9. If the binary

Pad number	Pad name	Pad type	Signal type	Power voltage/current	Pad description
					value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
T12	DOUT_7	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 7. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 7. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
T13	AGND	Ground			AGND common ground 0V
T14	DOUT_5	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pad is High gain ADC Output bit 5. The DOUT[10:0] pad data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pad uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 5. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pad. Otherwise, Low gain data will appear on DOUT[10:0], including this pad. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.

Scientific Package Pin Diagram and Pin list

Scientific Package Pin Diagram



Scientific package Pin List

The CIS1910 Scientific Package is a 101-pin ceramic leadless chip carrier (LCC package). The list shown below provides a complete description of the pin names, their functions and electrical requirements. Note the suffix L is appended to pins on left side of the sensor, and the suffix R is appended to pins on right side of the sensor.

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
1	AGND	Ground			AGND common ground 0V
2	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each	AVDD analog supply

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
				line time, Ripple < 1mV RMS	
3	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
4	VTX1_NEG_L	Power		0~-1.5v/80mA max, Ripple < 100µV RMS	TX1 negative supply
5	AGND	Ground			AGND common ground 0V
6	VTX1_POS_L	Power		3.3v/80mA max, Ripple < 1 mV RMS	TX1 positive supply
7	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
8	AVDD_RST1_L	Power		2.7-3.0v/1 mA, Ripple < 10 µV RMS	AVDD_RST1 reset supply
9	AGND	Ground			AGND common ground 0V
10	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
11	AGND	Ground			AGND common ground 0V
12	AVDD_RST2_L	Power		3.0v/1mA, Ripple < 10µV RMS	AVDD_RST2 reset supply
13	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
14	VTX2_POS_L	Power		3.3v/80mA max, Ripple < 1mV RMS	TX2 positive supply
15	AGND	Ground			AGND common ground 0V
16	VTX2_NEG_L	Power		+0.8v to -1.5v 80mA max, Ripple < 1mV RMS	TX2 negative supply
17	AVDD_PIX	Power		3.3v/10mA avg, Ripple < 100µV RMS	Pixel source follower supply
18	VCAL_L	Input	Analog		Optional column calibration reference voltage. Normally not used and so this pin is left as no connection or tied to ground. When it is used, the user inputs a fixed

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					voltage (2.5V-1.0V, 1mA), when Register 2 bit 18 = 0 (not the default). With this Register setting, VCAL is connected to the column amplifier inputs (instead of the pixel floating diffusion voltages being connected to the column amplifier inputs).
19	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
20	TX2	Input	1.8v lvcmos		Global TX2 Charge dump control, rise/fall time < 500ns, Skew < 100ns, Ripple < 1mV RMS
21	AGND	Ground			AGND common ground 0V
22	TX1	Input	1.8v lvcmos		Global TX1 Charge transfer control, rise/fall time < 500ns, Skew < 100ns, Ripple < 100µV RMS
23	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
24	DATA_SEL	Input	1.8v lvcmos		DATA_SEL = 0 selects wavetable A for sensor readout and wavetable B for read/write access. DATA_SEL = 1 selects wavetable B for sensor readout and wavetable A for read/write access. Typically, for Rolling Shutter operation, wavetable A is always used fro sensor readout, so DATA_SEL = 0 (fixed). For Global Shutter operation, DATA_SEL = 0 selects wavetable A (the GS Reset frame) and DATA_SEL = 1 selects wavetable B (the GS Data frame) so DATA_SEL is constantly switching between 0 and 1.
25	AGND	Ground			AGND common ground 0V

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
26	READ	Input	1.8v lvcmos		External start/pause readout activities control Input from pin
27	DVDD_IO	Power		1.8v/65mA max, Ripple < 25mV RMS	DVDD digital core supply
28	COUNT_EN0	Output	1.8v hstl		External count and EXT_VRAMP synchronization Output, bit 0. Normally ignored unless EXT_VRAMP is being used (which it typically is not).
29	COUNT_EN1	Output	1.8v hstl		External count and EXT_VRAMP synchronization Output, bit 1. Normally ignored unless EXT_VRAMP is being used (which it typically is not).
30	AGND	Ground			AGND common ground 0V
31	CHAR_TRAN	Output	1.8v hstl		Marker pulse indicating when data sampling of the floating node voltage is occurring for the selected row. This signal comes directly from the wavetable without any modification. In Global Shutter, the user must supply TX1, TX2, and DATA_SEL inputs on external pins, and the timing of these signals should (usually) be correlated with CHARGE_TRANS.
32	DVDD_IO	Power		1.8v/65mA max, Ripple < 25mV RMS	DVDD digital core supply
33	SYNC	Output	1.8v hstl		Marker pulse for line or frame. This signal comes from the wavetable and will pulse once at the beginning of each line (if Register 11 bit 14 = 0, the default) or once at the beginning of each frame (if Register 11 bit 14 = 1).
34	FVAL	Output	1.8v hstl		Frame valid Output, also called F_VALID. Will be high when data from the

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					physical array (i.e. active imager rows and dark rows, but not pre-scan rows) is being output on the DOUT/DOUT_LG pins.
35	LVAL	Output	1.8v hstl		Line valid Output, also called L_VALID. Will be high once each line during the period each line time when data is appearing on the DOUT/DOUT_LG pins.
36	AGND	Ground			AGND common ground 0V
37	DOUT_LG0	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 0. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
38	DVDD_IO	Power		1.8v/65mA max, Ripple < 25mV RMS	DVDD digital core supply
39	DOUT_0	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 0. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 0. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					chip.
40	DOUT_LG2	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 2. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
41	DOUT_2	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 2. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 2. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
42	AGND	Ground			AGND common ground 0V
43	DOUT_LG4	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 4. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
44	DOUT_4	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 4. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 4. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
45	DOUT_LG6	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 6. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
46	DVDD_IO	Power		1.8v/65mA max, Ripple < 25mV RMS	DVDD digital core supply
47	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
48	DOUT_6	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 6. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1,

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 6. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
49	DOUT_LG8	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 8. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
50	DOUT_8	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 8. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 8. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case,

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					DOUT[10:0] is in Gray code and must be converted to binary off-chip.
51	AGND	Ground			AGND common ground 0V
52	DOUT_LG10	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 10. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
53	DOUT_10	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 10. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 10. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
54	SCLK_PIN	Input	1.8v hstl		System clock. Input frequency should be between 30 MHz and 283 MHz.
55	CLK_OUT	Output	1.8v hstl		Clock to synchronize the data Output.

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					This output clock is from the user-supplied input clock SCLK. CLK_OUT may have some phase shift relative to SCLK but it will be of the same frequency. The phase of the data on the DOUT and DOUT_LG pins is aligned to the phase of CLK_OUT.
56	AGND	Ground			AGND common ground 0V
57	DOUT_9	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 9. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 9. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
58	DOUT_LG9	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 9. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
59	DOUT_7	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 7. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 7. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
60	DOUT_LG7	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 7. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
61	DOUT_5	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 5. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 5. If the binary

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
62	DOUT_LG5	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 5. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
63	DOUT_3	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 3. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 3. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
64	DOUT_LG3	Output	1.8v hstl		If Register 2 bit 20 = 0 (the

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					default), this pin is Low gain ADC Output bit 3. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
65	AGND	Ground			AGND common ground 0V
66	DOUT_1	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is High gain ADC Output bit 1. The DOUT[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, data multiplexing is enabled and this pin uses the contents of Register 5 as a threshold to select the Low or High gain of ADC Output bit 1. If the binary value of the High gain channel is less than or equal to the threshold, High gain data will appear on DOUT[10:0], including this pin. Otherwise, Low gain data will appear on DOUT[10:0], including this pin. In any case, DOUT[10:0] is in Gray code and must be converted to binary off-chip.
67	DOUT_LG1	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is Low gain ADC Output bit 1. The DOUT_LG[10:0] pin data is in Gray code and must be converted to binary off-chip. If Register 2 bit 20 = 1, this pin is forced to 0.
68	DOUT_11	Output	1.8v hstl		If Register 2 bit 20 = 0 (the default), this pin is always 0 because the DOUT[10:0] pins will only output data

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					from the High gain channel. If Register 2 bit 20 = 1, data multiplexing for the DOUT pins is enabled, and this Output will be logic 0 when DOUT[10:0] is High gain data and this Output will be logic 1 when DOUT[10:0] is Low gain data.
69	DVDD_IO	Power		1.8v/65mA max, Ripple < 25mV RMS	DVDD digital core supply
70	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply
71	RESET_B	Input	1.8v lvcmos		Sensor reset (active low) RESET_B = 0 will reset all state machines and reload default values to the registers. The effect of a RESETB = 0 on the chip is equivalent to power cycling the chip.
72	AGND	Ground			AGND common ground 0V
73	TMS_PAD	Input	1.8v lvcmos		SPI active low chip enable (ceb)
74	TRSTB_PAD	Input	1.8v lvcmos		SPI reset input (active low) This pin is optional but it is still functional in that a logic 0 on this pin will put the SPI controller in a reset state that prevents the other SPI pins from working. Therefore this pin should be tied to logic 1.
75	AGND	Ground			AGND common ground 0V
76	SCAN_MODE	Input	1.8v lvcmos		Input switch to put the sensor into “Scan Mode” when logic 1 is input. SCAN_MODE is an internal BAE test so the customer should always tie this pin to ground.
77	DVDD_IO	Power		1.8v/65mA max, Ripple < 25mV RMS	DVDD digital core supply

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
78	TDI_PAD	Input	1.8v lvcmos		SPI serial data Input (si)
79	TCK_PAD	Input	1.8v lvcmos		SPI clock (clk) This clock must be 25 Mhz or less.
80	TDO_PAD	Output	1.8v hstl		SPI data Output (so)
81	PWR_DN_B	Input	1.8v lvcmos		Power Down Input (active low). Setting this pin to logic 0 has the same effect as setting Register 2 bit 25 to 1. It enables the low power control register, Register 12.
82	VPTAT	Output	Analog		Temperature sensor Output. This pin will output a voltage of slightly over 2 Volts at room temperature that will change linearly with temperature with a slope of 5 to 7 mV per degree Celsius. The exact calibration of offset and slope for VPTAT must be performed by the user with a reference temperature sensor (e.g. a thermocouple).
83	RTRIM	Output	Analog		External current reference resistor pin. This pin must have a 12.2 kΩ resistor attached to this pin at one end and tied to ground at the other end. Providing this pin with a path to ground through a 12.2 kΩ resistor is necessary for the functioning of the column amplifiers.
84	EXT_VRAMP	Input	Analog		Optional EXT_VRAMP voltage that can be used in place of the internally provided VRAMP wheb Register 2 bit 16 = 1. Normally this pin is not

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
					used and can be left as a no connection or tied to ground. If it is used, the user inputs the ADC ramp voltage (from 1.0V to 2.5V, 20mA) using timing signals from COUNT_EN[1:0].
85	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
86	AGND	Ground			AGND common ground 0V
87	VCAL_R	Input	Analog		Optional column calibration reference voltage. Normally not used and so this pin is left as no connection or tied to ground. When it is used, the user inputs a fixed voltage (2.5V-1.0V, 1mA), when Register 2 bit 18 = 0 (not the default). With this Register setting, VCAL is connected to the column amplifier inputs (instead of the pixel floating diffusion voltages being connected to the column amplifier inputs).
88	AVDD_PIX	Power		3.3v/10mA avg, Ripple < 100µV RMS	Pixel source follower supply
89	VTX2_NEG_R	Power		+0.8v to -1.5v /80mA max, Ripple < 1mV RMS	TX2 negative supply
90	AGND	Ground			AGND common ground 0V
91	VTX2_POS_R	Power		3.3v/80mA max, Ripple < 1mV RMS	TX2 positive supply
92	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
93	AVDD_RST2_R	Power		3.0v/1mA, Ripple < 10µV RMS	AVDD_RST2 reset supply
94	AGND	Ground			AGND common ground 0V
95	AVDD_RST1_R	Power		2.7-3.0v/1 mA, Ripple < 10 µV RMS	AVDD_RST1 reset supply

Pin number	Pin name	Pin type	Signal type	Power requirements	Pin Description
96	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
97	VTX1_POS_R	Power		3.3v/80mA max, Ripple < 1 mV RMS	TX1 positive supply
98	AGND	Ground			AGND common ground 0V
99	VTX1_NEG_R	Power		0~-1.5v/80mA max, Ripple < 100µV RMS	TX1 negative supply
100	AVDD	Power		3.3v/90mA average, 170mA peak on 5% duty cycle for each line time, Ripple < 1mV RMS	AVDD analog supply
101	DVDD	Power		1.8v/160 mA max, Ripple < 25 mV RMS	DVDD digital core supply

Monochromatic Quantum Efficiency

Unless otherwise specified, this datasheet assumes the CIS1910 sensor is monochromatic (i.e. it has no color filter), and a QE curve for the monochromatic sensor is shown in Figure 32. However, adding a color filter is an option with the CIS1910. The color filter spatial arrangement is shown in Figure 33, and the QE curves of the RGB color filters are shown in Figure 34.

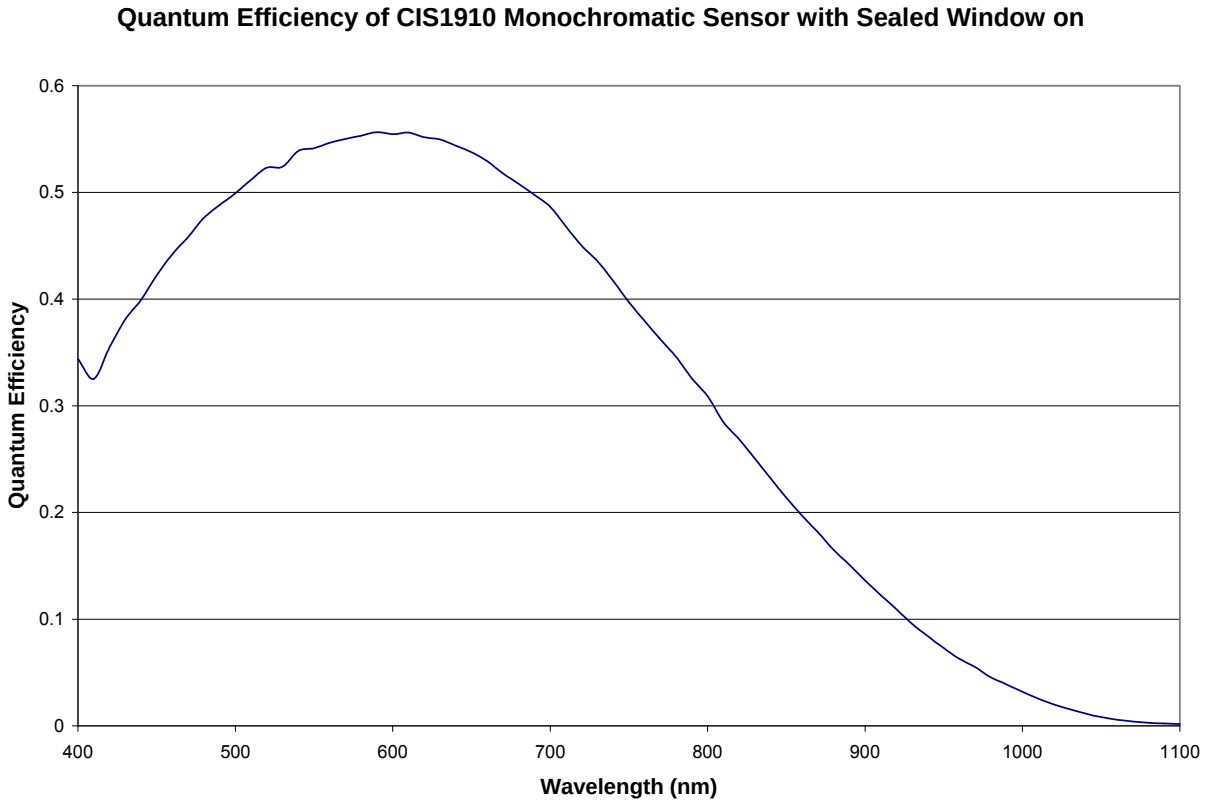


Figure 32. Typical QE versus wavelength plot for a monochromatic sensor

A table showing the monochromatic Quantum Efficiency at increments of 10 nm is shown on the next page. Values shown are typical. Data was taken with the Sealed window on.

WaveLength	Monochromatic	WaveLength	Monochromatic	WaveLength	Monochromatic
400 nm	0.34	640 nm	0.54	880 nm	0.17
410 nm	0.33	650 nm	0.54	890 nm	0.15
420 nm	0.35	660 nm	0.53	900 nm	0.14
430 nm	0.38	670 nm	0.52	910 nm	0.12
440 nm	0.40	680 nm	0.51	920 nm	0.11
450 nm	0.42	690 nm	0.50	930 nm	0.10
460 nm	0.44	700 nm	0.49	940 nm	0.08
470 nm	0.46	710 nm	0.47	950 nm	0.07
480 nm	0.47	720 nm	0.45	960 nm	0.06
490 nm	0.49	730 nm	0.44	970 nm	0.06
500 nm	0.50	740 nm	0.42	980 nm	0.05
510 nm	0.51	750 nm	0.40	990 nm	0.04
520 nm	0.52	760 nm	0.38	1000 nm	0.03
530 nm	0.52	770 nm	0.36	1010 nm	0.03
540 nm	0.54	780 nm	0.35	1020 nm	0.02
550 nm	0.54	790 nm	0.33	1030 nm	0.02
560 nm	0.55	800 nm	0.31	1040 nm	0.01
570 nm	0.55	810 nm	0.28	1050 nm	0.01
580 nm	0.55	820 nm	0.27	1060 nm	0.01
590 nm	0.56	830 nm	0.25	1070 nm	0.00
600 nm	0.55	840 nm	0.23	1080 nm	0.00
610 nm	0.56	850 nm	0.21	1090 nm	0.00
620 nm	0.55	860 nm	0.20	1100 nm	0.00
630 nm	0.55	870 nm	0.18		

Color Filter Array (CFA) Option

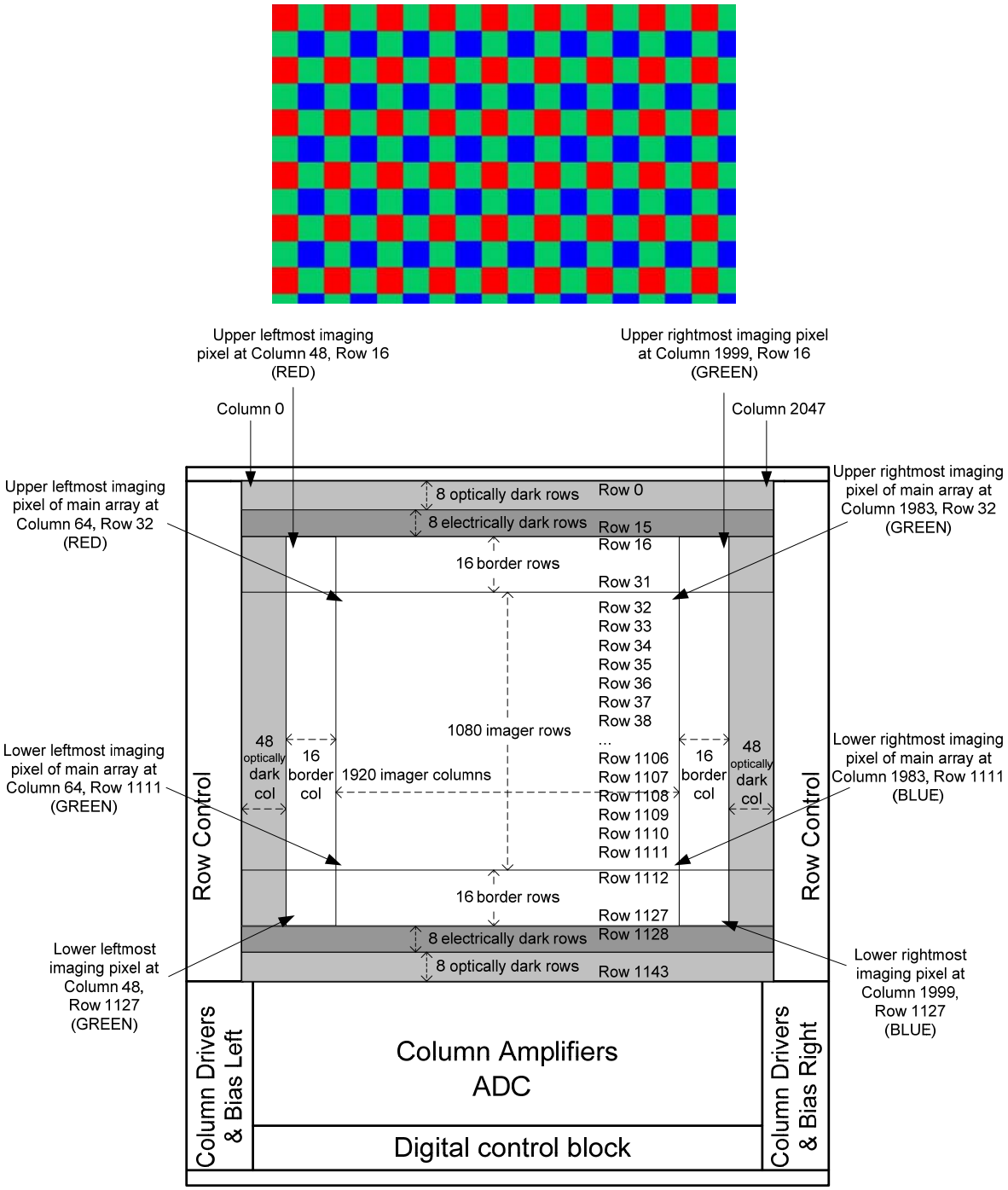


Figure 33. Color Filter Array

The Bayer pattern RGB Color Filter Array (CFA) covers the 1952 (H) x 1112 (V) imaging pixels and extends 2 pixels deep into the dark pixels region on all 4 sides.
Even numbered rows are Red/Green, with even columns Red and odd columns Green.
Odd numbered rows are Green/Blue, with even columns Green and odd columns Blue.

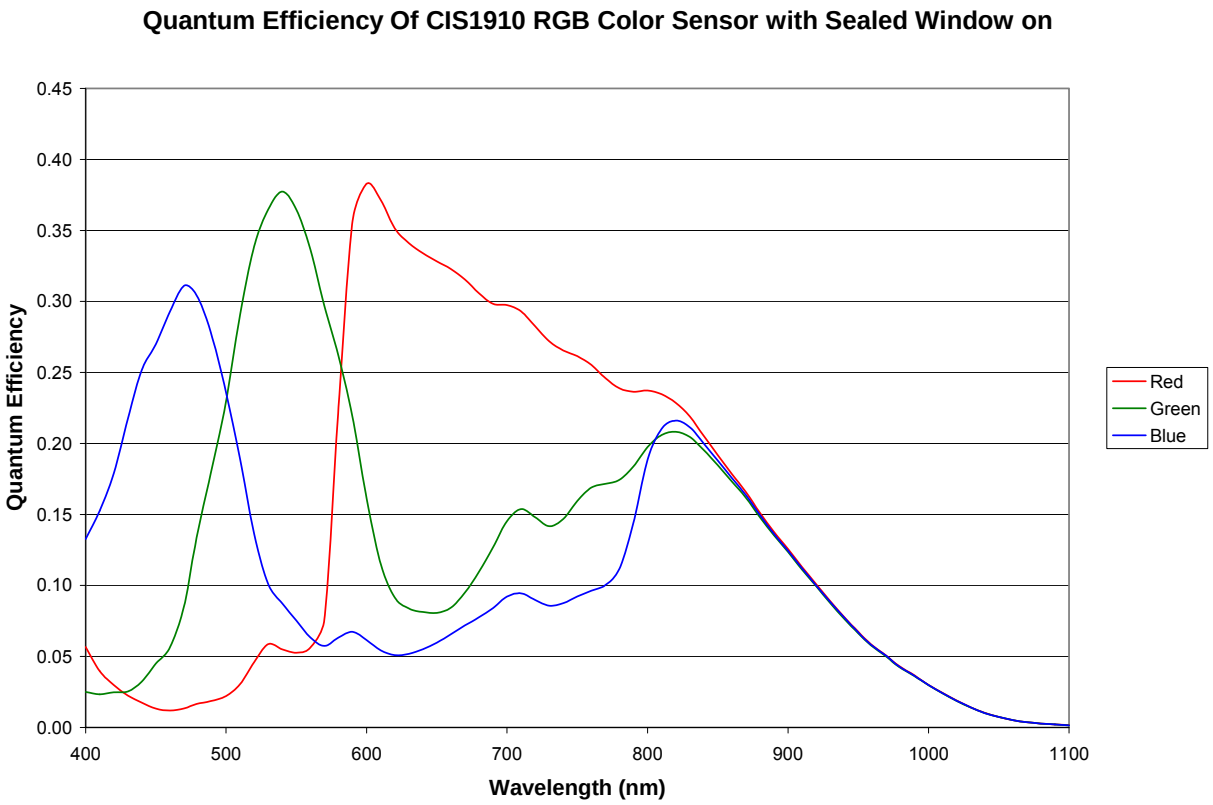


Figure 34. CFA QE Curves

A table showing the RGB color Quantum Efficiency at increments of 10 nm is shown on the next page. Values shown are typical. Data was taken with the Sealed window on.

WaveLength	Red	Green	Blue	WaveLength	Red	Green	Blue
400 nm	0.06	0.03	0.13	760 nm	0.26	0.17	0.10
410 nm	0.04	0.02	0.15	770 nm	0.25	0.17	0.10
420 nm	0.03	0.02	0.18	780 nm	0.24	0.17	0.11
430 nm	0.02	0.03	0.22	790 nm	0.24	0.18	0.14
440 nm	0.02	0.03	0.25	800 nm	0.24	0.20	0.19
450 nm	0.01	0.05	0.27	810 nm	0.23	0.21	0.21
460 nm	0.01	0.06	0.29	820 nm	0.23	0.21	0.22
470 nm	0.01	0.09	0.31	830 nm	0.22	0.20	0.21
480 nm	0.02	0.13	0.30	840 nm	0.21	0.20	0.20
490 nm	0.02	0.18	0.28	850 nm	0.19	0.18	0.19
500 nm	0.02	0.23	0.24	860 nm	0.18	0.17	0.18
510 nm	0.03	0.29	0.19	870 nm	0.17	0.16	0.16
520 nm	0.05	0.34	0.14	880 nm	0.15	0.15	0.15
530 nm	0.06	0.36	0.10	890 nm	0.14	0.14	0.14
540 nm	0.05	0.38	0.09	900 nm	0.13	0.12	0.12
550 nm	0.05	0.36	0.08	910 nm	0.11	0.11	0.11
560 nm	0.06	0.34	0.06	920 nm	0.10	0.10	0.10
570 nm	0.08	0.30	0.06	930 nm	0.09	0.09	0.09
580 nm	0.23	0.26	0.06	940 nm	0.08	0.08	0.08
590 nm	0.36	0.22	0.07	950 nm	0.07	0.07	0.07
600 nm	0.38	0.16	0.06	960 nm	0.06	0.06	0.06
610 nm	0.37	0.12	0.05	970 nm	0.05	0.05	0.05
620 nm	0.35	0.09	0.05	980 nm	0.04	0.04	0.04
630 nm	0.34	0.08	0.05	990 nm	0.04	0.04	0.04
640 nm	0.33	0.08	0.06	1000 nm	0.03	0.03	0.03
650 nm	0.33	0.08	0.06	1010 nm	0.02	0.02	0.02
660 nm	0.32	0.08	0.07	1020 nm	0.02	0.02	0.02
670 nm	0.32	0.09	0.07	1030 nm	0.01	0.01	0.01
680 nm	0.31	0.11	0.08	1040 nm	0.01	0.01	0.01
690 nm	0.30	0.13	0.08	1050 nm	0.01	0.01	0.01
700 nm	0.30	0.15	0.09	1060 nm	0.01	0.01	0.01
710 nm	0.29	0.15	0.09	1070 nm	0.00	0.00	0.00
720 nm	0.28	0.15	0.09	1080 nm	0.00	0.00	0.00
730 nm	0.27	0.14	0.09	1090 nm	0.00	0.00	0.00
740 nm	0.27	0.15	0.09	1100 nm	0.00	0.00	0.00
750 nm	0.26	0.16	0.09				

Cosmetic Specifications

Defect classification	Criteria	Maximum Count	Comments
Hot Pixels in Dark Frame	± 6 sigma from the mean	2000	Low gain only
Cold/Warm Pixels in Light Frame – Minor Defects	> 15% from the mean	2000	Low gain only
Cold/Warm Pixels in Light Frame – Major Defects	> 50% from the mean	25	Low gain only
Small Cluster in Light Frame – Qty Allowed	± 6 sigma from the mean 2 < Size <= 20pix	50	Low gain only
Large Cluster in Light Frame– Qty Allowed	± 6 sigma from the mean Size > 20pix	0	Low gain only
Column -- Qty Allowed	± 10% gain variation from the mean	0	Low gain only, Light frame – dark frame
Row -- Qty Allowed	± 10% gain variation from the mean	0	Low gain only, Light frame – dark frame

Test conditions
Blemish tests are performed in Rolling Shutter mode; light frame captured at 50% of saturation. Dark frame captured at 91 ms integration time.

Defect measurements are performed on the full active pixel array.

Storage Conditions

Parameter	Minimum	Maximum	Units
Temperature	-40	+85	ºC

Handling Precautions

To avoid damaging the device during handling, special care must be used with strict ESD controls. Use only ESD protected tools and ESD protected workstations. Operators must be equipped with approved ESD safe garments and use approved grounding equipment.

Revision History

Date	Revision	Description
June 2011	NR	Initial Release
July 2011	A	Incorporated Recommended Settings
August 2012	B	Changed name of sensor to CIS1910, added Standard package, updated color QE
December 2012	C	Altered die placement, tilt and rotation specs. Clarified standard package thermal pad grounding. Raised storage high temperature limit. Changed sensor nomenclature to have 4 digit suffix. Added revision disclaimer.

Disclaimer

BAE Systems reserves the right to make any changes to this product during an existing contract period providing it does not materially affect the form, fit or function of a Customer's next assembly product with BAE Systems' previously released design.

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