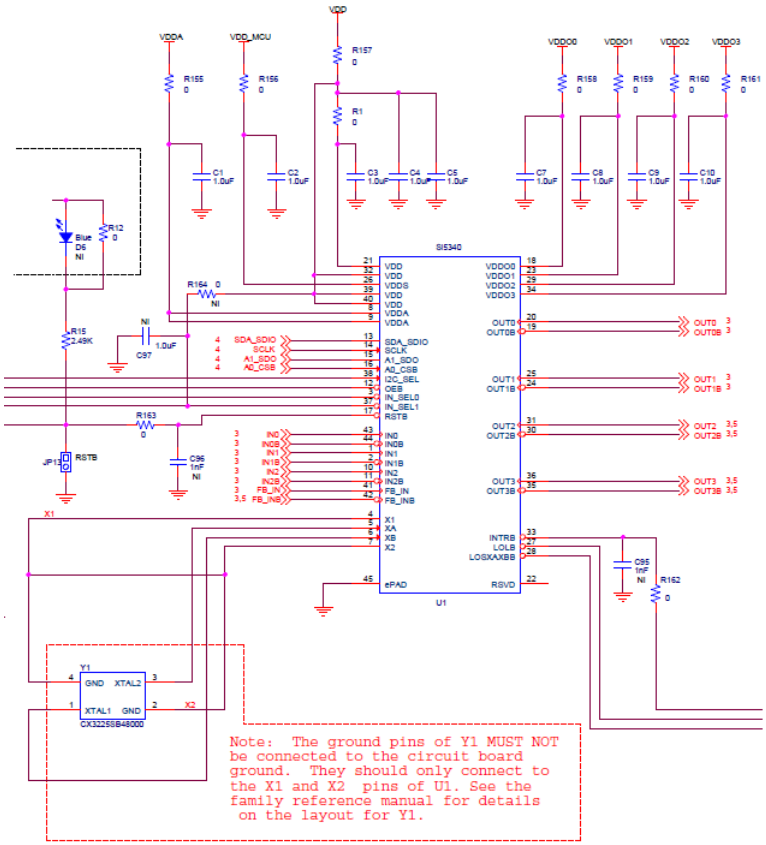
AN1051: Si534x/8x Schematic Review Checklist Application Note

This application note contains a schematic review checklist, which can be used as an initial step in evaluating an Si534x/8x schematic design. Considering the items listed in this document before committing to layout will contribute to a successful design.

Ilustrated below is an excerpt from the Si5340-D-EB evaluation board schematic.



KEY POINTS

- This schematic review checklist application note applies to Silicon Labs Si534x/8x clock generators and jitter attenuators.
- This document addresses these topics:
  - Crystal/External Reference
  - Input Clocks
  - Output Clocks
  - Power Supply Distribution Network
  - Serial Communication
  - Digital I/O

1. Introduction

This schematic review checklist application note applies to Silicon Labs Si534x/8x devices. As of this writing, these include the following products:

- Si5340
- Si5341
- Si5342
- Si5342H
- Si5344
- Si5344H
- Si5345
- Si5346
- Si5347
- Si5348
- Si5380

Please review this checklist and consider each of the listed topics in your board's schematic design.

It is a good idea when getting started to make sure you have the latest documentation, especially the data sheet and reference manuals. These documents are all available from http://www.silabs.com. Evaluation board documentation such as for the Si5345-D-EVB are available at http://www.silabs.com/products/clocksoscillators/pages/developmenttools.aspx.

Please note that there are 2 reference documents that apply to every Si534x/8x device. The first is a Reference Manual (RM) or Family Reference Manual (FRM) that contains technical application details such as register programming and layout considerations for each device or device family. Examples are the *Si5380 Reference Manual* and the *Any-Frequency, Any-Output Jitter-Attenuators/Clock Multipliers Si5345, Si5344, Si5342 Family Reference Manual.* Unless otherwise noted, the terms RM or Reference Manual will refer to the device-specific reference document.

The second is a stand-alone crystal reference document that applies to *all* Si534x/8x devices. This is the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO, and OCXOs Reference Manual. It is essentially a list of approved crystals and crystal oscillators.

2. Checklist

2.1 Crystal/External Reference

A crystal or external reference clock is required to be connected at the XA/XB pins for all the jitter attenuators and independent (i.e., no output clock) clock generators. The crystal or external reference determines the close-in phase noise of the output clocks. The items listed here are intended to insure that the crystal operates properly and that external noise is minimized.

2.1.1 Crystal

1. Crystal selected as specified in the data sheet? For a list of suitable crystals, see the *Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual.*
2. Crystal connected directly to DUT XA and XB? Please see the applicable device reference manual for layout details.
3. Make sure that the crystal pins designated X1 and X2 are **not** connected to PCB GND. The guard ring around the crystal connects to DUT pins X1 and X2 only.
4. Make sure there are no crystal external load capacitors.

2.1.2 External Reference

In this context, external reference means an XO, TCXO, or OCXO connected to the device's XA or XA and XB pins in lieu of a crystal.

1. Selection appropriate? Any oscillator applied to the crystal input pins should have the correct frequency and low enough phase noise and jitter to achieve output clock jitter requirements. See application note *AN905: Si534x External References: Optimizing Performance* for guidance at http://www.silabs.com/support%20documents/technicaldocs/an905.pdf. For a list of suitable oscillators, please see the *Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual.*
2. AC-coupling caps per RM recommendations?
3. Terminations correct per RM recommendations?
4. Split termination for differential clock signals at XA and XB? (Please see explanation of this approach under Input Clocks.)
5. Leave pins X1 and X2 unconnected in this case unlike the crystal case.
6. Single-ended reference oscillators should be connected to XA and not XB in order to obtain LOSXAXB support.

2.2 Input Clocks

The primary considerations here are signal integrity and optimizing input clock placement.

1. AC-coupling caps per RM recommendations?
2. Terminations correct per RM recommendations?
3. Input clock connections correct for CMOS? Make sure the Project File selects the Standard input buffer. The Pulsed LVCMOS buffer is only used by exception for low frequency (≤ 1 MHz) low duty cycle single-ended DC-coupled LVCMOS.
4. Please consider the use of a "split termination" for input differential clock signals if the board may be noisy and there is room to do so. A split termination for input clocks is a conservative approach to common-mode (CM) noise suppression. It is a modification of the standard textbook terminations described in the Reference Manual and is discussed in the Knowledge Base article, "Terminating Differential Transmission Lines to Minimize CM Noise." Below is an illustration modified after the diagram cited in that article.

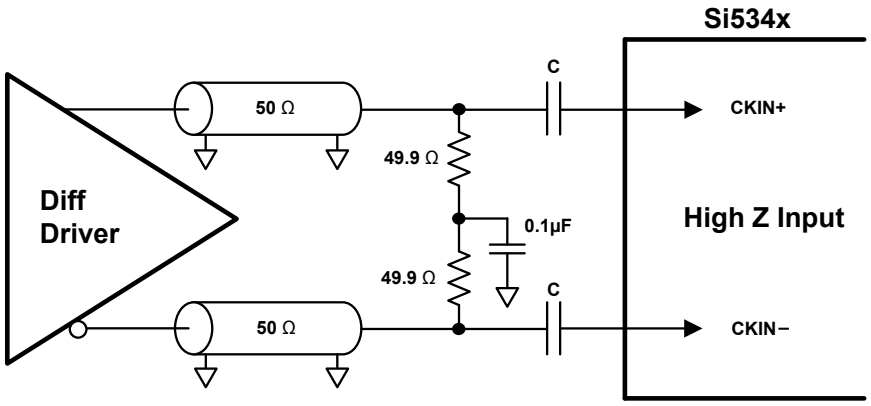
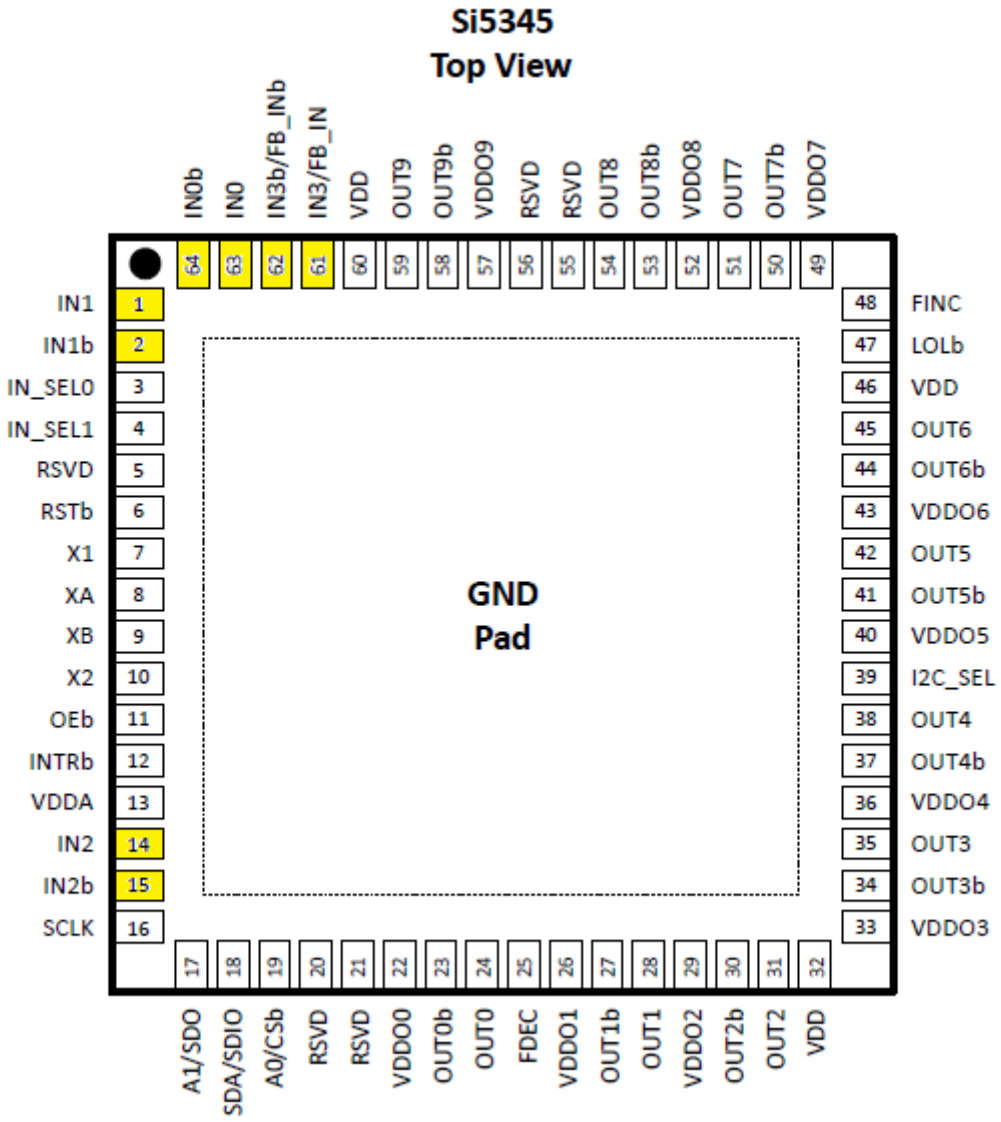


Figure 2.1. Example Split Termination

5. Connection to the single-pin CMOS clock inputs on Si5348 IN3/IN4 correct per RM?
6. In general, input clock selections are preferred based on maximum distance from XA/XB pins. This reduces the possibility of XA/XB crosstalk to input clock traces in the PCB. For example, see the following figure taken from the Si5345 data sheet.



In this specific example, proximity and orthogonality to the XA and XB pins suggest the preferred input clocks in order would be IN3, IN0, IN1, IN2.

2.3 Output Clocks

The primary considerations here are signal integrity, supporting ZDB (Zero Delay Buffer) mode if necessary, and optimizing output clock placement.

1. AC-coupling caps per RM recommendations?
2. No DC-connected shunt resistors on device pins? This is common for LVPECL but these devices do not support that configuration.
3. Series or NE termination components required for CMOS or HCSL per RM recommendations?
4. Are pin assignments optimized to reduce crosstalk? Use CBPro Clock Placement Wizard to optimize output clock locations.
5. Select differential output clocks over single-ended CMOS output clocks. See application note *AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems*.
6. ZDB mode application?
   a. Does the device support ZDB mode?
   b. If so, route the nearest shortest route output clock fed back to IN3/FB_IN. Input and output pin polarities are such that no vias are needed to make this connection. The application must get polarity correct.

2.4 Power Supply Distribution Network

1. 1.8 V to VDD?
2. 3.3 V to VDDA?
3. 1.8, 2.5, or 3.3 V to VDDOn?

   Note: VDDOn here refers to the VDDO for each output clock buffer. For example, the Si5345 has VDDO0, VDDO1, ... VDDO9.

4. Bypass Capacitors are, generally, not critical. Here are some guidelines:
   a. VDD: 1 µF per pin, as close as possible. (The customer EVB uses 1 µf//0.1 µF//series to an inductor and shunt 0.1 µF.)
   b. VDDA: 1 µF per pin, as close as possible.
   c. VDDOn: 1 µF per pin, as close as possible.
5. Ferrite Bead or Inductor
   a. Probably not needed on any supply. Can replace 0 Ω initially.
   b. If you have a series ferrite bead or inductor, you may want to consider adding additional bulk capacitance.
   c. The CEVB 30 Ω inductor on VDD is not neeed.

2.5 Serial Communication

1. Are the connections correct for I^2C, 3-wire, or 4-wire SPI?
2. If I^2C is used, are the bus pull-up resistors present? Only 1 set of resistors should be used (no duplicates with same bus on different schematic pages.)
3. Verify A0/A1 connections are unique for each Silicon Labs device on an I^2C bus.
4. Consider including provisions for a male 10-pin header to support the Field Programmer. (Optional but not recommended for Field Programmer support.)

2.6 Digital I/O

1. External pullups and pulldowns:
   a. Any digital inputs that must be pulled or tied externally? Si5347 :: FDEC. OE1b
   b. Any that may be added to be conservative? (Our PUs/PDs are relatively weak.)
   c. Any unnecessary and just waste power?
2. Recommend that even unused digital I/O be connected to at least a test pad, pin, or via just in case.

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