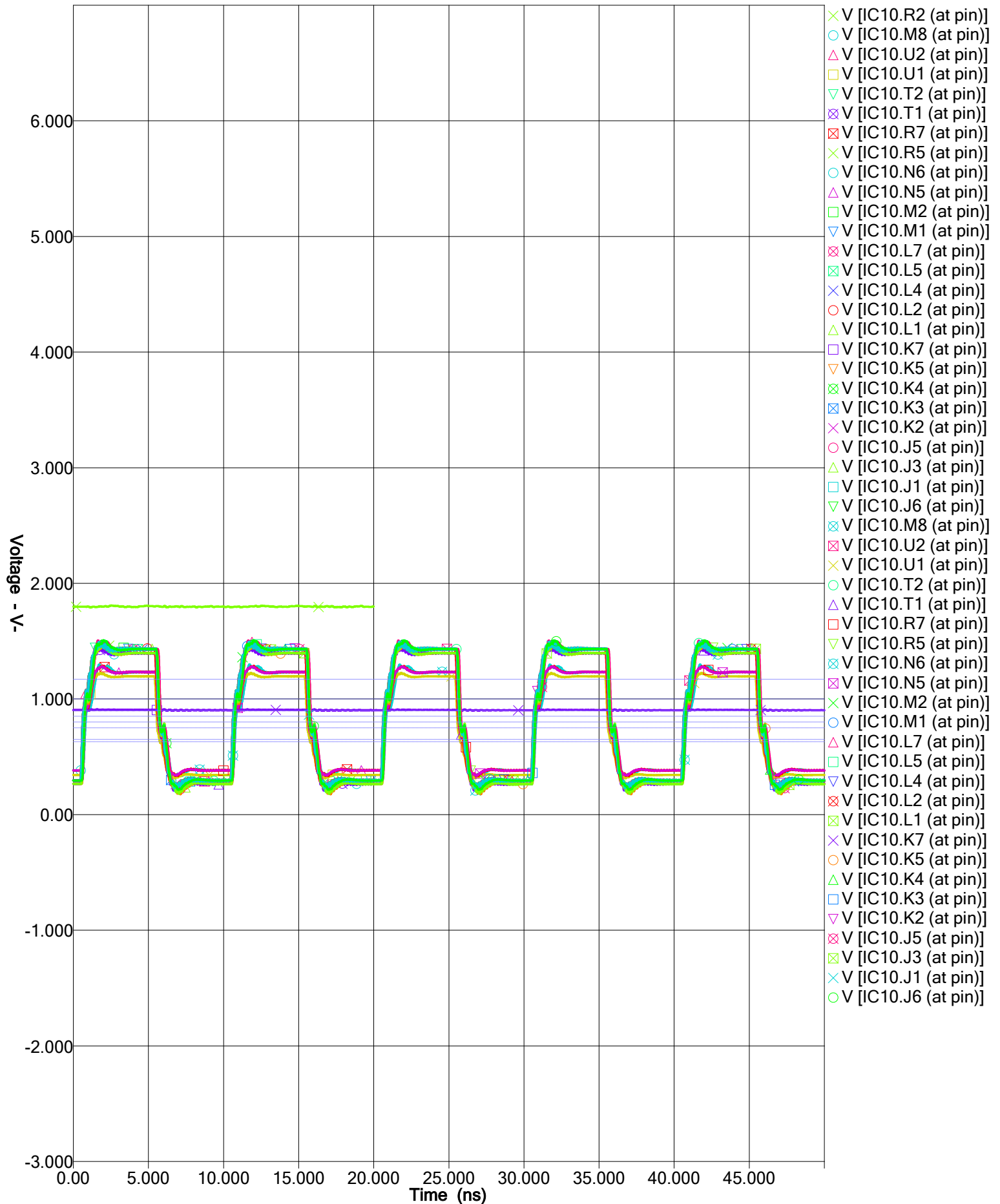


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Design file: SPEKTROP2_PROCESSOR_BOARD_V1_39.HYP

Designer: Piotr Zdunek

HyperLynx v9.4.2



Date: Sunday Jan. 21, 2018 Time: 1:19:42

Net name: FPGA_BANK34_HSTL_IN_IO5

Show Latest Waveform = YES, Show Previous Waveform = YES