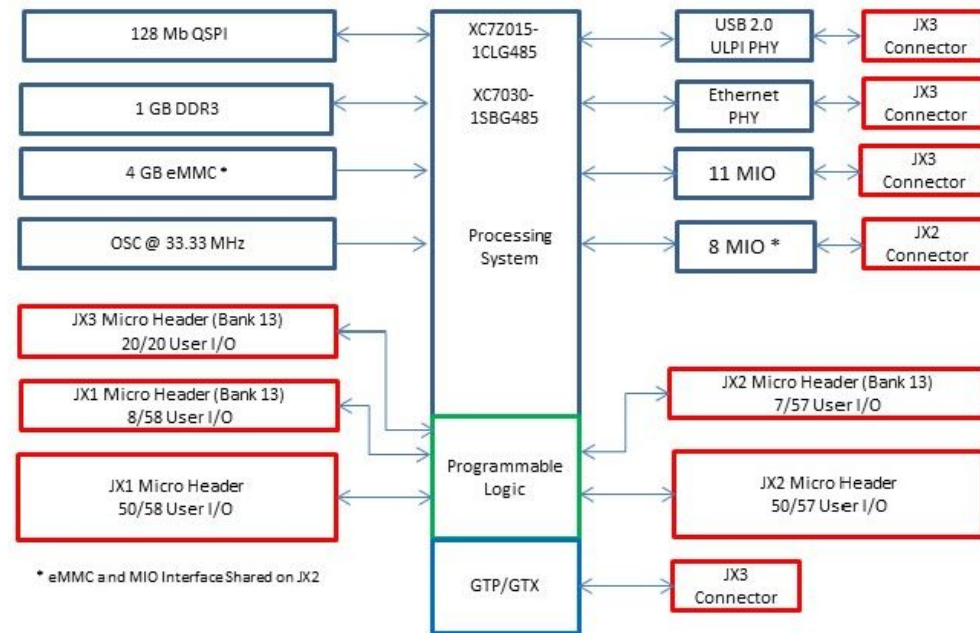
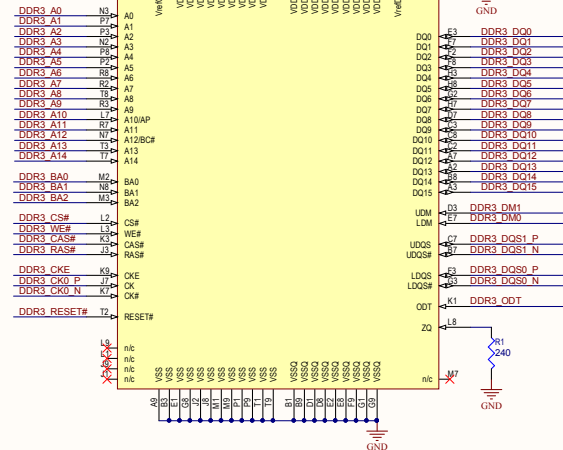


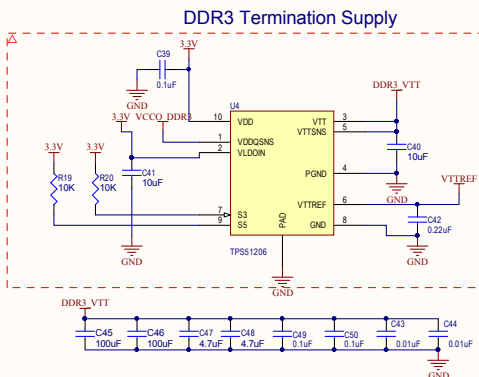
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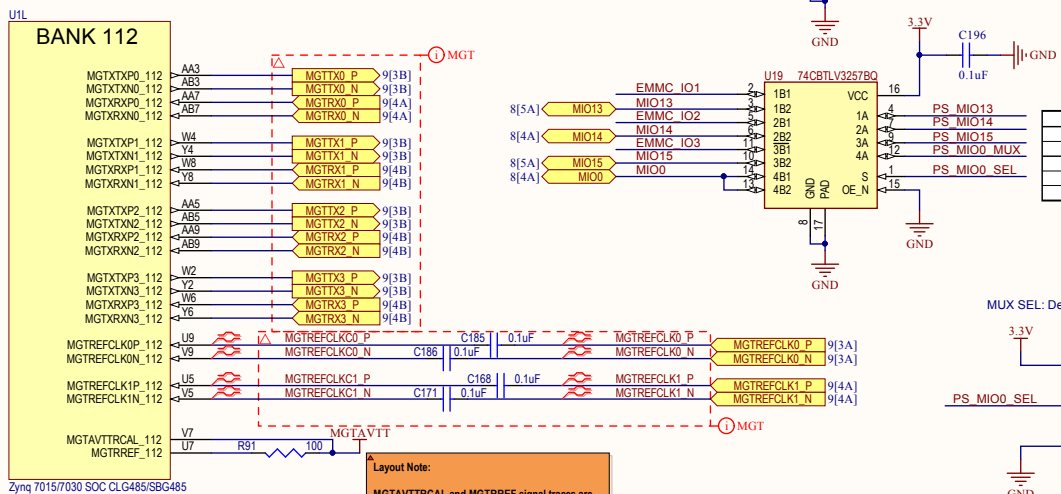
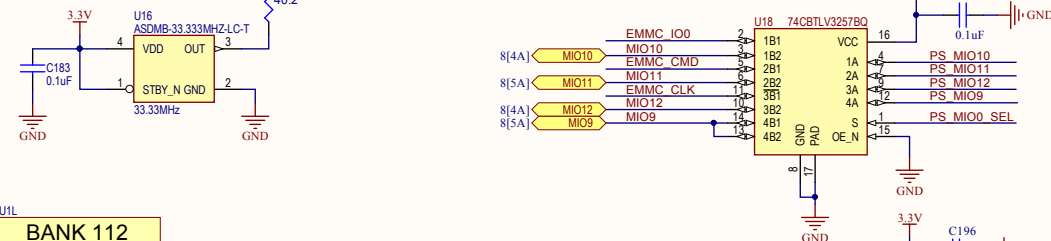
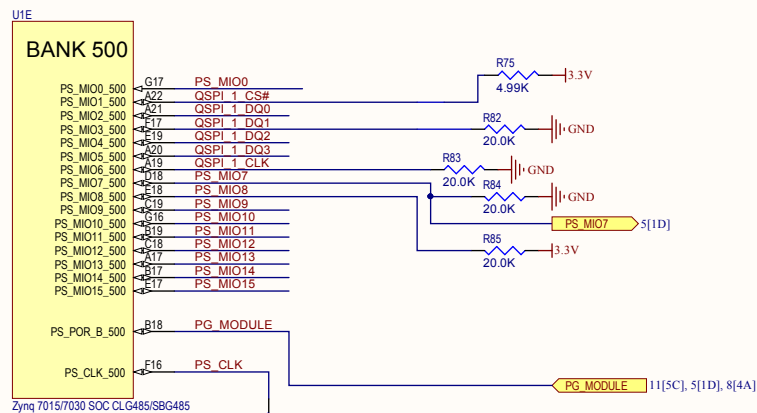
The diagram shows the timing of various signals relative to the clock. The signals are grouped into two main sections: DQ3_VT1 (left) and DQ3_VT2 (right). The signals include data bus lines (DQ3_A14-DQ3_A0, DQ3_BA0-DQ3_BA2, DQ3_CSE, DQ3_WEN, DQ3_RAS#, DQ3_C00T), reset (DQ3_RESET#), and clock signals (DQ3_CK0_P, DQ3_CK0_N, DQ3_CKE). The timing parameters are indicated by numbers in the diagram, such as 40.2, 80.6, and 80.0.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms



NOTE:
RESET# requires 1K resistor
for PD, to maintain logic high
through FPGA
Configuration. See
UG933p62

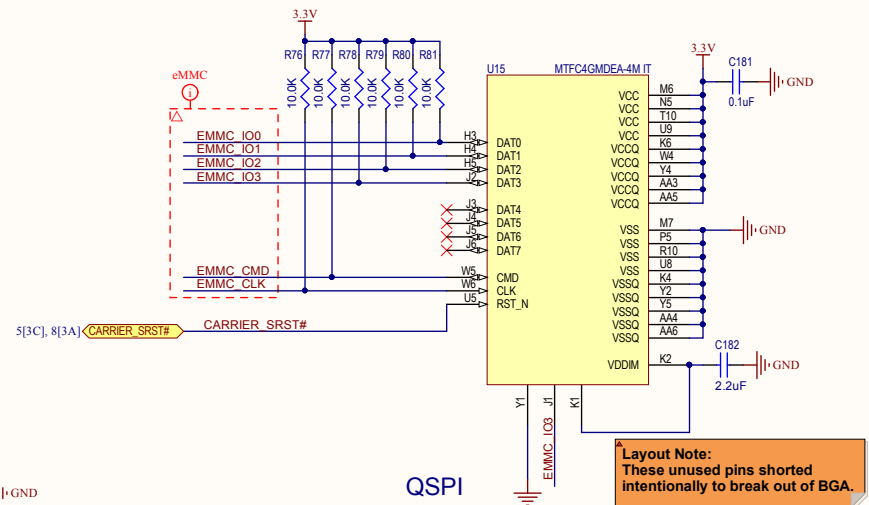
Zynq PS MIO - Bank 500



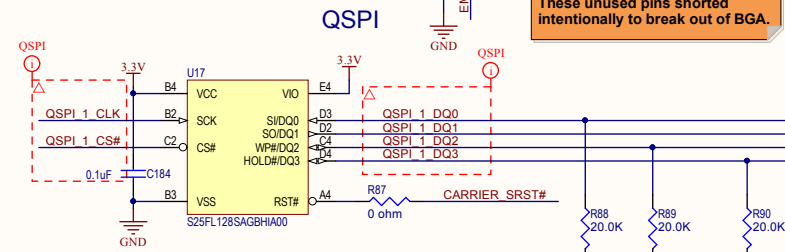
Layout Note:

MGTAVTTRCAL and MGTREF signal traces are to be of equal length.

Embedded eMMC: 2GB, 4GB, 8GB

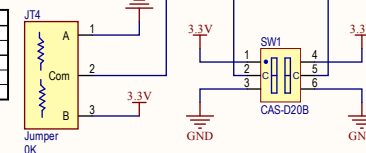


Layout Note:
These unused pins shorted intentionally to break out of BGA.

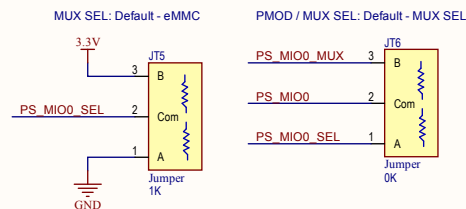



Boot Mode Select

BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD	X	HIGH (1-2)	HIGH (4-5)
JTAG	X	LOW (2-3)	LOW (5-6)
IND JTAG	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG	LOW (1-2)	LOW (2-3)	LOW (5-6)

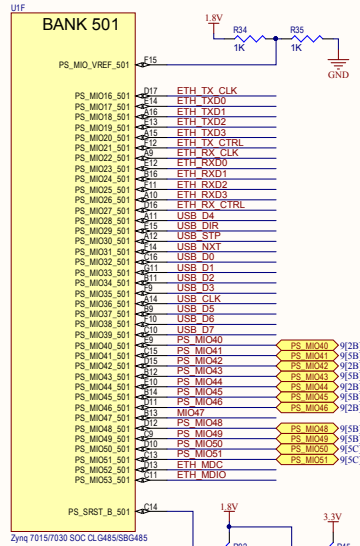


CASCADE JTAG - DEFAULT MODE



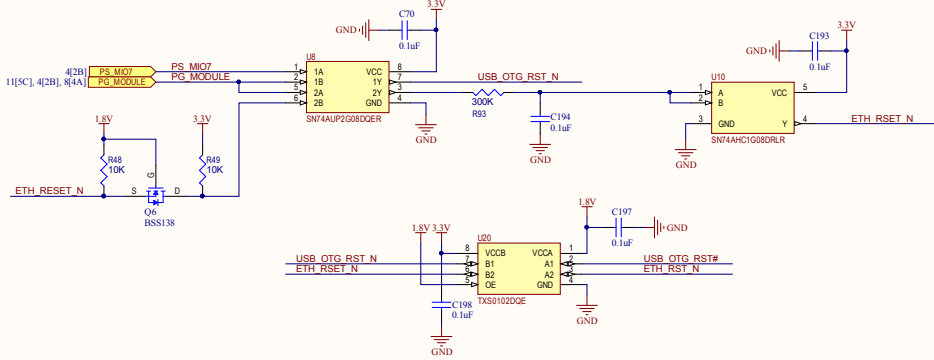
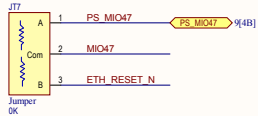
 Avnet Engineering Services			
Title: 04 - GTP, QSPI FLASH, eMMC.SchDoc			
Size: B	Document Number: PicoZed 7015/7030		Rev: C
Date: 3/11/2016		Sheet 4 of 12	

Zynq PS MIO - Bank 501

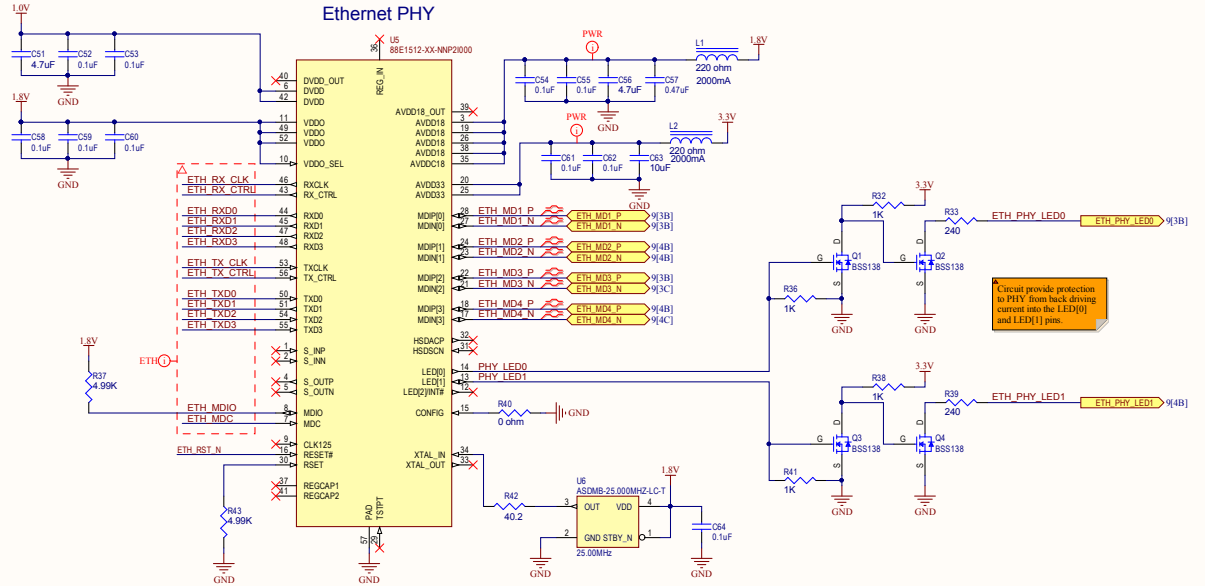


Zynq 7015/7030 SOC CLG485/SBG485

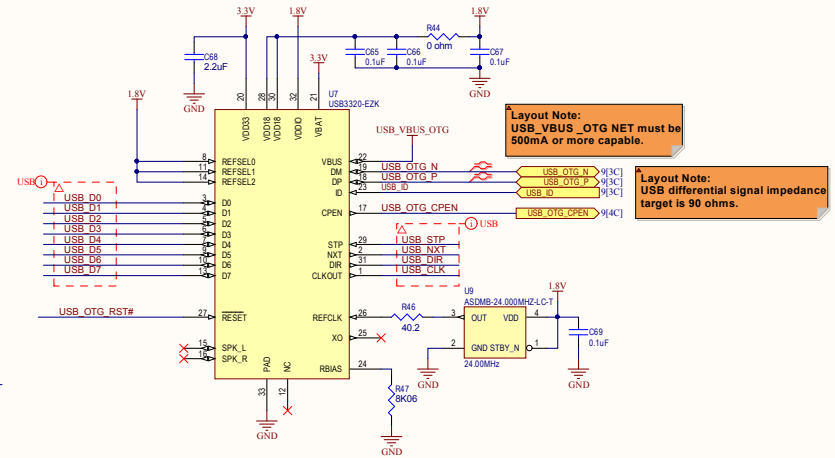
CARRIER_SRST# CARRIER_SRST# 4[4B], 8[3A]



Ethernet PHY

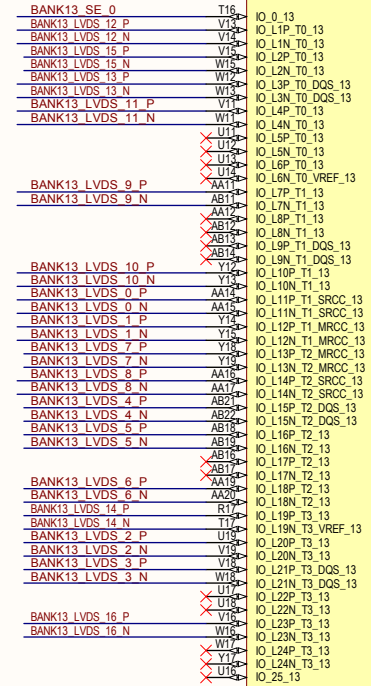
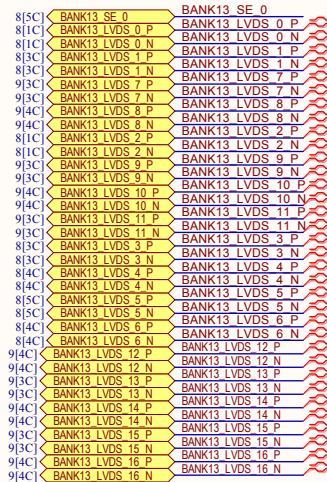
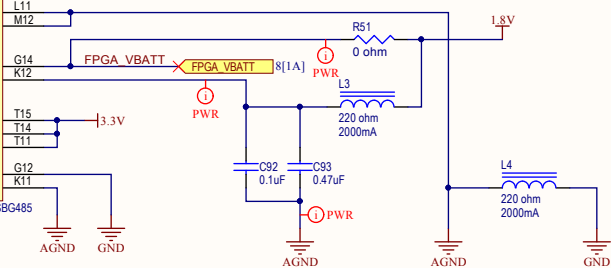
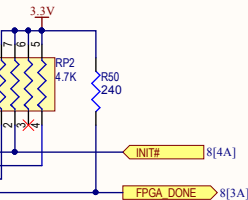
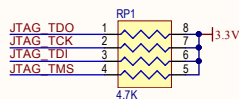
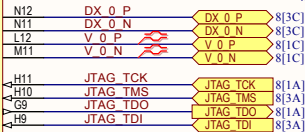
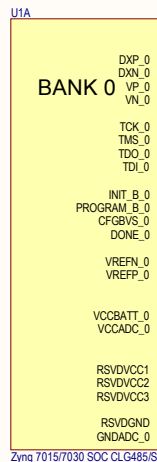


USB 2.0 OTG

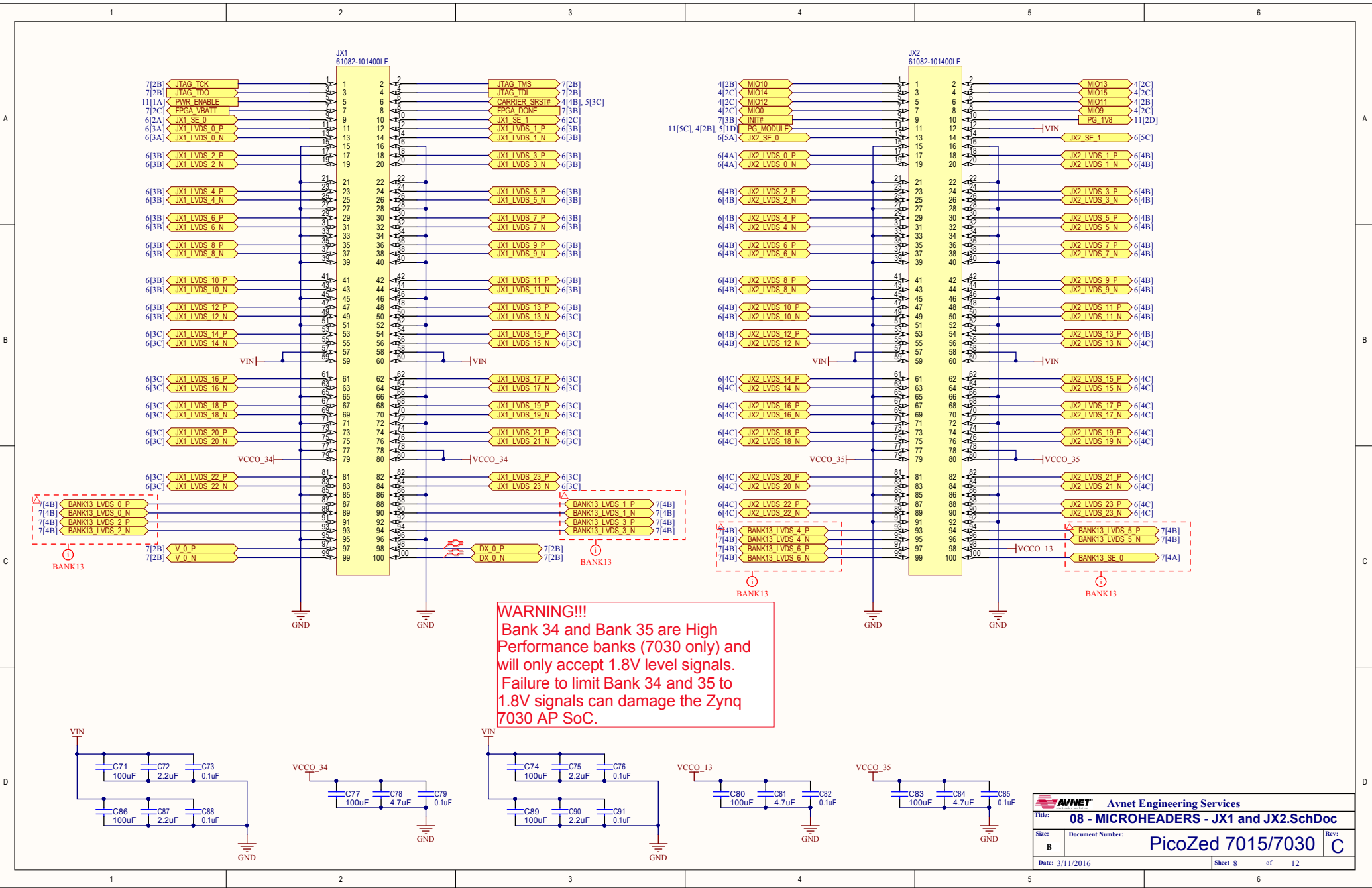


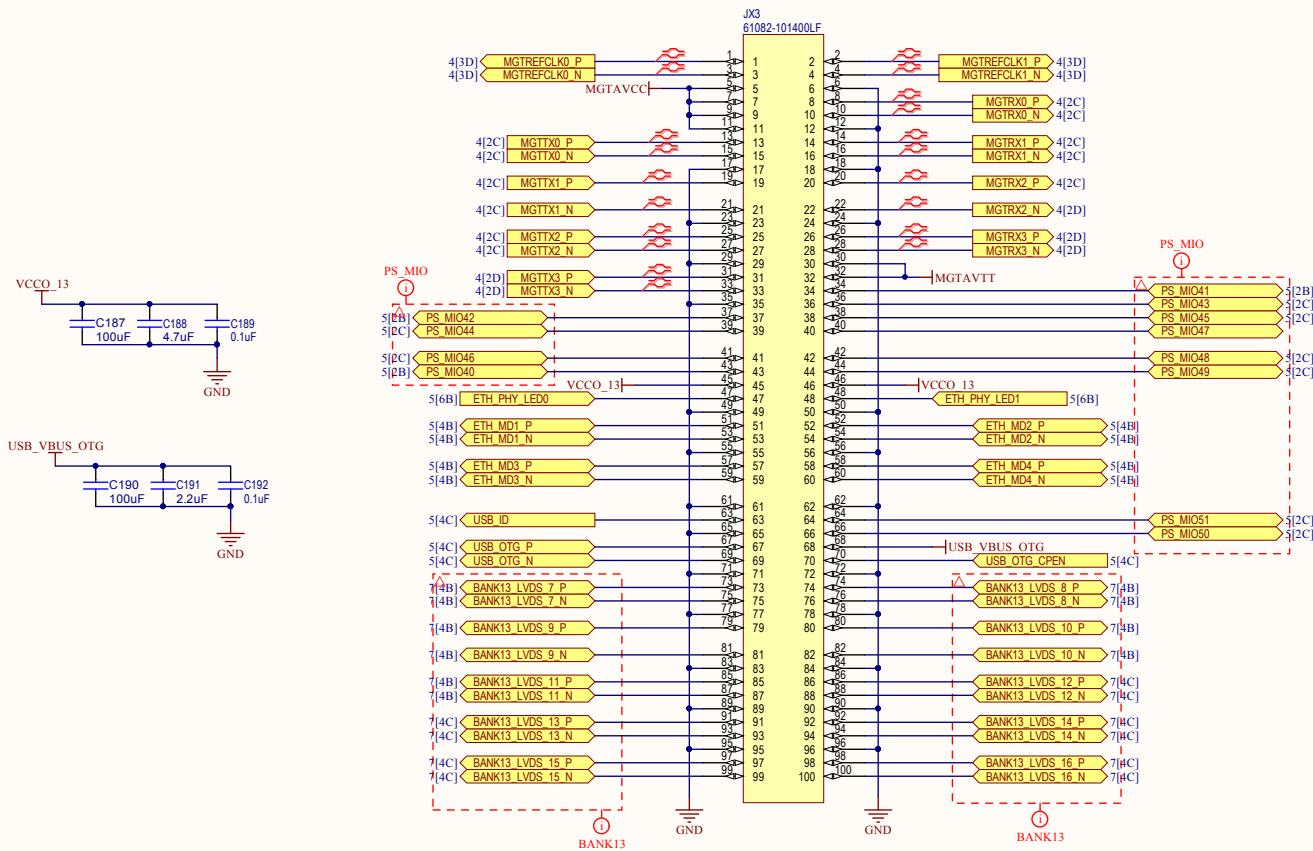
Layout Note: USB_VBUS_OTG NET must be 500mA or more capable.

Layout Note: USB differential signal impedance target is 90 ohms.



Zynq 7015/7030 SOC CLG485/SBG485



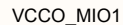
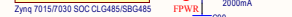


ZYNQ MIO POTENTIAL MAPPING OPTIONS:

SDIO INTERFACE
 PS_MIO40 - SD_CLK through a 40.2-ohm RES
 PS_MIO41 - SD_CMD
 PS_MIO42 - SD_D0
 PS_MIO43 - SD_D1
 PS_MIO44 - SD_D2
 PS_MIO45 - SD_D3
 PS_MIO46 - SD_CD

UART INTERFACE
 PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
 PS_MIO49 - UART_TXD (Tie to the RXD pin of a UART)

USB INTERFACE
 PS_MIO40 - DATA
 PS_MIO41 - DIR
 PS_MIO42 - STP
 PS_MIO43 - NXT
 PS_MIO44 - DATA
 PS_MIO45 - DATA
 PS_MIO46 - DATA
 PS_MIO47 - DATA
 PS_MIO48 - CK
 PS_MIO49 - DATA
 PS_MIO50 - DATA



Revision History

Rev B

Original release

Rev C

- 1) Updated Block Diagram
- 2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
- 3) Added RC time constant to ETHERNET RESET
- 4) DDR3L/DDR3 option note added
- 5) Renamed 1.5V and DDR3_0V75 power nets
- 6) Changed U4.2 connection from 1.8V to 3.3V
- 7) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins

Rev C - Update

- 1) PUDC Default value changed to VCCO
- 2) C194 value changed to fix Ethernet Reset RC time constant
- 3) QSPI_CS resistor value changed to 4.99K

Rev C - Update 3/11/16

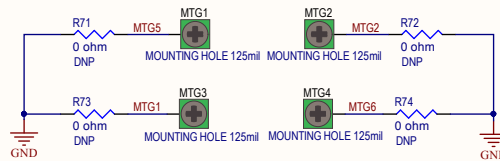
- 1) Updated Block Diagram w/ Both Packages
- 2) Updated Zynq Symbol Naming w/ Both Packages

Mechanicals:

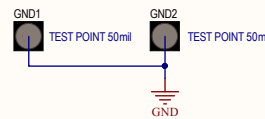


PCB
Z7P2P-Z70xx-PCB-C

PCB Mounting Holes



GND Test Points



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