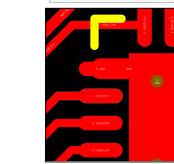


▲ Make sure the pad 6 is connected directly to the EP, without other connections. Through applied polygon cutout



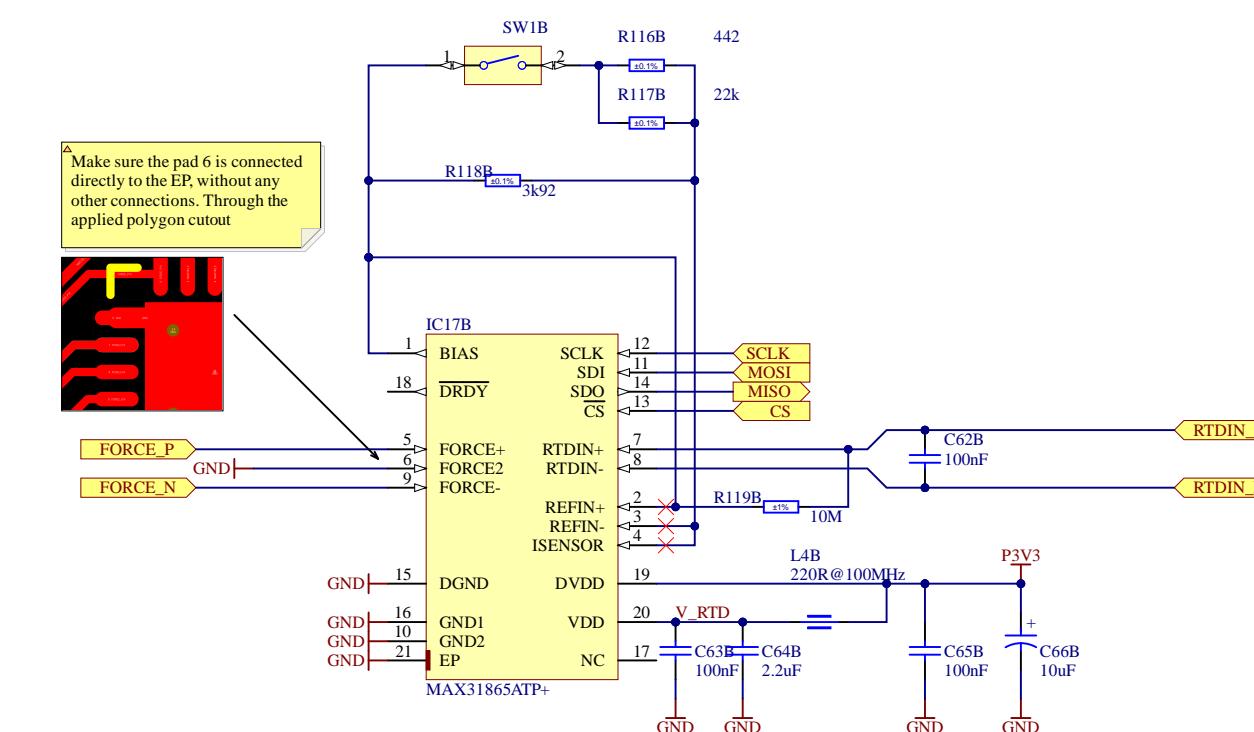
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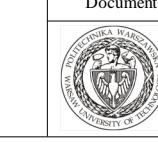


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RTD converter

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Designer	L.Pajak	
Drawn by	L.Pajak	15.07.2024
Check by	G.Kasprowicz	-
Last Mod.	-	24.08.2024
File	RTD.SchDoc	
Print Date	12.09.2024 00:08:38	Sheet 2 of 8
Size	A3	Rev 1.0

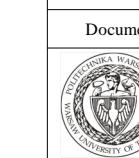
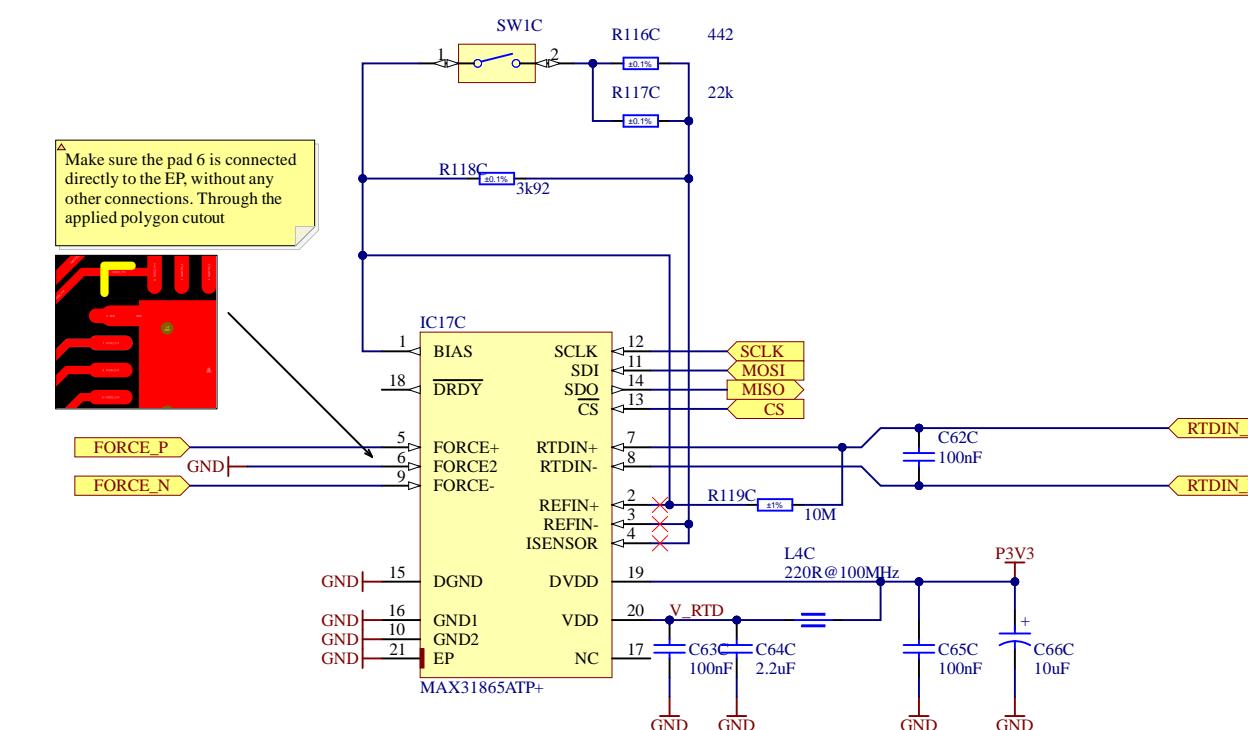
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	Drawn by L.Pajak
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	Sheet 2 of 8
PWIE Nowowiejska 15/19 00-665 Warsaw	Size A3 Rev 1.0
Contact lpajak84@gmail.com	

RTD converter

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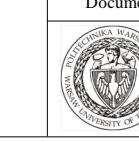
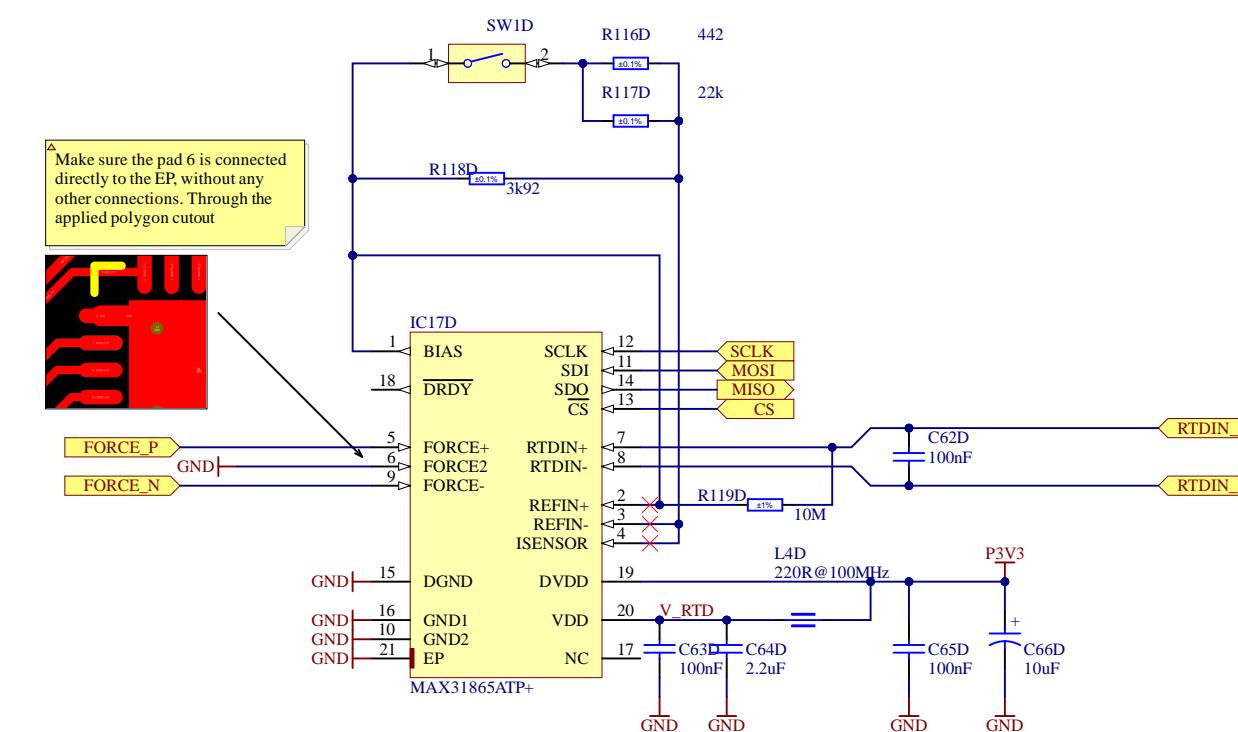
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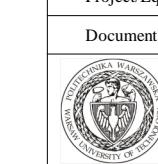
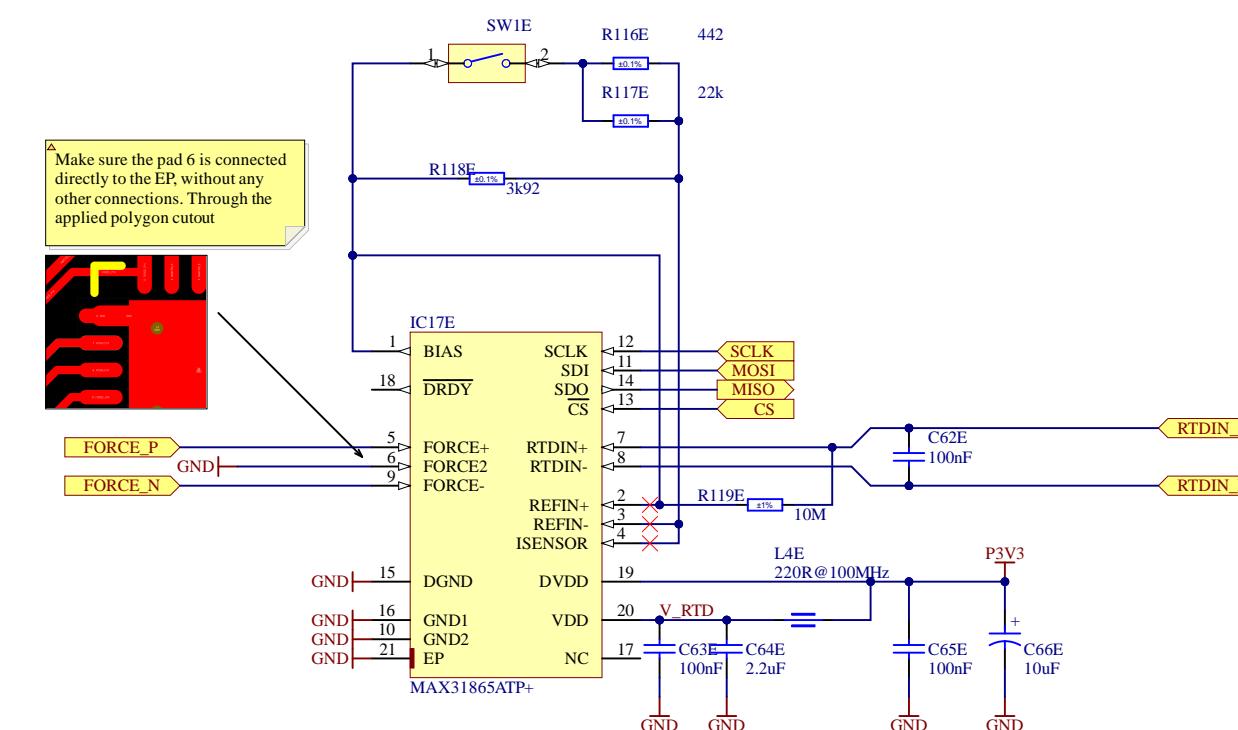
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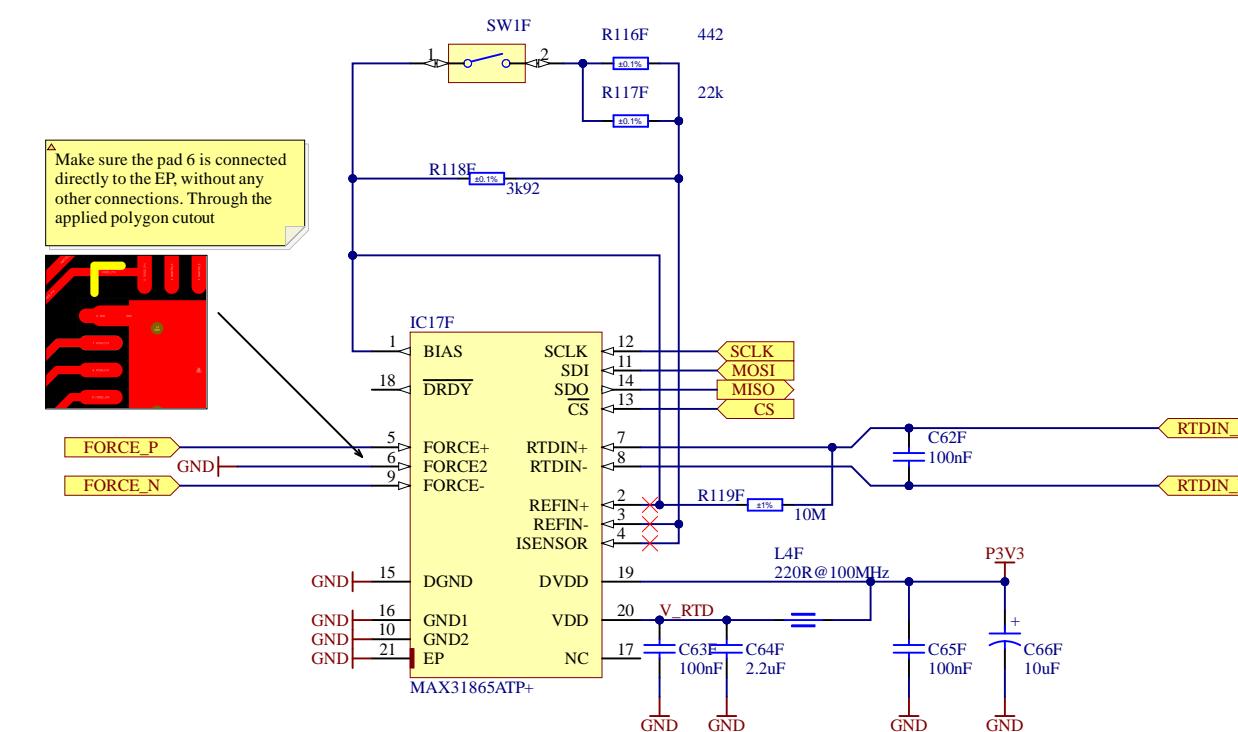
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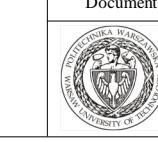
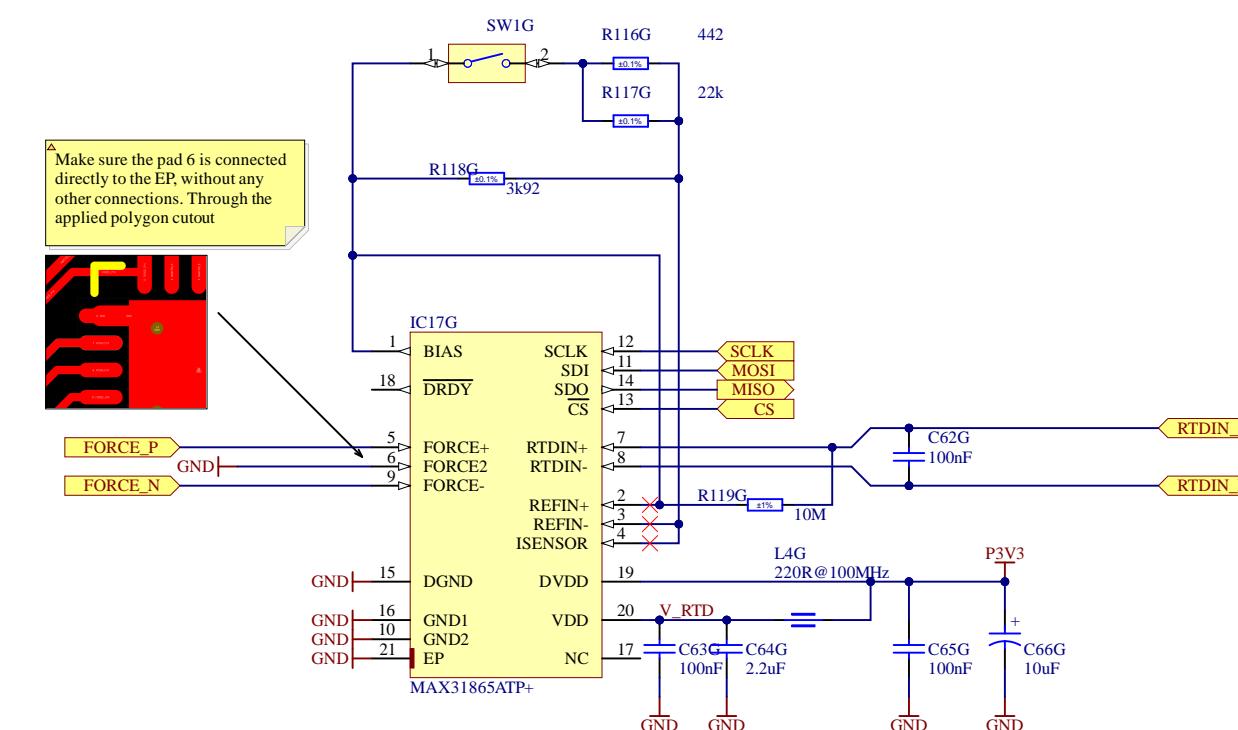
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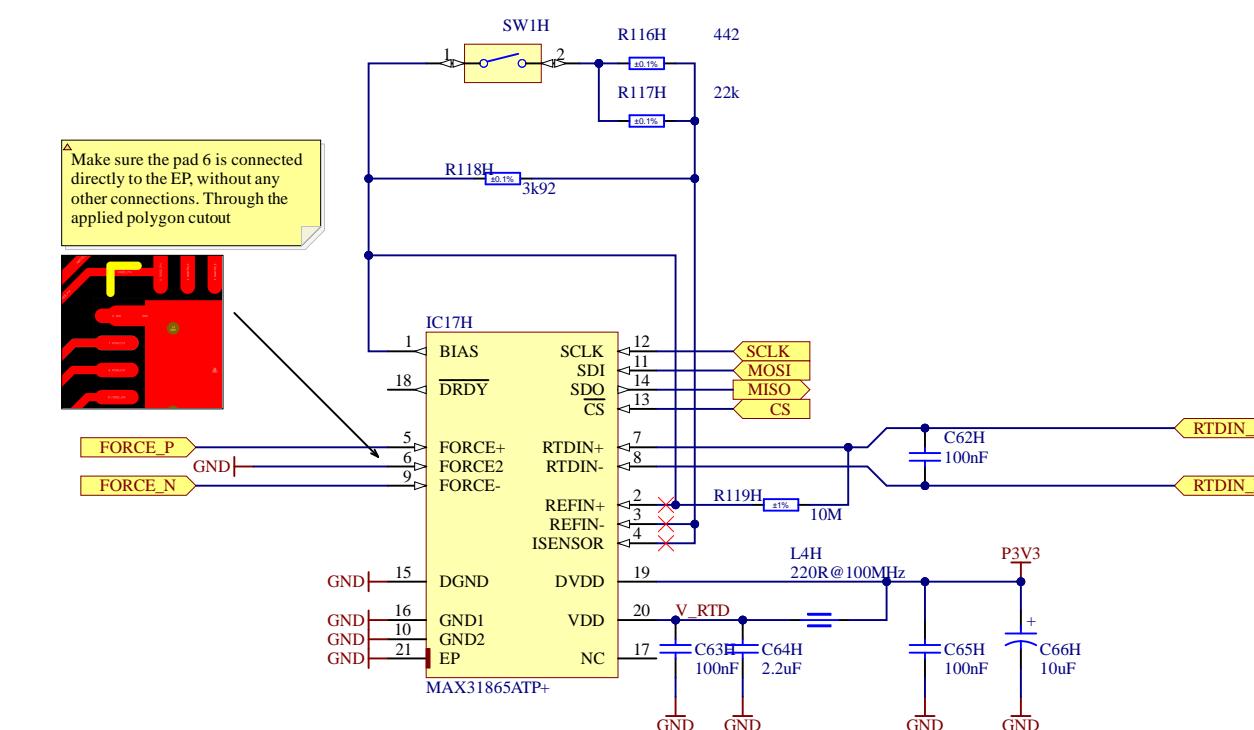
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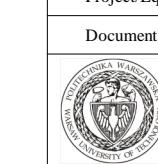
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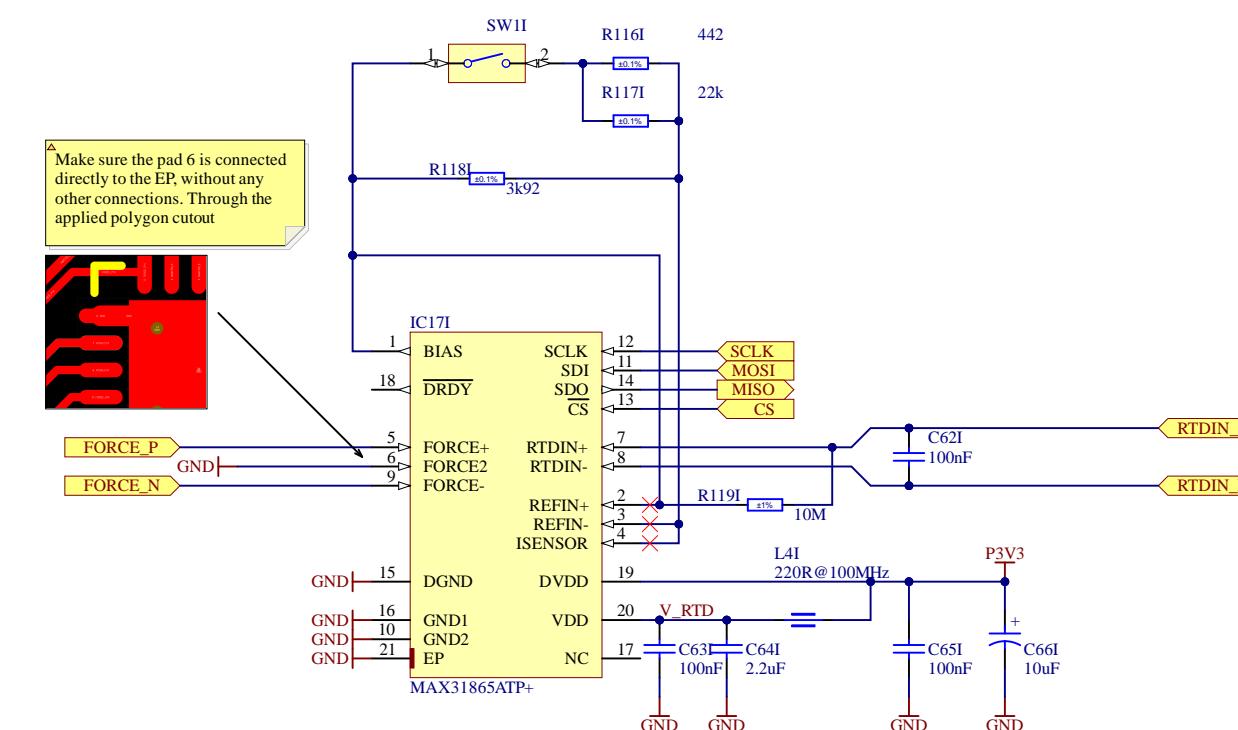
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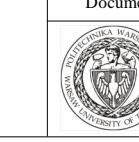


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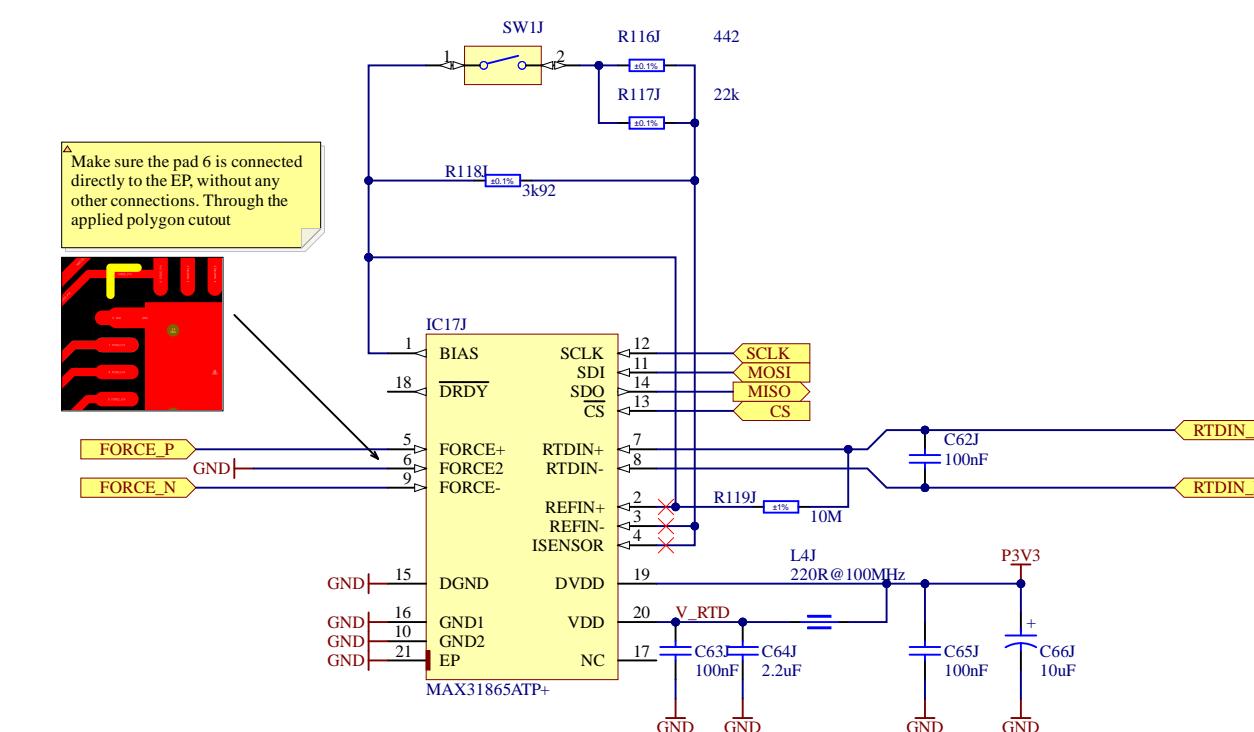
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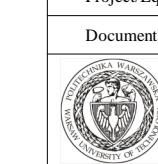
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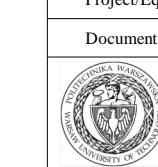
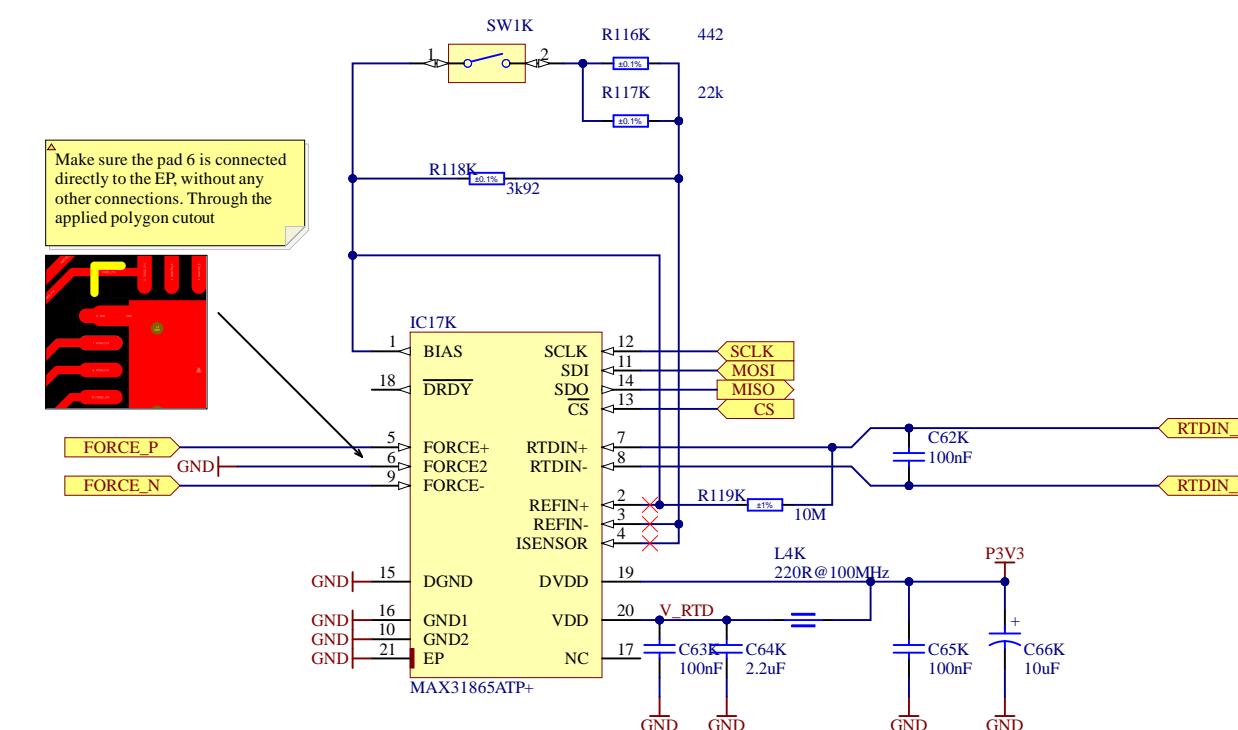
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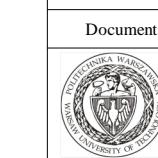
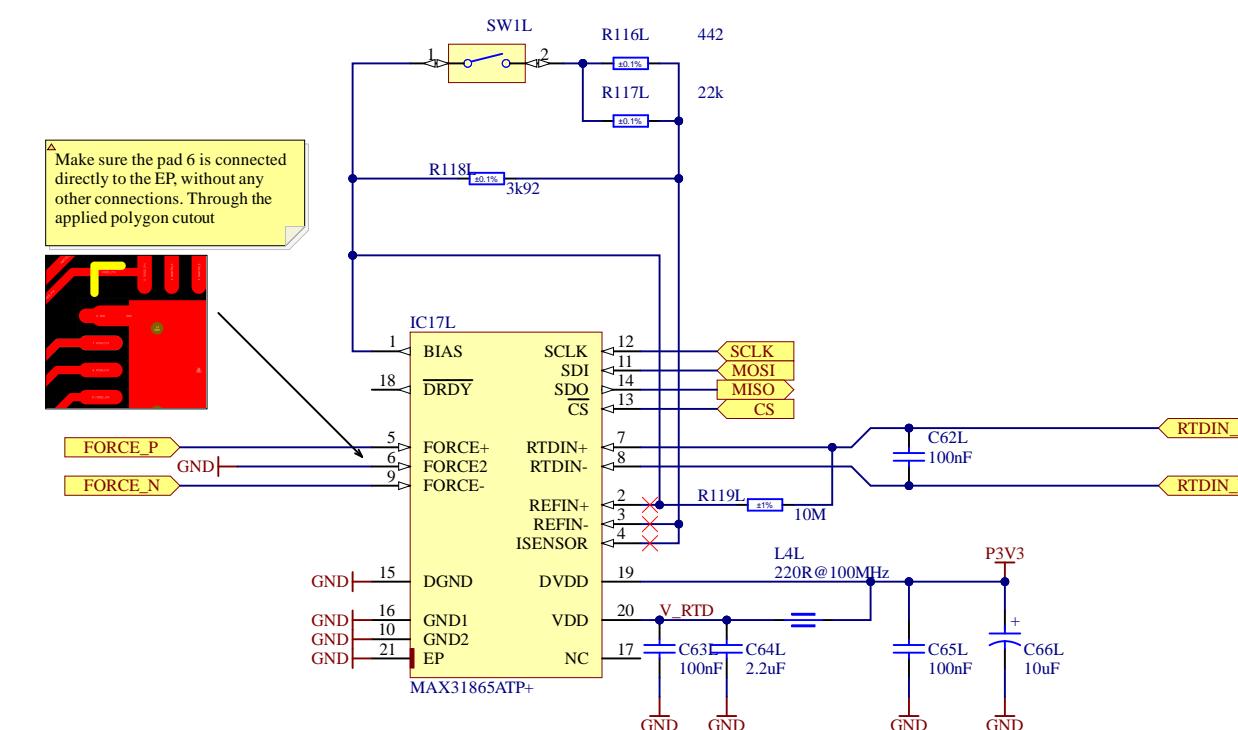
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Drawn by	L.Pajak	15.07.2024
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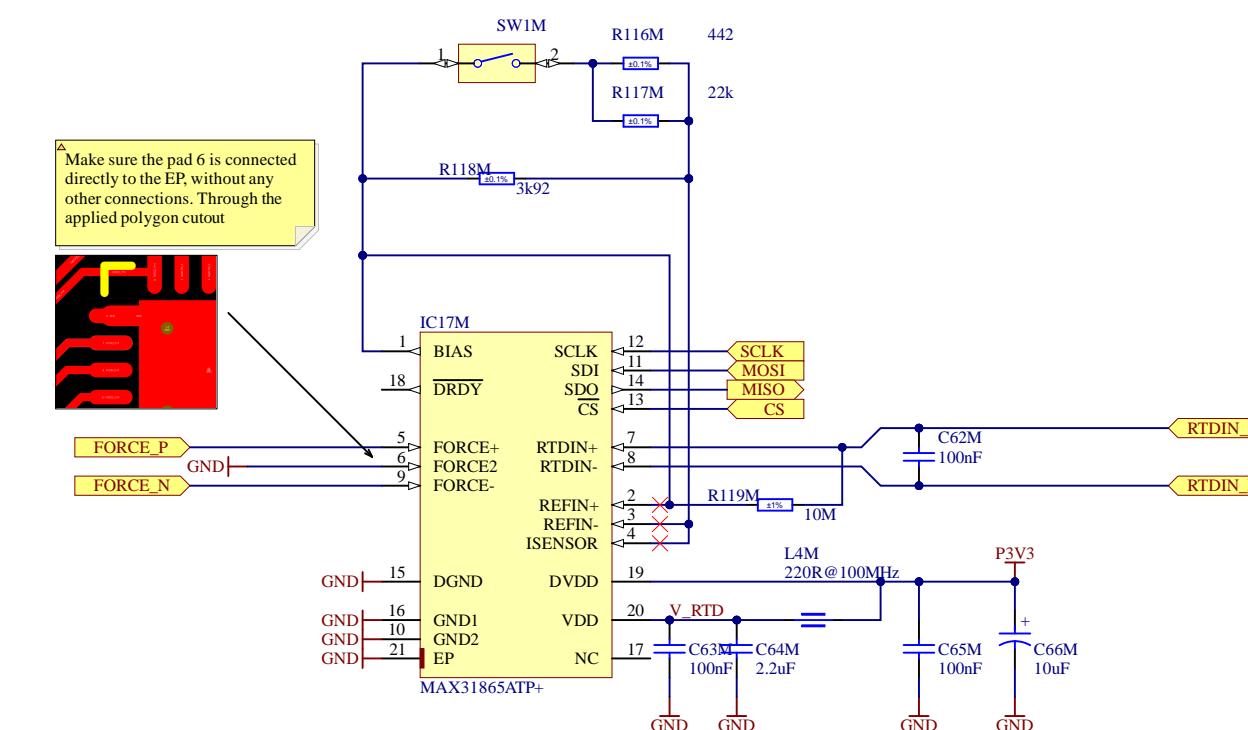
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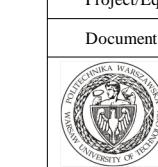
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File	RTD.SchDoc
Print Date	12.09.2024 00:08:40
Sheet	2 of 8
Size	A3
Rev	1.0

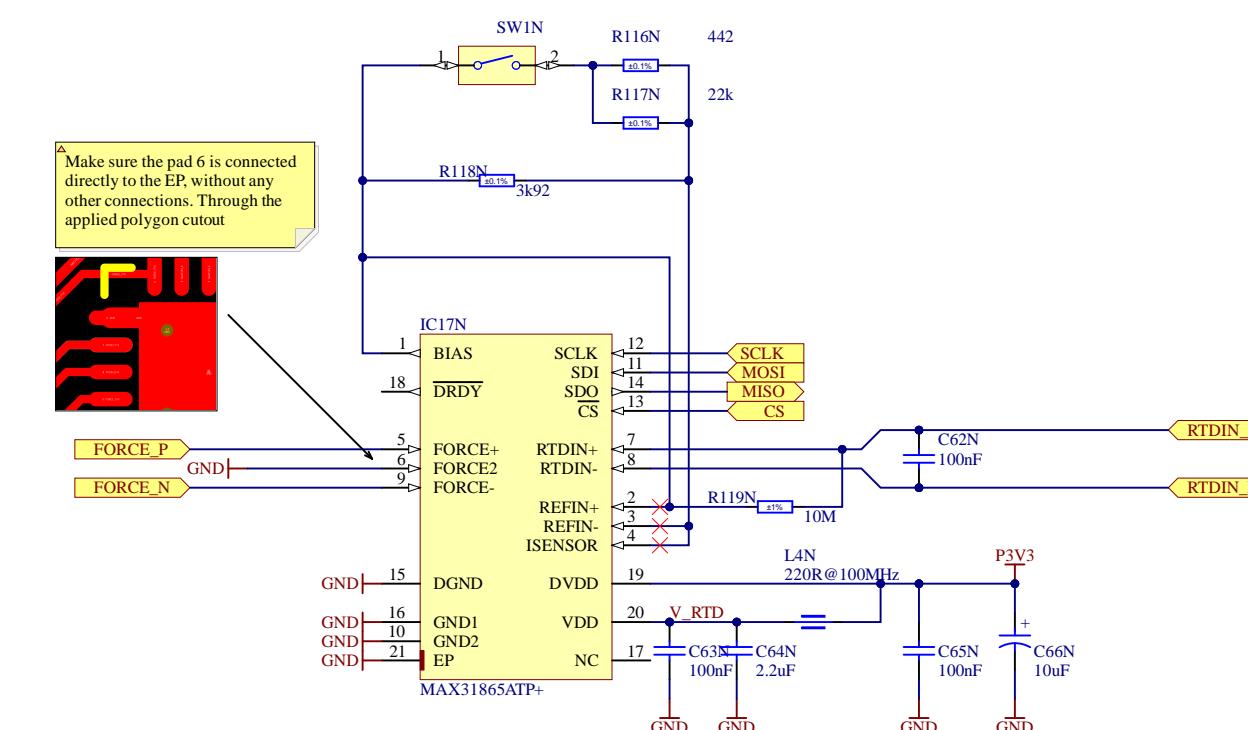
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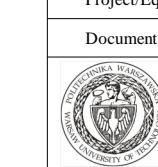
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Rev	1.0

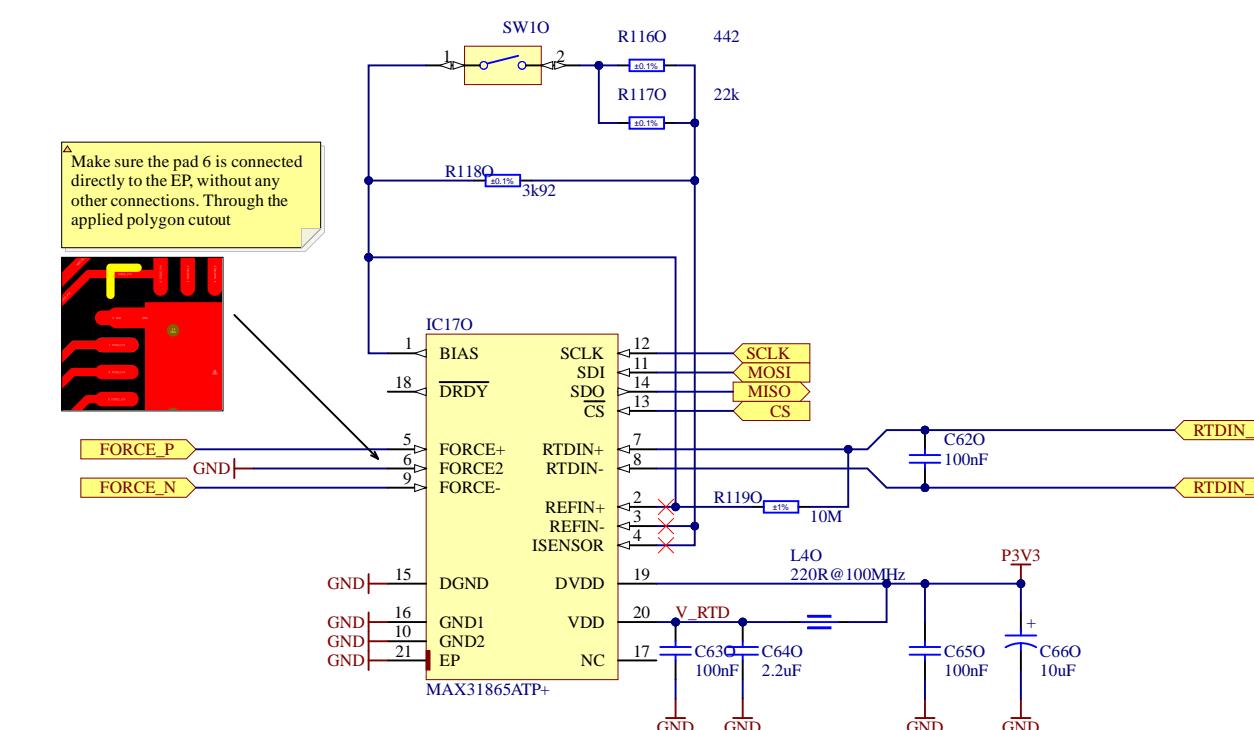
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Last Mod.	-
File	RTD.SchDoc
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Sheet	2 of 8
Size	A3
Rev	1.0

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Contact lpajak84@gmail.com

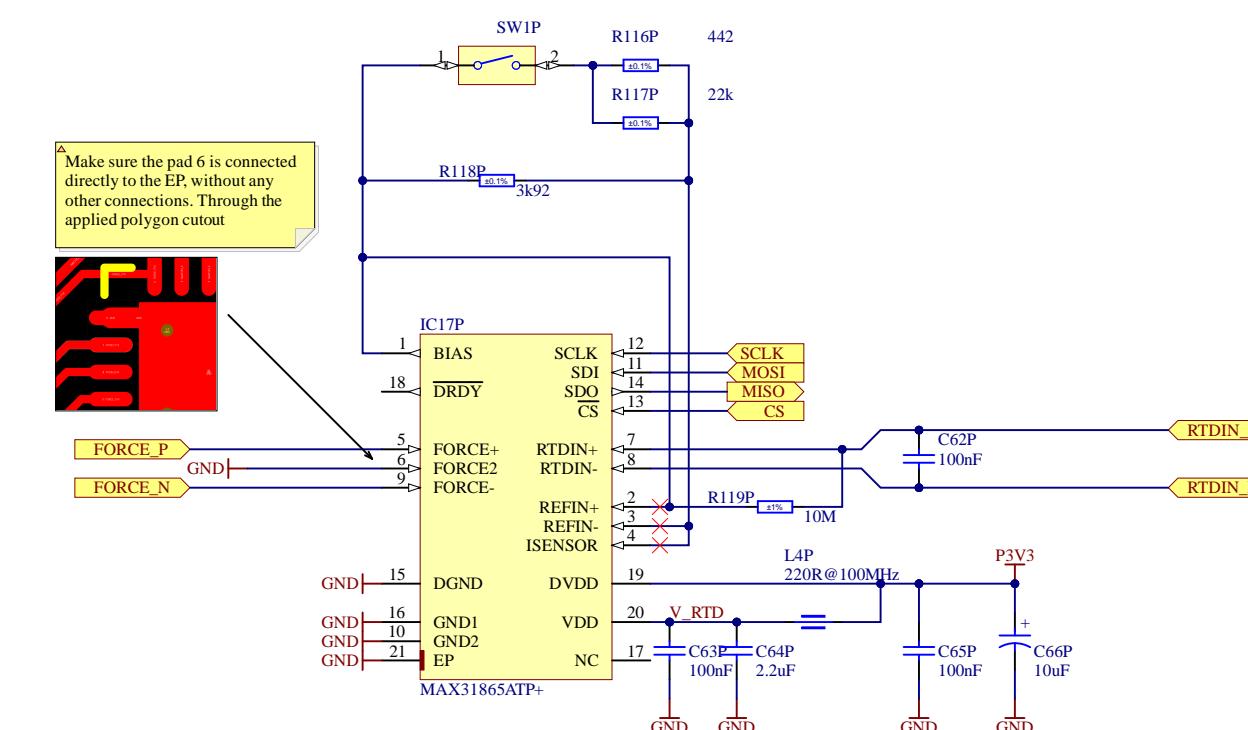
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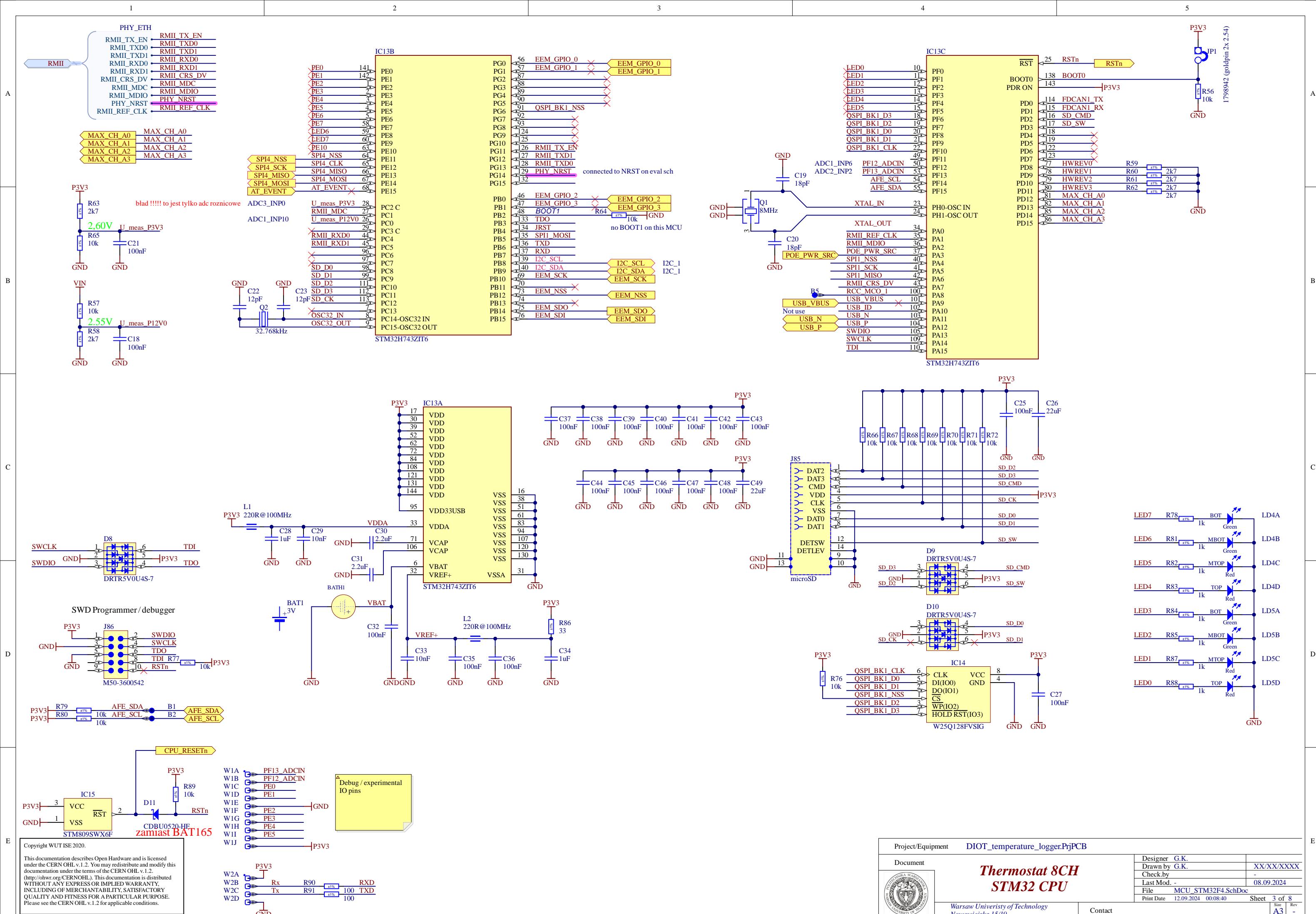


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Check by	G.Kasprowicz
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Sheet	2 of 8
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69138200004
1 TFORCE_P00
2 TRTDIN_P08
3 TRTDIN_N00
4 TFORCE_N08

P2
1 TFORCE_P08
2 TRTDIN_P08
3 TRTDIN_N08
4 TFORCE_N08

P3
1 TFORCE_P01
2 TRTDIN_P01
3 TRTDIN_N01
4 TFORCE_N01

P5
1 TFORCE_P02
2 TRTDIN_P02
3 TRTDIN_N02
4 TFORCE_N02

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P9
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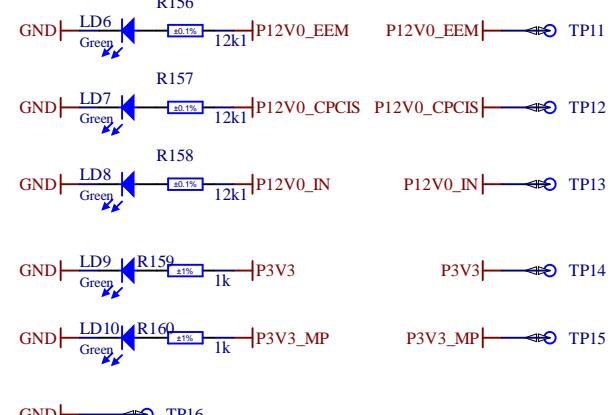
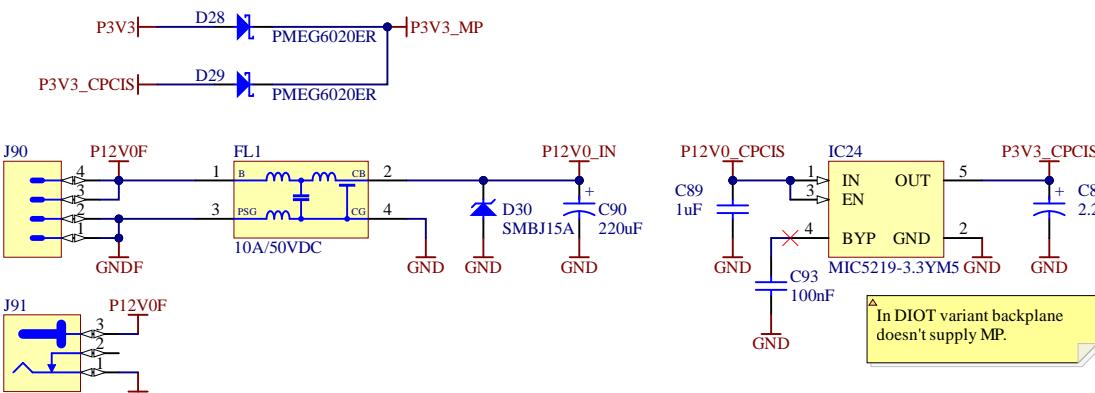
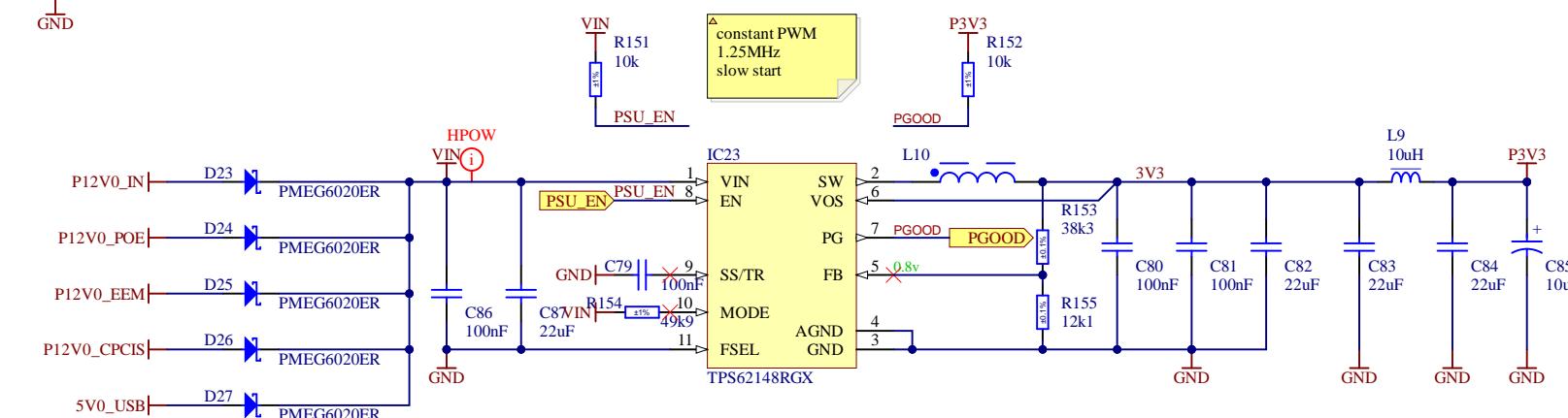
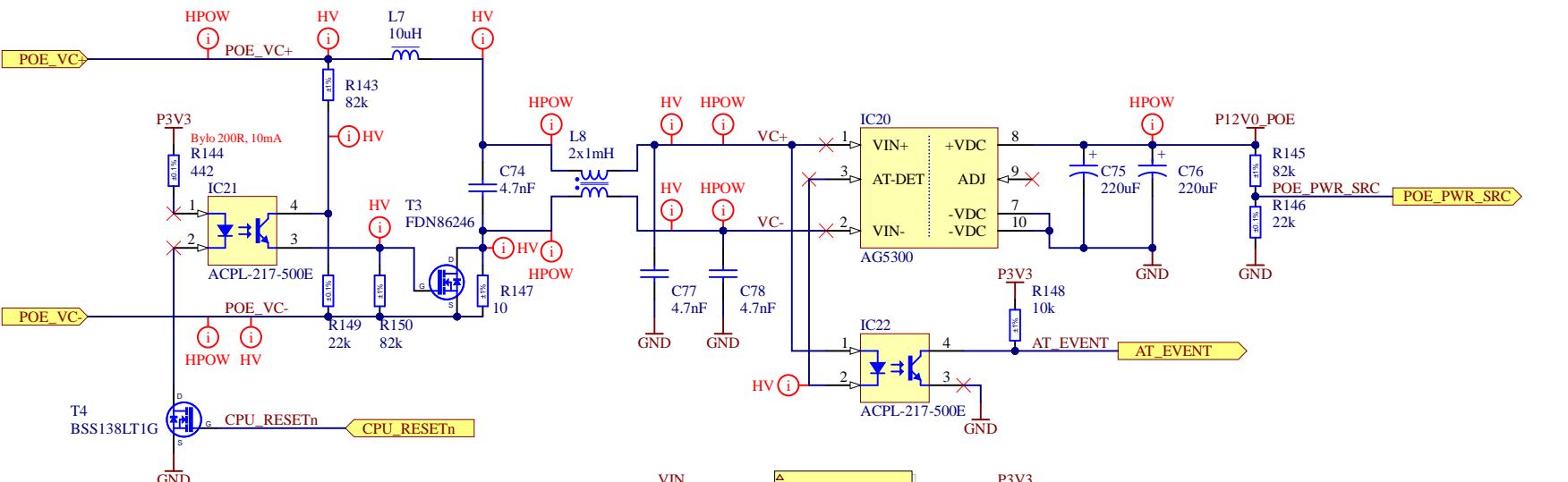
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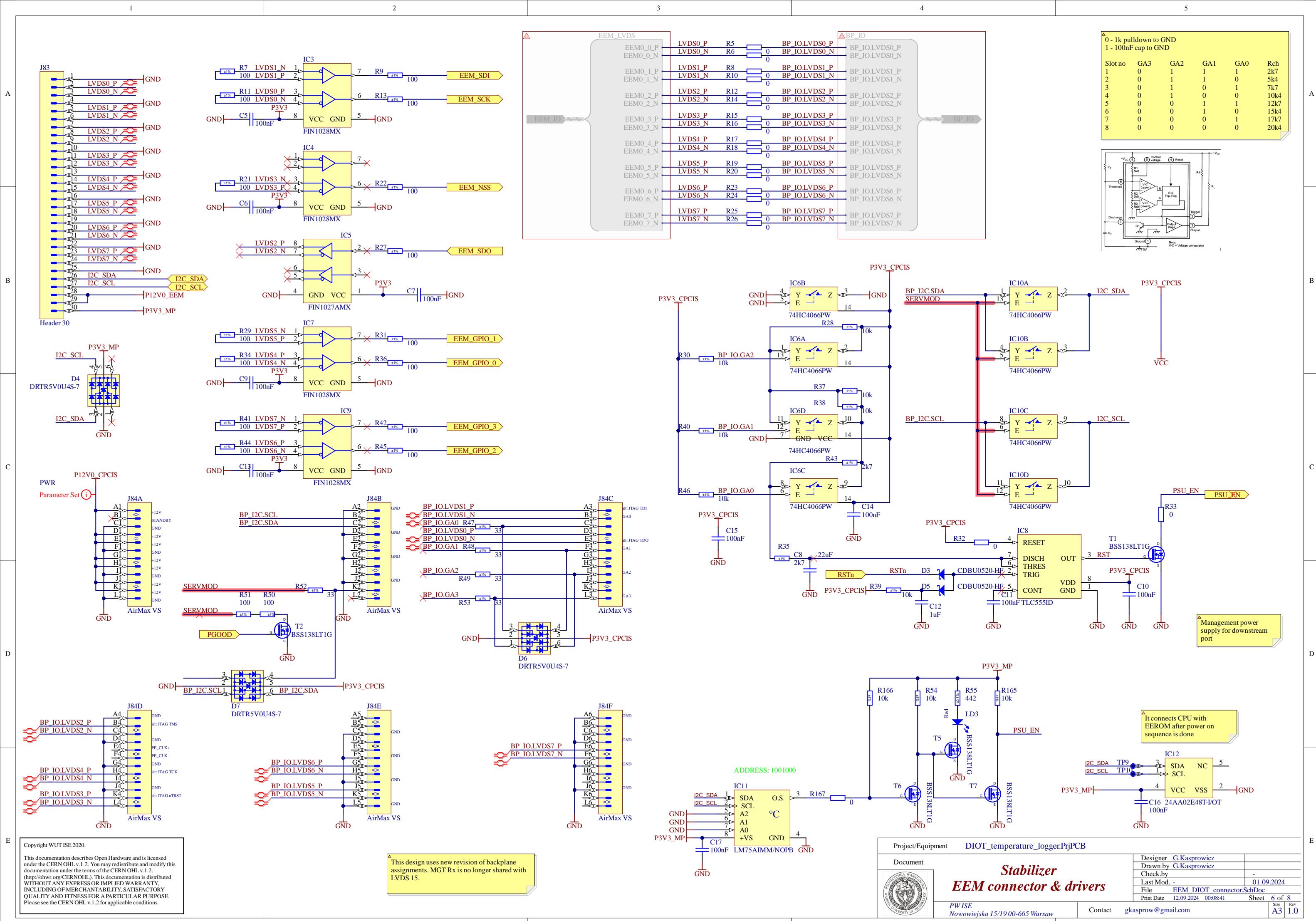
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C1 Undefined GND1
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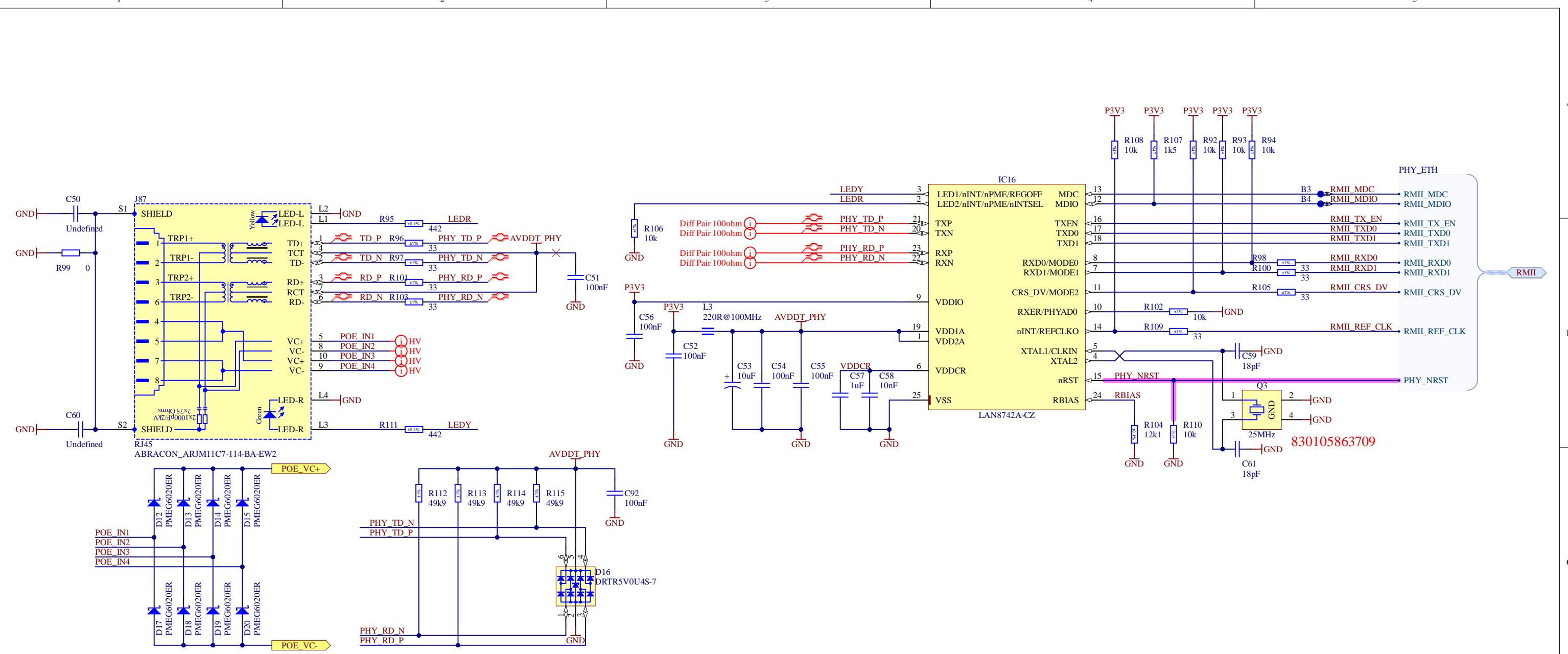


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This design uses new revision of backplane assignments. MGT Rx is no longer shared with LVDS 15.

Project/Equipment: DIOT_temperature_logger.PrtPCB
Document: Stabilizer EEM connector & drivers
Designer: G.Kasprowicz
Drawn by: G.Kasprowicz
Check by: -
Last Mod.: 01.09.2024
File: EEM_DIOT_connector.SchDoc
Print Date: 12.09.2024 00:08:41
Sheet 6 of 8
Size A3 Rev 1.0

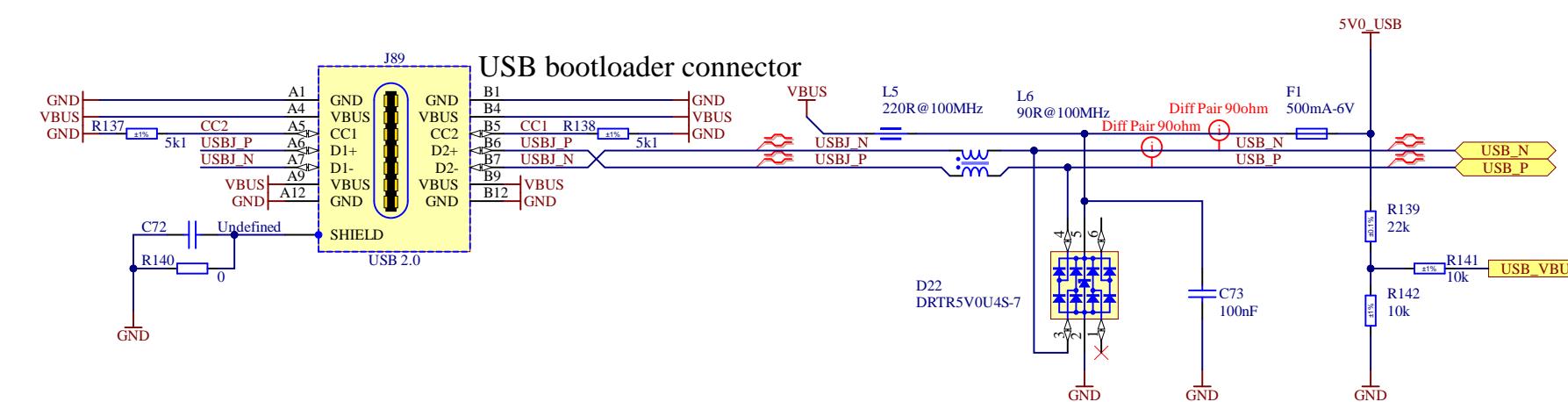
PWIESE Nowowiejska 15/19 00-665 Warsaw
Contact: gkasprow@gmail.com



Project/Equipment		DIOT_temperature_logger.PjPCB	
Document	Thermostat 8CH Ethernet	Designer	G.Kasprowicz
		Drawn by	G.Kasprowicz
		Check by	-
		Last Mod.	11.09.2024
		File	RMII_Ethernet.SchDoc
		Print Date	12.09.2024 00:08:41
		Sheet	7 of 8
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		Rev	1.0

PWIE
Nowowiejska 15/19 00-665 Warsaw

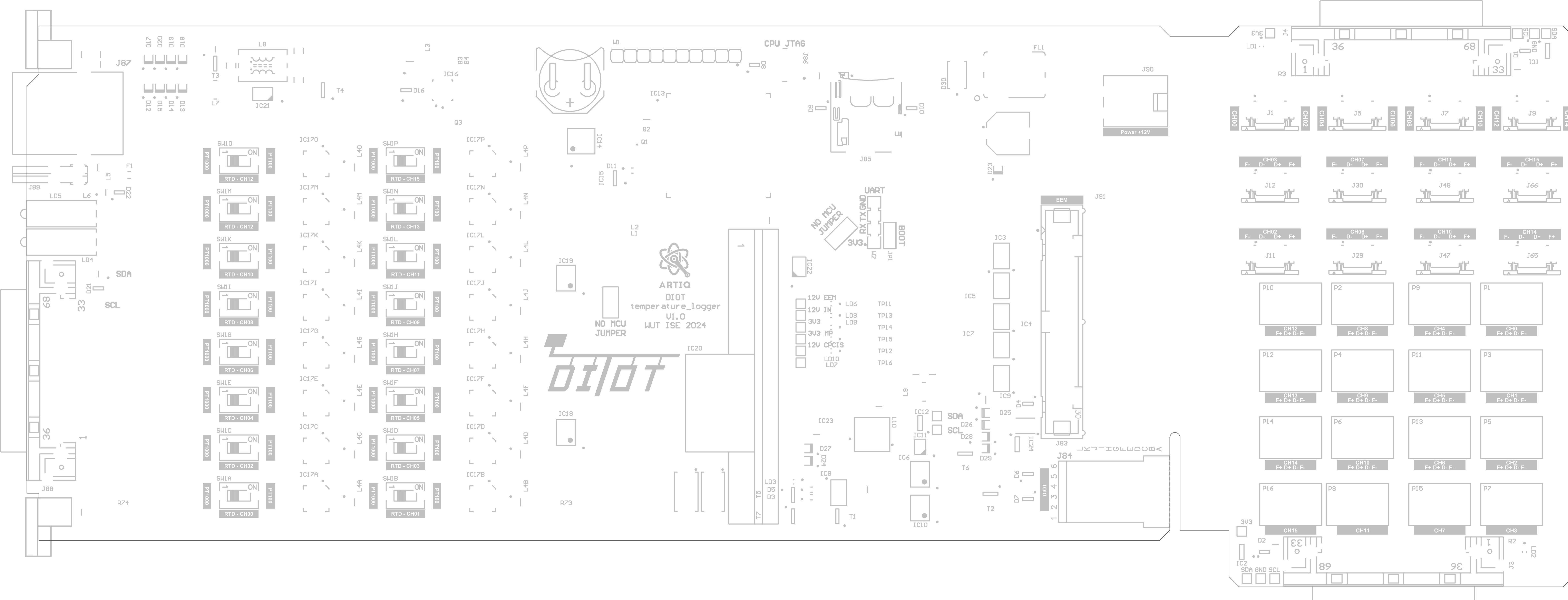
Contact gkasprow@gmail.com

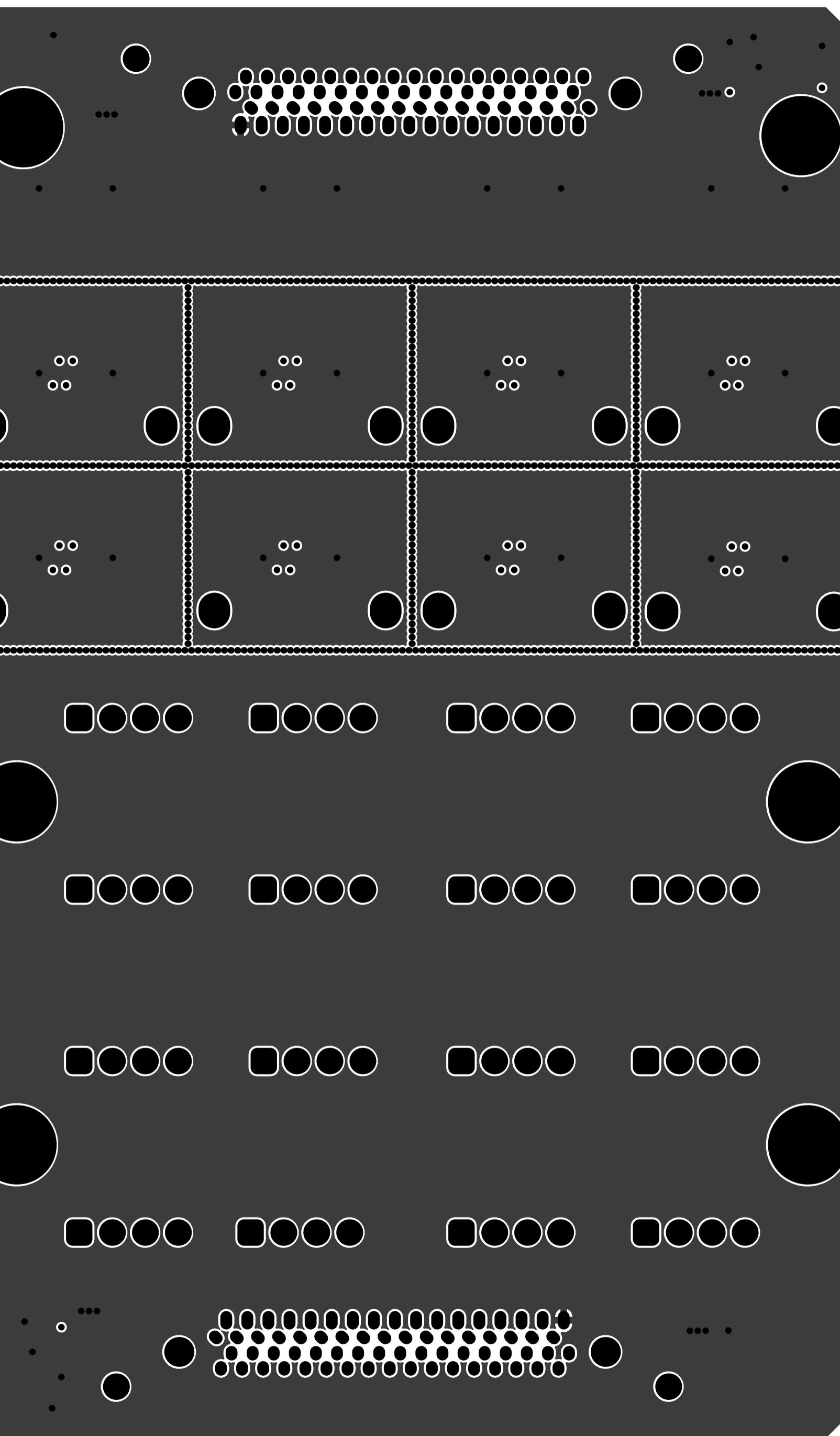
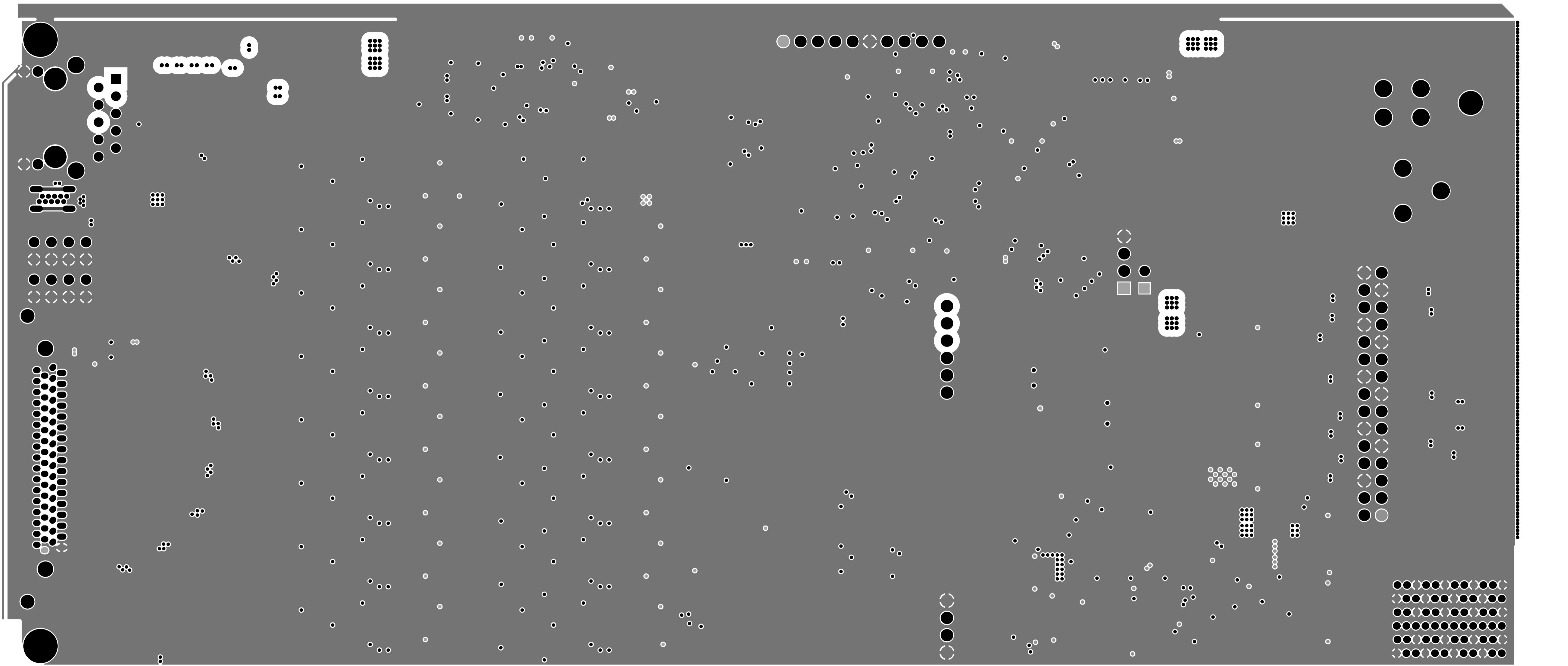


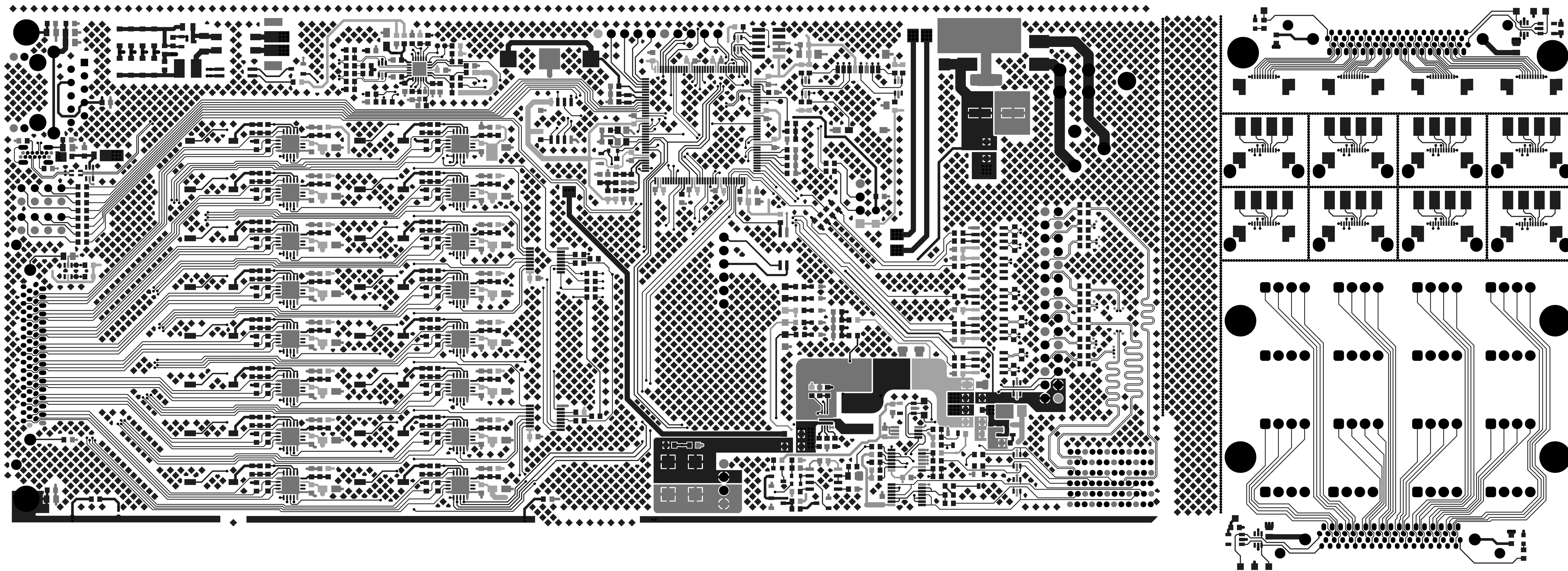
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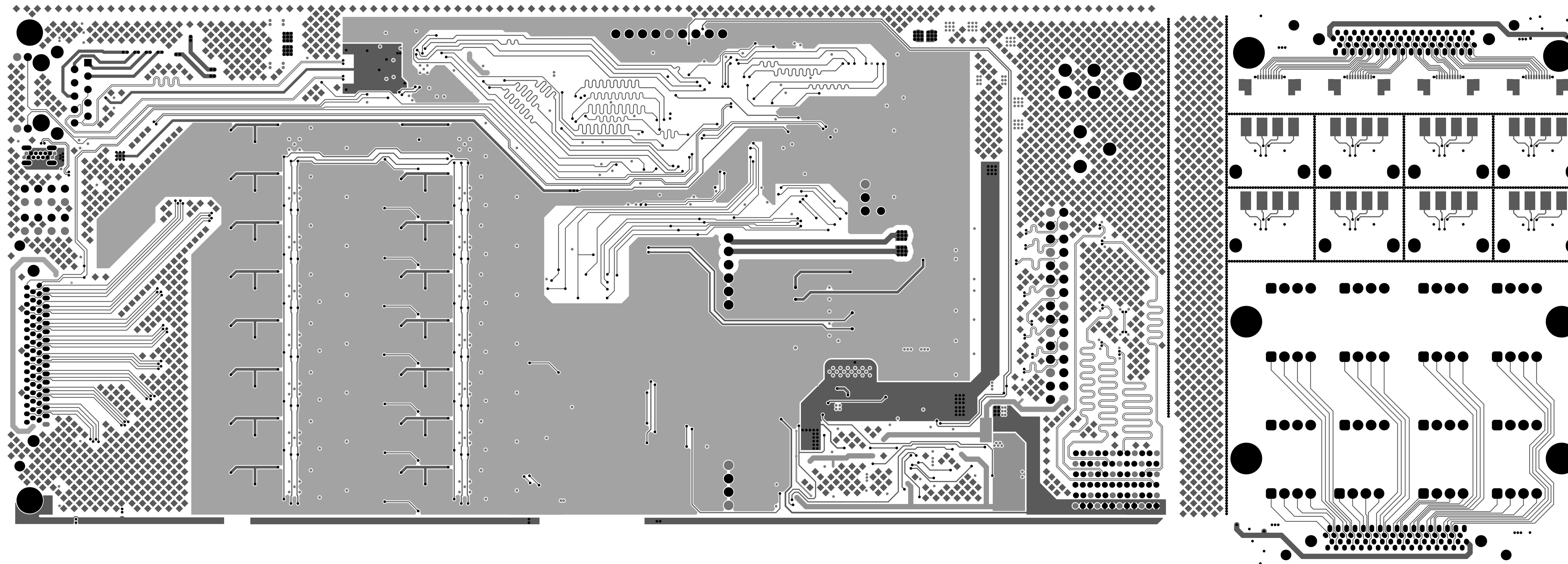
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(<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v. 1.2 for applicable conditions.

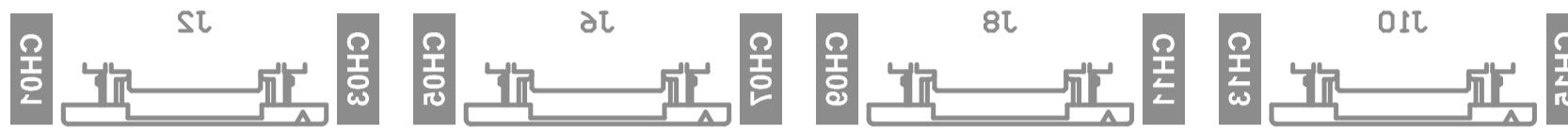
Project/Equipment	DIOT_temperature_logger.PjrPCB		
Document	<i>Thermostat 8CH USB connector</i>	Designer G.Kasprowicz	
		Drawn by G.Kasprowicz	
		Check by -	
	Last Mod. -		23.08.2024
	File USB.SchDoc		
	Print Date 12.09.2024 00:08:41	Sheet 8	of 8 Rev 1.0
PWIE Nowowiejska 15/19 00-665 Warsaw	Contact gkasprow@gmail.com		Size A3





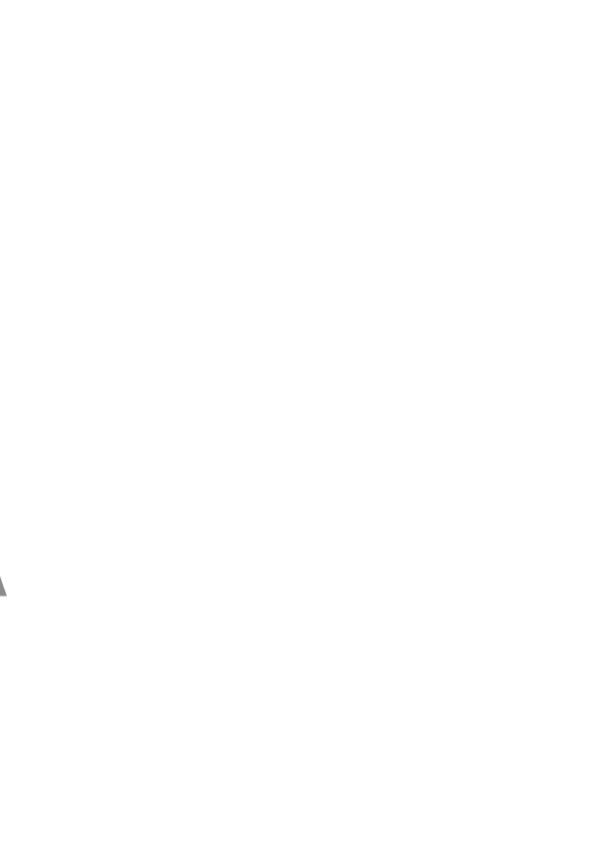




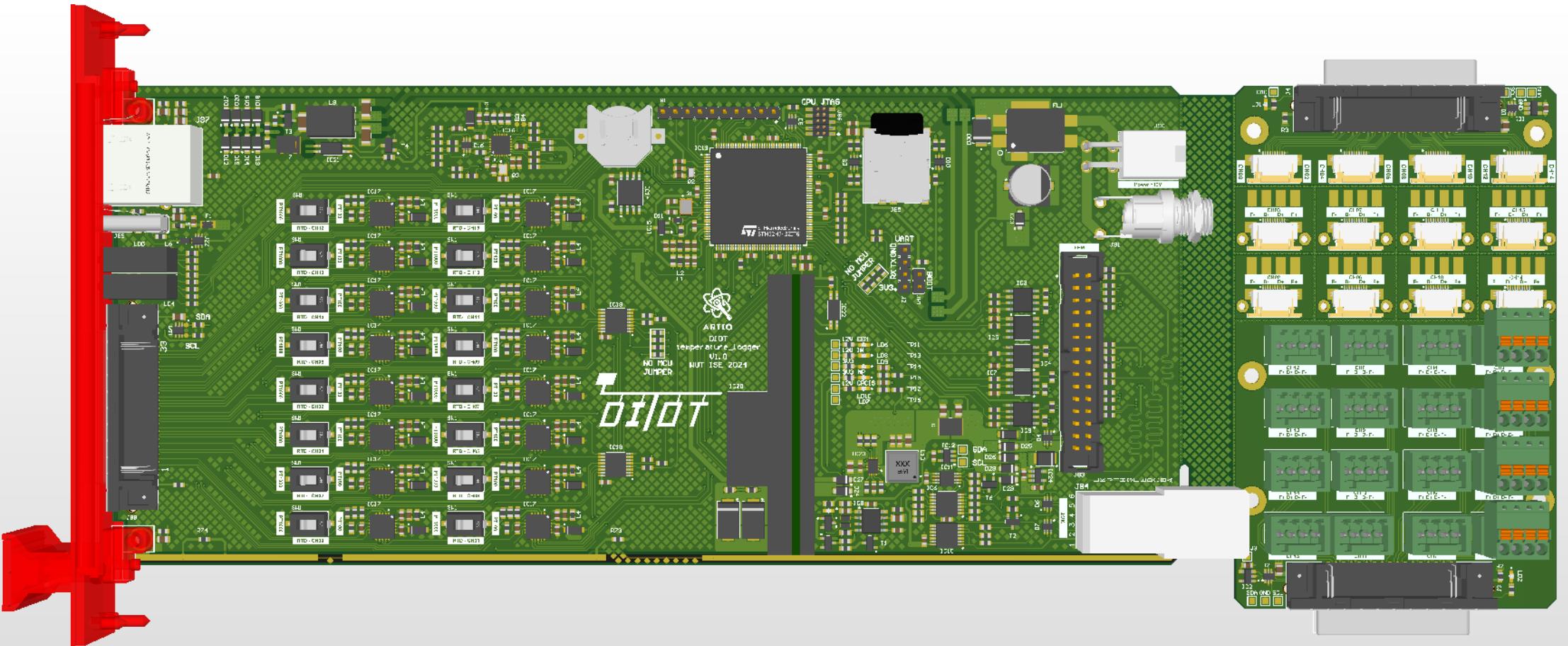


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Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1	TopOverlay			0mm	
2	TopSolder	Solder Resist		0.01001mm	3.5
3	TOP			0.035mm	
4	TOP 3313*1	PP-006		0.09939mm	4.1
5	MID1	CF-004		0.01519mm	
6	Dielectric2	Core-042		1.265mm	4.6
7	MID2	CF-004		0.01519mm	
8	BOT 3313*1	PP-006		0.09939mm	4.1
9	BOT			0.035mm	
10	BottomSolder	Solder Resist		0.01001mm	3.5
11	BottomOverlay			0mm	
	Height : 1.58417mm				