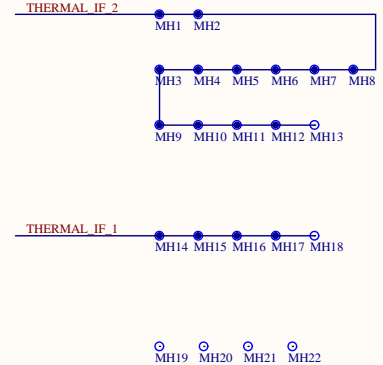
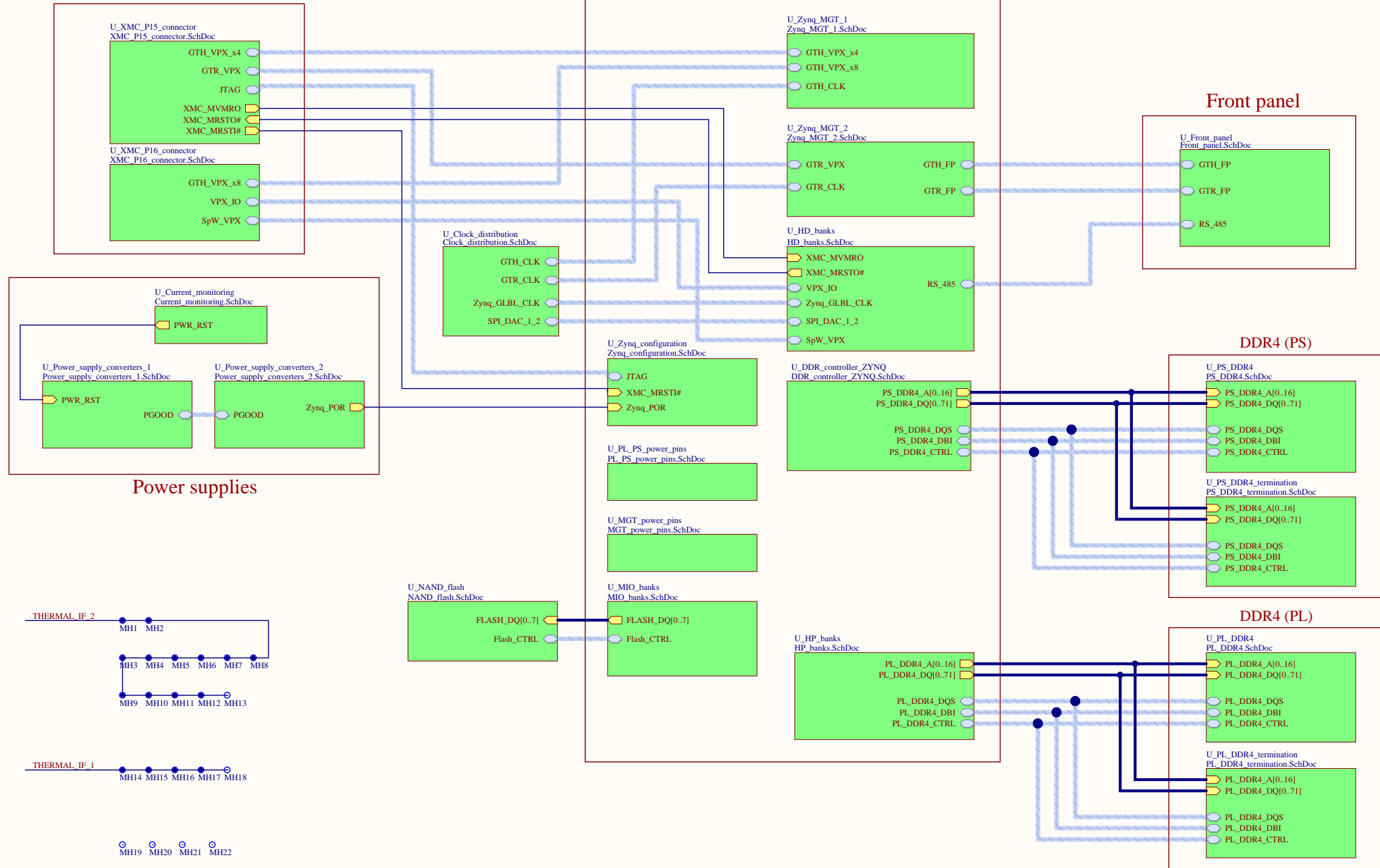
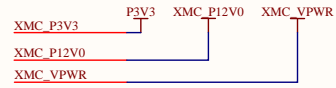
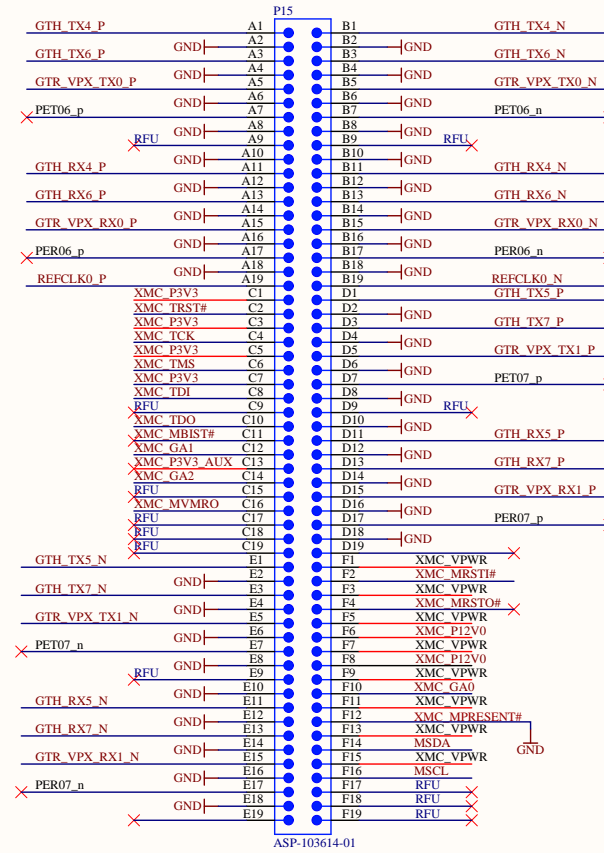


XMC connectors

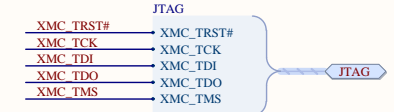
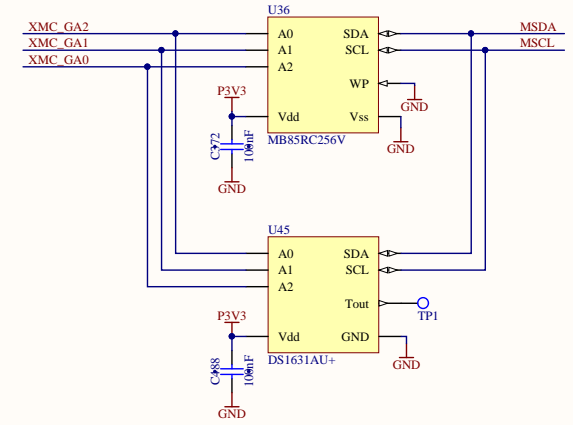
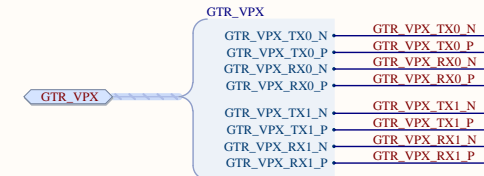
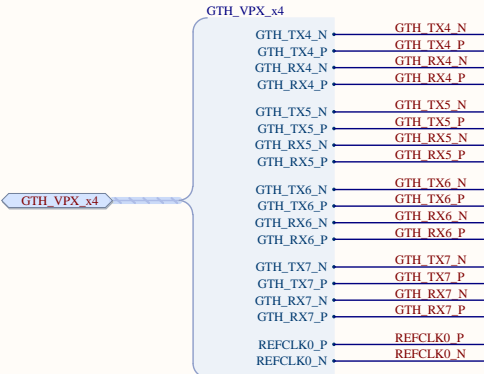
ZYNQ UltraScale+



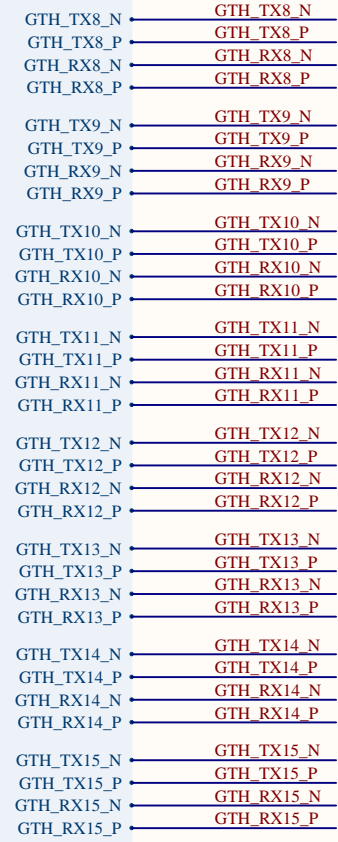
P15 Primary XMC connector



VPWR can be either +12V or +5V

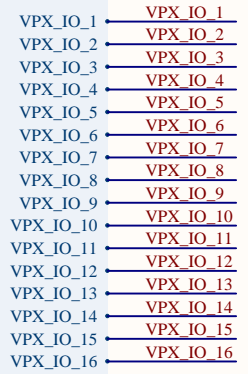


GTH_VPX_x8



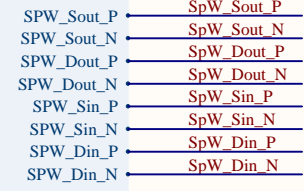
GTH_VPX_x8

VPX_IO

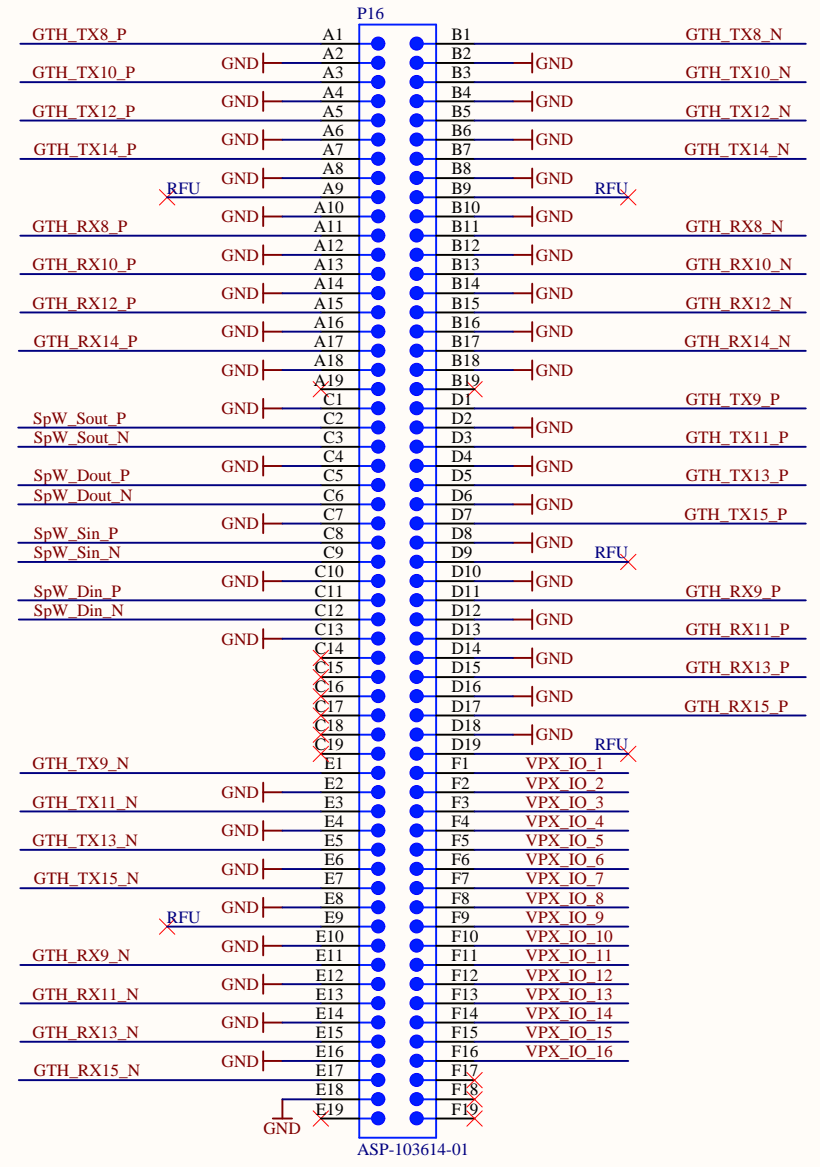


SpW_VPX

SpW_VPX



P16 Secondary XMC connector



Title XMC_P16_connector		
Size: A4	Number:3	Revision:1.0
Date: 10.07.2019	Time: 9:08:12	Sheet:3 of 22
File: D:\studies\MGR\PCB\XMC_P16_connector.SchDoc		



A

A

B

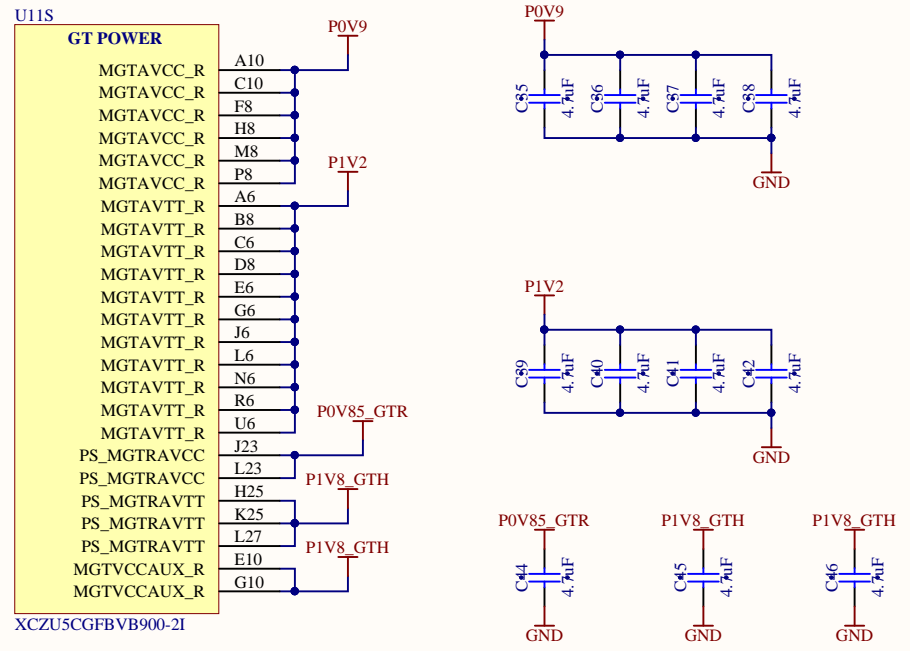
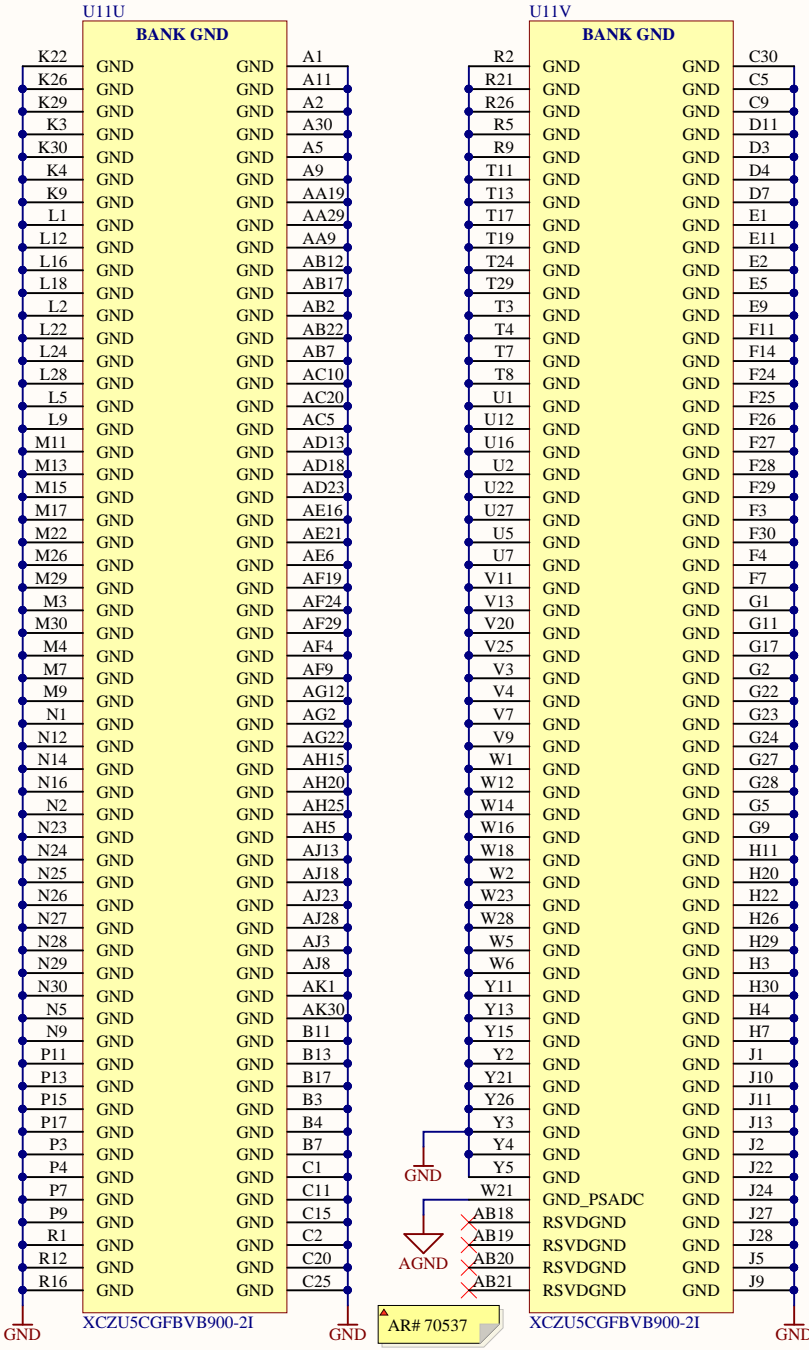
B

C

C

D

D

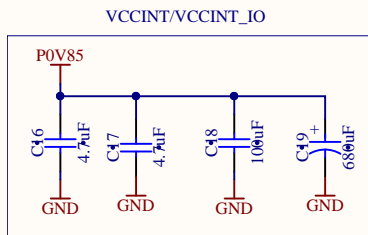
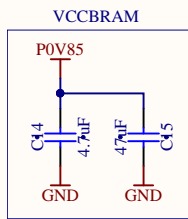
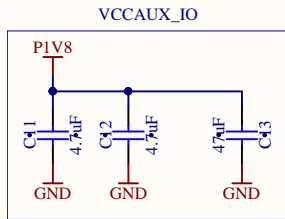
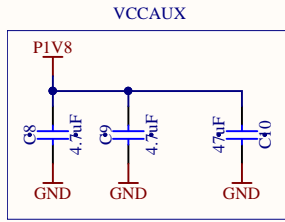
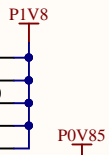


Title GT_power_gnd_pins		
Size: A4	Number: 4	Revision: 1.0
Date: 10.07.2019	Time: 9:08:13	Sheet 4 of 22
File: D:\studies\MGR\PCB\MGT_power_pins.SchDoc		



U11R	
PL CORE POWER	
VCCAUX	K10
VCCAUX	L10
VCCAUX_IO	M10
VCCAUX_IO	N10
VCCAUX_IO	P10
VCCBRAM	R10
VCCBRAM	T10
VCCBRAM	U10
VCCBRAM	V10
VCCINT	L11
VCCINT	L13
VCCINT	L17
VCCINT	M12
VCCINT	M14
VCCINT	M16
VCCINT	M18
VCCINT	N11
VCCINT	N13
VCCINT	N15
VCCINT	N17
VCCINT	P12
VCCINT	P14
VCCINT	P16
VCCINT	R11
VCCINT	R13
VCCINT	R17
VCCINT	T12
VCCINT	T16
VCCINT	U11
VCCINT	U13
VCCINT	U17
VCCINT	V12
VCCINT	V16
VCCINT	W11
VCCINT	W13
VCCINT	W15
VCCINT	Y12
VCCINT	Y14
VCCINT	T9
VCCINT_IO	U8
VCCINT_IO	U9
VCCINT_IO	V8

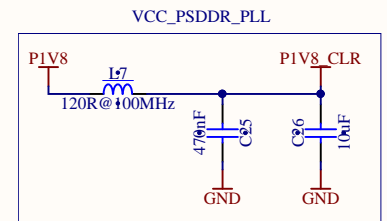
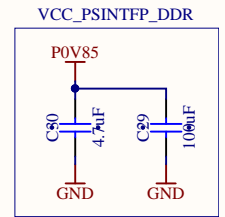
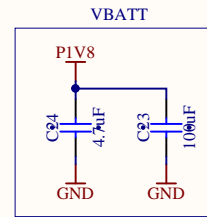
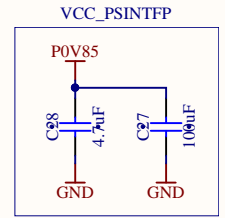
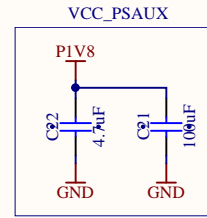
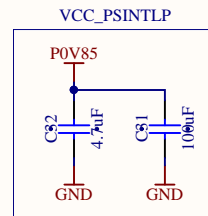
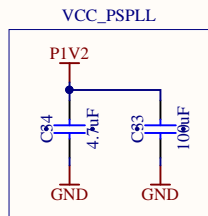
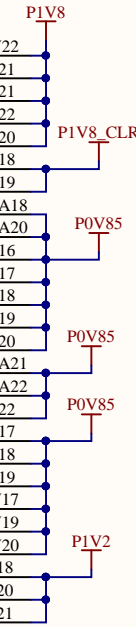
XCZU5CGFBVB900-2I



U11T

PS CORE POWER	
VCC_PSADC	W22
VCC_PSAUX	U21
VCC_PSAUX	V21
VCC_PSAUX	V22
VCC_PSBATT	U20
VCC_PSDDR_PLL	U18
VCC_PSDDR_PLL	U19
VCC_PSINTFP	AA18
VCC_PSINTFP	AA20
VCC_PSINTFP	Y16
VCC_PSINTFP	Y17
VCC_PSINTFP	Y18
VCC_PSINTFP	Y19
VCC_PSINTFP	Y20
VCC_PSINTFP_DDR	AA21
VCC_PSINTFP_DDR	AA22
VCC_PSINTFP_DDR	Y22
VCC_PSINTLP	V17
VCC_PSINTLP	V18
VCC_PSINTLP	V19
VCC_PSINTLP	W17
VCC_PSINTLP	W19
VCC_PSINTLP	W20
VCC_PSPLL	T18
VCC_PSPLL	T20
VCC_PSPLL	T21

XCZU5CGFBVB900-2I



Careful design recommended.
See UG583 p. 27

Title **PL_PS_power_pins**

Size: A4 Number: 5 Revision: 1.0

Date: 10.07.2019 Time: 9:08:13 Sheet 5 of 22

File: D:\studies\MGR\PCB\PL_PS_power_pins.SchDoc



LTM4644:
0V85 - 143K
0V9 - 121K
1V2 - 60K4
1V5 - 40K2
1V8 - 30K1
3V3 - 13K3
5V0 - 8K25

LPD:
VCC_PSINTLP 0,85V
VCC_PSPLL 1,2V
VCC_PSADC 1,8V
VCC_PSAUX 1,8V (bank 500)
VCCO_PSIO 1,8V (bank 500)

FPD:
VCC_PSINTFP 0,85V
VCC_PSINTFP_DDR 0,85V
VCC_PSDDDR_PLL 1,8V
VCCO_PSDDDR 1,2V
PS_MGTRAVCC 0,85V
PS_MGTRAVTT 1,8V

PL:
VCCINT 0,85V
VCCINT_IO 0,85V
VCCBRAM 0,85V
VCCO_PSDDDR 1,2V
VCCCAUX 1,8V
VCCCAUX_IO 1,8V

MGTAUCC_R 0,9V
MGTAUVT_R 1,2V
MGTVCCAUCC_R 1,8V

VCCO 1,2V

Sequencing

LPD:
1. VCC_PSINTLP
2. VCC_PSAUX, VCC_PSADC, VCC_PSPLL
3. VCC_PSIO

FPD:
1. VCC_PSINTFP, VCC_PSINTFP_DDR
2. PS_MGTRAVCC, VCC_PSDDDR_PLL
3. PS_MGTRAVTT, VCCO_PSDDDR

PL:
1. VCCINT, MGTAUCC_R
2. VCCINT_IO, VCCBRAM, MGTAUVT_R
3. VCCCAUX, VCCCAUX_IO
4. VCCO

MGTVCCAUCC - no recommended sequencing

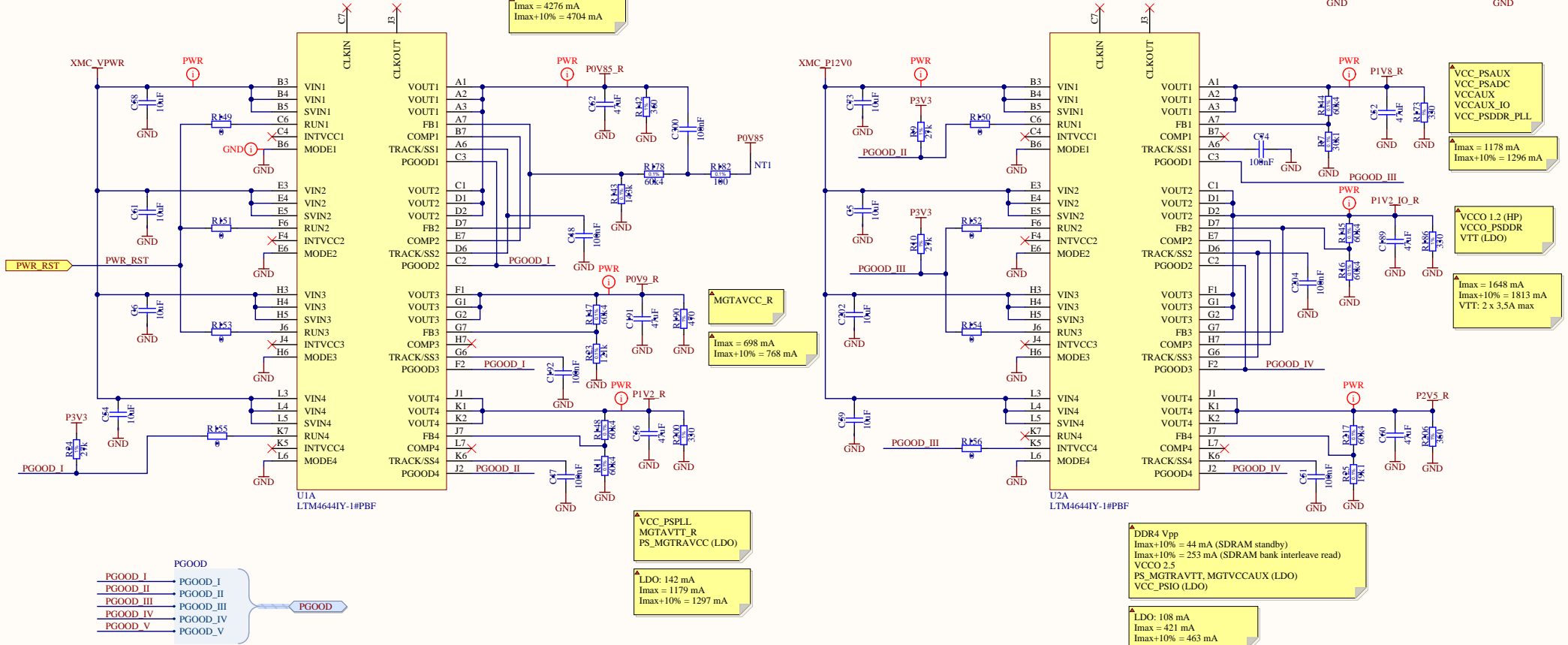
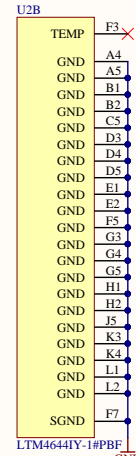
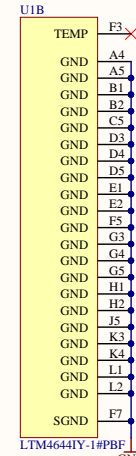
Supply currents [mA]

PWR	XPE	Iq	Startup
VCCINT	1552	684	+770
VCCINT_IO	395	59	+257 (with VCCBRAM)
VCCO 3.3	50	1	+50
VCCO 2.5	33	1	+50
VCCO 1.2	852	1	+50
VCCCAUX	137	90	+386 (with VCCCAUX_IO)
VCCCAUX_IO	630	32	+386 (with VCCCAUX)
VCCBRAM	4	9	+257 (with VCCINT_IO)
VCC_PSINTLP	82		
VCC_PSINTFP	333		
VCCO_PSDDDR	746		
PSINTFP_DDR	878		
VCC_PSPLL	33		
PSDDR_PLL	12		
VCC_PSADC	11		
VCC_PSAUX	2		
MGTVCCAUCC	61		
MGTAUCC_R	698		
MGTAUVT_R	1004		
PS_MGTRAVCC	142		
PS_MGTRAVTT	18		
VCCO_PSIO0	2		

DS925, p. 13

VCC_PSINTLP,
VCC_PSINTFP,
VCC_PSINTFP_DDR,
VCCINT,
VCCINT_IO,
VCCBRAM

I_{max} = 4276 mA
I_{max}+10% = 4704 mA



VCC_PSAUX,
VCC_PSADC,
VCCCAUX,
VCCCAUX_IO,
VCC_PSDDDR_PLL

I_{max} = 1178 mA
I_{max}+10% = 1296 mA

VCCO 1.2 (HP)
VCCO_PSDDDR
VTT (LDO)

I_{max} = 1648 mA
I_{max}+10% = 1813 mA
VTT: 2 x 3,5A max

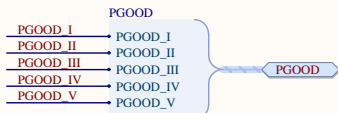
MGTAUCC_R
I_{max} = 698 mA
I_{max}+10% = 768 mA

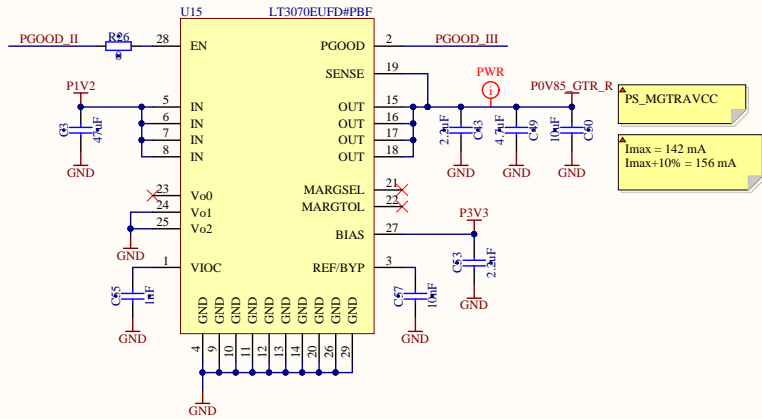
VCC_PSPLL
MGTAUVT_R
PS_MGTRAVCC (LDO)

LDO: 142 mA
I_{max} = 1179 mA
I_{max}+10% = 1297 mA

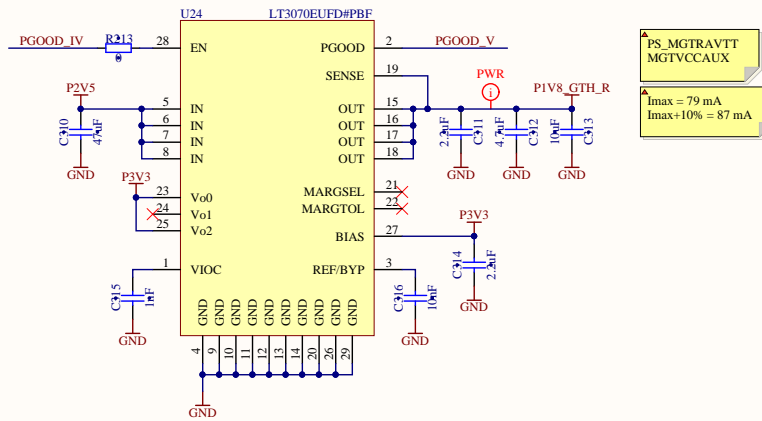
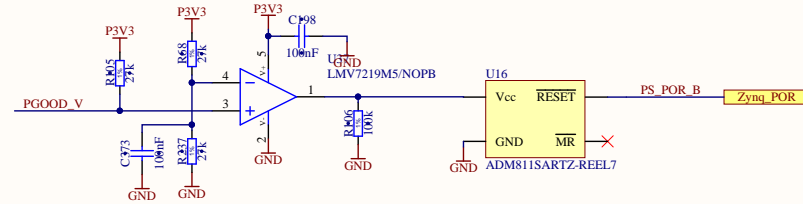
DDR4 V_{pp}
I_{max}+10% = 44 mA (SDRAM standby)
I_{max}+10% = 253 mA (SDRAM bank interleaved read)
VCCO 2.5
PS_MGTRAVTT, MGTVCCAUCC (LDO)
VCC_PSIO (LDO)

LDO: 108 mA
I_{max} = 421 mA
I_{max}+10% = 463 mA

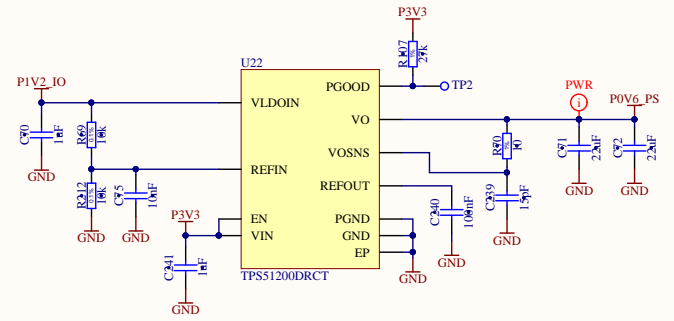




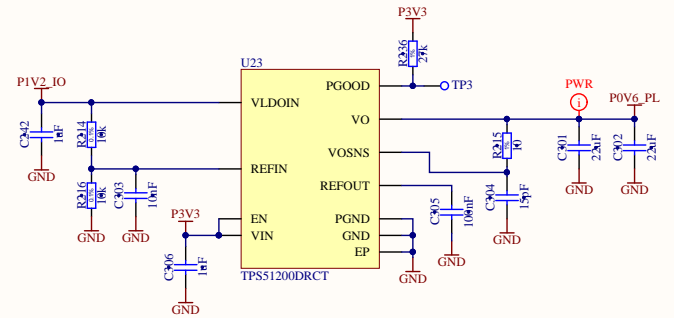
PS_MGTRAVCC
 I_{max} = 142 mA
 I_{max}+10% = 156 mA



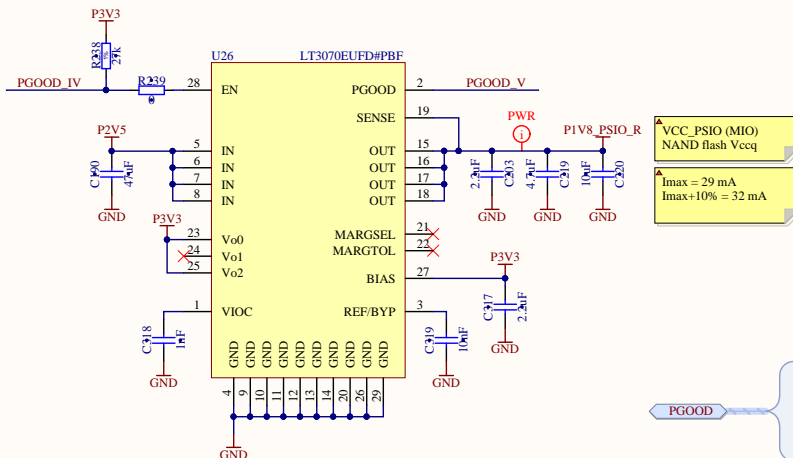
PS_MGTRAVTT
 MGTVCCAUX
 I_{max} = 79 mA
 I_{max}+10% = 87 mA



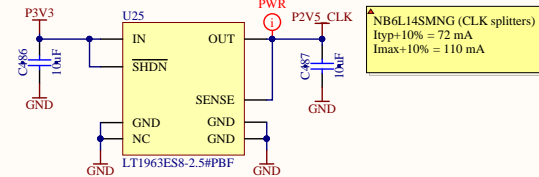
PS DDR4 termination



PL DDR4 termination



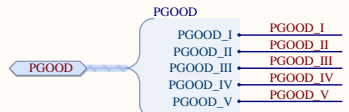
VCC_PSIO (MIO)
 NAND flash Vccq
 I_{max} = 29 mA
 I_{max}+10% = 32 mA

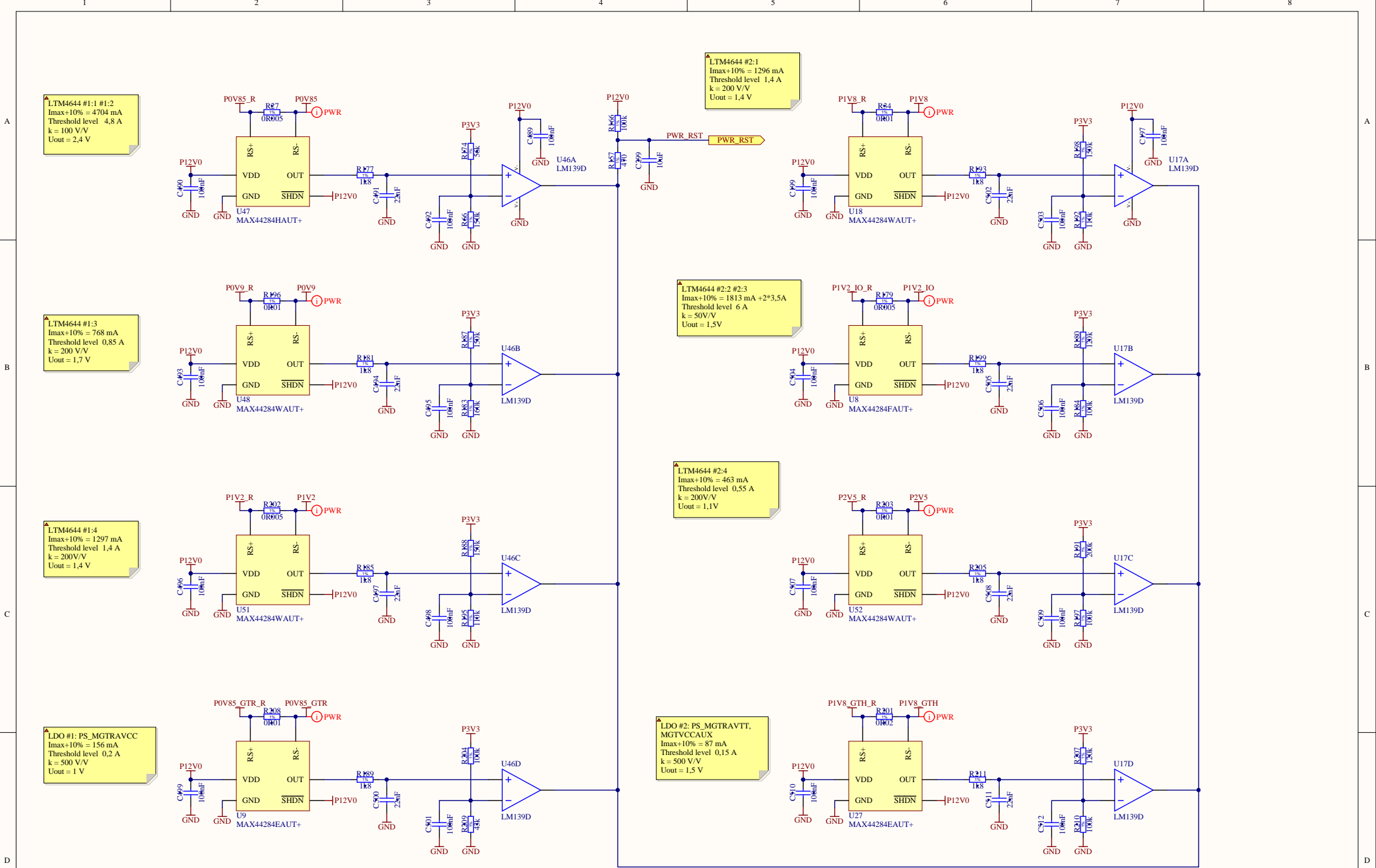


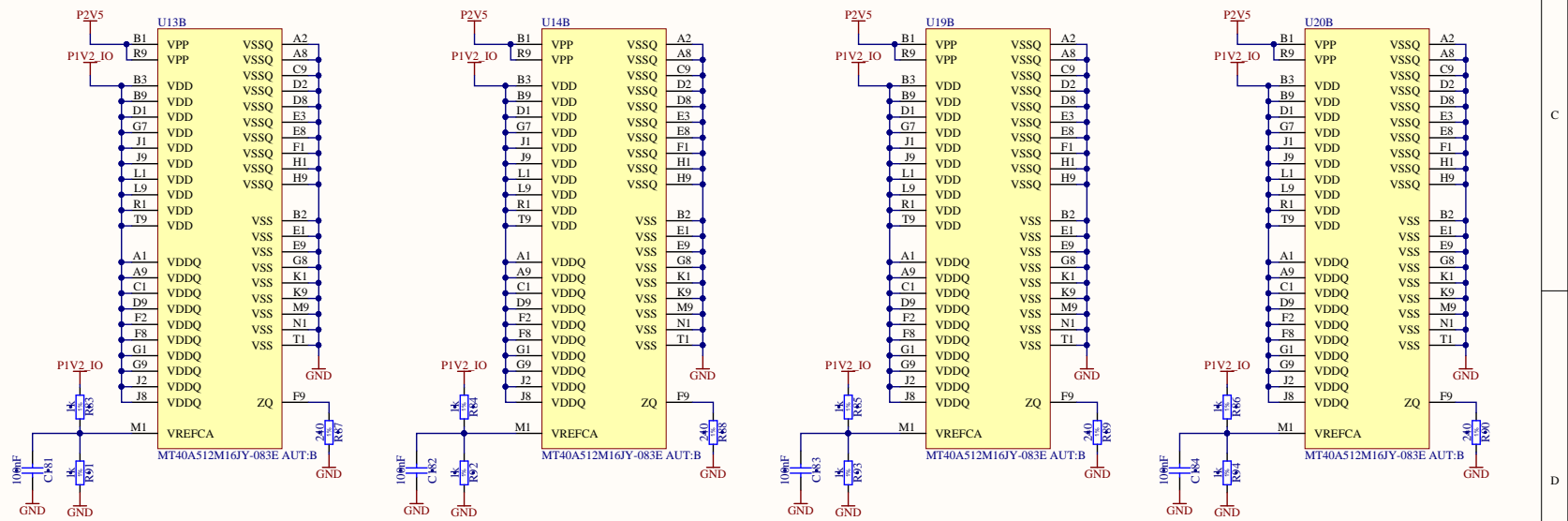
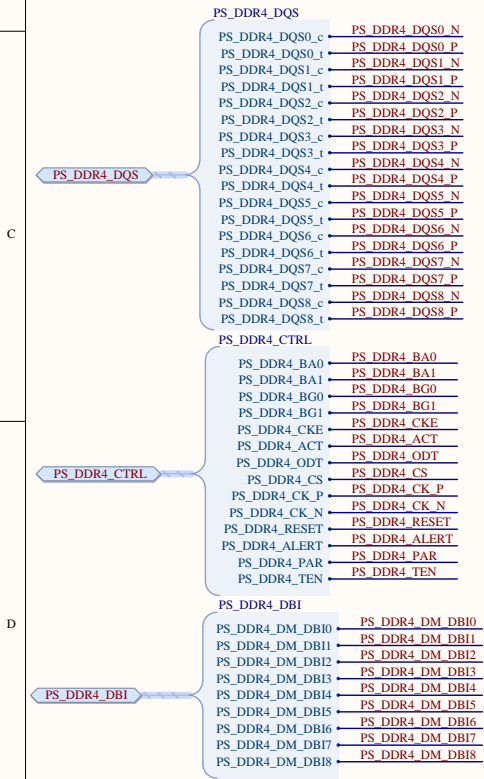
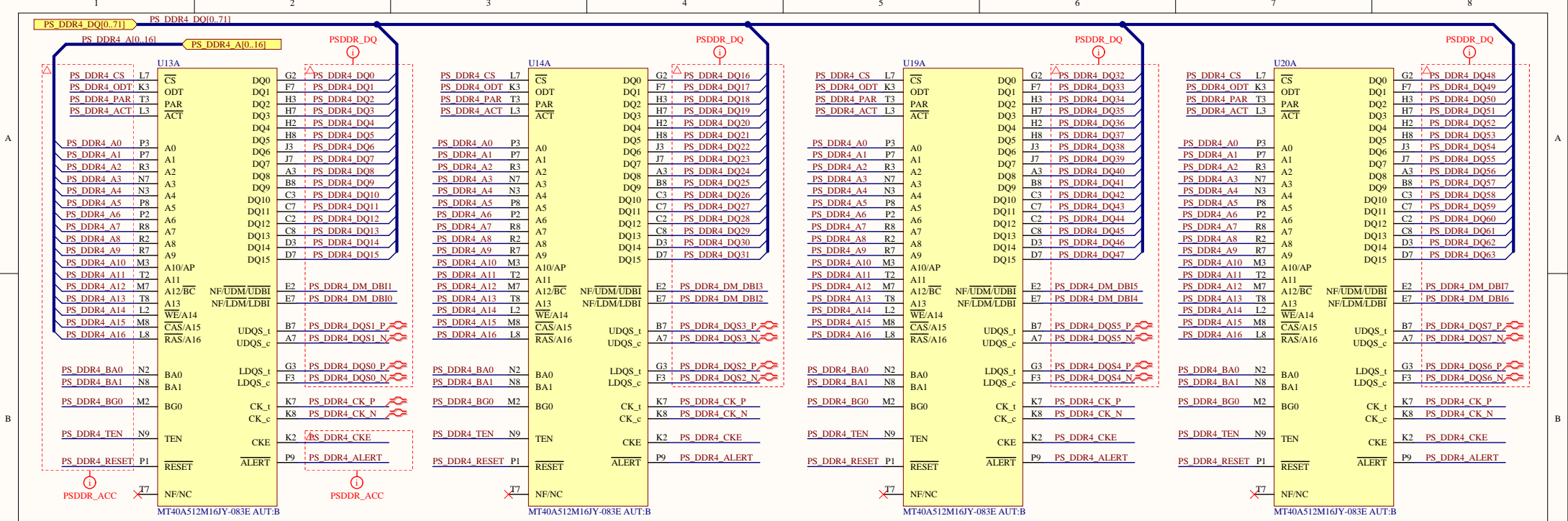
NB6L14SMNG (CLK splitters)
 I_{typ}+10% = 72 mA
 I_{max}+10% = 110 mA

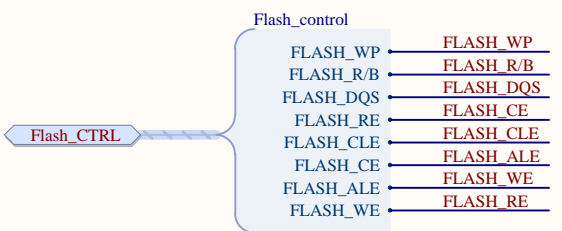
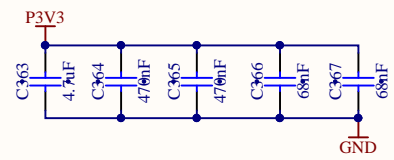
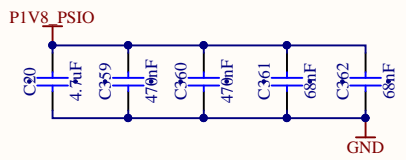
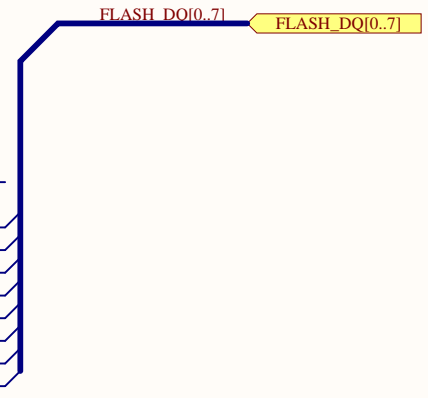
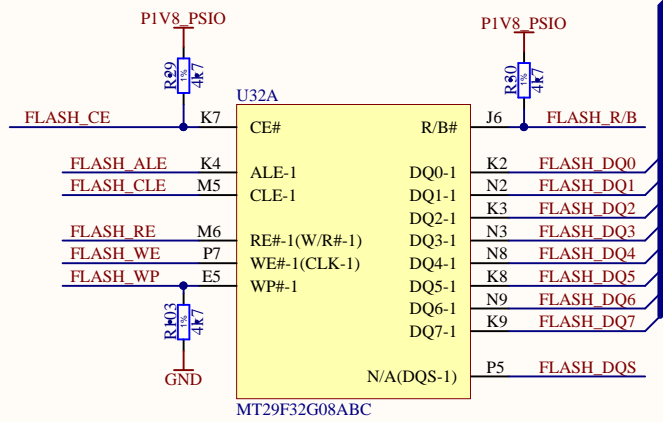
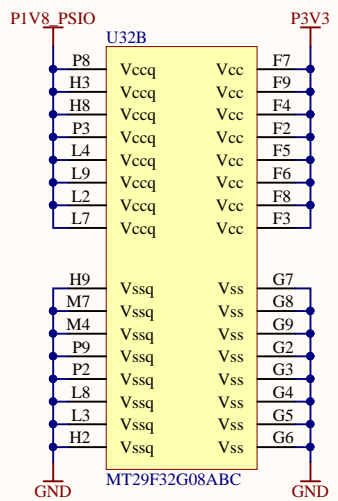
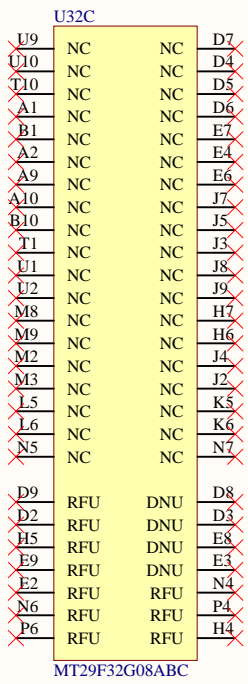
3.3V power supply:

P2V5_CLK LDO	100 mA
ASGTX 125	45 mA
ASGTX 156,25	45 mA
FRAM	200 mA
Thermometer	1.25 mA
TPSS1200 (1)	1 mA
TPSS1200 (2)	1 mA
LMV7219	2.2 mA
HD 45	100 mA
VCC_PSIO3	1 mA
SPX0018042	20 mA
NAND flash VCC	50 mA
SN65HVD1781D x 4	120 mA
Total	487 mA
Total+10%	536 mA



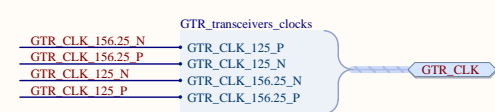
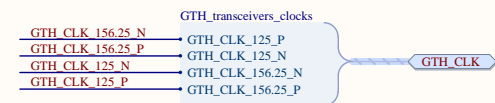
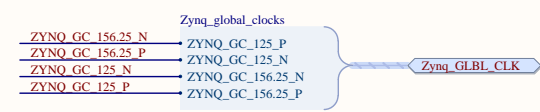
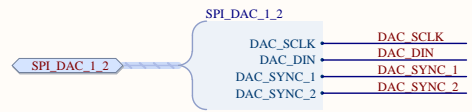
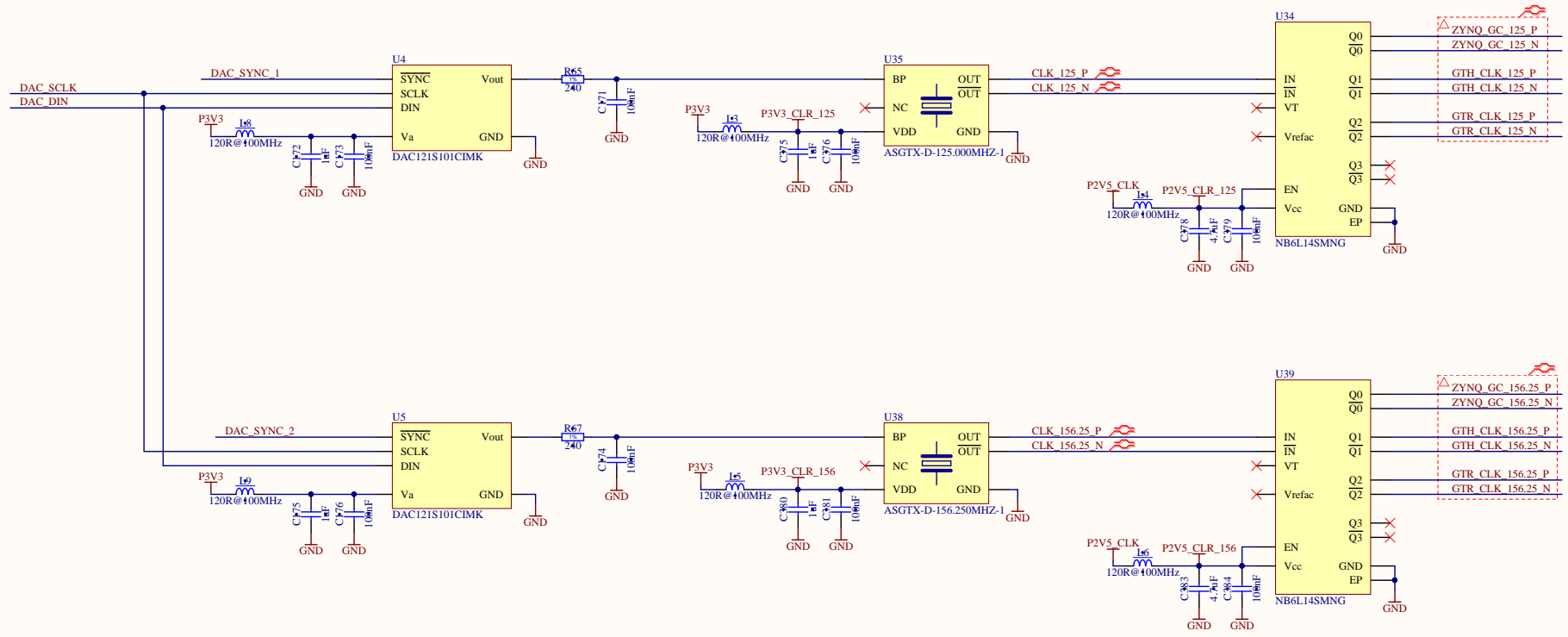






Title NAND_flash		
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Date: 10.07.2019	Time: 9:08:16	Sheet 13 of 22
File: D:\studies\MGR\PCB\NAND_flash.SchDoc		



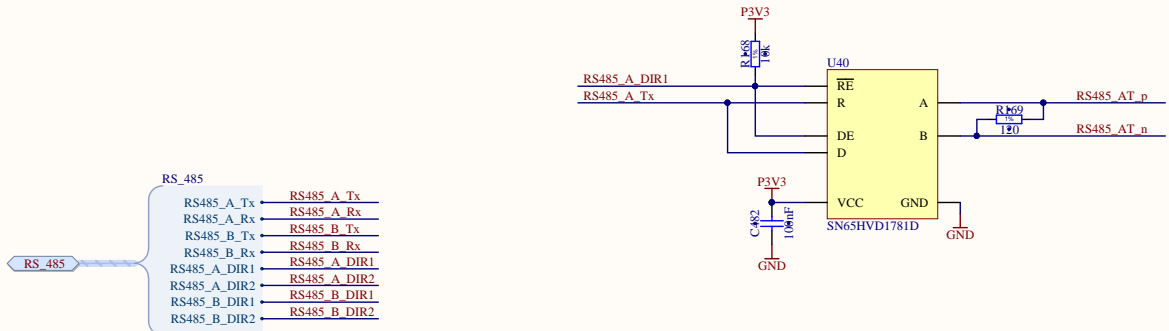


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Date: 10.07.2019	Time: 9:08:16	Sheet 14 of 22	*
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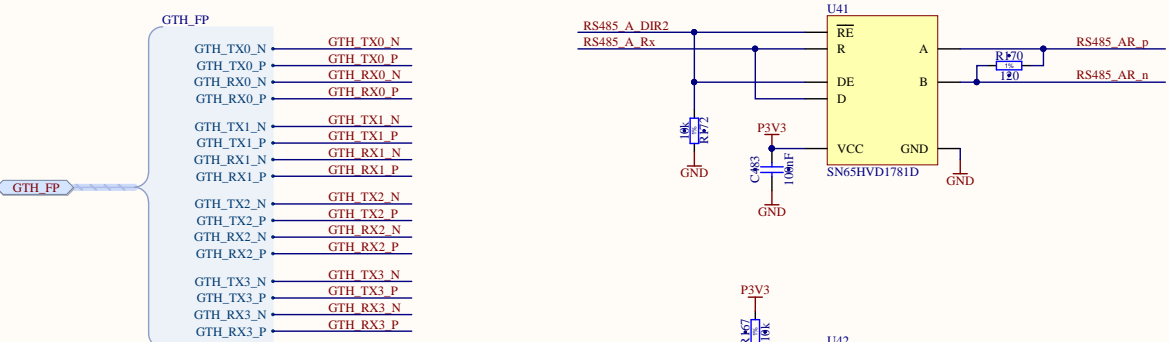


A

A



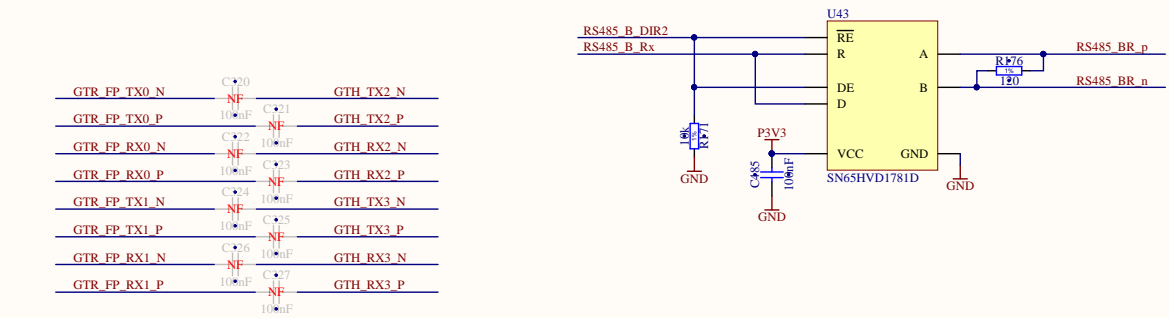
- RS_485**
- RS485_A_Tx → RS485_A_Tx
 - RS485_A_Rx → RS485_A_Rx
 - RS485_B_Tx → RS485_B_Tx
 - RS485_B_Rx → RS485_B_Rx
 - RS485_B_Rx1 → RS485_A_DIR1
 - RS485_A_DIR2 → RS485_A_DIR2
 - RS485_B_DIR1 → RS485_B_DIR1
 - RS485_B_DIR2 → RS485_B_DIR2



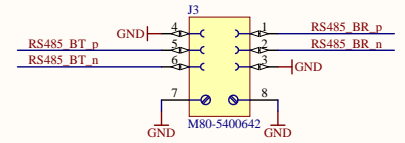
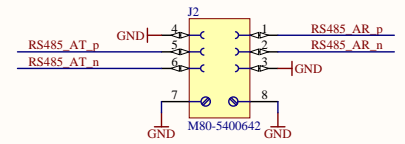
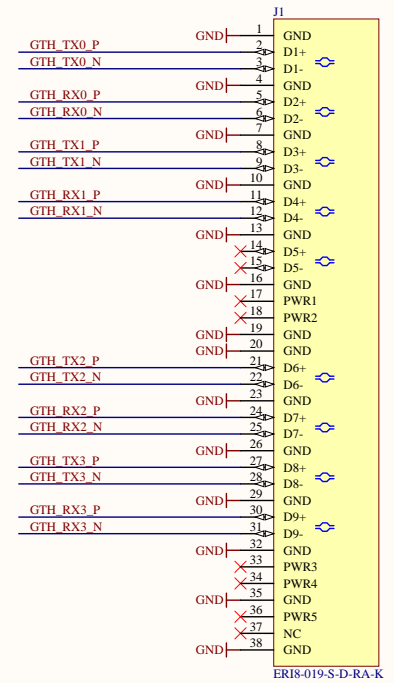
- GTH_FP**
- GTH_TX0_N → GTH_TX0_N
 - GTH_TX0_P → GTH_TX0_P
 - GTH_RX0_N → GTH_RX0_N
 - GTH_RX0_P → GTH_RX0_P
 - GTH_TX1_N → GTH_TX1_N
 - GTH_TX1_P → GTH_TX1_P
 - GTH_RX1_N → GTH_RX1_N
 - GTH_RX1_P → GTH_RX1_P
 - GTH_TX2_N → GTH_TX2_N
 - GTH_TX2_P → GTH_TX2_P
 - GTH_RX2_N → GTH_RX2_N
 - GTH_RX2_P → GTH_RX2_P
 - GTH_TX3_N → GTH_TX3_N
 - GTH_TX3_P → GTH_TX3_P
 - GTH_RX3_N → GTH_RX3_N
 - GTH_RX3_P → GTH_RX3_P



- GTR_FP**
- GTR_FP_TX0_N → GTR_FP_TX0_N
 - GTR_FP_TX0_P → GTR_FP_TX0_P
 - GTR_FP_RX0_N → GTR_FP_RX0_N
 - GTR_FP_RX0_P → GTR_FP_RX0_P
 - GTR_FP_TX1_N → GTR_FP_TX1_N
 - GTR_FP_TX1_P → GTR_FP_TX1_P
 - GTR_FP_RX1_N → GTR_FP_RX1_N
 - GTR_FP_RX1_P → GTR_FP_RX1_P



- GTR_FP_TX0_N → C470 → GTH_TX2_N
- GTR_FP_TX0_P → C421 → GTH_TX2_P
- GTR_FP_RX0_N → C422 → GTH_RX2_N
- GTR_FP_RX0_P → C423 → GTH_RX2_P
- GTR_FP_TX1_N → C424 → GTH_TX3_N
- GTR_FP_TX1_P → C425 → GTH_TX3_P
- GTR_FP_RX1_N → C426 → GTH_RX3_N
- GTR_FP_RX1_P → C427 → GTH_RX3_P



B

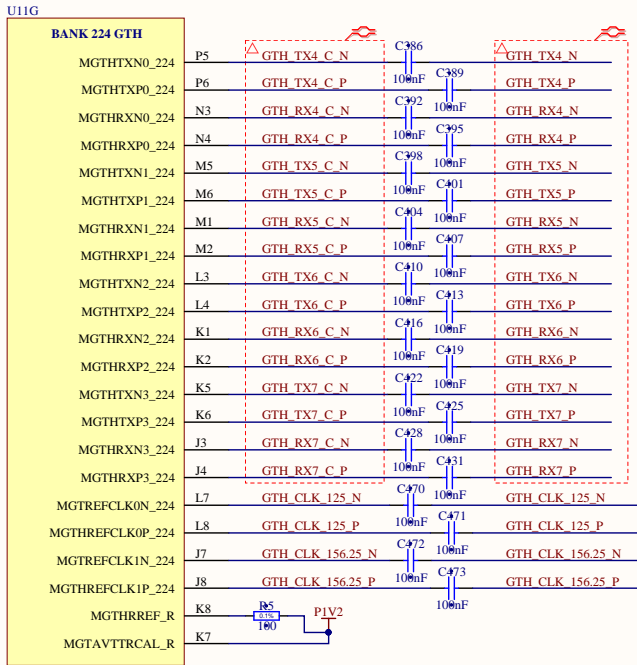
B

C

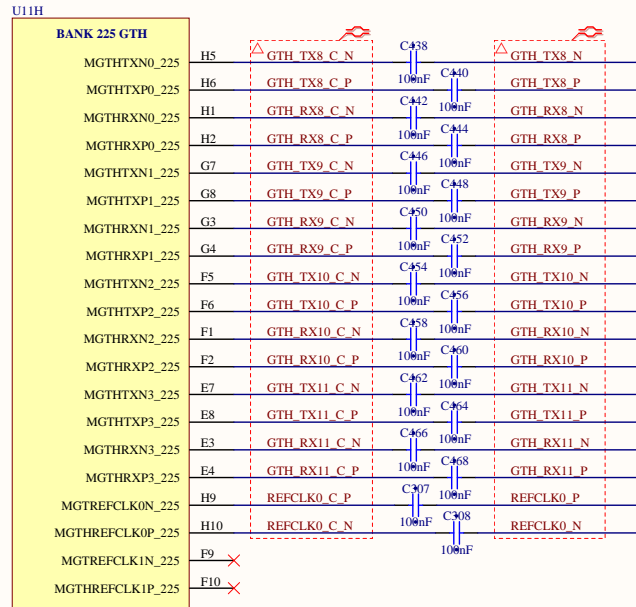
C

D

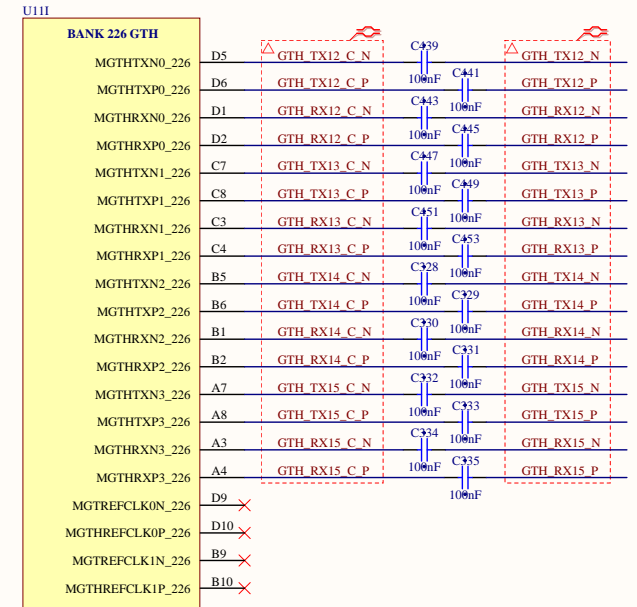
D



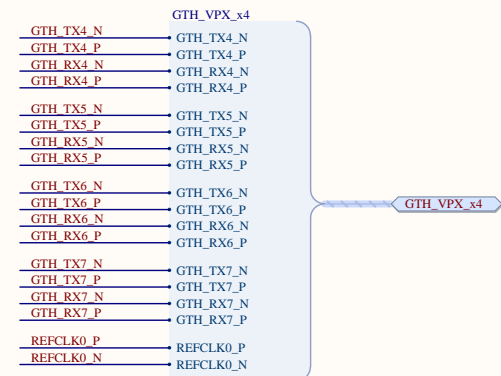
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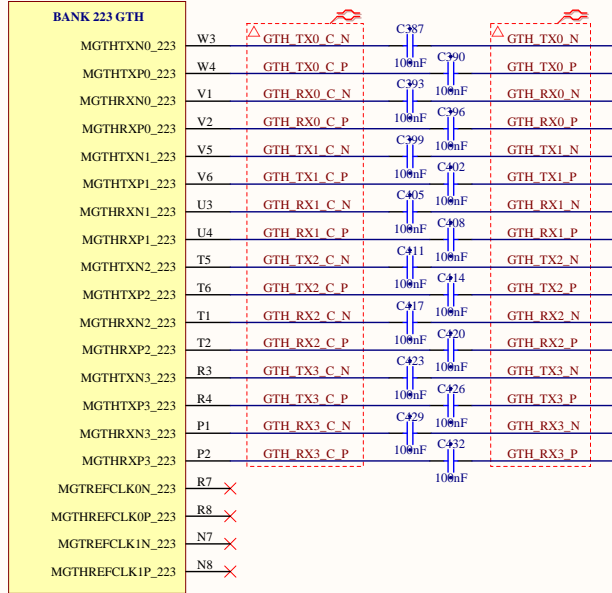
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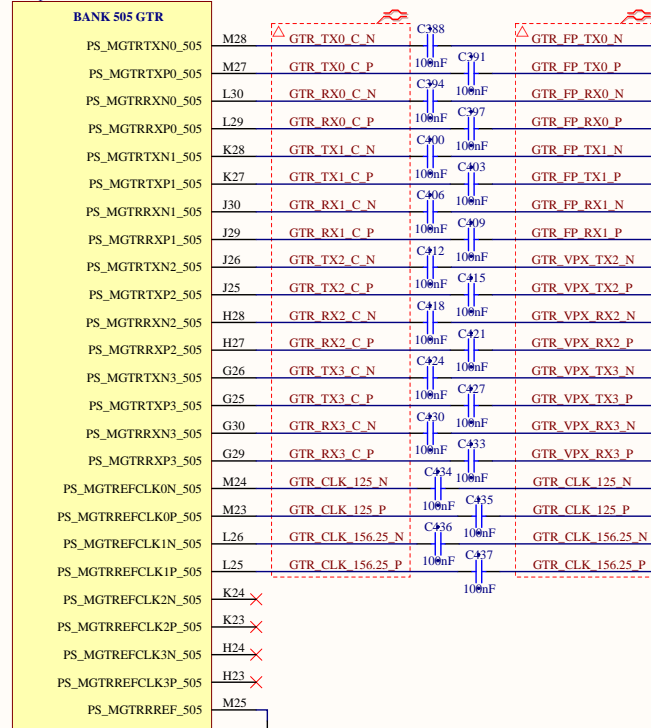


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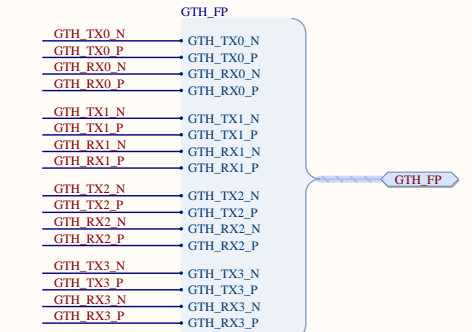
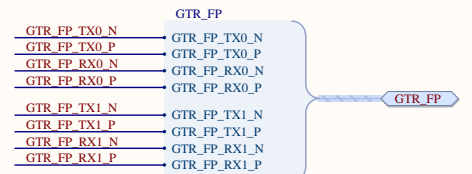
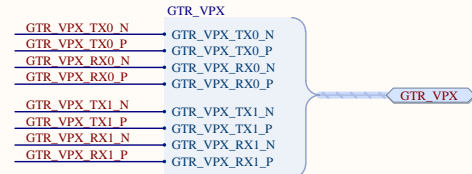


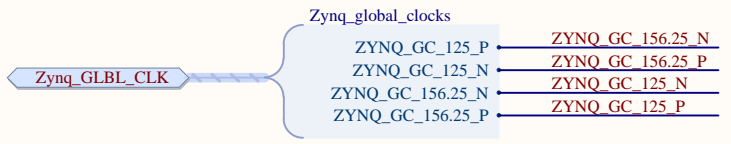
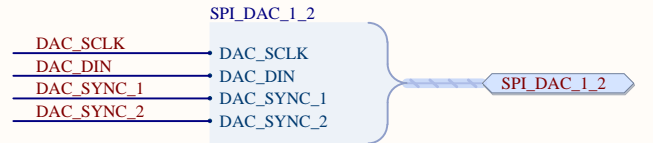
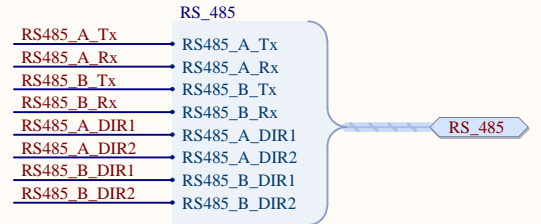
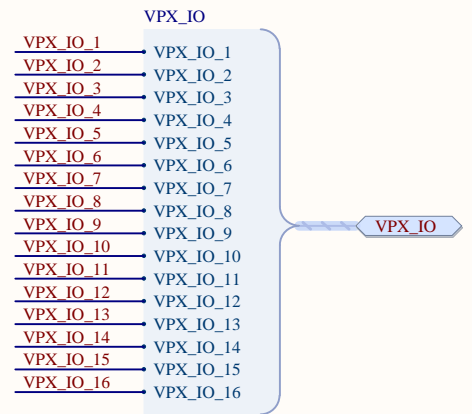
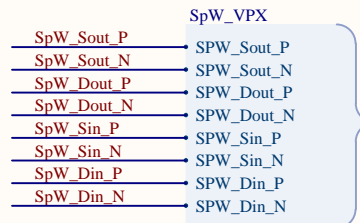
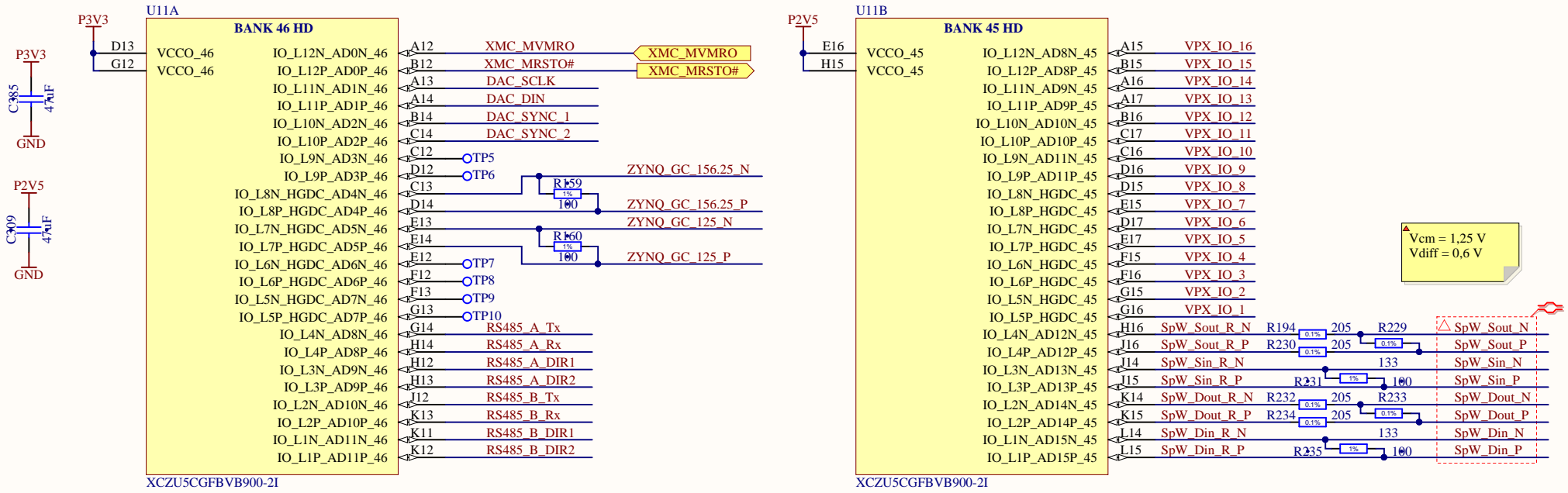
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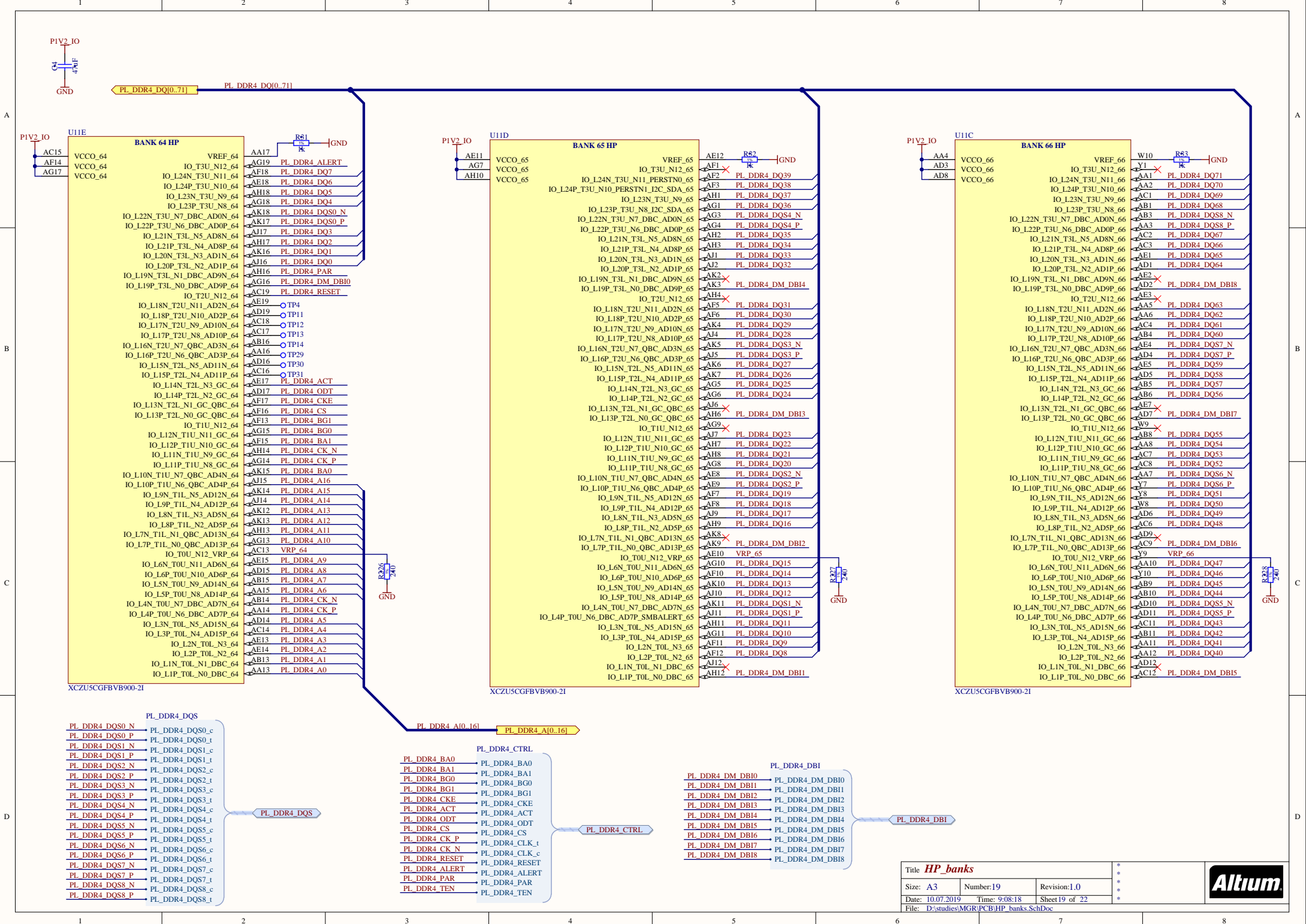
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File: D:\studies\MGR\PCB\HD_banks.SchDoc			*





- BANK 64 HP**
- VCC0_64 VREF_64
 AC15 IO_T3U_N12_64
 AF14 IO_L24N_T3U_N11_64
 AG17 IO_L24P_T3U_N10_64
 IO_L23N_T3U_N9_64
 IO_L23P_T3U_N8_64
 IO_L22N_T3U_N7_DBC_AD0N_64
 IO_L22P_T3U_N6_DBC_AD0P_64
 IO_L21N_T3L_N5_AD8N_64
 IO_L21P_T3L_N4_AD8P_64
 IO_L20N_T3L_N3_AD1N_64
 IO_L20P_T3L_N2_AD1P_64
 IO_L19N_T3L_N1_DBC_AD9N_64
 IO_L19P_T3L_N0_DBC_AD9P_64
 IO_T2U_N12_64
 IO_L18N_T2U_N11_AD2N_64
 IO_L18P_T2U_N10_AD2P_64
 IO_L17N_T2U_N9_AD10N_64
 IO_L17P_T2U_N8_AD10P_64
 IO_L16N_T2U_N7_QBC_AD3N_64
 IO_L16P_T2U_N6_QBC_AD3P_64
 IO_L15N_T2L_N5_AD11N_64
 IO_L15P_T2L_N4_AD11P_64
 IO_L14N_T2L_N3_GC_64
 IO_L14P_T2L_N2_GC_64
 IO_L13N_T2L_N1_GC_QBC_64
 IO_L13P_T2L_N0_GC_QBC_64
 IO_T1U_N12_64
 IO_L12N_T1U_N11_GC_64
 IO_L12P_T1U_N10_GC_64
 IO_L11N_T1U_N9_GC_64
 IO_L11P_T1U_N8_GC_64
 IO_L10N_T1U_N7_QBC_AD4N_64
 IO_L10P_T1U_N6_QBC_AD4P_64
 IO_L9N_T1L_N5_AD12N_64
 IO_L9P_T1L_N4_AD12P_64
 IO_L8N_T1L_N3_ADSN_64
 IO_L8P_T1L_N2_ADS5_64
 IO_L7N_T1L_N1_QBC_AD13N_64
 IO_L7P_T1L_N0_QBC_AD13P_64
 IO_T0U_N12_VRP_64
 IO_L6N_T0U_N11_AD6N_64
 IO_L6P_T0U_N10_AD6P_64
 IO_L5N_T0U_N9_AD14N_64
 IO_L5P_T0U_N8_AD14P_64
 IO_L4N_T0U_N7_DBC_AD7N_64
 IO_L4P_T0U_N6_DBC_AD7P_64
 IO_L3N_T0L_N5_AD15N_64
 IO_L3P_T0L_N4_AD15P_64
 IO_L2N_T0L_N3_64
 IO_L2P_T0L_N2_64
 IO_L1N_T0L_N1_DBC_64
 IO_L1P_T0L_N0_DBC_64

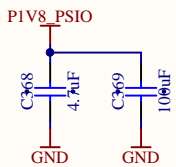
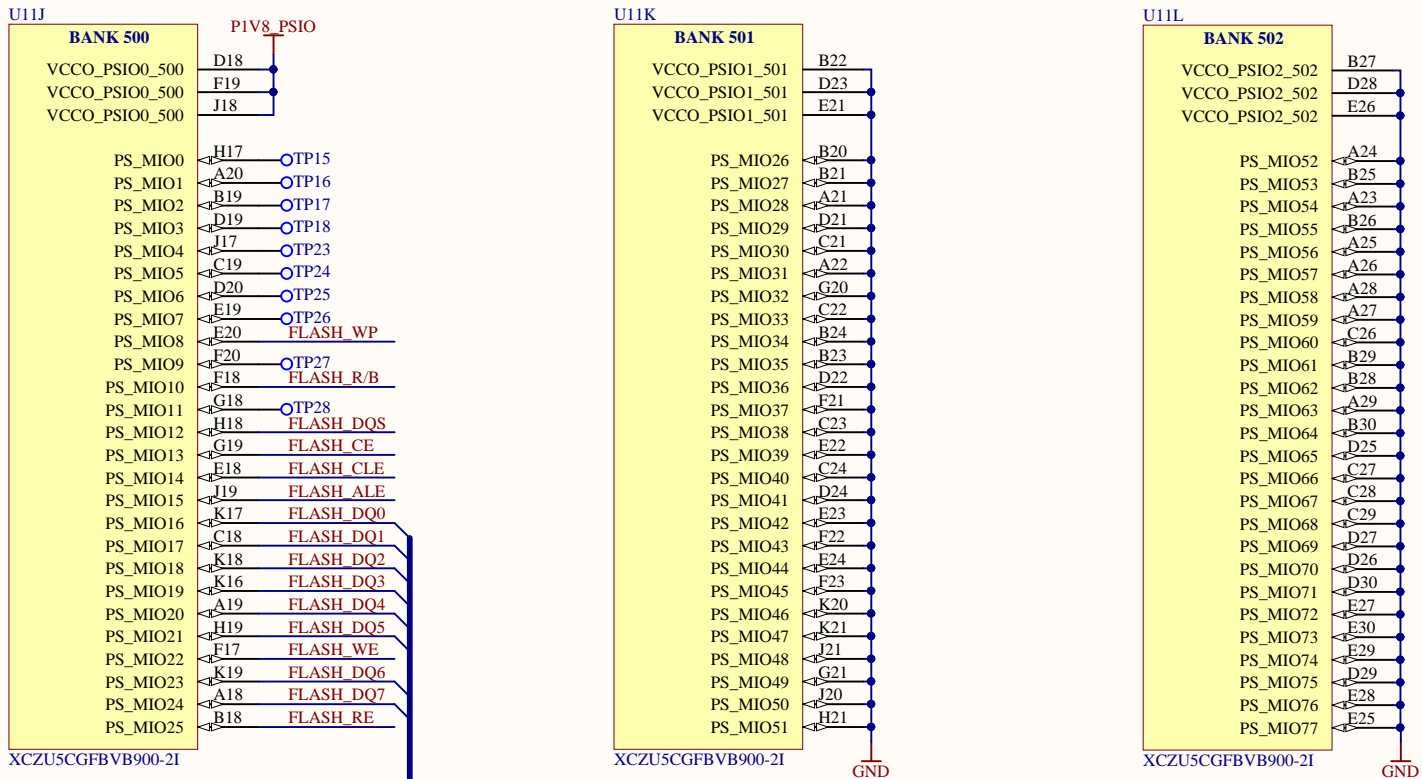
- BANK 65 HP**
- VCC0_65 VREF_65
 AE11 IO_T3U_N12_65
 AG7 IO_L24N_T3U_N11_PERSTN0_65
 AH10 IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65
 IO_L23N_T3U_N9_65
 IO_L23P_T3U_N8_I2C_SDA_65
 IO_L22N_T3U_N7_DBC_AD0N_65
 IO_L22P_T3U_N6_DBC_AD0P_65
 IO_L21N_T3L_N5_AD8N_65
 IO_L21P_T3L_N4_AD8P_65
 IO_L20N_T3L_N3_AD1N_65
 IO_L20P_T3L_N2_AD1P_65
 IO_L19N_T3L_N1_DBC_AD9N_65
 IO_L19P_T3L_N0_DBC_AD9P_65
 IO_T2U_N12_65
 IO_L18N_T2U_N11_AD2N_65
 IO_L18P_T2U_N10_AD2P_65
 IO_L17N_T2U_N9_AD10N_65
 IO_L17P_T2U_N8_AD10P_65
 IO_L16N_T2U_N7_QBC_AD3N_65
 IO_L16P_T2U_N6_QBC_AD3P_65
 IO_L15N_T2L_N5_AD11N_65
 IO_L15P_T2L_N4_AD11P_65
 IO_L14N_T2L_N3_GC_65
 IO_L14P_T2L_N2_GC_65
 IO_L13N_T2L_N1_GC_QBC_65
 IO_L13P_T2L_N0_GC_QBC_65
 IO_T1U_N12_65
 IO_L12N_T1U_N11_GC_65
 IO_L12P_T1U_N10_GC_65
 IO_L11N_T1U_N9_GC_65
 IO_L11P_T1U_N8_GC_65
 IO_L10N_T1U_N7_QBC_AD4N_65
 IO_L10P_T1U_N6_QBC_AD4P_65
 IO_L9N_T1L_N5_AD12N_65
 IO_L9P_T1L_N4_AD12P_65
 IO_L8N_T1L_N3_ADSN_65
 IO_L8P_T1L_N2_ADS5_65
 IO_L7N_T1L_N1_QBC_AD13N_65
 IO_L7P_T1L_N0_QBC_AD13P_65
 IO_T0U_N12_VRP_65
 IO_L6N_T0U_N11_AD6N_65
 IO_L6P_T0U_N10_AD6P_65
 IO_L5N_T0U_N9_AD14N_65
 IO_L5P_T0U_N8_AD14P_65
 IO_L4N_T0U_N7_DBC_AD7N_65
 IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65
 IO_L3N_T0L_N5_AD15N_65
 IO_L3P_T0L_N4_AD15P_65
 IO_L2N_T0L_N3_65
 IO_L2P_T0L_N2_65
 IO_L1N_T0L_N1_DBC_65
 IO_L1P_T0L_N0_DBC_65

- BANK 66 HP**
- VCC0_66 VREF_66
 AA4 IO_T3U_N12_66
 AD3 IO_L24N_T3U_N11_66
 AD8 IO_L24P_T3U_N10_66
 IO_L23N_T3U_N9_66
 IO_L23P_T3U_N8_66
 IO_L22N_T3U_N7_DBC_AD0N_66
 IO_L22P_T3U_N6_DBC_AD0P_66
 IO_L21N_T3L_N5_AD8N_66
 IO_L21P_T3L_N4_AD8P_66
 IO_L20N_T3L_N3_AD1N_66
 IO_L20P_T3L_N2_AD1P_66
 IO_L19N_T3L_N1_DBC_AD9N_66
 IO_L19P_T3L_N0_DBC_AD9P_66
 IO_T2U_N12_66
 IO_L18N_T2U_N11_AD2N_66
 IO_L18P_T2U_N10_AD2P_66
 IO_L17N_T2U_N9_AD10N_66
 IO_L17P_T2U_N8_AD10P_66
 IO_L16N_T2U_N7_QBC_AD3N_66
 IO_L16P_T2U_N6_QBC_AD3P_66
 IO_L15N_T2L_N5_AD11N_66
 IO_L15P_T2L_N4_AD11P_66
 IO_L14N_T2L_N3_GC_66
 IO_L14P_T2L_N2_GC_66
 IO_L13N_T2L_N1_GC_QBC_66
 IO_L13P_T2L_N0_GC_QBC_66
 IO_T1U_N12_66
 IO_L12N_T1U_N11_GC_66
 IO_L12P_T1U_N10_GC_66
 IO_L11N_T1U_N9_GC_66
 IO_L11P_T1U_N8_GC_66
 IO_L10N_T1U_N7_QBC_AD4N_66
 IO_L10P_T1U_N6_QBC_AD4P_66
 IO_L9N_T1L_N5_AD12N_66
 IO_L9P_T1L_N4_AD12P_66
 IO_L8N_T1L_N3_ADSN_66
 IO_L8P_T1L_N2_ADS5_66
 IO_L7N_T1L_N1_QBC_AD13N_66
 IO_L7P_T1L_N0_QBC_AD13P_66
 IO_T0U_N12_VRP_66
 IO_L6N_T0U_N11_AD6N_66
 IO_L6P_T0U_N10_AD6P_66
 IO_L5N_T0U_N9_AD14N_66
 IO_L5P_T0U_N8_AD14P_66
 IO_L4N_T0U_N7_DBC_AD7N_66
 IO_L4P_T0U_N6_DBC_AD7P_66
 IO_L3N_T0L_N5_AD15N_66
 IO_L3P_T0L_N4_AD15P_66
 IO_L2N_T0L_N3_66
 IO_L2P_T0L_N2_66
 IO_L1N_T0L_N1_DBC_66
 IO_L1P_T0L_N0_DBC_66

- PL_DDR4_DQS**
- PL_DDR4_DQS0_N
 - PL_DDR4_DQS0_P
 - PL_DDR4_DQS1_N
 - PL_DDR4_DQS1_P
 - PL_DDR4_DQS2_N
 - PL_DDR4_DQS2_P
 - PL_DDR4_DQS3_N
 - PL_DDR4_DQS3_P
 - PL_DDR4_DQS4_N
 - PL_DDR4_DQS4_P
 - PL_DDR4_DQS5_N
 - PL_DDR4_DQS5_P
 - PL_DDR4_DQS6_N
 - PL_DDR4_DQS6_P
 - PL_DDR4_DQS7_N
 - PL_DDR4_DQS7_P
 - PL_DDR4_DQS8_N
 - PL_DDR4_DQS8_P

- PL_DDR4_CTRL**
- PL_DDR4_BA0
 - PL_DDR4_BA1
 - PL_DDR4_BG0
 - PL_DDR4_BG1
 - PL_DDR4_CKE
 - PL_DDR4_ACT
 - PL_DDR4_ODT
 - PL_DDR4_CS
 - PL_DDR4 CK_P
 - PL_DDR4 CK_N
 - PL_DDR4 RESET
 - PL_DDR4_ALERT
 - PL_DDR4_PAR
 - PL_DDR4_TEN

- PL_DDR4_DBI**
- PL_DDR4_DM_DBI0
 - PL_DDR4_DM_DBI1
 - PL_DDR4_DM_DBI2
 - PL_DDR4_DM_DBI3
 - PL_DDR4_DM_DBI4
 - PL_DDR4_DM_DBI5
 - PL_DDR4_DM_DBI6
 - PL_DDR4_DM_DBI7
 - PL_DDR4_DM_DBI8



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