



# Experiment Control with the ARTIQ/DAX Control Ecosystem

Paweł Kulik  
Mikołaj Sowiński  
Tomasz Przywózki

IEEE International Conference on Quantum Computing and Engineering - QCE24 Montreal



# About us

**The Faculty of Electronics and Information Technology**

**Warsaw University of Technology**

- **Electronics for High Energy and Quantum Physics research group**

<https://github.com/elhep>

- **Sinara Open-Hardware Project**

<https://github.com/sinara-hw/>

## Disclaimer

ARTIQ is originally authored by

*Bourdeauducq, Sébastien et al. (2016). ARTIQ 1.0. Zenodo. 10.5281/zenodo.51303*

and currently is maintained and developed by M-Labs with and the community.

# Organization

Slides and source codes

[https://github.com/elhep/artiq\\_dax\\_tutorial\\_materials](https://github.com/elhep/artiq_dax_tutorial_materials)

ARTIQ7 manual (used for this tutorial):

<https://m-labs.hk/artiq/manual-legacy/introduction.html>

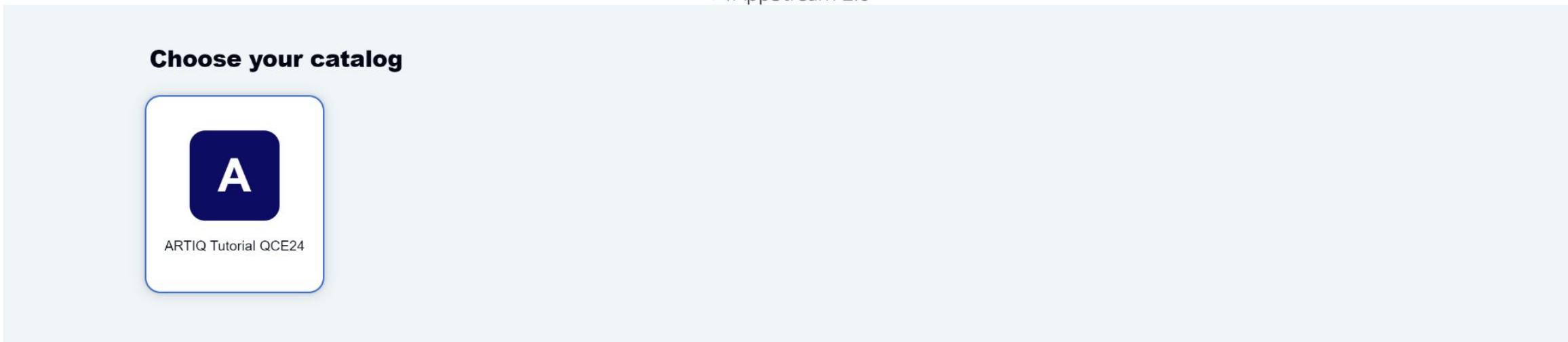
# Organization

Connect to virtual desktop using your personal link

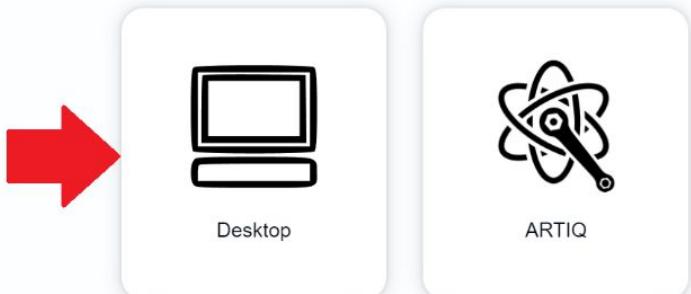


# Organization

1. Connect to virtual desktop using your personal link

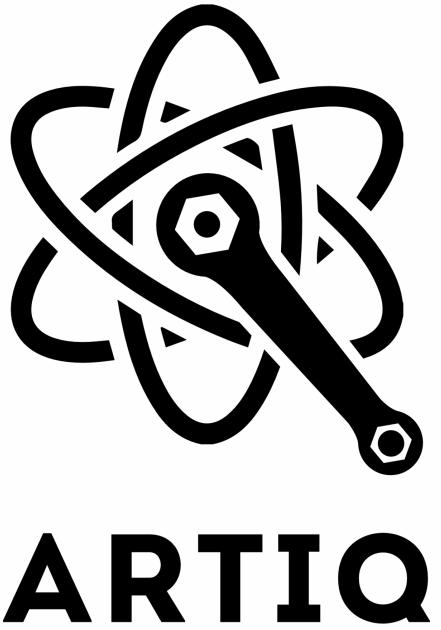


**Choose your application to get started**



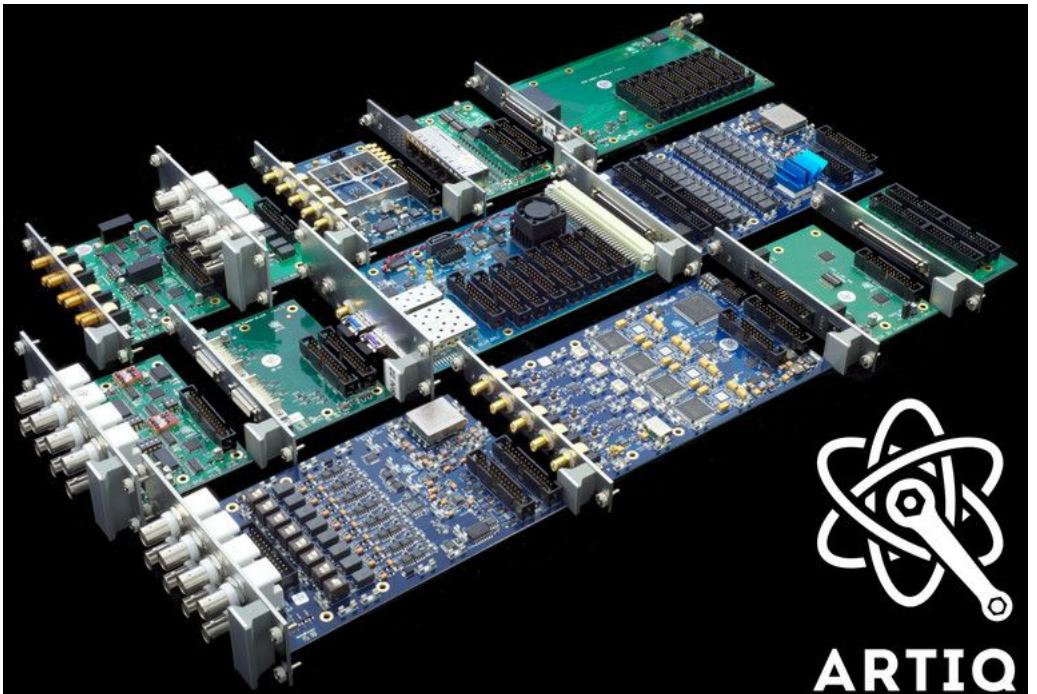
# Glossary

- ARTIQ - Advanced Real-Time Infrastructure for Quantum physics



# Glossary

- ARTIQ
- Sinara - Hardware designed for ARTIQ



# Glossary

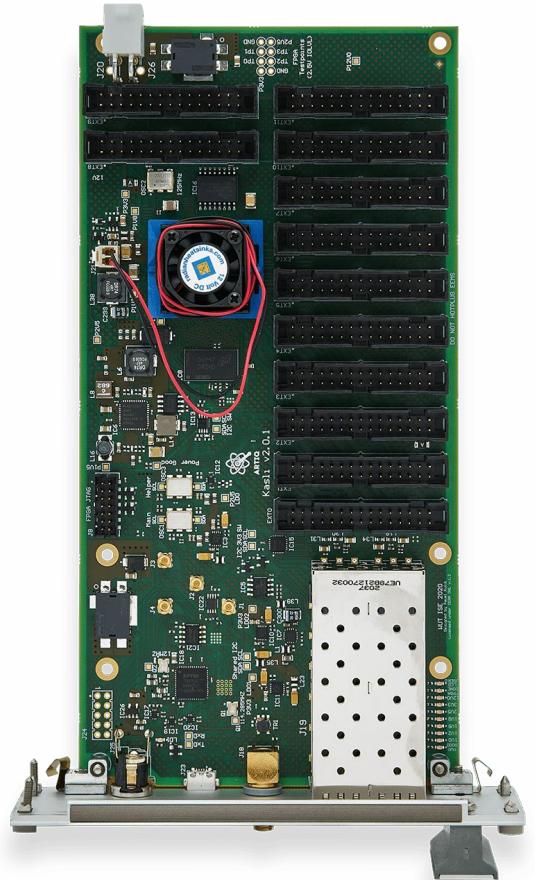
- ARTIQ
- Sinara
- DAX - Duke ARTIQ Extensions

# Glossary

- ARTIQ
- Sinara
- DAX
- (D)RTIO – (Distributed) Real Time Input/Output

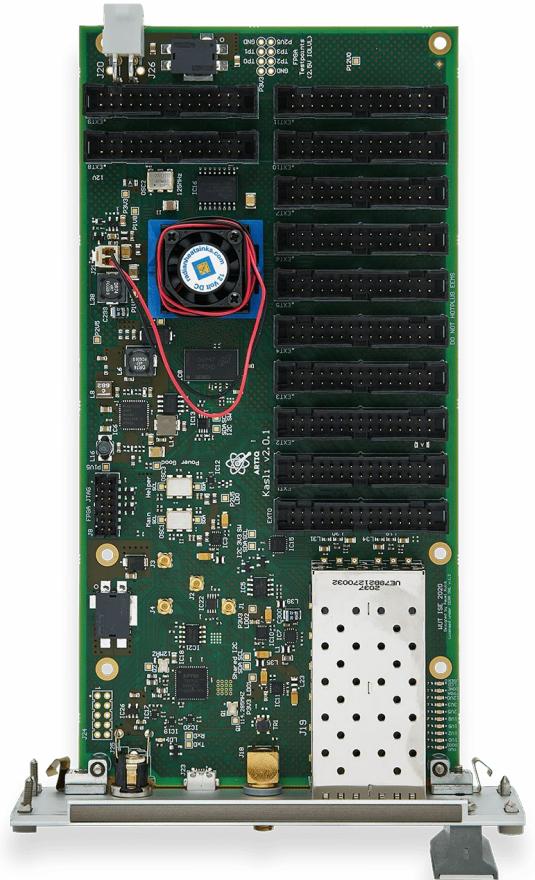
# Glossary

- ARTIQ
- Sinara
- DAX
- (D)RTIO
- Controller



# Glossary

- ARTIQ
- Sinara
- DAX
- (D)RTIO
- Controller
- Satellite - secondary controller



# Glossary

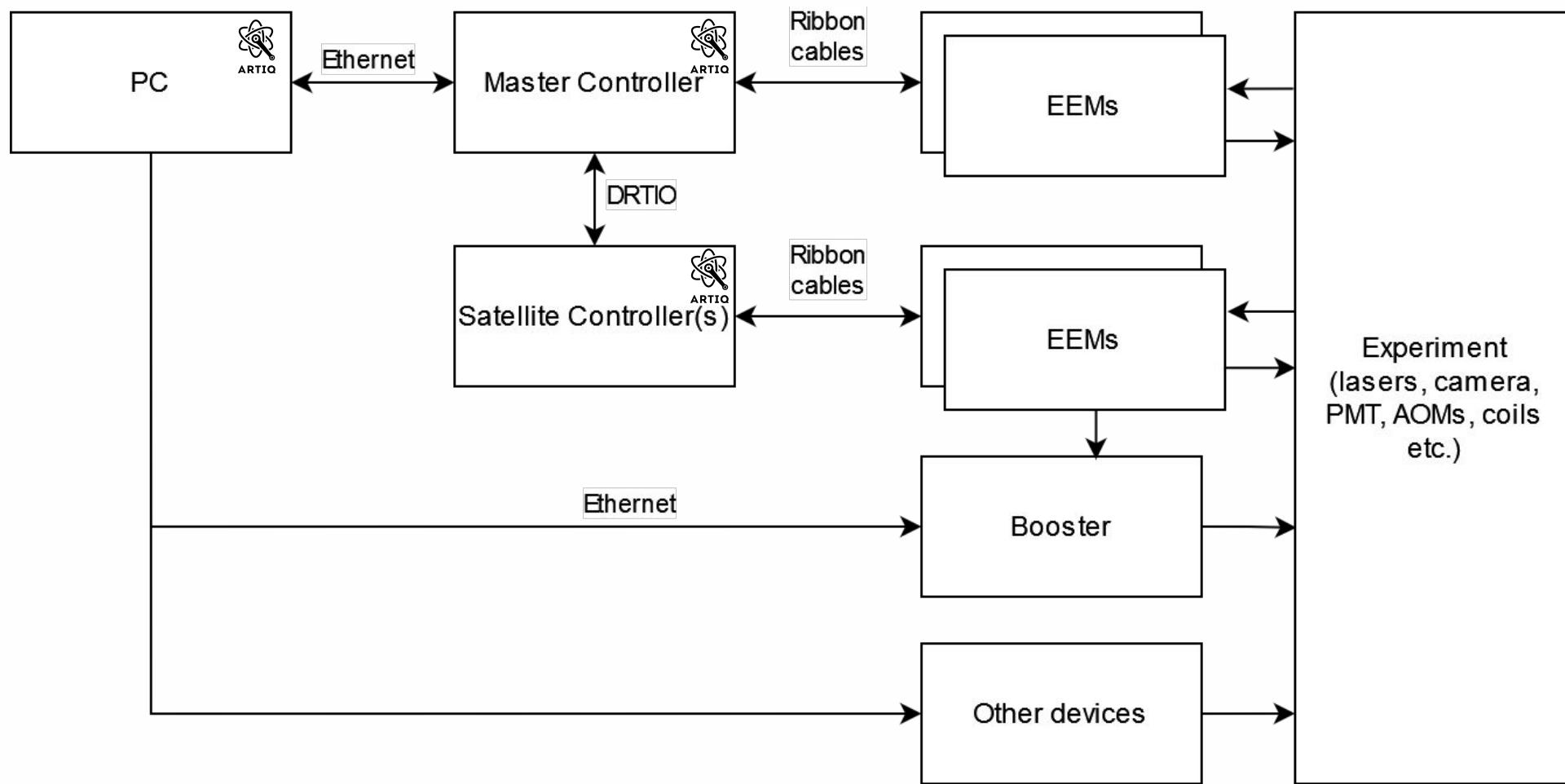
- ARTIQ
- Sinara
- DAX
- (D)RTIO
- Controller
- Satellite
- Gateware - firmware for the FPGA



# Glossary

- ARTIQ
- Sinara
- DAX
- (D)RTIO
- Controller
- Satellite
- Gateware
- hard real-time - all or nothing

# ARTIQ system architecture



# What does ARTIQ code look like?

- Python
- Build stage
- Run stage
- Analyze stage

```
7   class SystemExample(EnvExperiment):
8       def build(self):
9           self.setattr_device("core")
10          self.setattr_device("core_dma")
11          self.fastino = [self.get_device("fastino" + str(i)) for i in range(3)]
12          n = 1 << 11
13          self.signal = [[0] * 16 for _ in range(n)]
14          self.signal2 = [[0] * 16 for _ in range(n)]
15          for i in range(n):
16              self.fastino[0].voltage_group_to_mu([4*np.sin(200*np.pi*i/n])*32, self.signal[i])
17          for i in range(n):
18              self.fastino[0].voltage_group_to_mu([19.9*(i % 2)-9.95]*32, self.signal2[i])
19
20
21      @kernel
22      def run(self):
23          self.core.break_realtime()
24          self.core.reset()
25          self.init()
26          self.core.break_realtime()
27
28          # No interpolation
29          self.record_waveform()
30          self.play_waveform()
31
32      @kernel
33      def init(self):
34          for fastino in self.fastino:
35              fastino.init()
36              fastino.set_hold(0xffffffff)
37              delay(8*ns)
38              fastino.set_group(0, [0.*V]*32)
39              delay(1*us)
40              fastino.update(0xffffffff)
41              delay(10*ms)
42          self.core.break_realtime()
43
44      @kernel
45      def record_waveform(self):
46          with self.core_dma.record("fastino_direct"):
47              for i in range(len(self.signal)):
48                  t = now_mu()
49                  with parallel:
50                      self.fastino[0].set_group_mu(0, self.signal[i])
51                      self.fastino[1].set_group_mu(0, self.signal[i])
52                      self.fastino[2].set_group_mu(0, self.signal[i])
53                  at_mu(t+self.core.seconds_to_mu(32*8*ns))
54                  with parallel:
55                      self.fastino[0].update(0xffffffff)
56                      self.fastino[1].update(0xffffffff)
57                      self.fastino[2].update(0xffffffff)
58
59                  # Frame period is 392 ns - we have to align to it to have predictable updates
60                  at_mu(t+self.core.seconds_to_mu(392*1*ns))
61
62          self.core.break_realtime()
63
64      @kernel
65      def play_waveform(self):
66          dma_handle = self.core_dma.get_handle("fastino_direct")
67          self.core.break_realtime()
68          for _ in range(10):
69              self.core_dma.playback_handle(dma_handle)
70
71      @kernel
72      def fastino_output(self, voltage):
73          # Set all Fastino channels to some voltage, starting from input parameter and incrementing by 0.2 V
74          for i in range(32):
75              self.fastino[0].set_dac(i, voltage + 0.2 * i)
76              delay(100 * us)
77              self.fastino[1].set_dac(i, voltage + 0.2 * i)
78              delay(100 * us)
79              self.fastino[2].set_dac(i, voltage + 0.2 * i)
80              delay(100 * us)
81
82              self.fastino[0].update(0xffffffff)
83              self.fastino[1].update(0xffffffff)
84
85      def analyze(self):
86          pass
```

# What does ARTIQ code look like?

- Python
- Build stage
  - Declare devices
  - Add arguments
  - Precalculate variables

```
7   class SystemExample(EnvExperiment):
8       def build(self):
9           self.setattr_device("core")
10          self.setattr_device("core_dma")
11          self.fastino = [self.get_device("fastino" + str(i)) for i in range(3)]
12          n = 1 << 11
13          self.signal = [[0] * 16 for _ in range(n)]
14          self.signal2 = [[0] * 16 for _ in range(n)]
15          for i in range(n):
16              self.fastino[0].voltage_group_to_mu([4*np.sin(200*np.pi*i/n])*32, self.signal[i])
17          for i in range(n):
18              self.fastino[0].voltage_group_to_mu([19.9*(i % 2)-9.95]*32, self.signal2[i])
19
20
21      @kernel
22      def run(self):
23          self.core.break_realtime()
24          self.core.reset()
25          self.init()
26          self.core.break_realtime()
27
28          # No interpolation
29          self.record_waveform()
30          self.play_waveform()
31
32      @kernel
33      def init(self):
34          for fastino in self.fastino:
35              fastino.init()
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61          self.core.break_realtime()
62
63
64      @kernel
65      def play_waveform(self):
66          dma_handle = self.core_dma.get_handle("fastino_direct")
67          self.core.break_realtime()
68          for _ in range(10):
69              self.core_dma.playback_handle(dma_handle)
70
71
72      @kernel
73      def fastino_output(self, voltage):
74          # Set all Fastino channels to some voltage, starting from input parameter and incrementing by 0.2 V
75          for i in range(32):
76              self.fastino[0].set_dac(i, voltage + 0.2 * i)
77              delay(100 * us)
78              self.fastino[1].set_dac(i, voltage + 0.2 * i)
79              delay(100 * us)
80              self.fastino[2].set_dac(i, voltage + 0.2 * i)
81              delay(100 * us)
82
83          self.fastino[0].update(0xffffffff)
84          self.fastino[1].update(0xffffffff)
85
86      def analyze(self):
87          pass
```

# What does ARTIQ code look like?

- Python
- Build stage
- Run stage
  - Access to the FPGA
  - Hard real-time on the FPGA
  - RPC between PC and the FPGA

```
20
21 @kernel
22 def run(self):
23     self.core.break_realtime()
24     self.core.reset()
25     self.init()
26     self.core.break_realtime()
27
28     # No interpolation
29     self.record_waveform()
30     self.play_waveform()
31
32 @kernel
33 def init(self):
34     for fastino in self.fastino:
35         fastino.init()
36         fastino.set_hold(0xffffffff)
37         delay(8*ns)
38         fastino.set_group(0, [0.*V]*32)
39         delay(1*us)
40         fastino.update(0xffffffff)
41         delay(10*ms)
42         self.core.break_realtime()
```

```
7
8 class SystemExample(EnvExperiment):
9     def build(self):
10         self.setattr_device("core")
11         self.setattr_device("core_dma")
12         self.fastino = [self.get_device("fastino" + str(i)) for i in range(3)]
13         n = 1 << 11
14         self.signal = [[0] * 16 for _ in range(n)]
15         self.signal2 = [[0] * 16 for _ in range(n)]
16         for i in range(n):
17             self.fastino[0].voltage_group_to_mu([4*np.sin(200*np.pi*i/n])*32, self.signal[i])
18         for i in range(n):
19             self.fastino[0].voltage_group_to_mu([19.9*(i % 2)-9.95]*32, self.signal2[i])
20
21     @kernel
22     def run(self):
23         self.core.break_realtime()
24         self.core.reset()
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
639
640
641
642
643
644
645
646
647
648
649
649
650
651
652
653
654
655
656
657
658
659
659
660
661
662
663
664
665
666
667
668
669
669
670
671
672
673
674
675
676
677
678
679
679
680
681
682
683
684
685
686
687
687
688
689
689
690
691
692
693
694
695
696
697
697
698
699
699
700
701
702
703
704
705
706
707
708
709
709
710
711
712
713
714
715
716
717
718
719
719
720
721
722
723
724
725
726
727
728
729
729
730
731
732
733
734
735
736
737
737
738
739
739
740
741
742
743
744
745
745
746
747
747
748
749
749
750
751
752
753
754
755
756
756
757
758
758
759
759
760
761
762
763
764
765
765
766
766
767
767
768
768
769
769
770
771
772
773
774
775
775
776
776
777
777
778
778
779
779
780
781
782
783
784
784
785
785
786
786
787
787
788
788
789
789
790
791
792
793
794
795
795
796
796
797
797
798
798
799
799
800
801
802
803
804
805
806
807
808
809
809
810
810
811
811
812
812
813
813
814
814
815
815
816
816
817
817
818
818
819
819
820
820
821
821
822
822
823
823
824
824
825
825
826
826
827
827
828
828
829
829
830
830
831
831
832
832
833
833
834
834
835
835
836
836
837
837
838
838
839
839
840
840
841
841
842
842
843
843
844
844
845
845
846
846
847
847
848
848
849
849
850
850
851
851
852
852
853
853
854
854
855
855
856
856
857
857
858
858
859
859
860
860
861
861
862
862
863
863
864
864
865
865
866
866
867
867
868
868
869
869
870
870
871
871
872
872
873
873
874
874
875
875
876
876
877
877
878
878
879
879
880
880
881
881
882
882
883
883
884
884
885
885
886
886
887
887
888
888
889
889
890
890
891
891
892
892
893
893
894
894
895
895
896
896
897
897
898
898
899
899
900
900
901
901
902
902
903
903
904
904
905
905
906
906
907
907
908
908
909
909
910
910
911
911
912
912
913
913
914
914
915
915
916
916
917
917
918
918
919
919
920
920
921
921
922
922
923
923
924
924
925
925
926
926
927
927
928
928
929
929
930
930
931
931
932
932
933
933
934
934
935
935
936
936
937
937
938
938
939
939
940
940
941
941
942
942
943
943
944
944
945
945
946
946
947
947
948
948
949
949
950
950
951
951
952
952
953
953
954
954
955
955
956
956
957
957
958
958
959
959
960
960
961
961
962
962
963
963
964
964
965
965
966
966
967
967
968
968
969
969
970
970
971
971
972
972
973
973
974
974
975
975
976
976
977
977
978
978
979
979
980
980
981
981
982
982
983
983
984
984
985
985
986
986
987
987
988
988
989
989
990
990
991
991
992
992
993
993
994
994
995
995
996
996
997
997
998
998
999
999
1000
1000
1001
1001
1002
1002
1003
1003
1004
1004
1005
1005
1006
1006
1007
1007
1008
1008
1009
1009
1010
1010
1011
1011
1012
1012
1013
1013
1014
1014
1015
1015
1016
1016
1017
1017
1018
1018
1019
1019
1020
1020
1021
1021
1022
1022
1023
1023
1024
1024
1025
1025
1026
1026
1027
1027
1028
1028
1029
1029
1030
1030
1031
1031
1032
1032
1033
1033
1034
1034
1035
1035
1036
1036
1037
1037
1038
1038
1039
1039
1040
1040
1041
1041
1042
1042
1043
1043
1044
1044
1045
1045
1046
1046
1047
1047
1048
1048
1049
1049
1050
1050
1051
1051
1052
1052
1053
1053
1054
1054
1055
1055
1056
1056
1057
1057
1058
1058
1059
1059
1060
1060
1061
1061
1062
1062
1063
1063
1064
1064
1065
1065
1066
1066
1067
1067
1068
1068
1069
1069
1070
1070
1071
1071
1072
1072
1073
1073
1074
1074
1075
1075
1076
1076
1077
1077
1078
1078
1079
1079
1080
1080
1081
1081
1082
1082
1083
1083
1084
1084
1085
1085
1086
1086
1087
1087
1088
1088
1089
1089
1090
1090
1091
1091
1092
1092
1093
1093
1094
1094
1095
1095
1096
1096
1097
1097
1098
1098
1099
1099
1100
1100
1101
1101
1102
1102
1103
1103
1104
1104
1105
1105
1106
1106
1107
1107
1108
1108
1109
1109
1110
1110
1111
1111
1112
1112
1113
1113
1114
1114
1115
1115
1116
1116
1117
1117
1118
1118
1119
1119
1120
1120
1121
1121
1122
1122
1123
1123
1124
1124
1125
1125
1126
1126
1127
1127
1128
1128
1129
1129
1130
1130
1131
1131
1132
1132
1133
1133
1134
1134
1135
1135
1136
1136
1137
1137
1138
1138
1139
1139
1140
1140
1141
1141
1142
1142
1143
1143
1144
1144
1145
1145
1146
1146
1147
1147
1148
1148
1149
1149
1150
1150
1151
1151
1152
1152
1153
1153
1154
1154
1155
1155
1156
1156
1157
1157
1158
1158
1159
1159
1160
1160
1161
1161
1162
1162
1163
1163
1164
1164
1165
1165
1166
1166
1167
1167
1168
1168
1169
1169
1170
1170
1171
1171
1172
1172
1173
1173
1174
1174
1175
1175
1176
1176
1177
1177
1178
1178
1179
1179
1180
1180
1181
1181
1182
1182
1183
1183
1184
1184
1185
1185
1186
1186
1187
1187
1188
1188
1189
1189
1190
1190
1191
1191
1192
1192
1193
1193
1194
1194
1195
1195
1196
1196
1197
1197
1198
1198
1199
1199
1200
1200
1201
1201
1202
1202
1203
1203
1204
1204
1205
1205
1206
1206
1207
1207
1208
1208
1209
1209
1210
1210
1211
1211
1212
1212
1213
1213
1214
1214
1215
1215
1216
1216
1217
1217
1218
1218
1219
1219
1220
1220
1221
1221
1222
1222
1223
1223
1224
1224
1225
1225
1226
1226
1227
1227
1228
1228
1229
1229
1230
1230
1231
1231
1232
1232
1233
1233
1234
1234
1235
1235
1236
1236
1237
1237
1238
1238
1239
1239
1240
1240
1241
1241
1242
1242
1243
1243
1244
1244
1245
1245
1246
1246
1247
1247
1248
1248
1249
1249
1250
1250
1251
1251
1252
1252
1253
1253
1254
1254
1255
1255
1256
1256
1257
1257
1258
1258
1259
1259
1260
1260
1261
1261
1262
1262
1263
1263
1264
1264
1265
1265
1266
1266
1267
1267
1268
1268
1269
1269
1270
1270
1271
1271
1272
1272
1273
1273
1274
1274
1275
1275
1276
1276
1277
1277
1278
1278
1279
1279
1280
1280
1281
1281
1282
1282
1283
1283
1284
1284
1285
1285
1286
1286
1287
1287
1288
1288
1289
1289
1290
1290
1291
1291
1292
1292
1293
1293
1294
1294
1295
1295
1296
1296
1297
1297
1298
1298
1299
1299
1300
1300
1301
1301
1302
1302
1303
1303
1304
1304
1305
1305
1306
1306
1307
1307
1308
1308
1309
1309
1310
1310
1311
1311
1312
1312
1313
1313
1314
1314
1315
1315
1316
1316
1317
1317
1318
1318
1319
1319
1320
1320
1321
1321
1322
1322
1323
1323
1324
1324
1325
1325
1326
1326
1327
1327
1328
1328
1329
1329
1330
1330
1331
1331
1332
1332
1333
1333
1334
1334
1335
1335
1336
1336
1337
1337
1338
1338
1339
1339
1340
1340
1341
1341
1342
1342
1343
1343
1344
1344
1345
1345
1346
1346
1347
1347
1348
1348
1349
1349
1350
1350
1351
1351
1352
1352
1353
1353
1354
1354
1355
1355
1356
1356
1357
1357
1358
1358
1359
1359
1360
1360
1361
1361
1362
1362
1363
1363
1364
1364
1365
1365
1366
1366
1367
1367
1368
1368
1369
1369
1370
1370
1371
1371
1372
1372
1373
1373
1374
1374
1375
1375
1376
1376
1377
1377
1378
1378
1379
1379
1380
1380
1381
1381
1382
1382
1383
1383
1384
1384
1385
1385
1386
1386
1387
1387
1388
1388
1389
1389
1390
1390
1391
1391
1392
1392
1393
1393
1394
1394
1395
1395
1396
1396
1397
1397
1398
1398
1399
1399
1400
1400
1401
1401
1402
1402
1403
1403
1404
1404
1405
1405
1406
1406
1407
1407
1408
1408
1409
1409
1410
1410
1411
1411
1412
1412
1413
1413
1414
1414
1415
1415
1416
1416
1417
1417
1418
1418
1419
1419
1420
1420
1421
1421
1422
1422
1423
1423
1424
1424
1425
1425
1426
1426
1427
1427
1428
1428
1429
1429
1430
1430
1431
1431
1432
1432
1433
1433
1434
1434
1435
1435
1436
1436
1437
1437
1438
1438
1439
1439
1440
1440
1441
1441
1442
1442
1443
1443
1444
1444
1445
1445
1446
1446
1447
1447
1448
1448
1449
1449
1450
1450
1451
1451
1452
1452
1453
1453
1454
1454
1455
1455
1456
1456
1457
1457
1458
1458
1459
1459
1460
1460
1461
1461
1462
1462
1463
1463
1464
1464
1465
1465
1466
1466
1467
1467
1468
1468
1469
1469
1470
1470
1471
1471
1472
1472
1473
1473
1474
1474
1475
1475
1476
1476
1477
1477
1478
1478
1479
1479
1480
1480
1481
1481
1482
1482
1483
1483
1484
1484
1485
1485
1486
1486
1487
1487
1488
1488
1489
1489
1490
1490
1491
1491
1492
1492
1493
1493
1494
1494
1495
1495
1496
1496
1497
1497
1498
1498
1499
1499
1500
1500
1501
1501
1502
1502
1503
1503
1504
1504
1505
1505
1506
1506
1507
1507
1508
1508
1509
1509
1510
1510
1511
1511
1512
1512
1513
1513
1514
1514
1515
1515
1516
1516
1517
1517
1518
1518
1519
1519
1520
1520
1521
1521
1522
1522
1523
1523
1524
1524
1525
1525
1526
1526
1527
1527
1528
1528
1529
1529
1530
1530
1531
1531
1532
1532
1533
1533
1534
1534
1535
1535
1536
1536
1537
1537
1538
1538
1539
1539
1540
1540
1541
1541
1542
1542
1543
1543
1544
1544
1545
1545
1546
1546
1547
1547
1548
1548
1549
1549
1550
1550
1551
1551
1552
1552
1553
1553
1554
1554
1555
1555
1556
1556
1557
1557
1558
1558
1559
1559
1560
1560
1561
1561
1562
1562
1563
1563
1564
1564
1565
1565
1566
1566
1567
1567
1568
1568
1569
1569
1570
1570
1571
1571
1572
1572
15
```

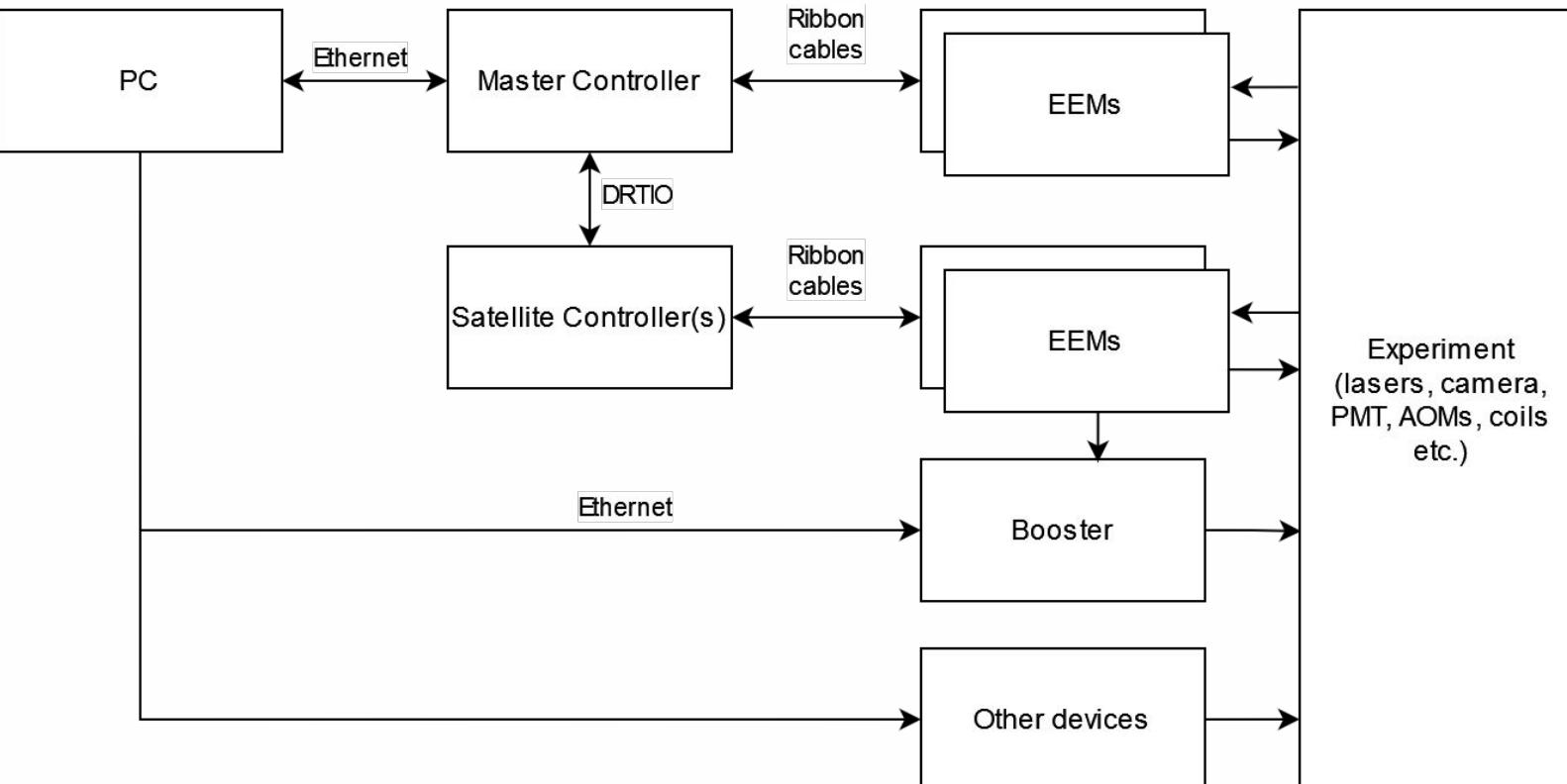
# What happens with my code?

- Python
- Build stage
- Run stage
  - Access to the FPGA
  - Hard real-time on the FPGA
  - RPC between PC and the FPGA

```
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
@kernel
def run(self):
    self.core.break_realtime()
    self.core.reset()
    self.init()
    self.core.break_realtime()

    # No interpolation
    self.record_waveform()
    self.play_waveform()

@kernel
def init(self):
    for fastino in self.fastino:
        fastino.init()
        fastino.set_hold(0xffffffff)
        delay(8*ns)
        fastino.set_group(0, [0.*V]*32)
        delay(1*us)
        fastino.update(0xffffffff)
        delay(10*ms)
    self.core.break_realtime()
```



# What does ARTIQ code look like?

- Python
- Build stage
- Run stage
- Analyze stage
  - Data analysis
  - Saving results to the database

```
84
85     def analyze(self):
86         pass
```

```
7
8 class SystemExample(EnvExperiment):
9     def build(self):
10        self.setattr_device("core")
11        self.setattr_device("core_dma")
12        self.fastino = [self.get_device("fastino" + str(i)) for i in range(3)]
13        n = 1 << 11
14        self.signal = [[0] * 16 for _ in range(n)]
15        self.signal2 = [[0] * 16 for _ in range(n)]
16        for i in range(n):
17            self.fastino[0].voltage_group_to_mu([4*np.sin(200*np.pi*i/n])*32, self.signal[i])
18        for i in range(n):
19            self.fastino[0].voltage_group_to_mu([19.9*(i % 2)-9.95]*32, self.signal2[i])
20
21 @kernel
22 def run(self):
23     self.core.break_realtime()
24     self.core.reset()
25     self.init()
26     self.core.break_realtime()
27
28 # No interpolation
29 self.record_waveform()
30 self.play_waveform()
31
32 @kernel
33 def init(self):
34     for fastino in self.fastino:
35         fastino.init()
36         fastino.set_hold(0xffffffff)
37         delay(8*ns)
38         fastino.set_group(0, [0.*V]*32)
39         delay(1*us)
40         fastino.update(0xffffffff)
41         delay(10*ms)
42     self.core.break_realtime()
43
44 @kernel
45 def record_waveform(self):
46     with self.core_dma.record("fastino_direct"):
47         for i in range(len(self.signal)):
48             t = now_mu()
49             with parallel:
50                 self.fastino[0].set_group_mu(0, self.signal[i])
51                 self.fastino[1].set_group_mu(0, self.signal[i])
52                 self.fastino[2].set_group_mu(0, self.signal[i])
53             at_mu(t+self.core.seconds_to_mu(32*8*ns))
54             with parallel:
55                 self.fastino[0].update(0xffffffff)
56                 self.fastino[1].update(0xffffffff)
57                 self.fastino[2].update(0xffffffff)
58
59             # Frame period is 392 ns - we have to align to it to have predictable updates
60             at_mu(t+self.core.seconds_to_mu(392*1*ns))
61
62     self.core.break_realtime()
63
64 @kernel
65 def play_waveform(self):
66     dma_handle = self.core_dma.get_handle("fastino_direct")
67     self.core.break_realtime()
68     for _ in range(10):
69         self.core_dma.playback_handle(dma_handle)
70
71 @kernel
72 def fastino_output(self, voltage):
73     # Set all Fastino channels to some voltage, starting from input parameter and incrementing by 0.2 V
74     for i in range(32):
75         self.fastino[0].set_dac(i, voltage + 0.2 * i)
76         delay(100 * us)
77         self.fastino[1].set_dac(i, voltage + 0.2 * i)
78         delay(100 * us)
79         self.fastino[2].set_dac(i, voltage + 0.2 * i)
80         delay(100 * us)
81
82         self.fastino[0].update(0xffffffff)
83         self.fastino[1].update(0xffffffff)
84
85     def analyze(self):
86         pass
```

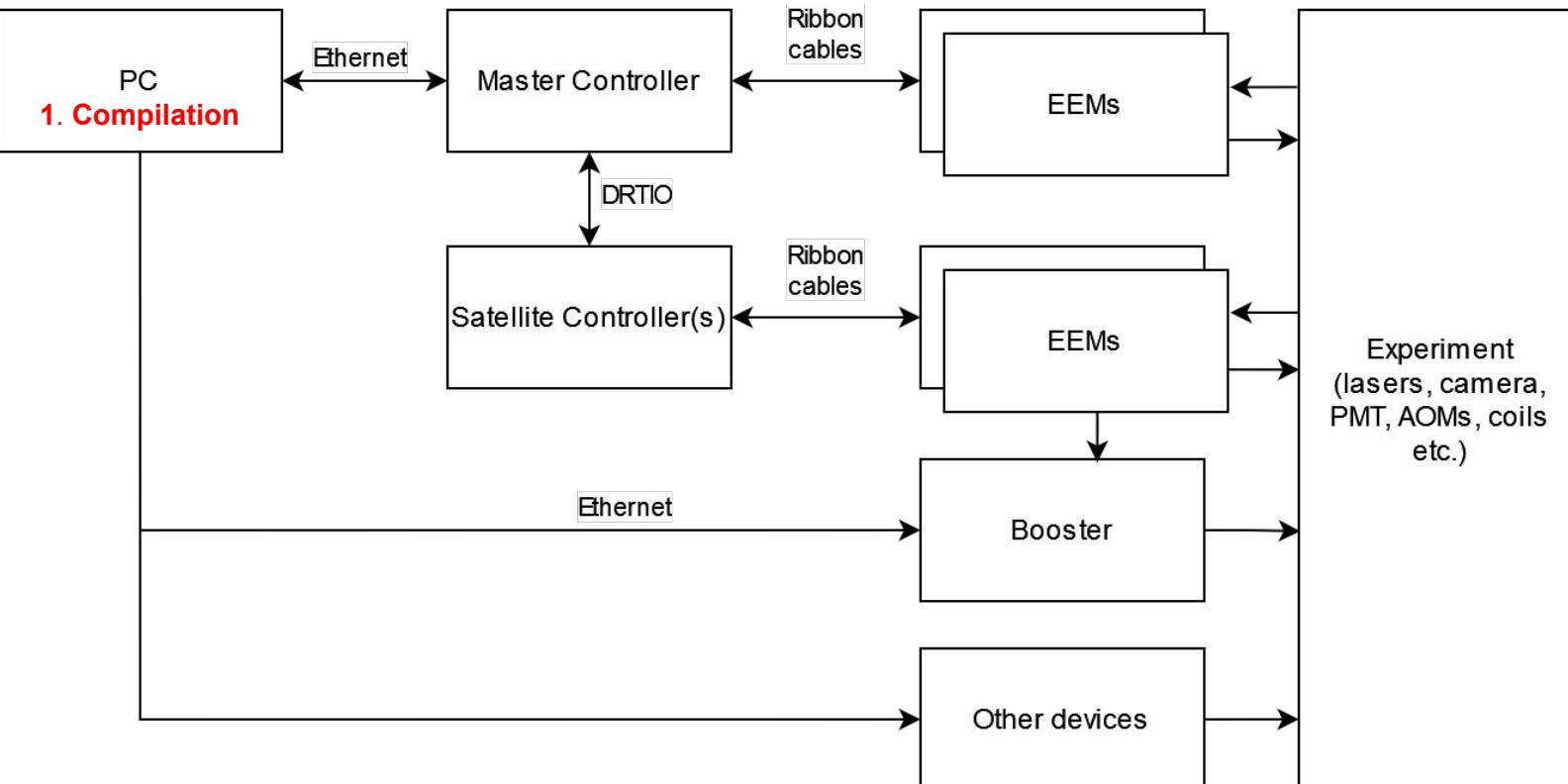
# What happens with my code?

- Python
- Build stage
- Run stage
  - Access to the FPGA
  - Hard real-time on the FPGA
  - RPC between PC and the FPGA

```
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
@kernel
def run(self):
    self.core.break_realtime()
    self.core.reset()
    self.init()
    self.core.break_realtime()

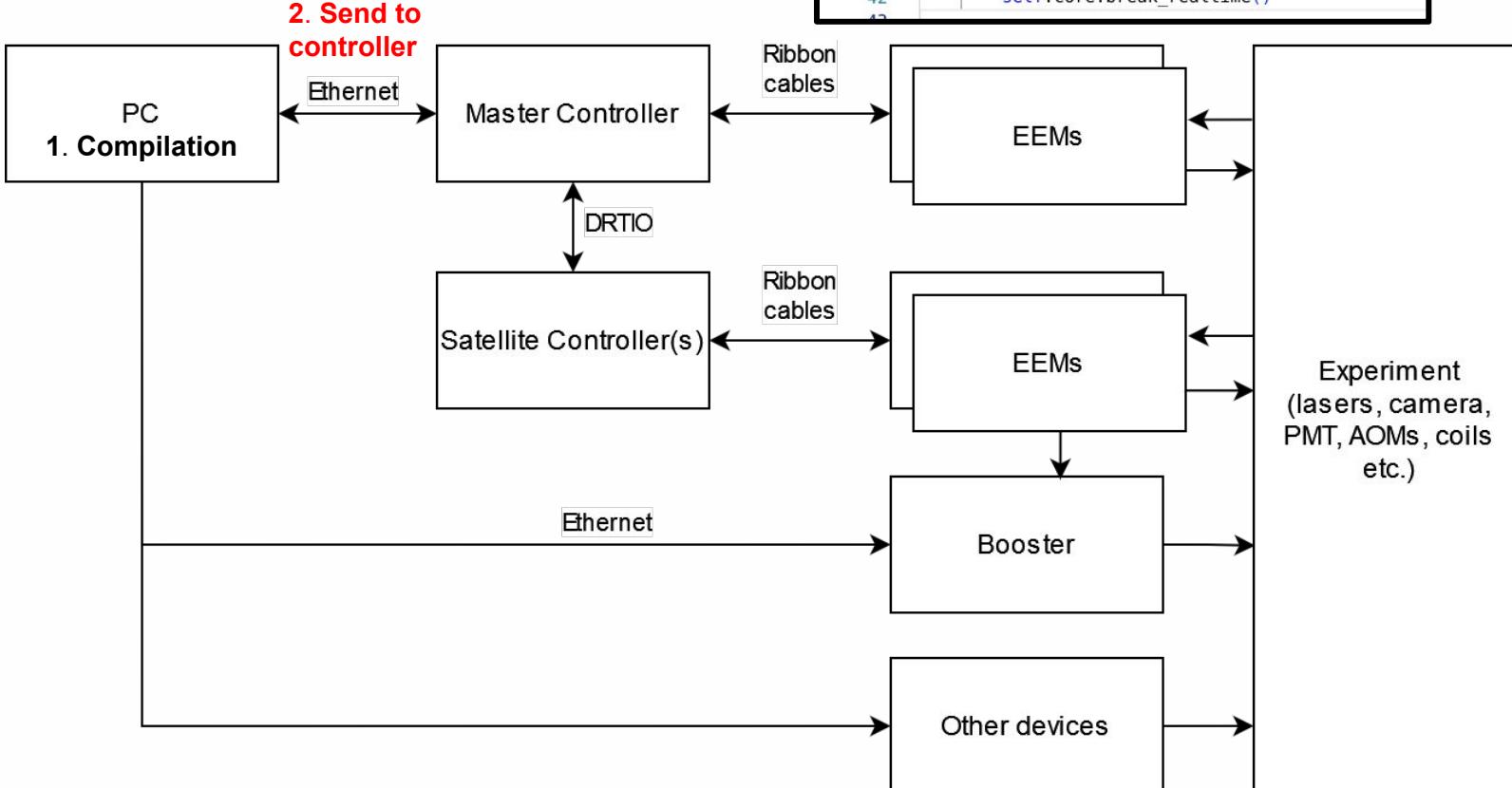
    # No interpolation
    self.record_waveform()
    self.play_waveform()

@kernel
def init(self):
    for fastino in self.fastino:
        fastino.init()
        fastino.set_hold(0xffffffff)
        delay(8*ns)
        fastino.set_group(0, [0.*V]*32)
        delay(1*us)
        fastino.update(0xffffffff)
        delay(10*ms)
    self.core.break_realtime()
```



# What happens with my code?

- Python
  - Build stage
  - Run stage
    - Access to the FPGA
    - Hard real-time on the FPGA
    - RPC between PC and the FPGA



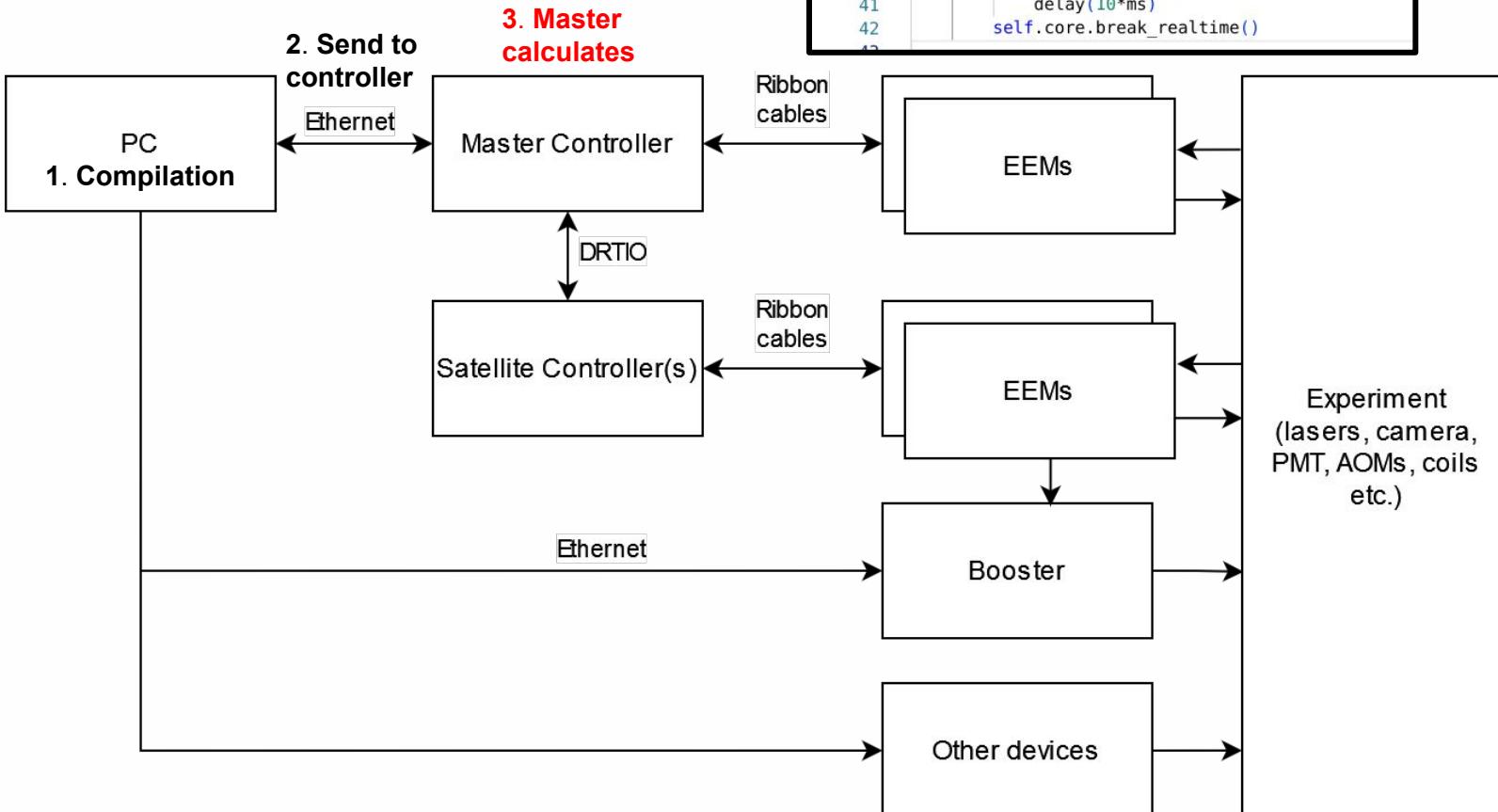
```
@kernel
def run(self):
    self.core.break_realtime()
    self.core.reset()
    self.init()
    self.core.break_realtime()

    # No interpolation
    self.record_waveform()
    self.play_waveform()

@kernel
def init(self):
    for fastino in self.fastino:
        fastino.init()
        fastino.set_hold(0xffffffff)
        delay(8*ns)
        fastino.set_group(0, [0.*V]*32)
        delay(1*us)
        fastino.update(0xffffffff)
        delay(10*ms)
    self.core.break_realtime()
```

# What happens with my code?

- Python
  - Build stage
  - Run stage
    - Access to the FPGA
    - Hard real-time on the FPGA
    - RPC between PC and the FPGA



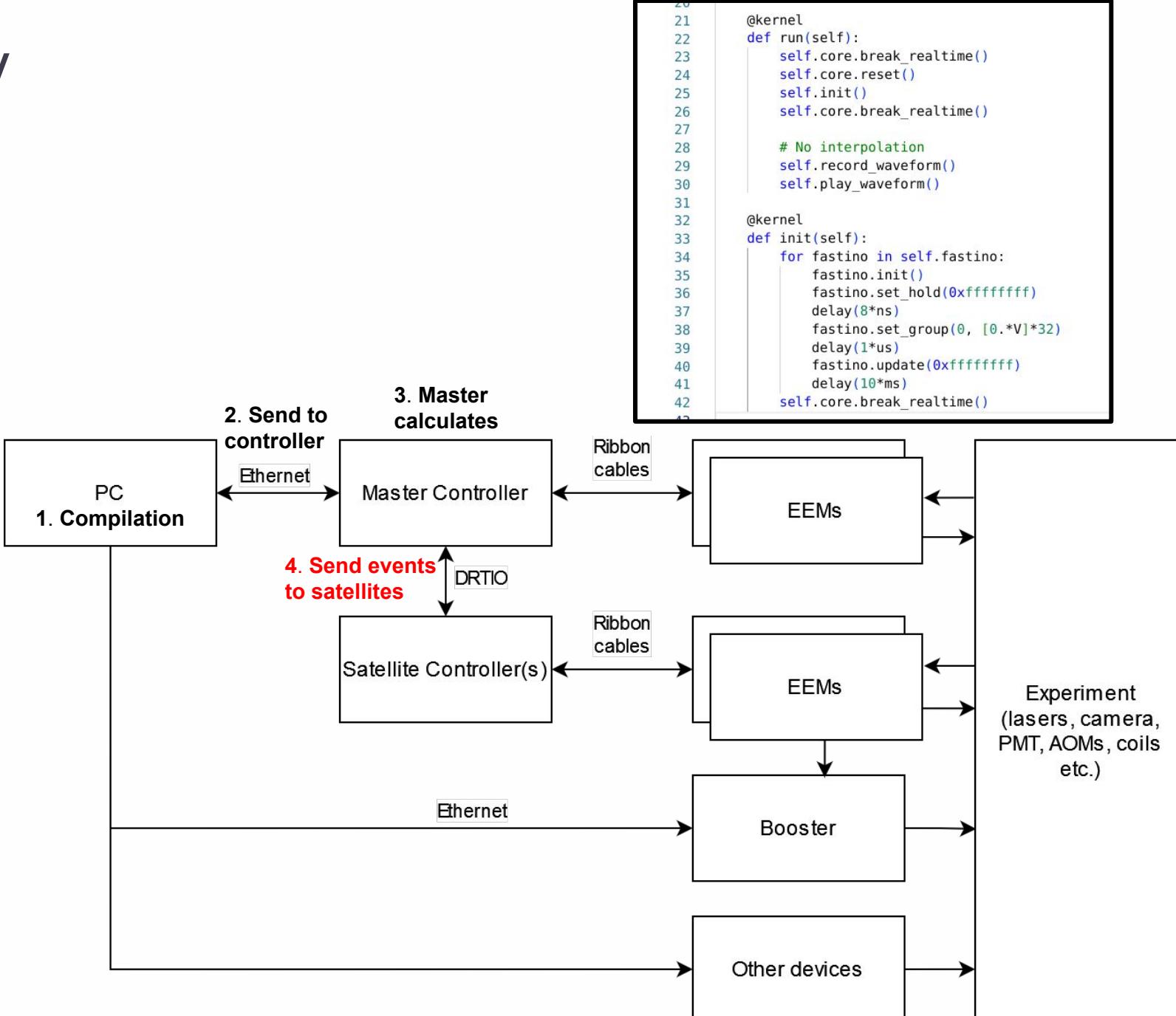
```
@kernel
def run(self):
    self.core.break_realtime()
    self.core.reset()
    self.init()
    self.core.break_realtime()

    # No interpolation
    self.record_waveform()
    self.play_waveform()

@kernel
def init(self):
    for fastino in self.fastino:
        fastino.init()
        fastino.set_hold(0xffffffff)
        delay(8*ns)
        fastino.set_group(0, [0.*V]*32)
        delay(1*us)
        fastino.update(0xffffffff)
        delay(10*ms)
    self.core.break_realtime()
```

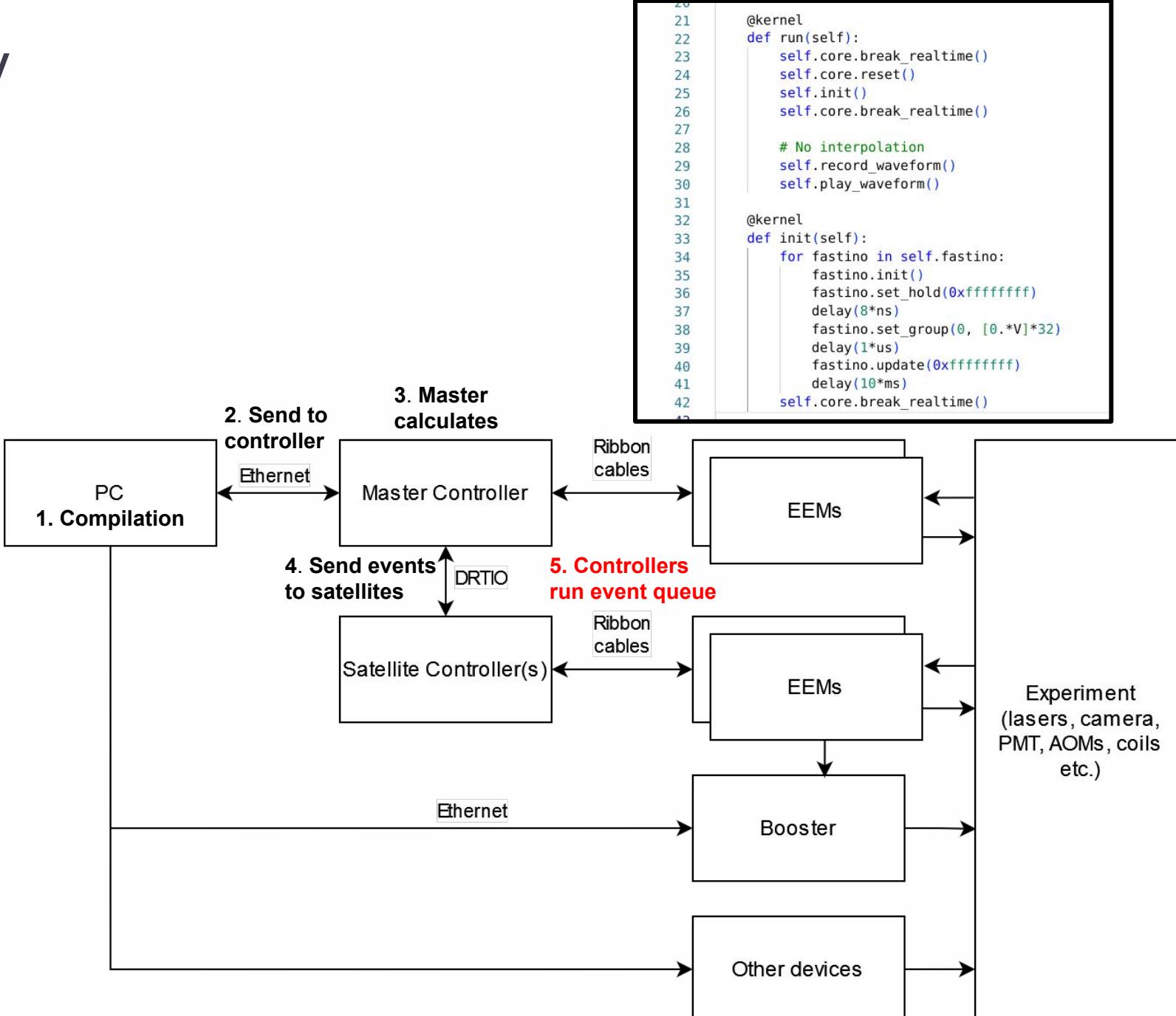
# What happens with my code?

- Python
- Build stage
- Run stage
  - Access to the FPGA
  - Hard real-time on the FPGA
  - RPC between PC and the FPGA



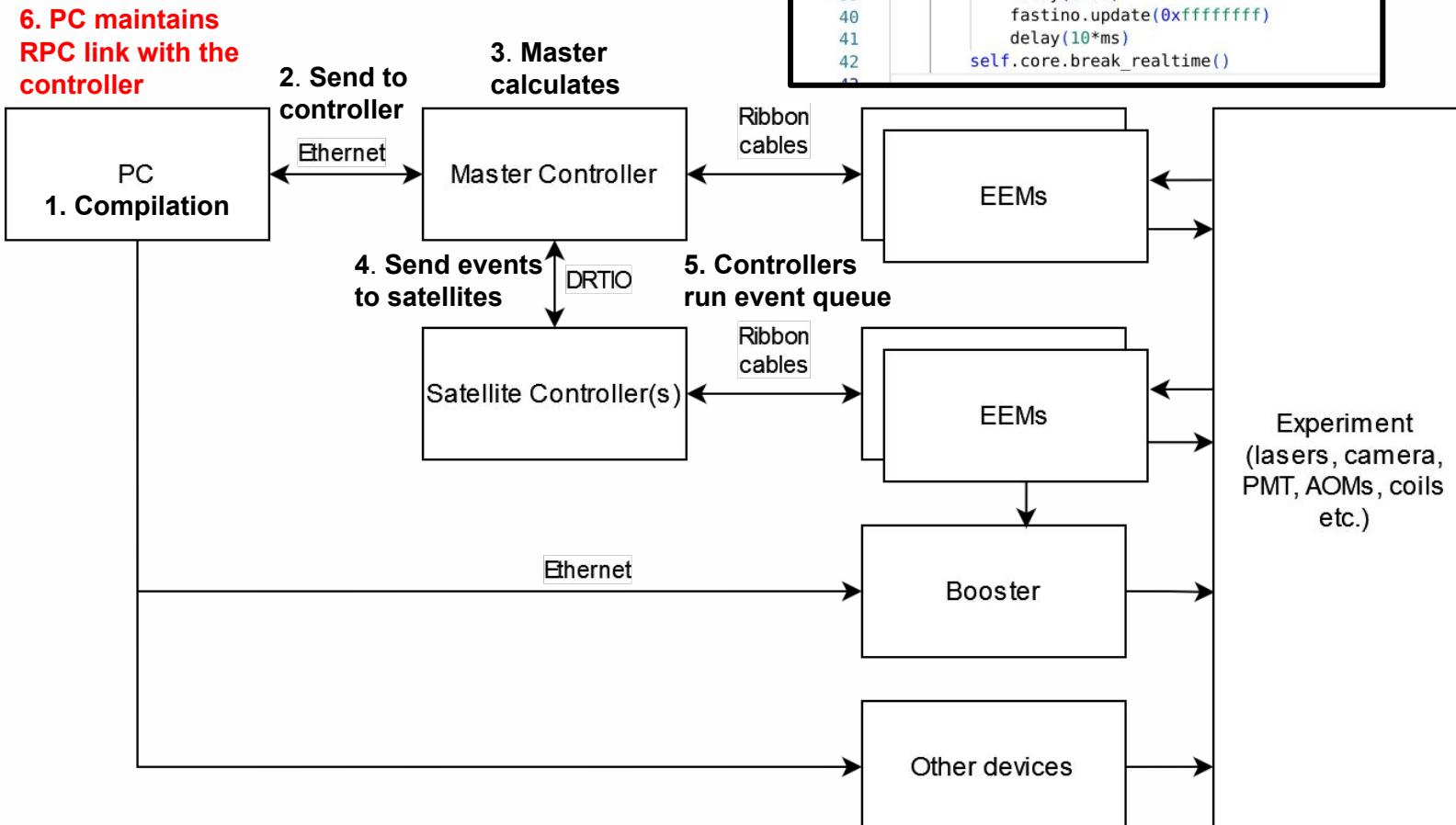
# What happens with my code?

- Python
- Build stage
- Run stage
  - Access to the FPGA
  - Hard real-time on the FPGA
  - RPC between PC and the FPGA



# What happens with my code?

- Python
- Build stage
- Run stage
  - Access to the FPGA
  - Hard real-time on the FPGA
  - RPC between PC and the FPGA

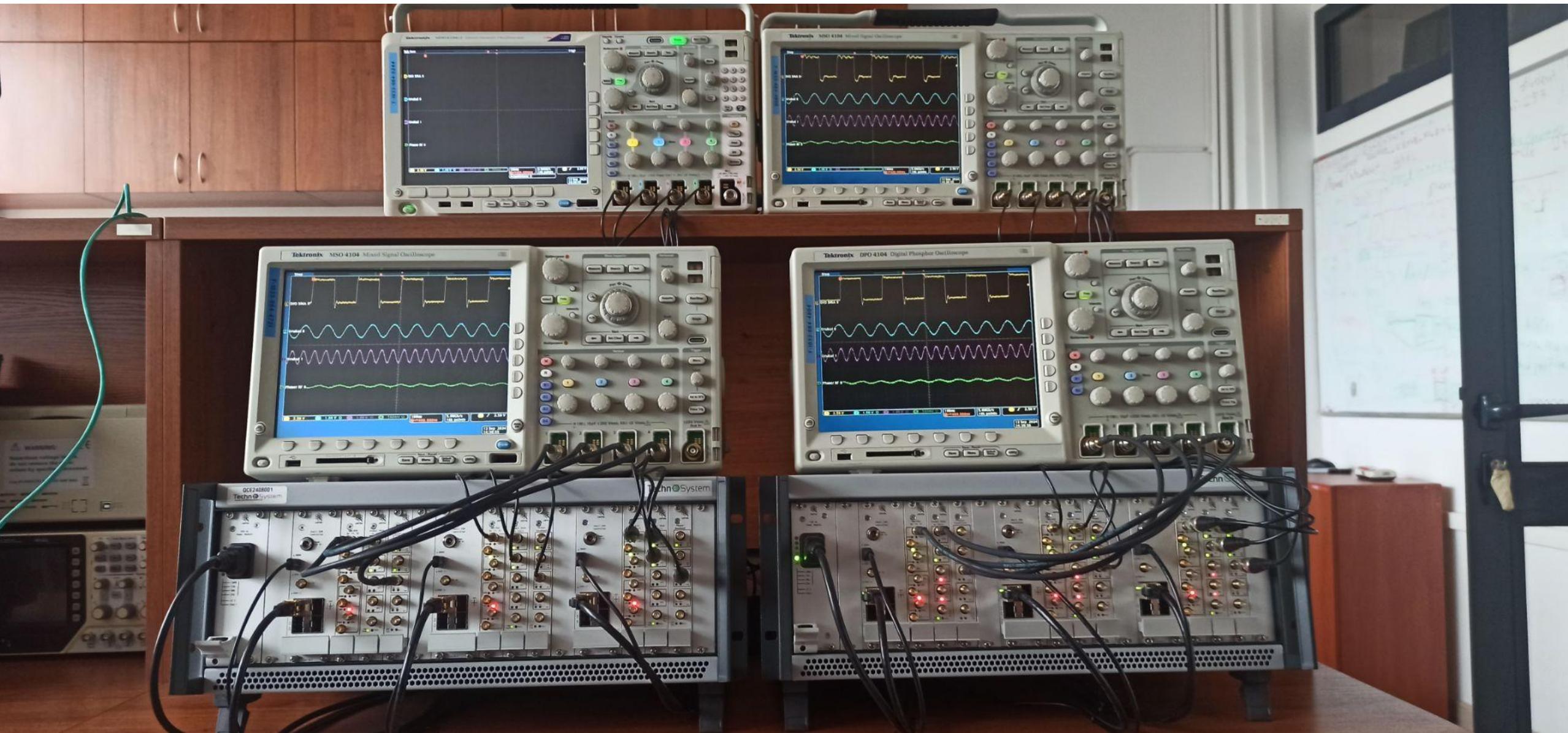


```
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
@kernel
def run(self):
    self.core.break_realtime()
    self.core.reset()
    self.init()
    self.core.break_realtime()

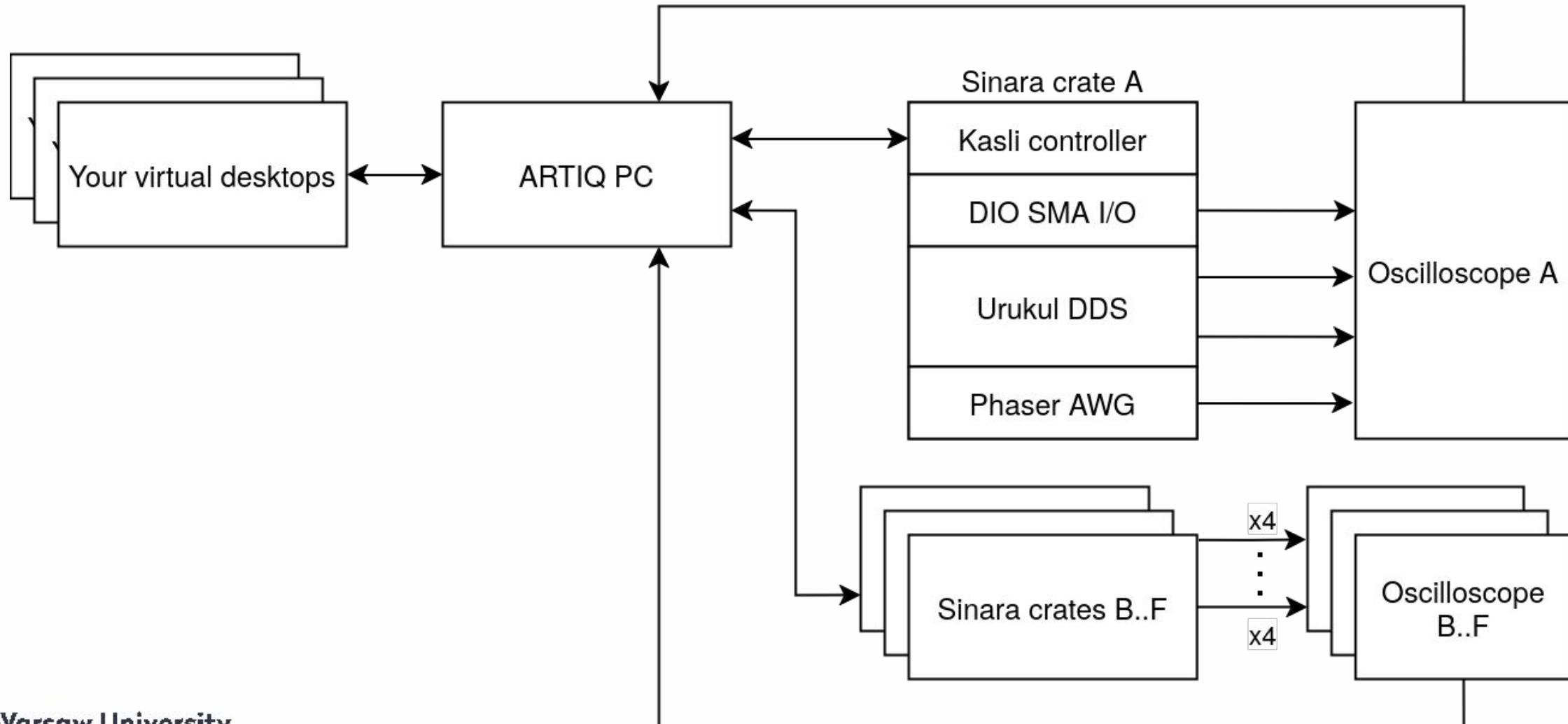
    # No interpolation
    self.record_waveform()
    self.play_waveform()

@kernel
def init(self):
    for fastino in self.fastino:
        fastino.init()
        fastino.set_hold(0xffffffff)
        delay(8*ns)
        fastino.set_group(0, [0.*V]*32)
        delay(1*us)
        fastino.update(0xffffffff)
        delay(10*ms)
    self.core.break_realtime()
```

# Devices that will be used

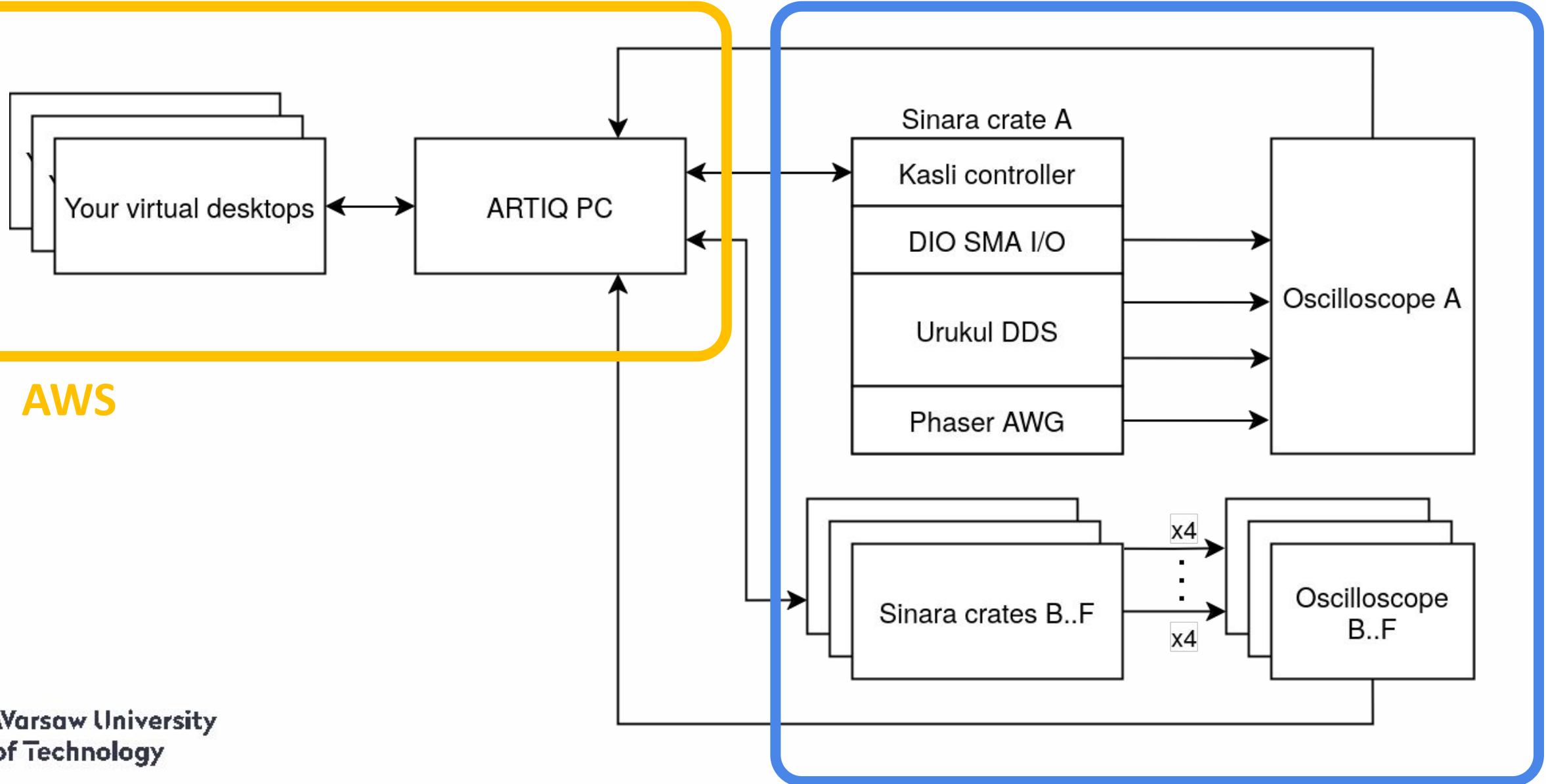


# Devices that will be used



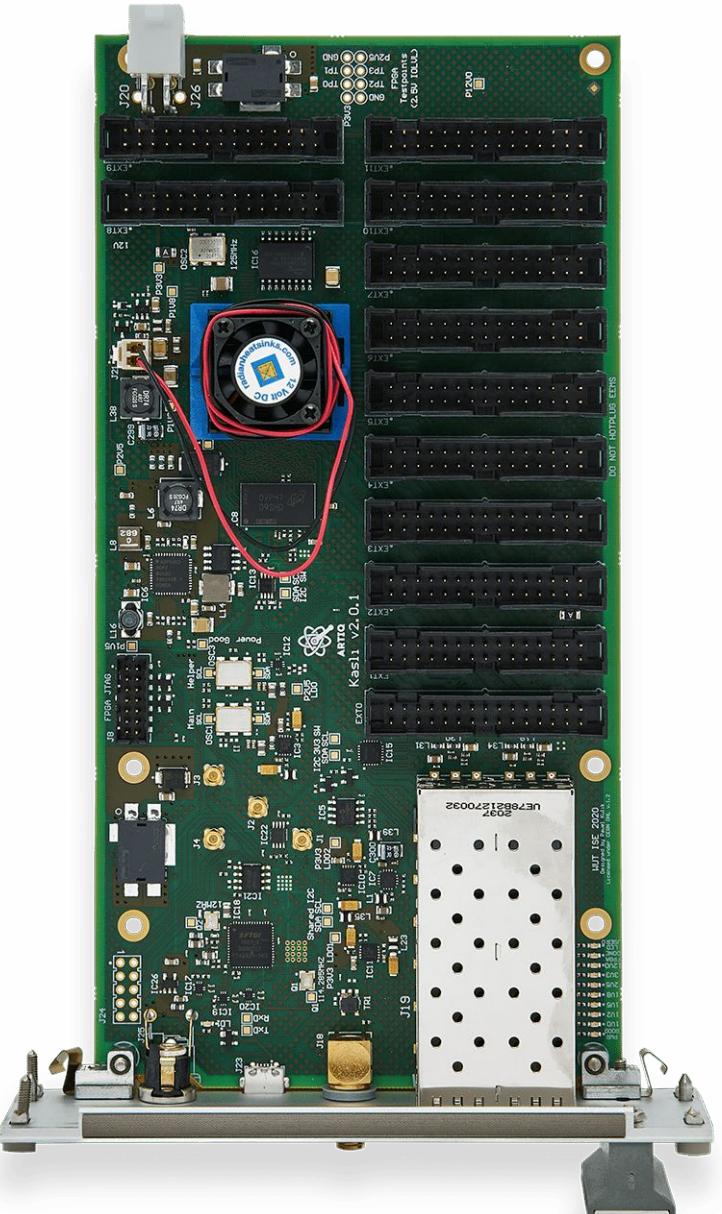
# Devices that will be used

Warsaw Lab



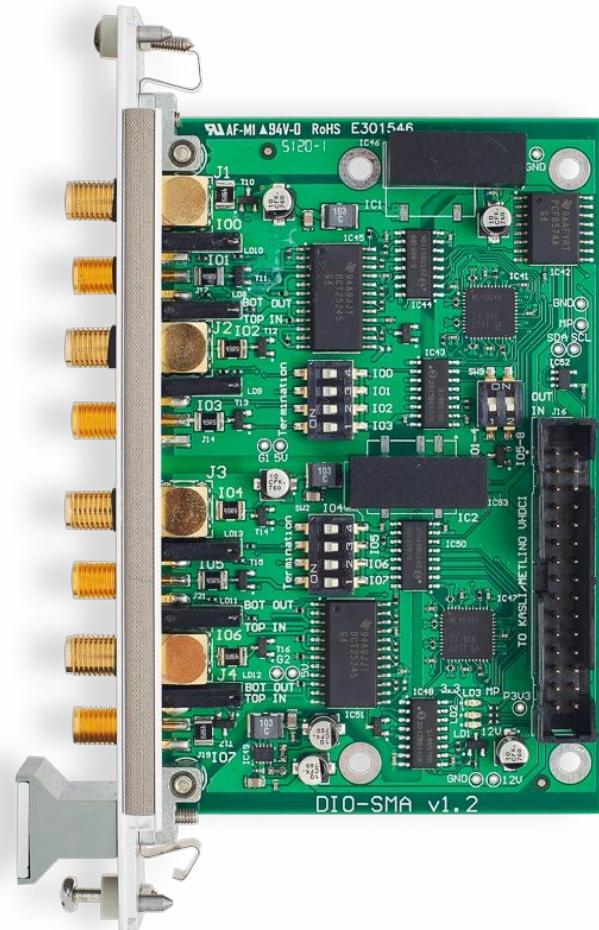
# Devices that will be used

- Kasli
  - AMD Artix-7 based controller
  - up to 12 peripherals
  - up to 3 downstream satellites
  - can be both master and satellite
  - <https://github.com/sinara-hw/Kasli>



# Devices that will be used

- Kasli
- DIO TTL
  - 8 digital IOs channels
  - selectable 50 Ohm termination
  - min. pulse width 5 ns
  - [https://github.com/sinara-hw/DIO\\_SMA/wiki](https://github.com/sinara-hw/DIO_SMA/wiki)



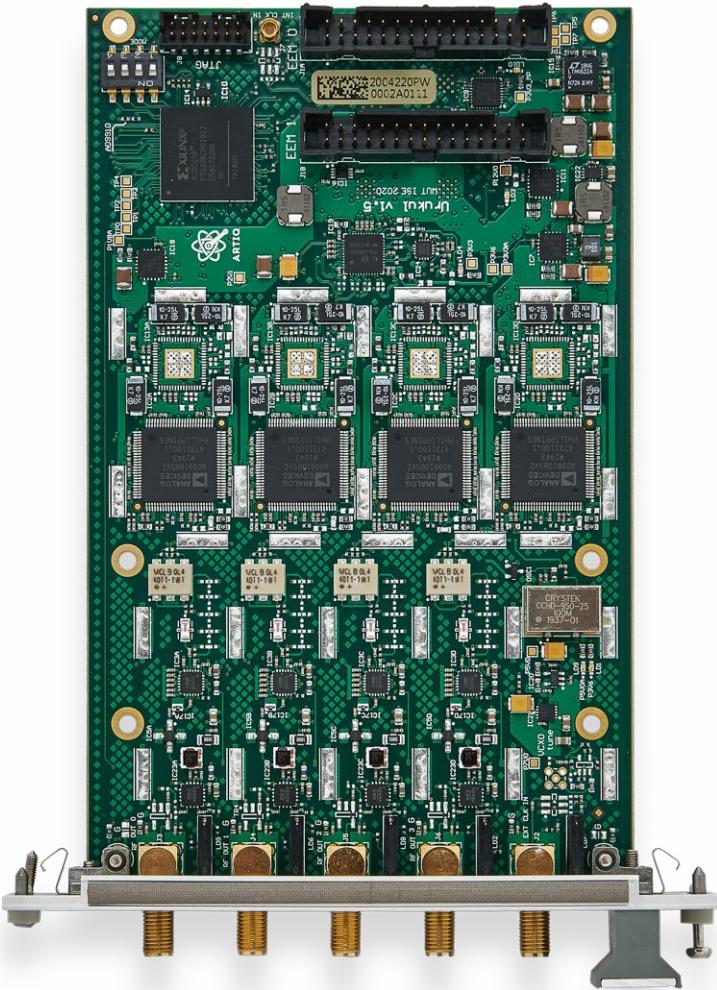
# Devices that will be used

- Kasli
- DIO TTL
- Urukul DDS
  - 4 channels GS/s DDS
  - frequency up to 400 MHz
  - ~0.25 Hz resolution
  - <https://github.com/sinara-hw/Urukul/wiki>



# Devices that will be used

- Kasli
- DIO TTL
- Urukul DDS: 3 independent “devices”
  - DDS
  - Attenuator
  - Output switch (on/off output signal)



# Devices that will be used

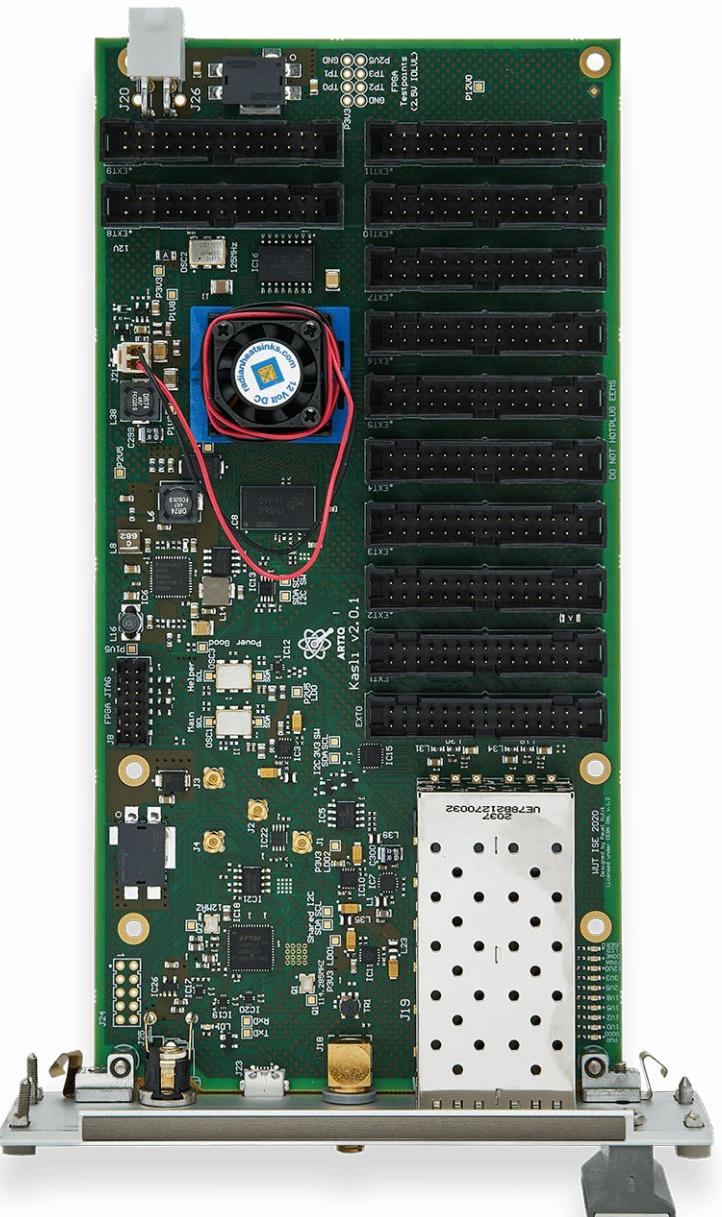
- Kasli
- DIO TTL
- Urukul DDS
- Phaser AWG
  - 2 channel 1.25 GS/s RF generator
  - baseband and upconverter variants
  - <https://github.com/sinara-hw/Phaser/wiki>



# What can I do in the FPGA?

- Subset of Python

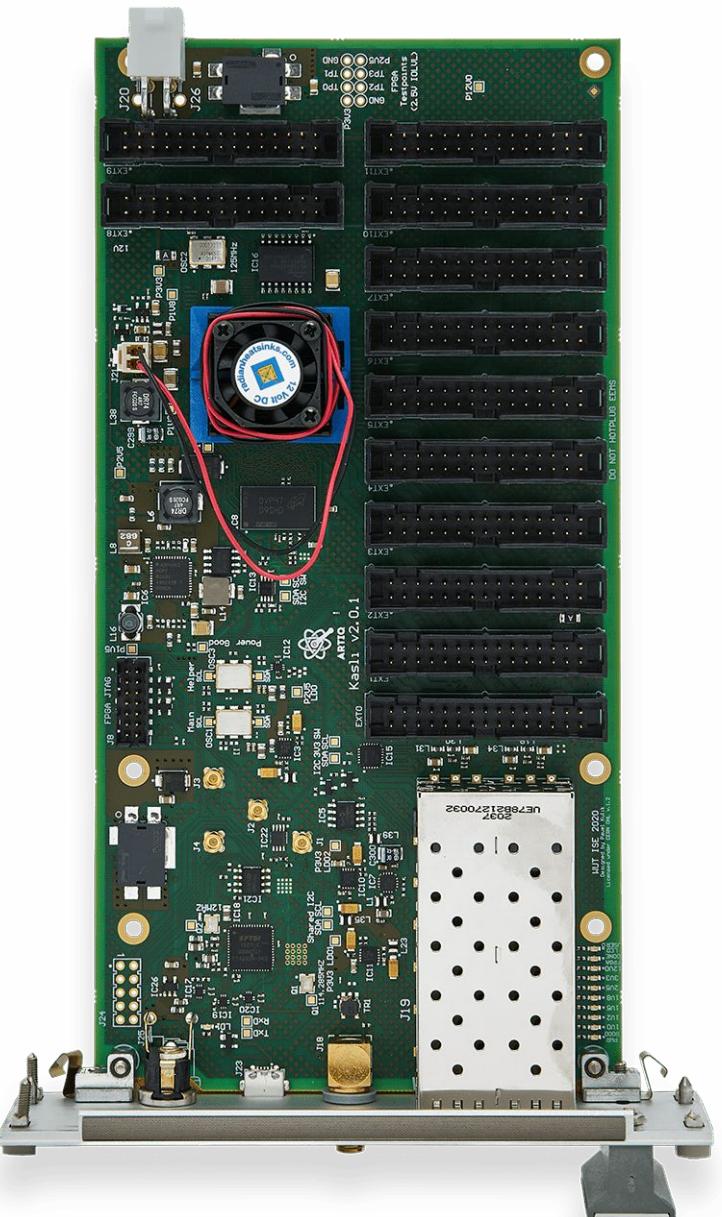
More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)



# What can I do in the FPGA?

- Subset of Python
- Conditionals (if)

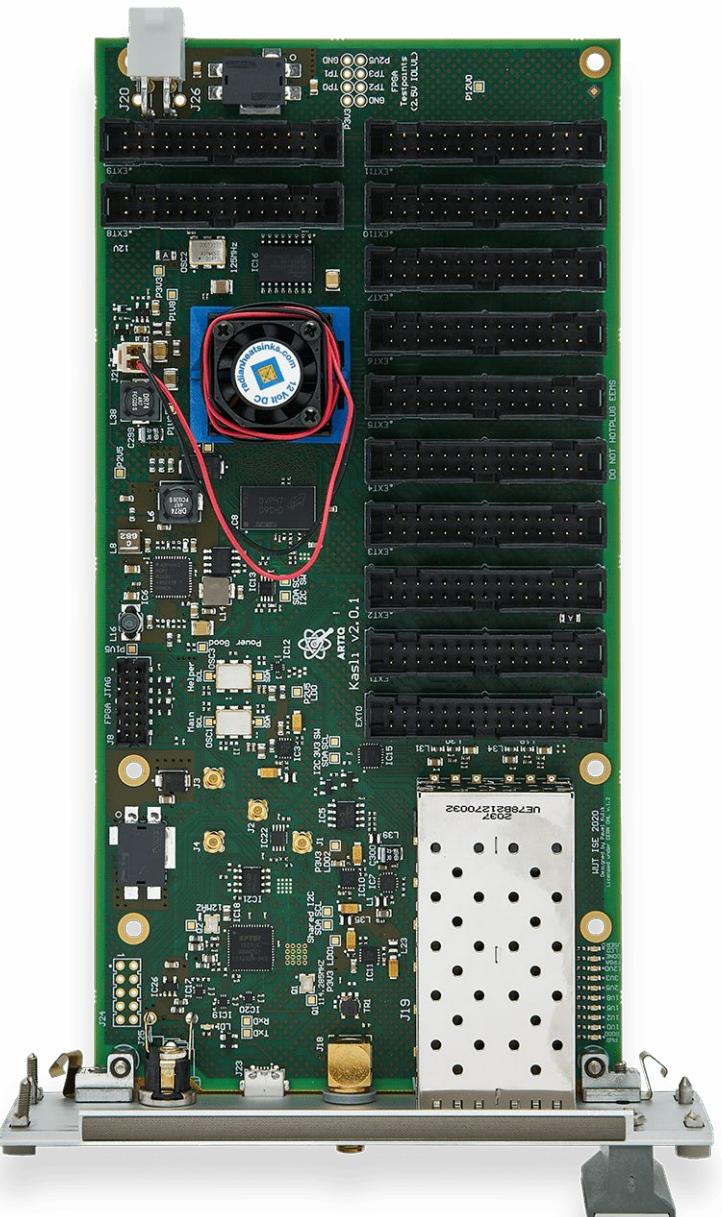
More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)



# What can I do in the FPGA?

- Subset of Python
  - Conditionals (if)
  - Loops, iterating over lists

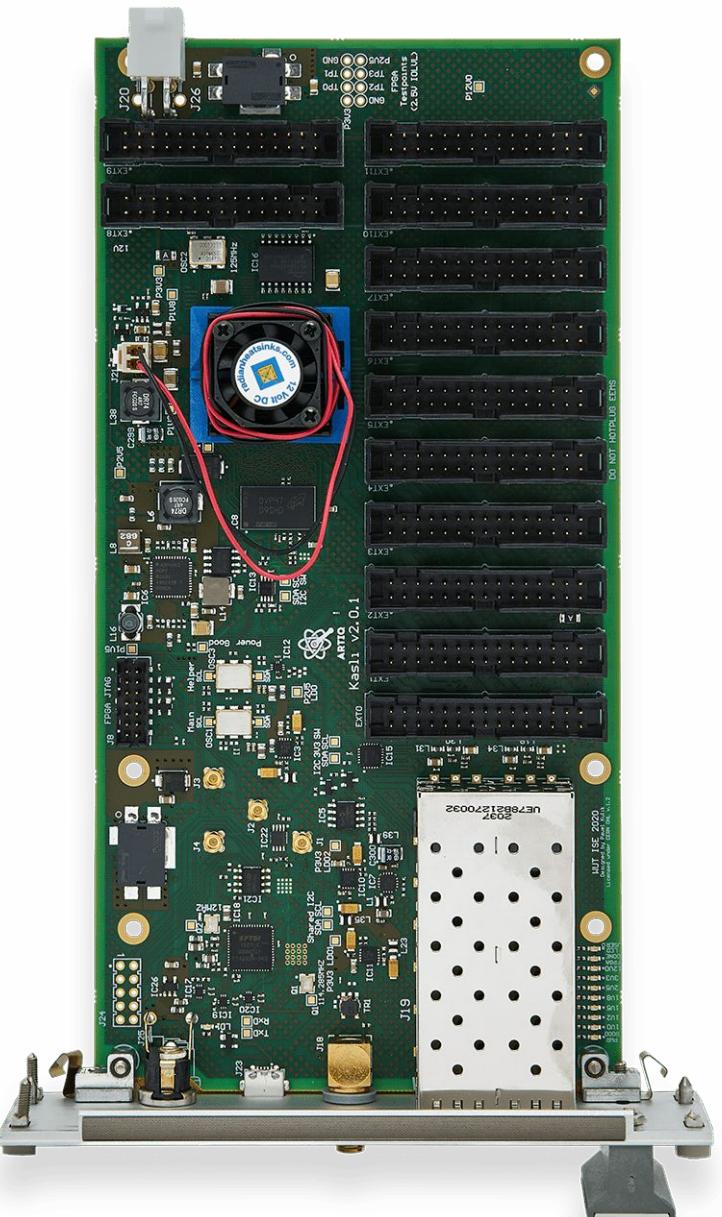
More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)



# What can I do in the FPGA?

- Subset of Python
- Conditionals (if)
- Loops, iterating over lists
- Exceptions

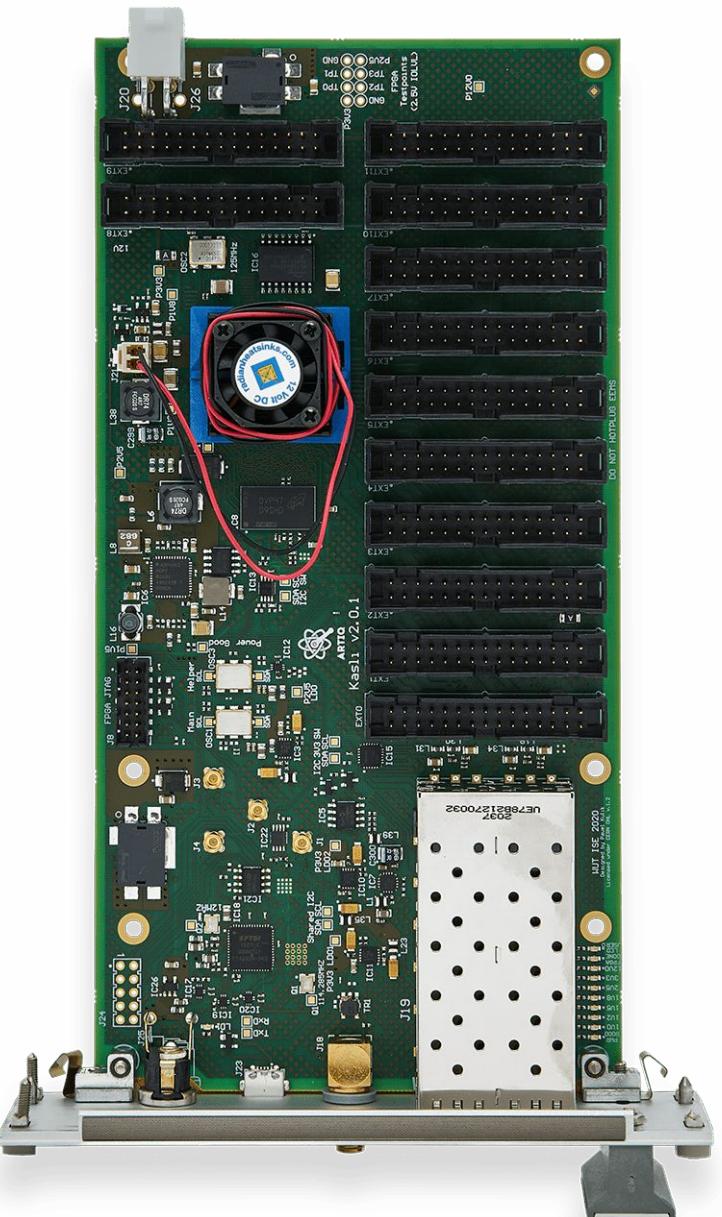
More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)



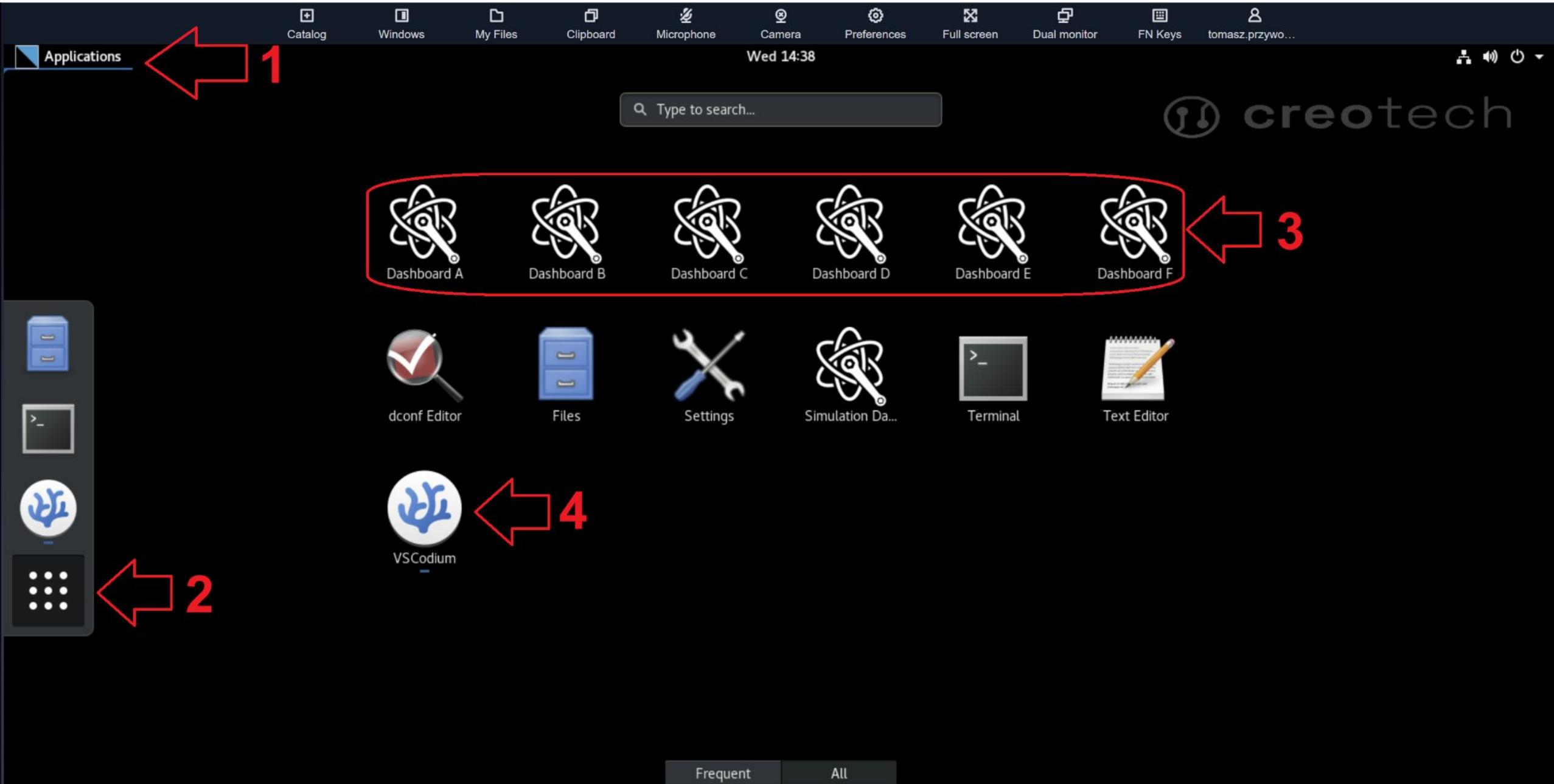
# What can I do in the FPGA?

- Subset of Python
  - Conditionals (if)
  - Loops, iterating over lists
  - Exceptions
  - Timing

More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)



# Organization



# Organization

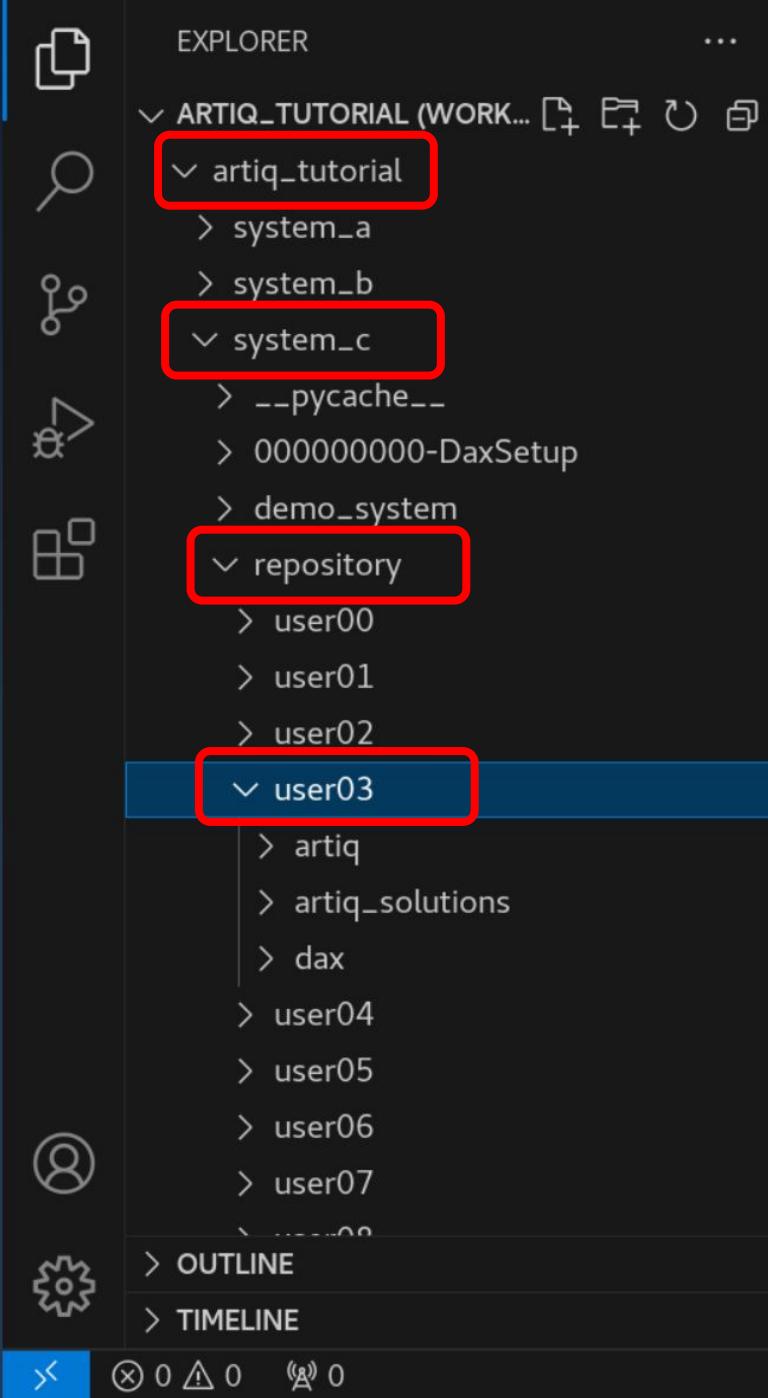
# artiq\_tutorial

**system\_<a..f>**

## repository

**user<00..11>**

artiq



# Organization

Applications ARTIQ Dashboard - System A ▾ Wed 14:56 ARTIQ Dashboard - System A

Applet: User 5 Scope View

ARTIQ<sup>7</sup>

Applets

Name	Command
<input type="checkbox"/> User 0 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 1 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 2 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 3 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 4 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input checked="" type="checkbox"/> User 5 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 6 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 7 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 8 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 9 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 10 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 11 Scope View	python /nix/artiq_dax_tutorial/applets/show

Explorer Shortcuts TTL DDS DAC Datasets Applets

Schedule

RID	Pipeline	Status	Prio	Due date	Revision	File	Class name
-----	----------	--------	------	----------	----------	------	------------

Schedule Log

# Organization

Applications ARTIQ Dashboard - System A ▾ Wed 14:56 ARTIQ Dashboard - System A

Applet: User 5 Scope View

ARTIQ<sup>7</sup>

Applets

Name	Command
<input type="checkbox"/> User 0 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 1 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 2 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 3 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 4 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input checked="" type="checkbox"/> User 5 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 6 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 7 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 8 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 9 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 10 Scope View	python /nix/artiq_dax_tutorial/applets/show
<input type="checkbox"/> User 11 Scope View	python /nix/artiq_dax_tutorial/applets/show

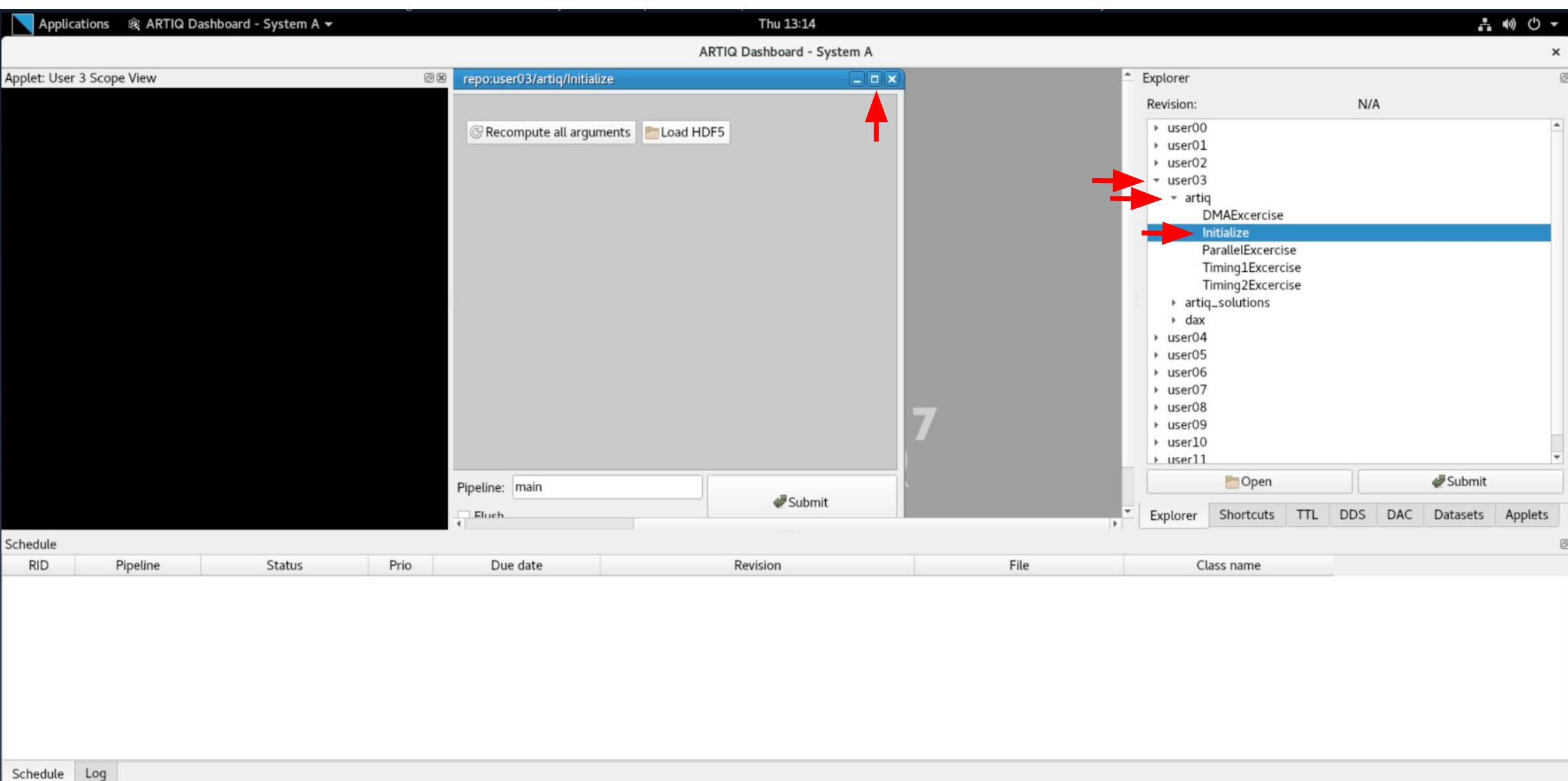
Explorer Shortcuts TTL DDS DAC Datasets Applets

Schedule

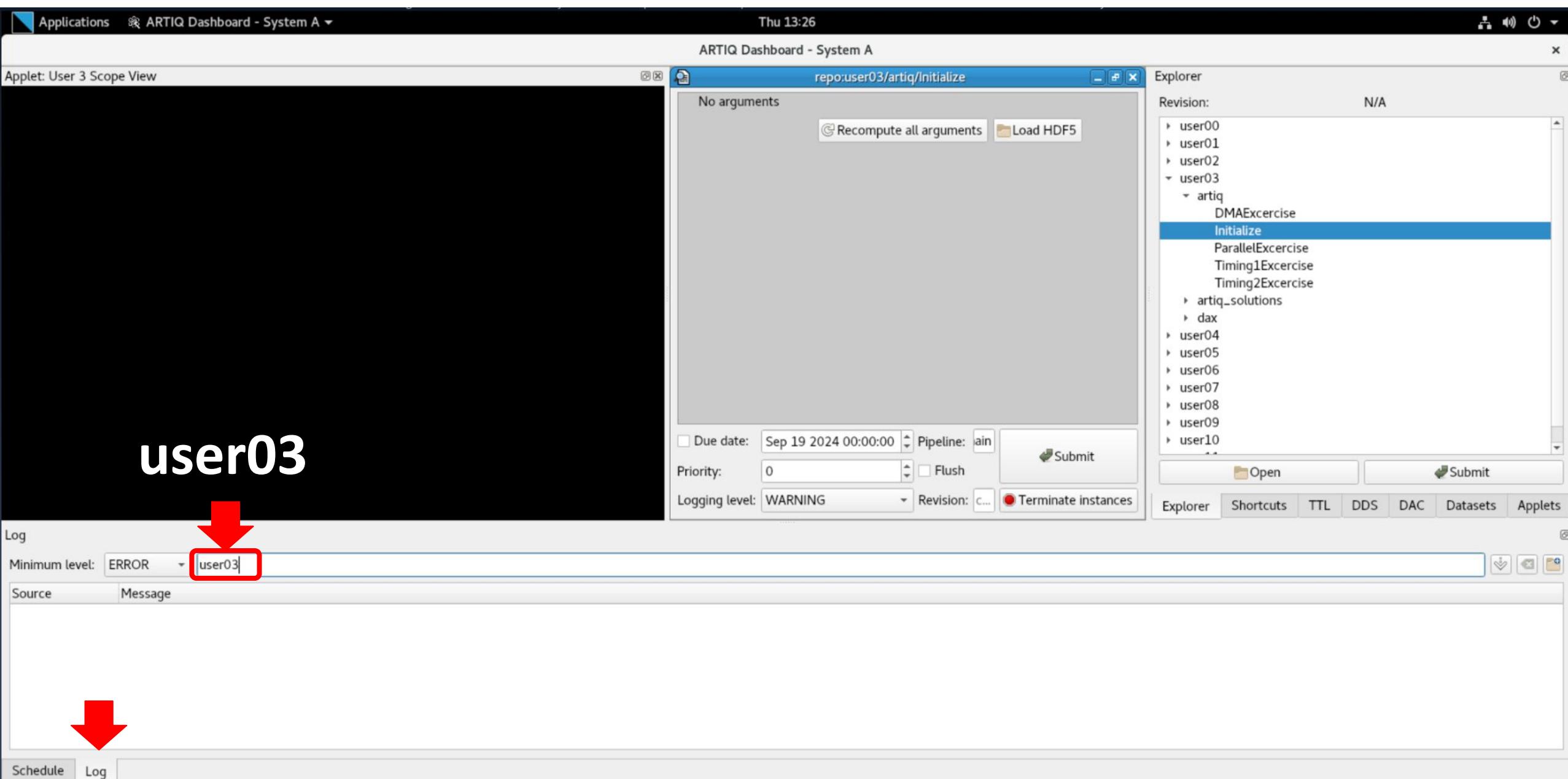
RID	Pipeline	Status	Prio	Due date	Revision	File	Class name
-----	----------	--------	------	----------	----------	------	------------

Schedule Log

# Organization



# Organization



# Organization

Applications ARTIQ Dashboard - System A

Thu 13:33

ARTIQ Dashboard - System A

Applet: User 3 Scope View

repo:user03/artiq/Initialize

No arguments

Recompute all arguments  Load HDF5

Due date: Sep 19 2024 00:00:00 Pipeline: main  Submit

Priority: 0  Flush

Logging level: WARNING Revision: c...  Terminate instances

Explorer

Revision: N/A

user01  
user02  
user03  
  artiq  
    DMAExcercise  
    Initialize  
    ParallelExcercise  
    Timing1Excercise  
    Timing2Excercise  
  artiq\_solutions  
  dax  
user04  
user05  
user06  
user07  
user08  
user09  
user10  
user11

Open  Submit

Schedule

RID	Pipeline	Status	Prio	Due date	Revision	File	Class name
1	main	running	0	N/A	user03/artiq/user03_initialize.py	Initialize	
2	main	prepare_done	0	N/A	user08/artiq/user08_initialize.py	Initialize	
3	main	pending	0	N/A	user08/artiq/user08_initialize.py	Initialize	

Schedule Log

The screenshot shows the ARTIQ Dashboard interface. At the top, there's a navigation bar with 'Applications' and the title 'ARTIQ Dashboard - System A'. The main area has a dark background with several windows open. One window is titled 'repo:user03/artiq/Initialize' and contains fields for due date, priority, and logging level, with a 'Submit' button. To the right is an 'Explorer' pane showing a hierarchical file structure under 'user03/artiq'. A red arrow points from the bottom of the 'Schedule' table towards the bottom-left corner. Another red arrow points from the bottom of the 'Initialize' entry in the 'Explorer' pane towards the bottom-left corner.

RID	Pipeline	Status	Prio	Due date	Revision	File	Class name
1	main	running	0	N/A	user03/artiq/user03_initialize.py	Initialize	
2	main	prepare_done	0	N/A	user08/artiq/user08_initialize.py	Initialize	
3	main	pending	0	N/A	user08/artiq/user08_initialize.py	Initialize	

# Organization

Applications ARTIQ Dashboard - System A

Thu 13:39

ARTIQ Dashboard - System A

Applet: User 3 Scope View

Jekt Stop

DIG SMA 0

Uralkul 0

Uralkul 1

Phaser RF 0

2.50 V 1.00 V 1.00 V 50.0mV 100ns 5.00GS/s 16k points 2.50 V

19 Sep 2024 12:33:55

No arguments

repo:user03/artiq/Initialize

Recompute all arguments Load HDF5

Due date: Sep 19 2024 00:00:00 Pipeline: ain Submit

Priority: 0 Flush

Logging level: WARNING Revision: c... Terminate instances

Explorer

Revision: N/A

user01  
user02  
user03  
user04  
user05  
user06  
user07  
user08  
user09  
user10  
user11

DMAExcercise  
Initialize  
ParallelExcercise  
Timing1Excercise  
Timing2Excercise

artiq\_solutions  
dax

Open Submit

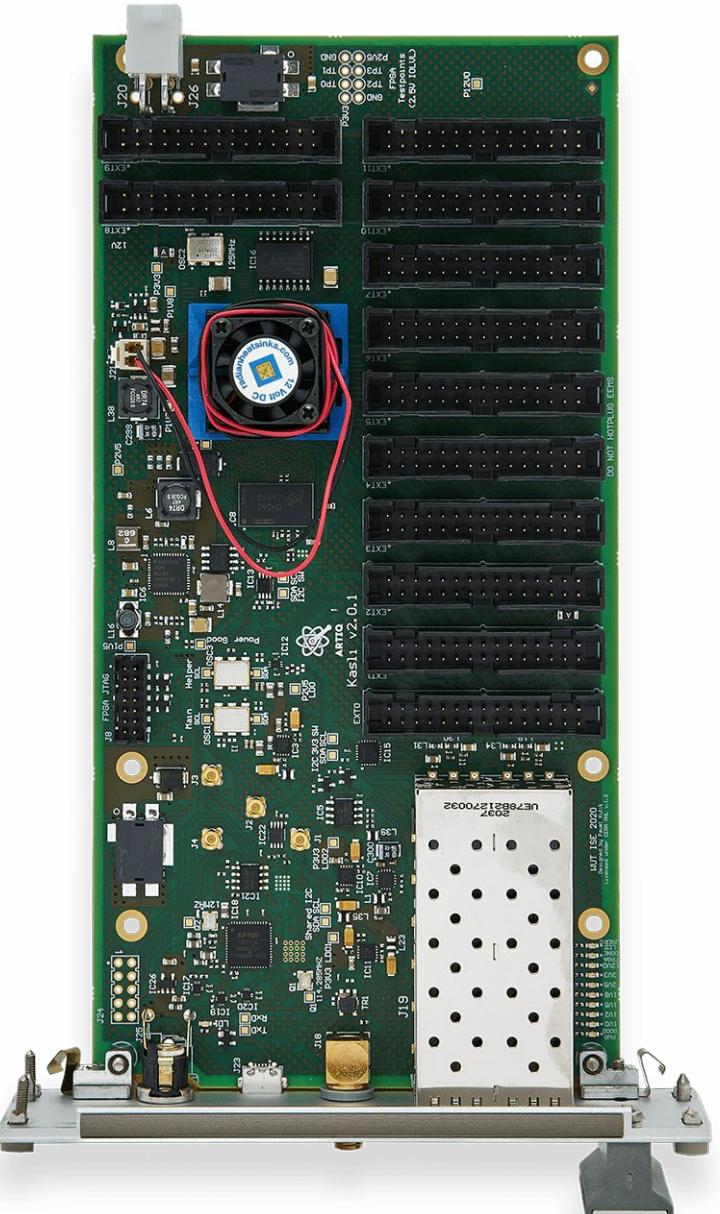
Schedule

RID	Pipeline	Status	Prio	Due date	Revision	File	Class name
-----	----------	--------	------	----------	----------	------	------------

Schedule Log

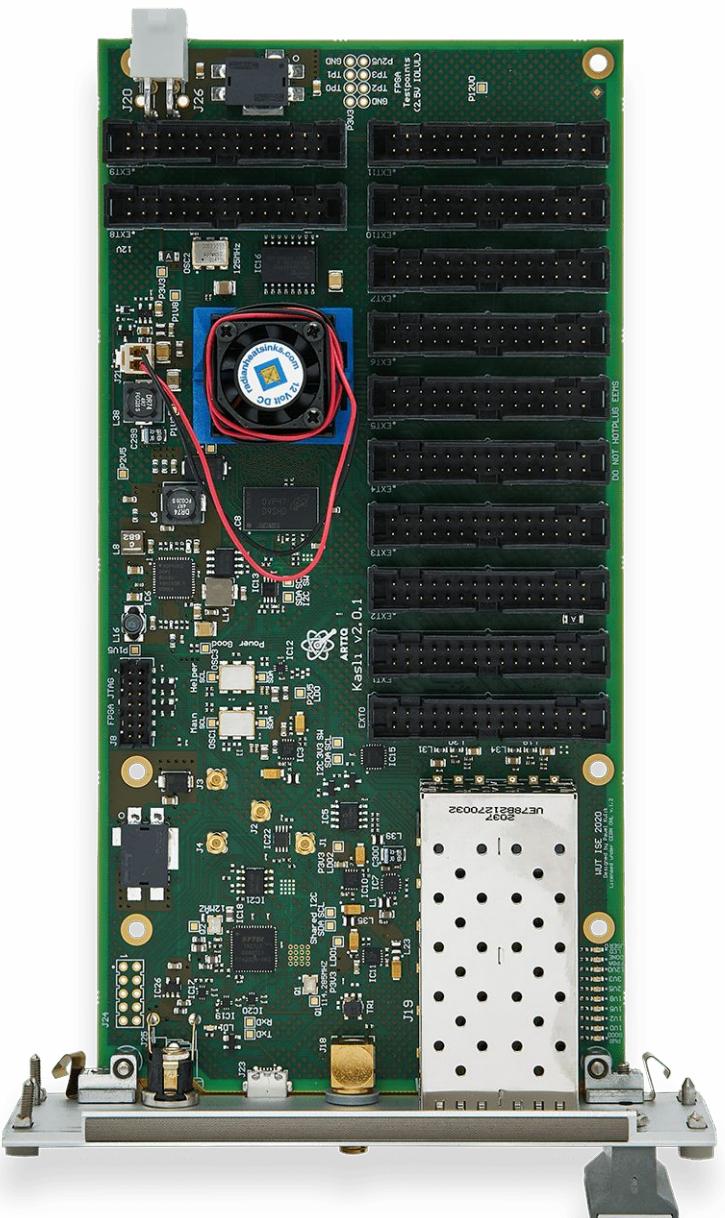
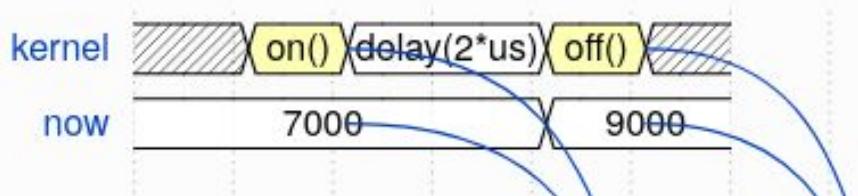
# Timing examples

```
ttl.on()  
delay(2*us)  
ttl.off()
```



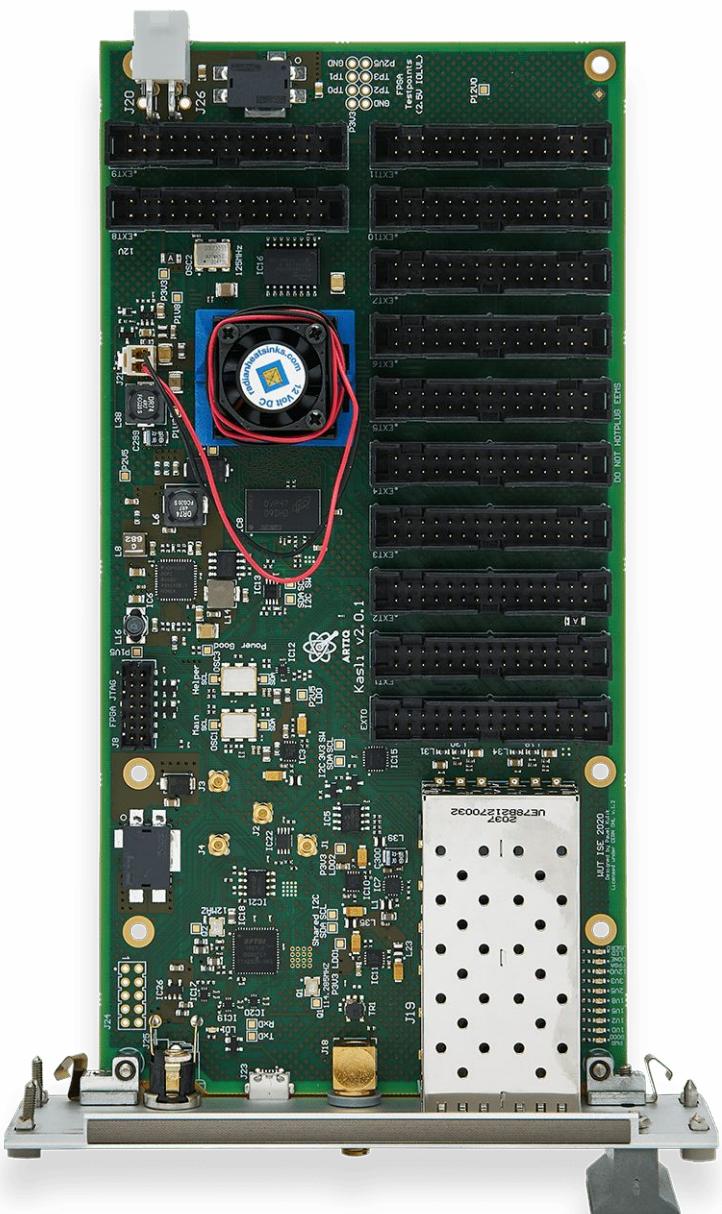
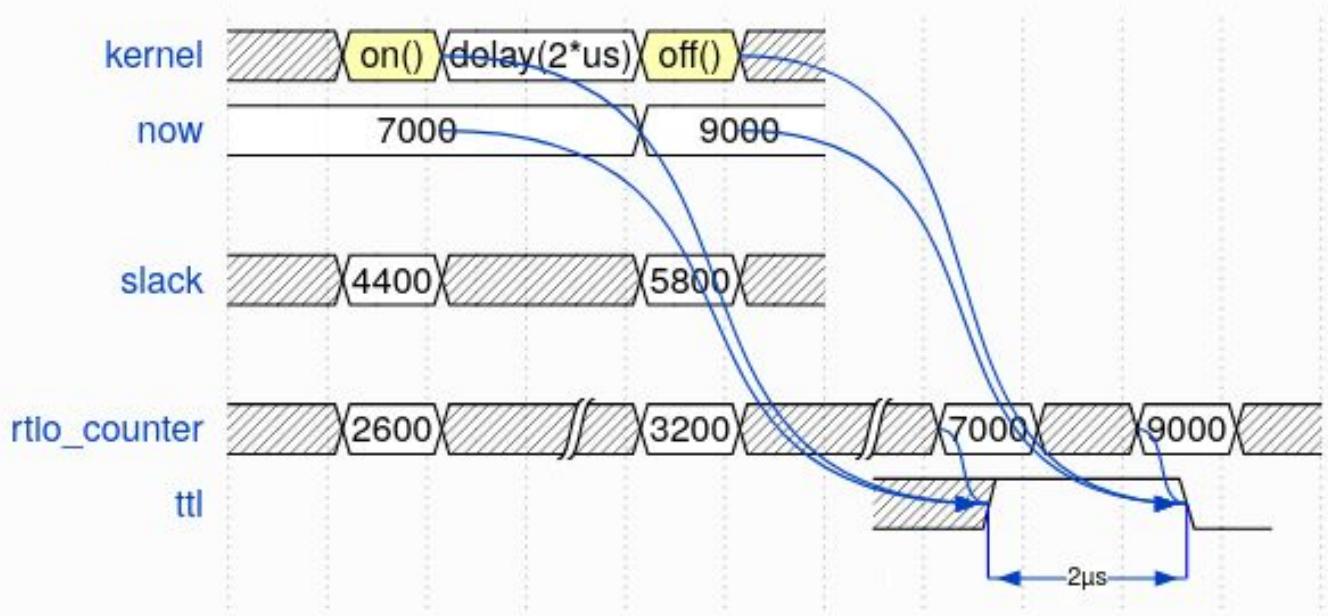
# Timing examples

```
ttl.on()  
delay(2*us)  
ttl.off()
```



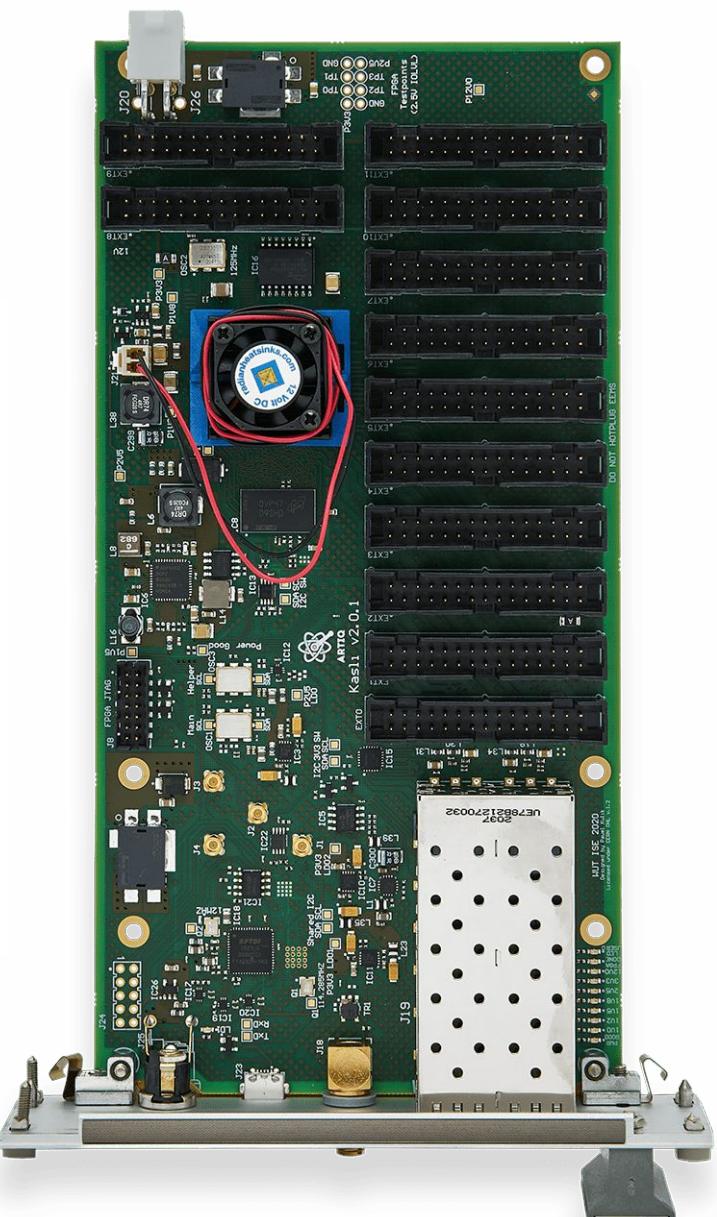
# Timing examples

```
tt1.on()  
delay(2*us)  
tt1.off()
```



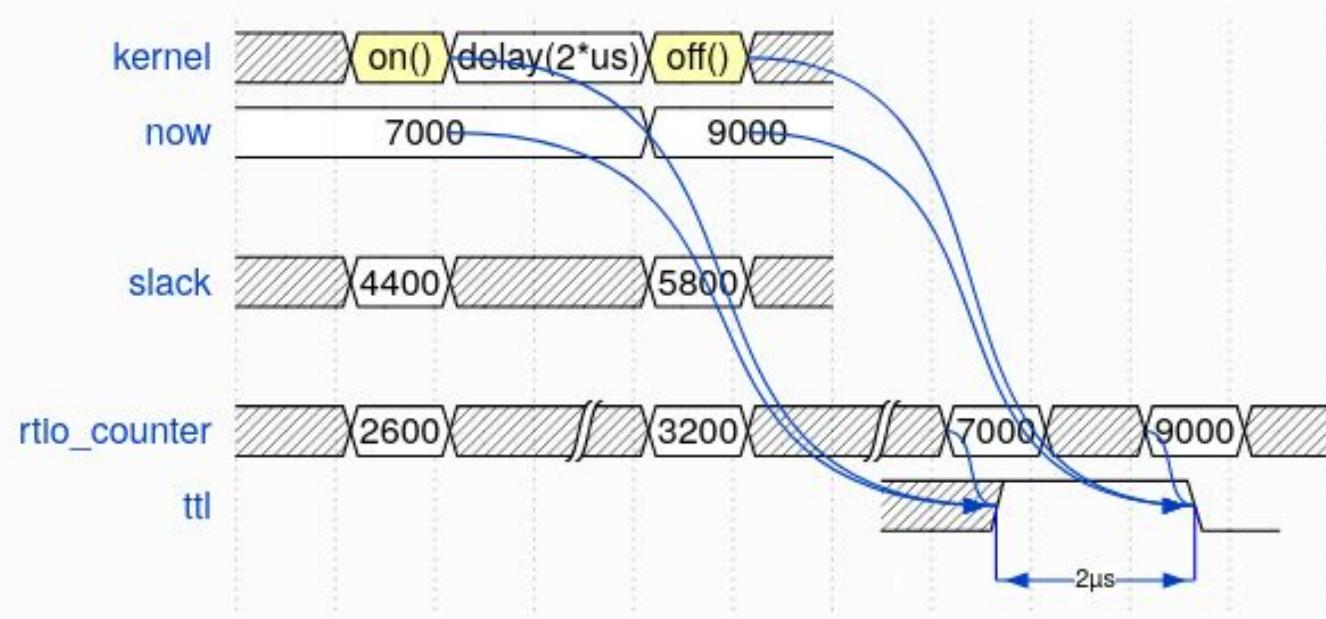
# Timing examples

```
for i in range(len(self.signal)):  
    t = now_mu()  
    with parallel:  
        self.fastino[0].set_group_mu(0, self.signal[i])  
        self.fastino[1].set_group_mu(0, self.signal[i])  
        self.fastino[2].set_group_mu(0, self.signal[i])  
    at_mu(t+self.core.seconds_to_mu(32*8*ns))  
    with parallel:  
        self.fastino[0].update(0xffffffff)  
        self.fastino[1].update(0xffffffff)  
        self.fastino[2].update(0xffffffff)  
  
    # Frame period is 392 ns - we have to align to it to have predictable updates  
    at_mu(t+self.core.seconds_to_mu(392*1*ns))
```



# Timing examples - exercise Timing1

```
ttl.on()  
delay(2*us)  
ttl.off()
```



Goal: create 2 pulses using both TTL methods (on/off and pulse) and delay function.

TTL methods:

- `ttl.on()`
- `ttl.off()`
- `ttl.pulse(duration)` - **hidden delay inside!**

Timing functions:

- `delay(duration)`

Dashboard arguments:

- FirstPulseWidth
- DelayToNextPulse
- SecondPulseWidth

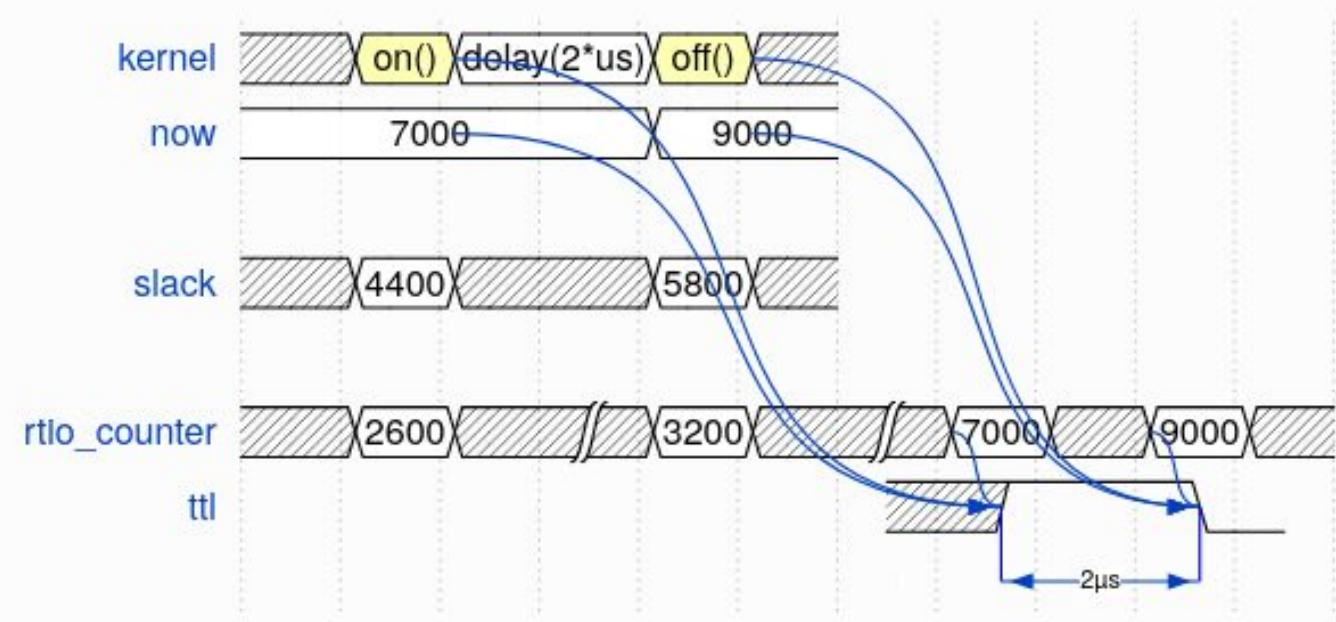
min. values: 10 ns

max. values: 400 ns

# Timing examples - exercise Timing2

```
ttl.on()  
delay(2*us)  
ttl.off()
```

```
t = now_mu()  
at_mu(t + self.core.seconds_to_mu(2 * us))
```



Goal: create 2 pulses using both TTL methods (on/off and pulse), now\_mu and at\_mu functions

TTL methods:

- ttl.on()
- ttl.off()
- ttl.pulse(*duration*) - **hidden delay inside!**

Timing functions:

- now\_mu() - returns current time pointer in machine units
- at\_mu(*time\_in\_mu*) - jump to exact time in machine units
- self.core.seconds\_to\_mu(*time\_value*) - convert time value in second to machine units

Dashboard arguments:

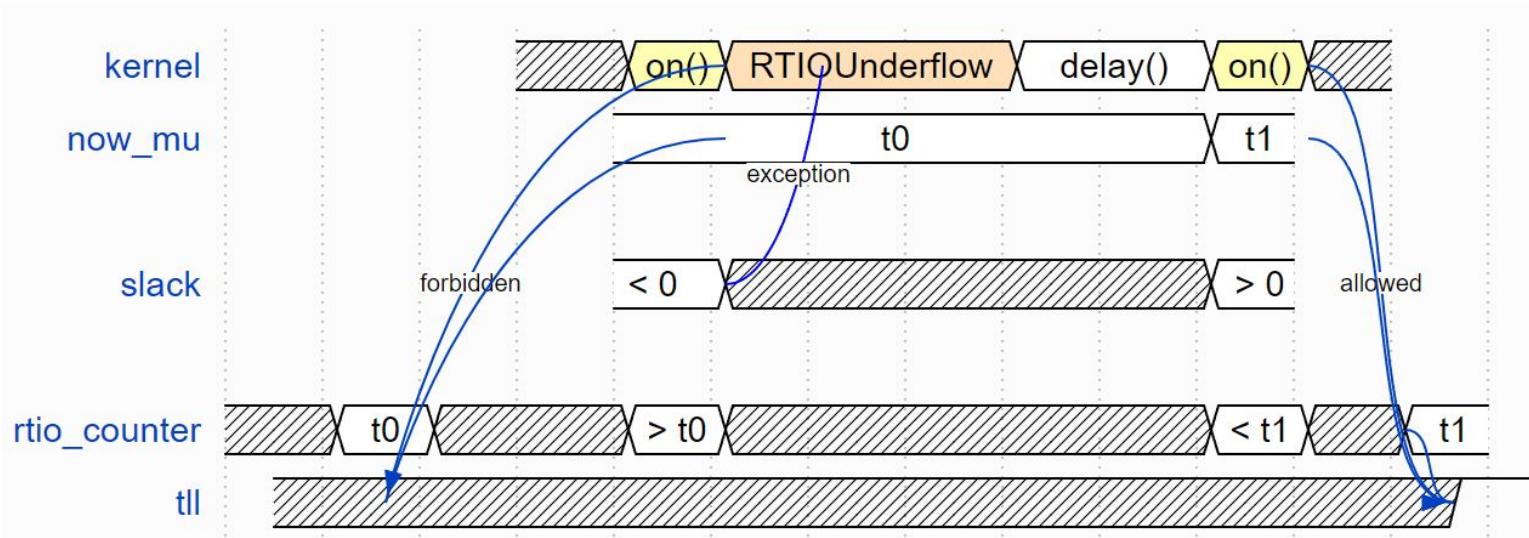
- FirstPulseWidth
- DelayToNextPulse
- SecondPulseWidth

min. values: 10 ns

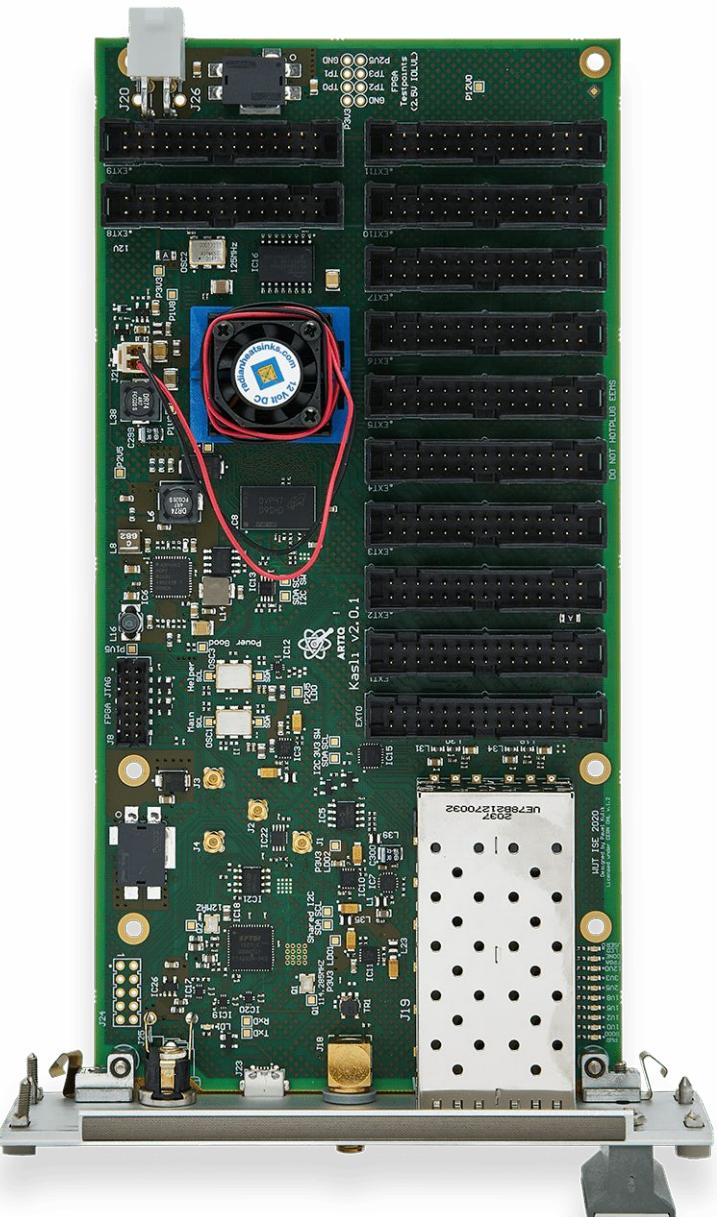
max. values: 400 ns

# RTIO Underflow + Exceptions

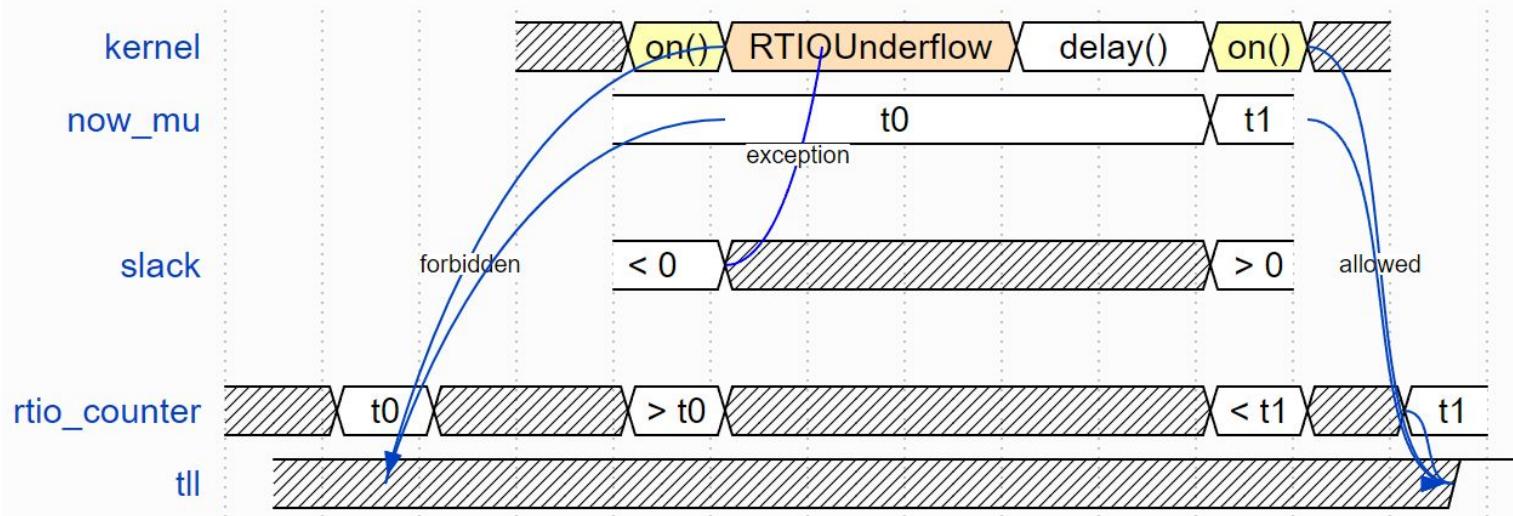
```
try:  
    ttl.on()  
except RTIUnderflow:  
    # try again at the next mains cycle  
    delay(16.6667*ms)  
    ttl.on()
```



# RTIO Underflow + Exceptions



# RTIO Underflow + Exceptions - exercise Timing3



TTL methods:

- ttl.on()
- ttl.off()
- ttl.pulse(*duration*)

Timing functions:

- delay(*duration*)

Dashboard arguments:

- Delay - time between next edge event

min. value: 10 ns

max. value: 1000 ns

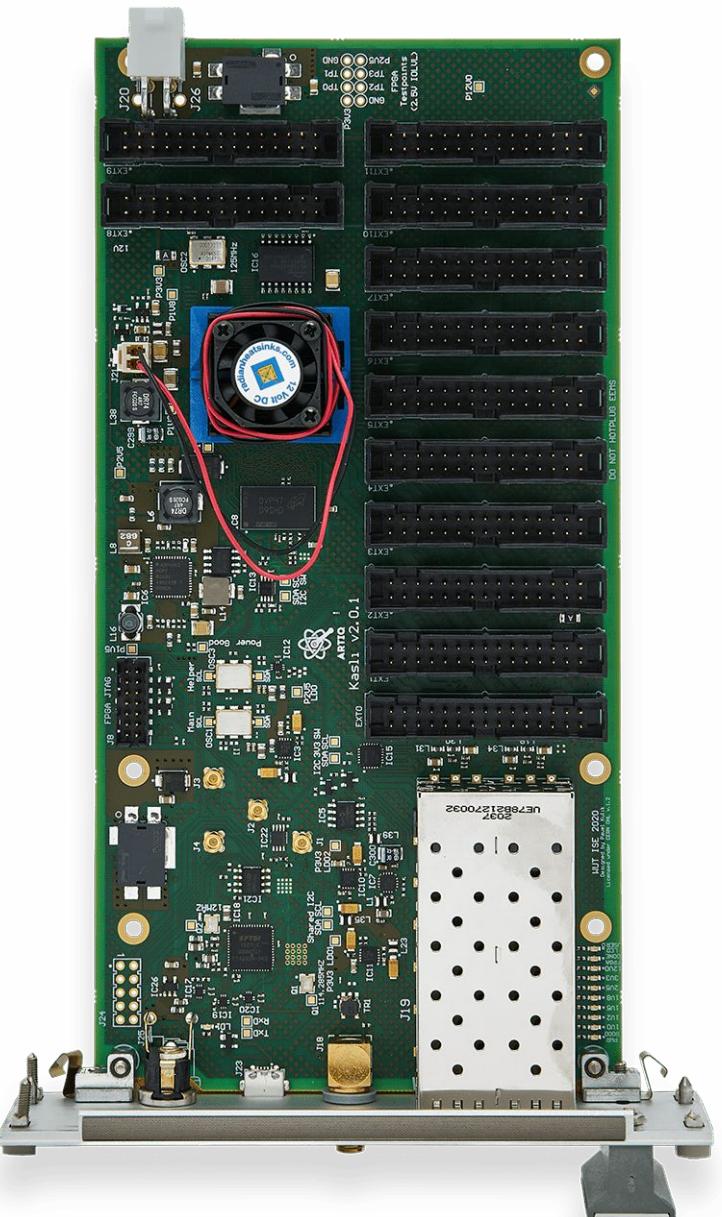
working min. value: ~390ns

**Goal:** create 10k iterations for loop. In each loop switch TTL on and off with delay between events.

# What can I do in the FPGA?

- Subset of Python
- Conditionals (if)
- Loops, iterating over lists
- Exceptions
- Timing
- DMA - prerecording sequences of events

More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)



# DMA

```
@kernel
def record(self):
    with self.core_dma.record("pulses"):
        # all RTIO operations now go to the "pulses"
        # DMA buffer, instead of being executed immediately.
        for i in range(50):
            self.ttl0.pulse(100*ns)
            delay(100*ns)

@kernel
def run(self):
    self.core.reset()
    self.record()
    # prefetch the address of the DMA buffer
    # for faster playback trigger
    pulses_handle = self.core_dma.get_handle("pulses")
    self.core.break_realtime()
    while True:
        # execute RTIO operations in the DMA buffer
        # each playback advances the timeline by 50*(100+100) ns
        self.core_dma.playback_handle(pulses_handle)
```

TTL methods:

- ttl.on()
- ttl.off()
- ttl.pulse(*duration*)

Timing functions:

- delay(*duration*)

Duration examples:

4 \* us; 400 \* ns

Dashboard arguments:

- Delay - time between next edge event

min. value: 10 ns

max. value: 1000 ns

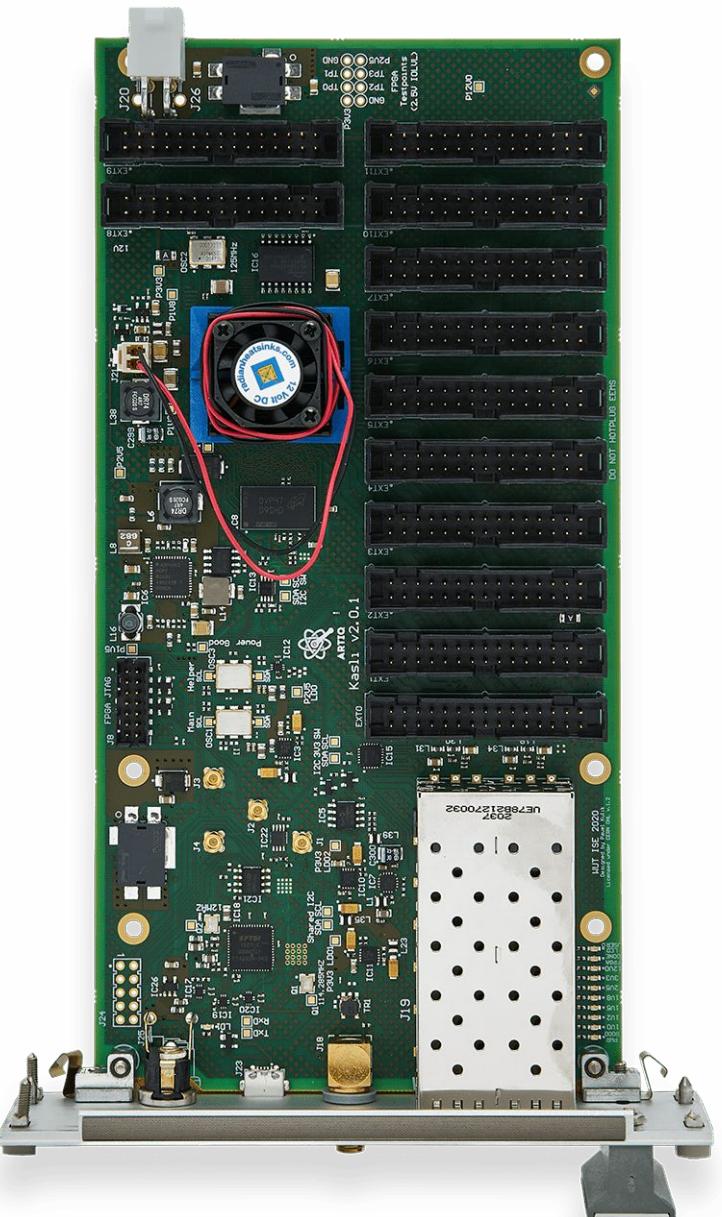
working min. value: ~195ns

**Goal:** create the same loop as in timing2 exercise but using DMA (100 iterations of loop + 100 iterations over DMA record)

# What can I do in the FPGA?

- Subset of Python
- Conditionals (if)
- Loops, iterating over lists
- Exceptions
- Timing
- DMA
- RPC

More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)

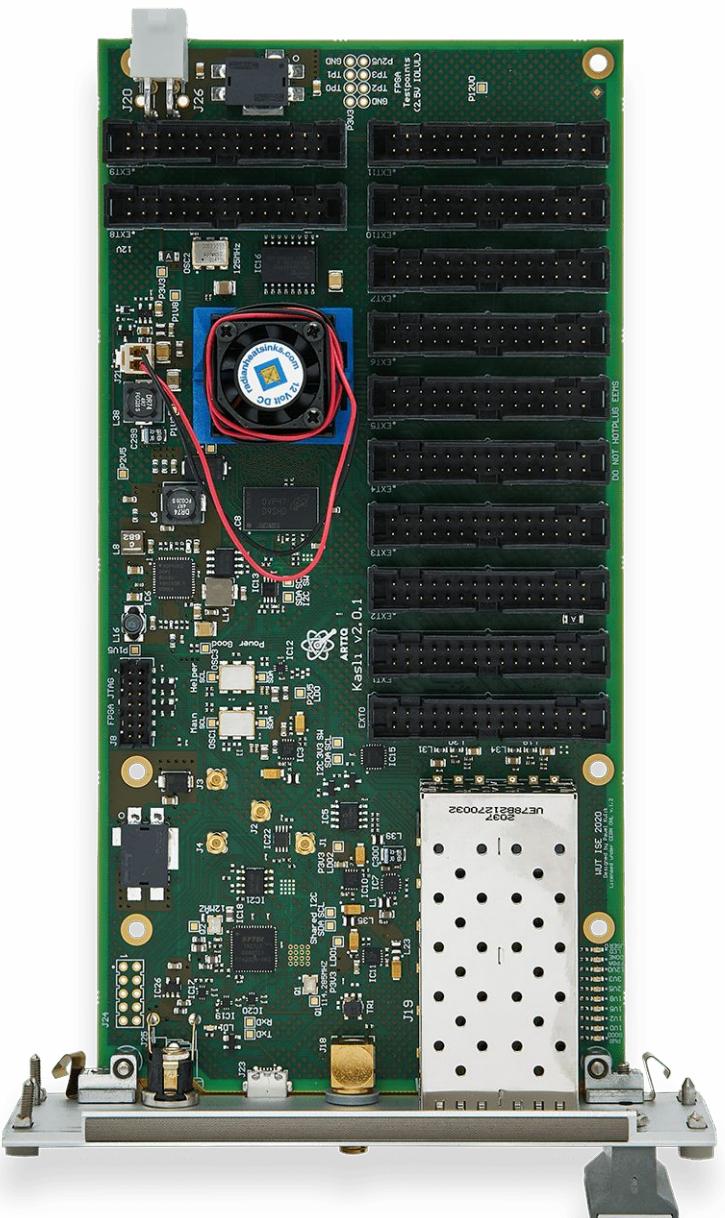


# RPC - remote procedure call

```
def input_led_state() -> TBool:
    return input("Enter desired LED state: ") == "1"

class LED(EnvExperiment):
    def build(self):
        self.setattr_device("core")
        self.setattr_device("led")

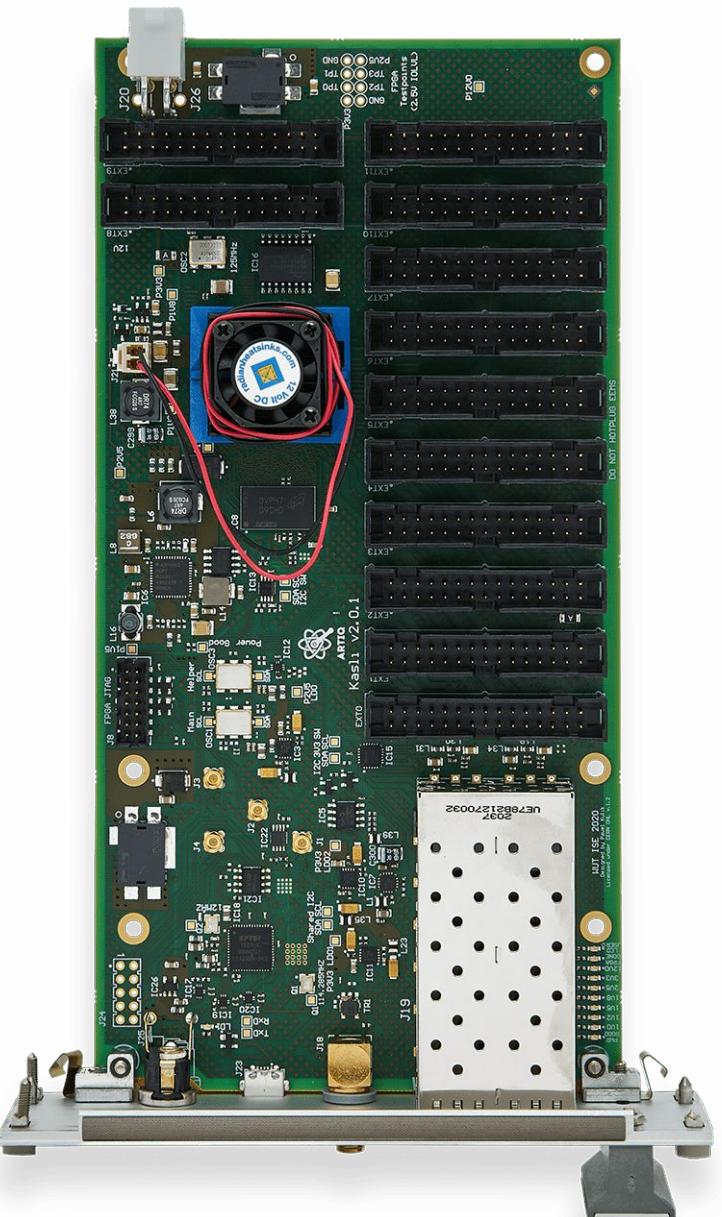
    @kernel
    def run(self):
        self.core.reset()
        s = input_led_state()
        self.core.break_realtime()
        if s:
            self.led.on()
        else:
            self.led.off()
```



# What can I do in the FPGA?

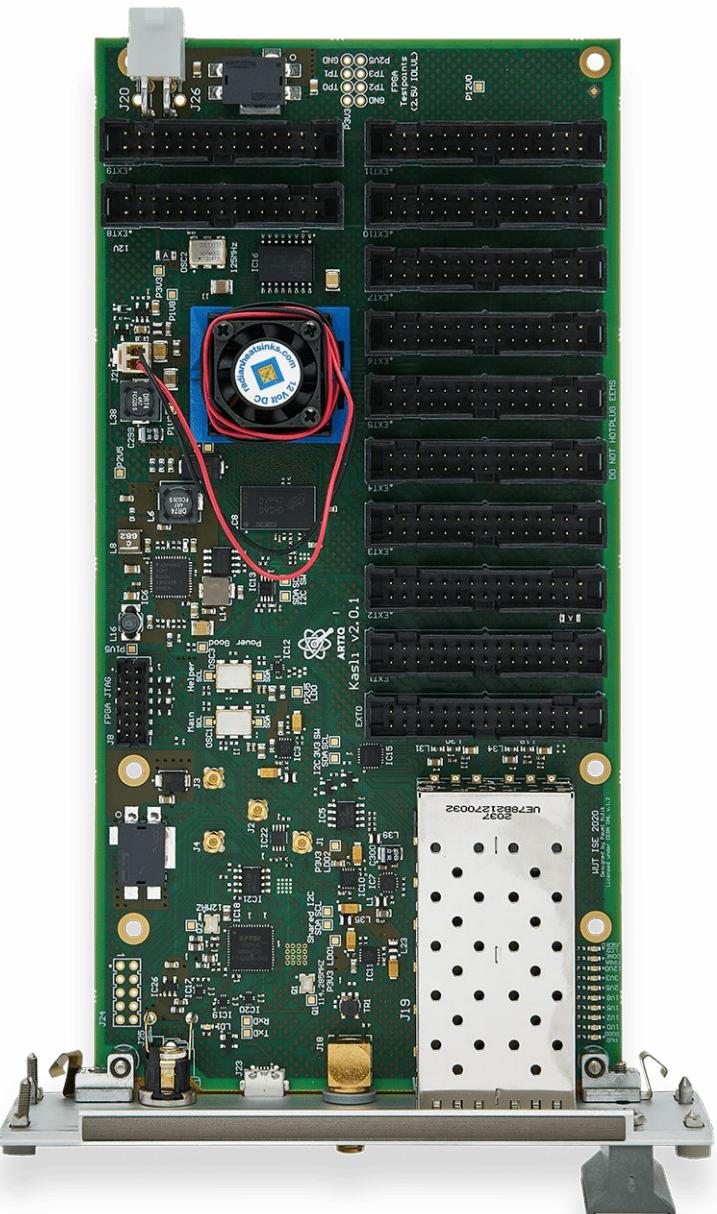
- Subset of Python
- Conditionals (if)
- Loops, iterating over lists
- Exceptions
- Timing
- DMA - prerecording sequences of events
- RPC
- Parallel operation

More detailed description: [m-labs.hk/artiq/manual/compiler.html](http://m-labs.hk/artiq/manual/compiler.html)



# Parallel and sequential blocks

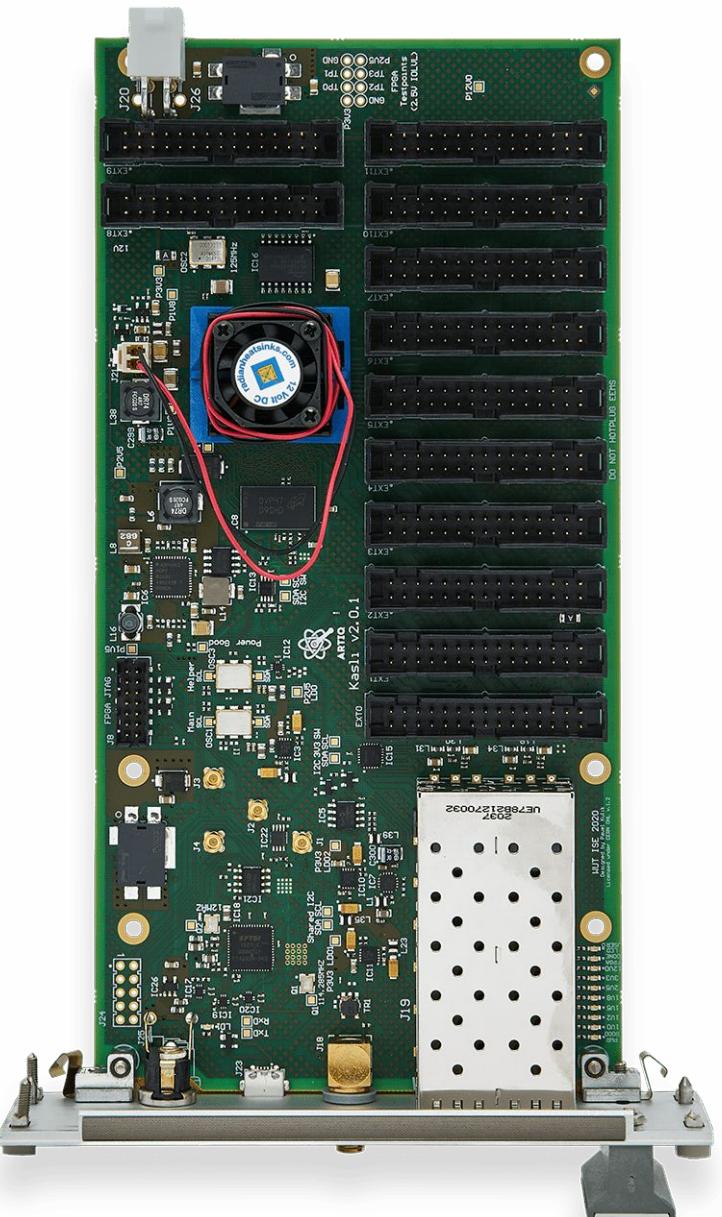
```
for i in range(1000000):
    with parallel:
        self.ttl0.pulse(2*us)
        self.ttl1.pulse(4*us)
    delay(4*us)
```



# Parallel and sequential blocks

```
for i in range(1000000):
    with parallel:
        self.ttl0.pulse(2*us)
        self.ttl1.pulse(4*us)
    delay(4*us)
```

```
for i in range(1000000):
    with parallel:
        with sequential:
            self.ttl0.pulse(2*us)
            delay(1*us)
            self.ttl0.pulse(1*us)
            self.ttl1.pulse(4*us)
    delay(4*us)
```



# Exercise: Synchronised TTL and DDS pulses

## TTL methods:

- `ttl.pulse(duration)`

## Timing functions:

- `delay(duration)`

## Duration examples:

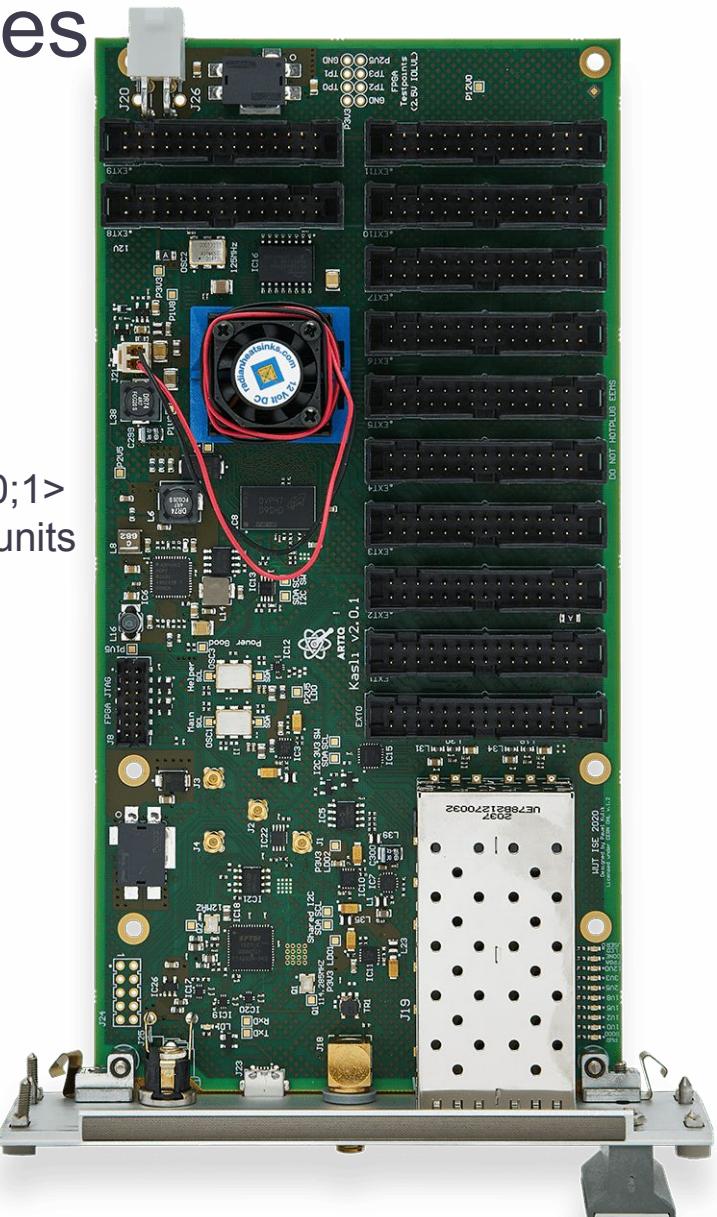
4 \* us; 400 \* ns

## Urukul channels methods:

- `channel.init()`
  - `channel.set(`  
*freq* - Float frequency in Hz  
*phase* - Float phase tuning word in turns  
*amplitude* - Float amplitude in units of full scale <0;1>
  - `channel.set_att(att)` - *att* - Float attenuator in SI units [0, 31.5 dB]
  - `channel.sw.on()`
  - `channel.sw.off()`

**Goal:** At the same time start ttl.pulse(200\*ns) and switch on both Urukul channels. Switch off first Urukul channel after 200 ns and second after 400 ns. Run second TTL pulse (100 ns wide) exactly 100 ns after first pulse. Manipulate time only with delay function.

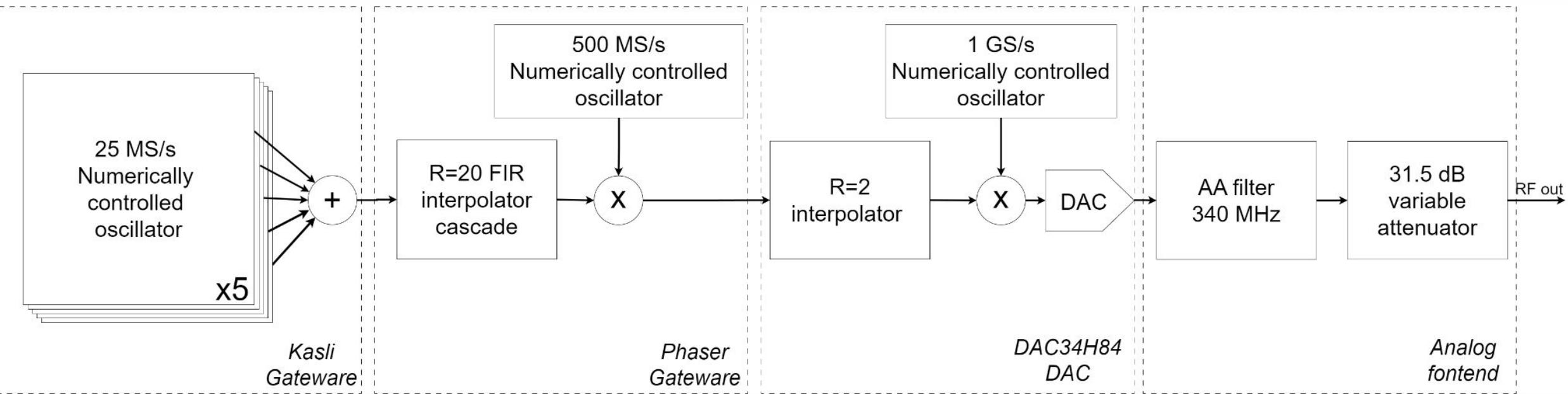
**Use parallel and sequential blocks.**

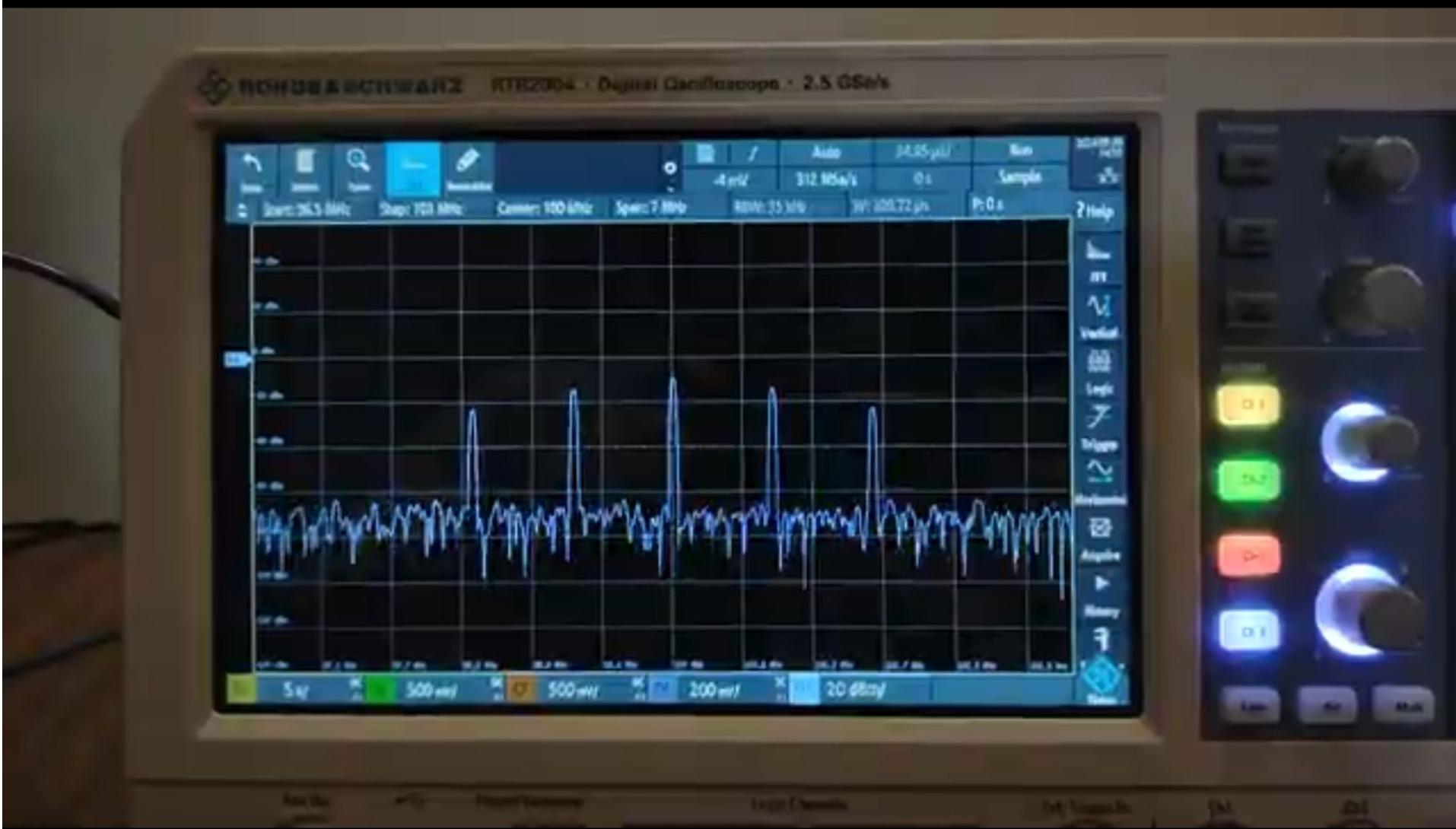


# Exercise: Synchronised TTLs and DDS pulses



# Demonstration: Phaser AWG





# Demonstration: Phaser AWG

```
def build(self):
    self.setattr_device("core")
    self.setattr_device("core_dma")
    self.setattr_device("phaser0")

    self.center_f = 97 * MHz

    freq_slopes = [
        np.linspace(2.8 * MHz, 1 * MHz, 100),
        np.linspace(2.9 * MHz, 2 * MHz, 100),
        np.full(100, 3 * MHz),
        np.linspace(3.1 * MHz, 4 * MHz, 100),
        np.linspace(3.2 * MHz, 5 * MHz, 100),
    ]

    amp_slopes = [
        np.linspace(0.375, 0.01, 100) * 0.9,
        np.linspace(0.10, 0.25, 100) * 0.9,
        np.linspace(0.05, 0.48, 100) * 0.9,
        np.linspace(0.10, 0.25, 100) * 0.9,
        np.linspace(0.375, 0.01, 100) * 0.9,
    ]

    # Make sure that summed amps never exceed 1.0 (full scale)
    assert all(sum(amps) <= 1.0 for amps in zip(*amp_slopes))

    self.ftw = [np.concatenate([slope, slope[::-1]]) for slope in freq_slopes]
    self.amps = [np.concatenate([slope, slope[::-1]]) for slope in amp_slopes]
    self.length = len(self.ftw[0])
```

# Demonstration: Phaser AWG

```
@kernel
def init(self):
    self.core.reset()
    self.core.break_realtime()

    self.phaser0.init()

@kernel
def run(self):
    self.init()

    phaser = self.phaser0

    phaser.channel[0].set_att(0 * dB)
    phaser.channel[0].set_duc_frequency(self.center_f)
    phaser.channel[0].set_duc_phase(0.25)
    phaser.channel[0].set_duc_cfg()

    delay(0.1 * ms)
    phaser.duc_stb()
    delay(0.1 * ms)

    while True:
        for i in range(self.length):
            for osc in range(5):
                phaser.channel[0].oscillator[osc].set_frequency(self.ftw[osc][i])
                phaser.channel[0].oscillator[osc].set_amplitude_phase(
                    self.amps[osc][i], phase=0.25)
                delay(5 * ms)
```

# Demonstration: Phaser AWG

```
@kernel
def init(self):
    self.core.reset()
    self.core.break_realtime()

    self.phaser0.init()

@kernel
def run(self):
    self.init()

    phaser = self.phaser0

    phaser.channel[0].set_att(0 * dB)
    phaser.channel[0].set_duc_frequency(self.center_f)
    phaser.channel[0].set_duc_phase(0.25)
    phaser.channel[0].set_duc_cfg()

    delay(0.1 * ms)
    phaser.duc_stb()
    delay(0.1 * ms)

    while True:
        for i in range(self.length):
            for osc in range(5):
                phaser.channel[0].oscillator[osc].set_frequency(self.ftw[osc][i])
                phaser.channel[0].oscillator[osc].set_amplitude_phase(
                    self.amps[osc][i], phase=0.25)
                delay(5 * ms)
```

# Demonstration: Phaser AWG

```
@kernel
def init(self):
    self.core.reset()
    self.core.break_realtime()

    self.phaser0.init()

@kernel
def run(self):
    self.init()

    phaser = self.phaser0

    phaser.channel[0].set_att(0 * dB)
    phaser.channel[0].set_duc_frequency(self.center_f)
    phaser.channel[0].set_duc_phase(0.25)
    phaser.channel[0].set_duc_cfg()

    delay(0.1 * ms)
    phaser.duc_stb()
    delay(0.1 * ms)

    while True:
        for i in range(self.length):
            for osc in range(5):
                phaser.channel[0].oscillator[osc].set_frequency(self.ftw[osc][i])
                phaser.channel[0].oscillator[osc].set_amplitude_phase(
                    self.amps[osc][i], phase=0.25)
                delay(5 * ms)
```

# Demonstration: Phaser AWG

```
@kernel
def init(self):
    self.core.reset()
    self.core.break_realtime()

    self.phaser0.init()

@kernel
def run(self):
    self.init()

    phaser = self.phaser0

    phaser.channel[0].set_att(0 * dB)
    phaser.channel[0].set_duc_frequency(self.center_f)
    phaser.channel[0].set_duc_phase(0.25)
    phaser.channel[0].set_duc_cfg()

    delay(0.1 * ms)
    phaser.duc_stb()
    delay(0.1 * ms)

while True:
    for i in range(self.length):
        for osc in range(5):
            phaser.channel[0].oscillator[osc].set_frequency(self.ftw[osc][i])
            phaser.channel[0].oscillator[osc].set_amplitude_phase(
                self.amps[osc][i], phase=0.25)
            delay(5 * ms)
```

# Demonstration: Phaser AWG

```
@kernel
def init(self):
    self.core.reset()
    self.core.break_realtime()

    self.phaser0.init()

@kernel
def run(self):
    self.init()

    phaser = self.phaser0

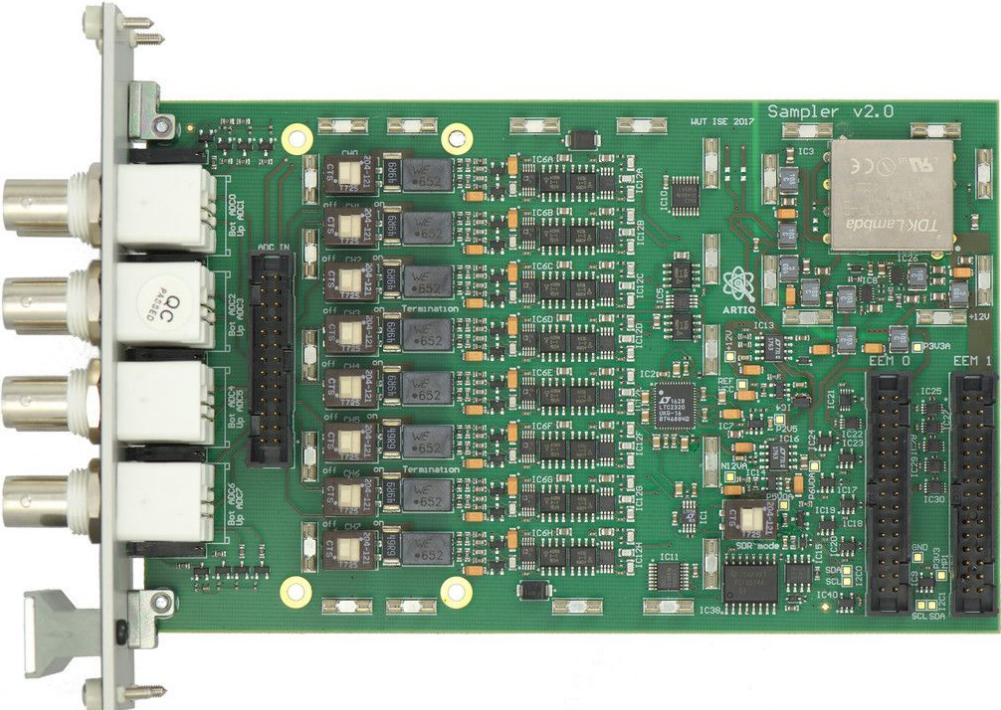
    phaser.channel[0].set_att(0 * dB)
    phaser.channel[0].set_duc_frequency(self.center_f)
    phaser.channel[0].set_duc_phase(0.25)
    phaser.channel[0].set_duc_cfg()

    delay(0.1 * ms)
    phaser.duc_stb()
    delay(0.1 * ms)

while True:
    for i in range(self.length):
        for osc in range(5):
            phaser.channel[0].oscillator[osc].set_frequency(self.ftw[osc][i])
            phaser.channel[0].oscillator[osc].set_amplitude_phase(
                self.amps[osc][i], phase=0.25)
            delay(5 * ms)
```

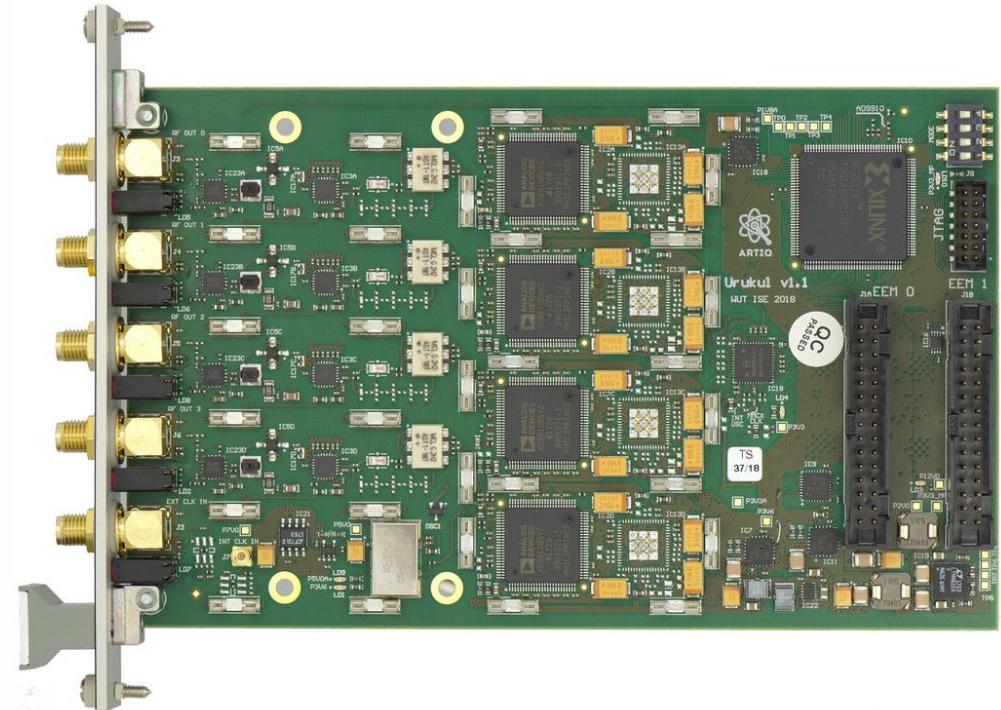
# Use cases

Sampler ADC



+

Urukul DDS



# Use cases

Frame Grabber

+

Camera

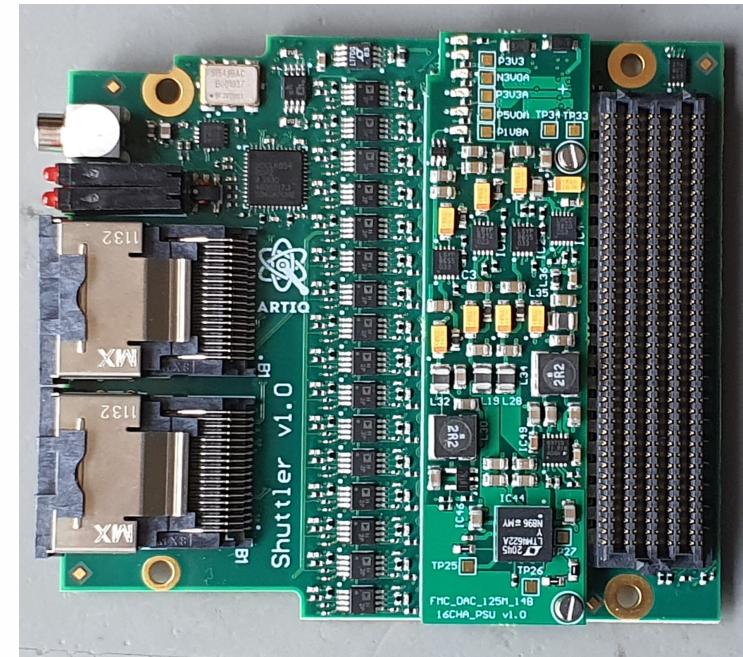
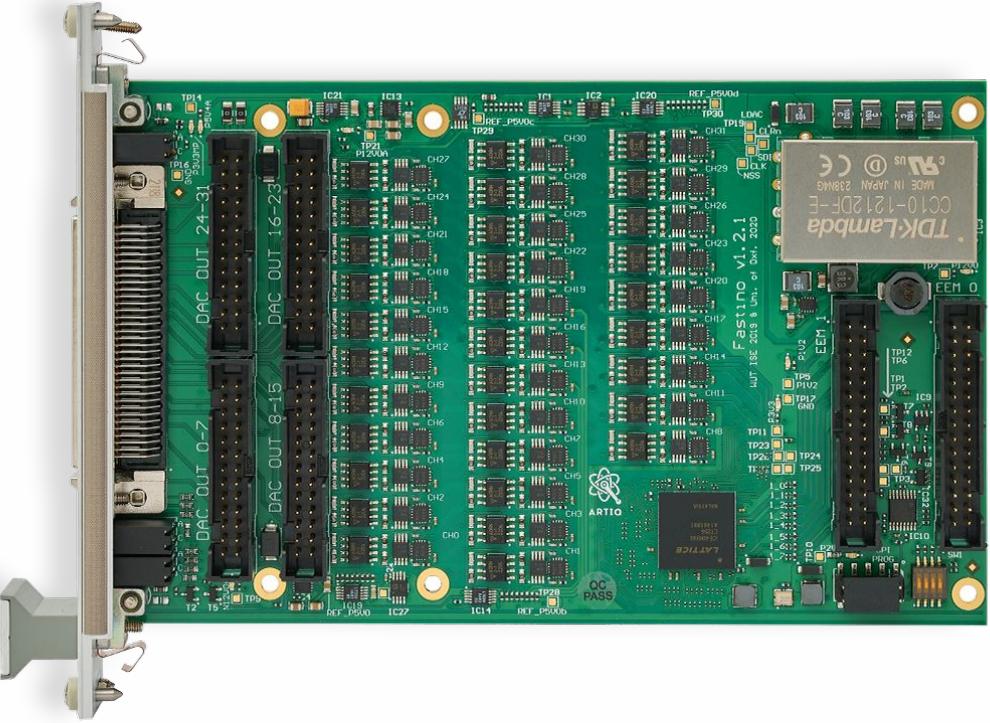


# Use cases

Fastino

or

Shuttler



[https://github.com/elhep/artiq\\_dax tutorial materials](https://github.com/elhep/artiq_dax_tutorial_materials)

If you have any questions, feel free to contact us:

- pawel.kulik@pw.edu.pl
- tomasz.przywozki@pw.edu.pl
- mikolaj.sowinski@pw.edu.pl

