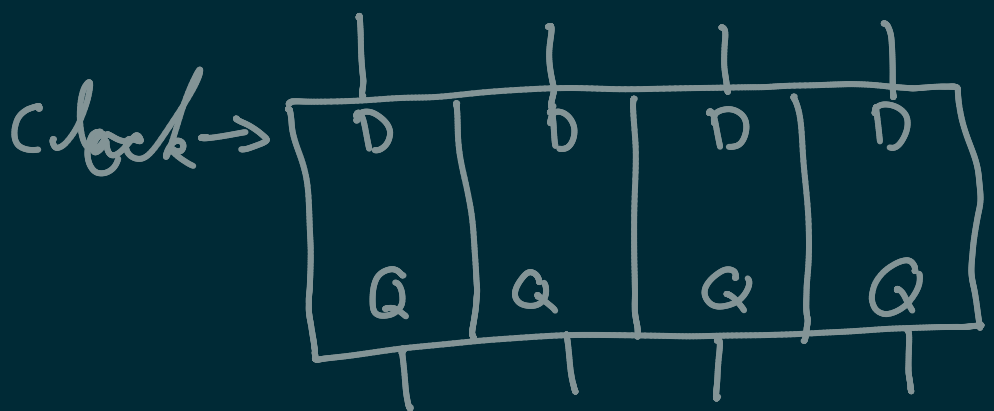
Register

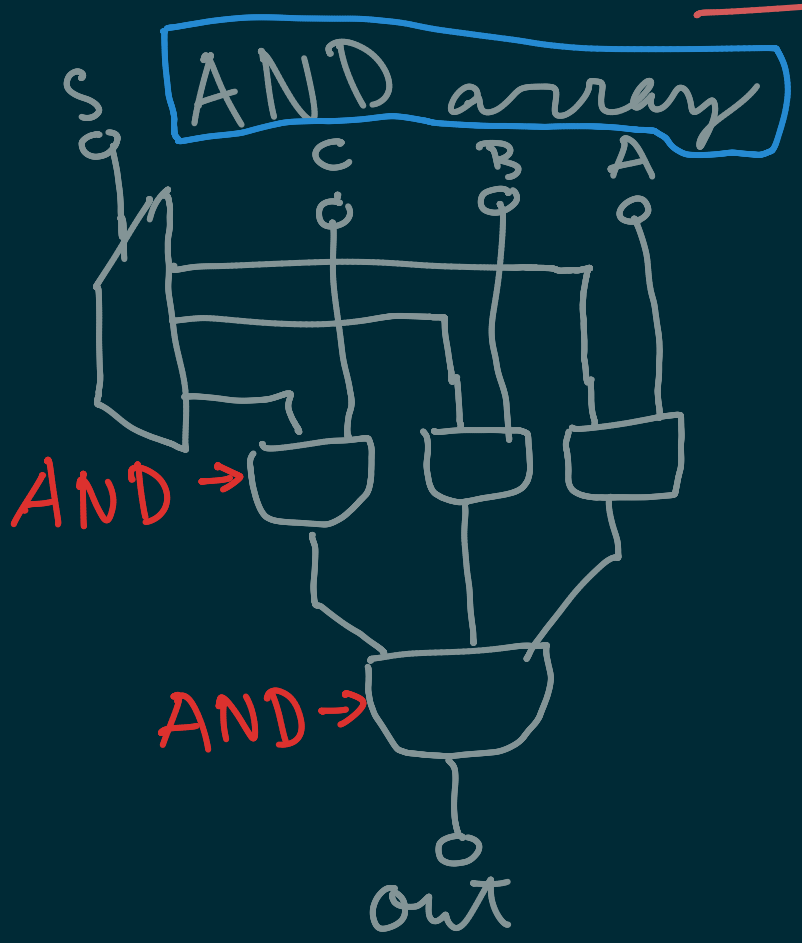
Flip flop = 1 bit memory cell

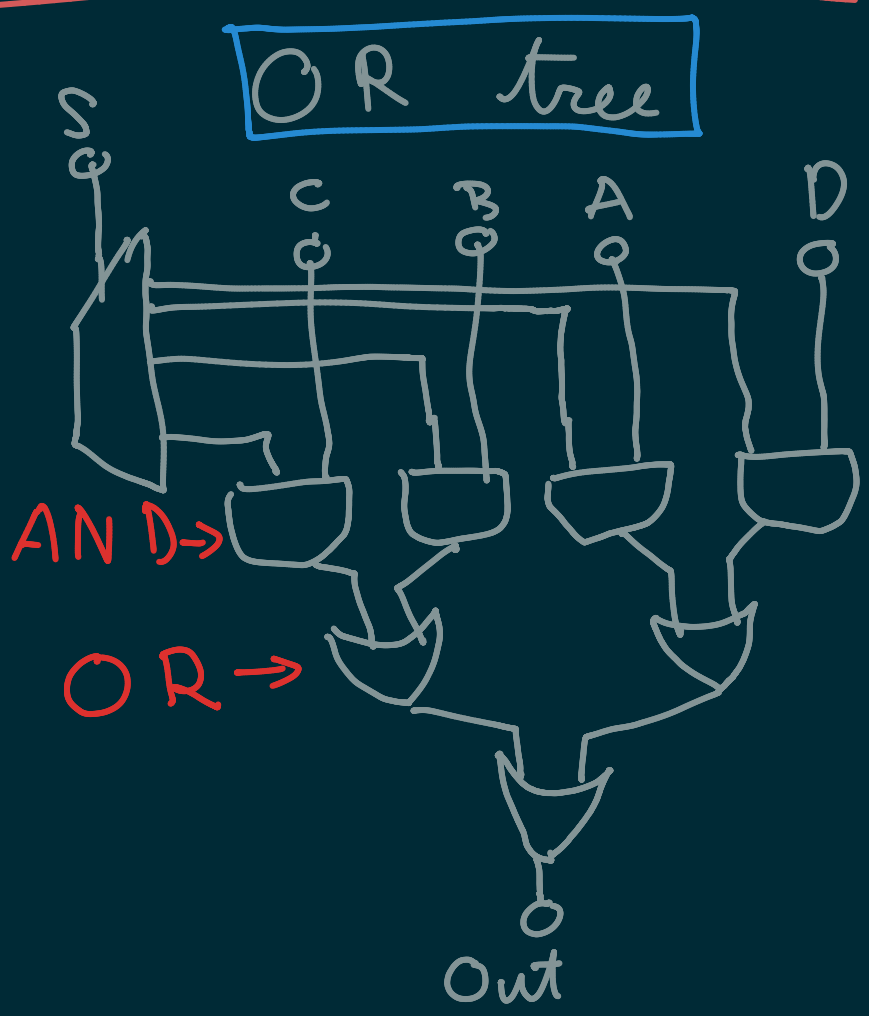
Register = group of n register

4 bit register : 4 flipflops : 4 bits word

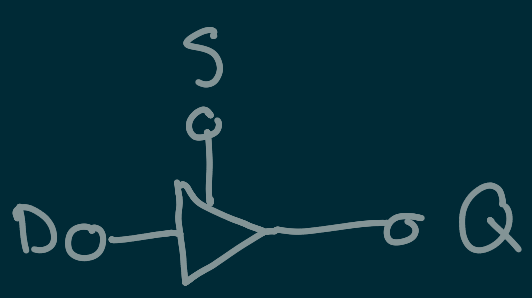


SRAM Multiplexer



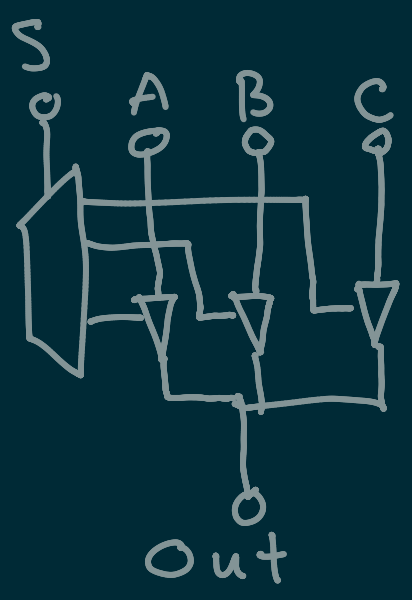


Tri-State buffer



S	Q
0	Z (High Impedance)
1	D

SRAM Multiplexer with tri-state buffers

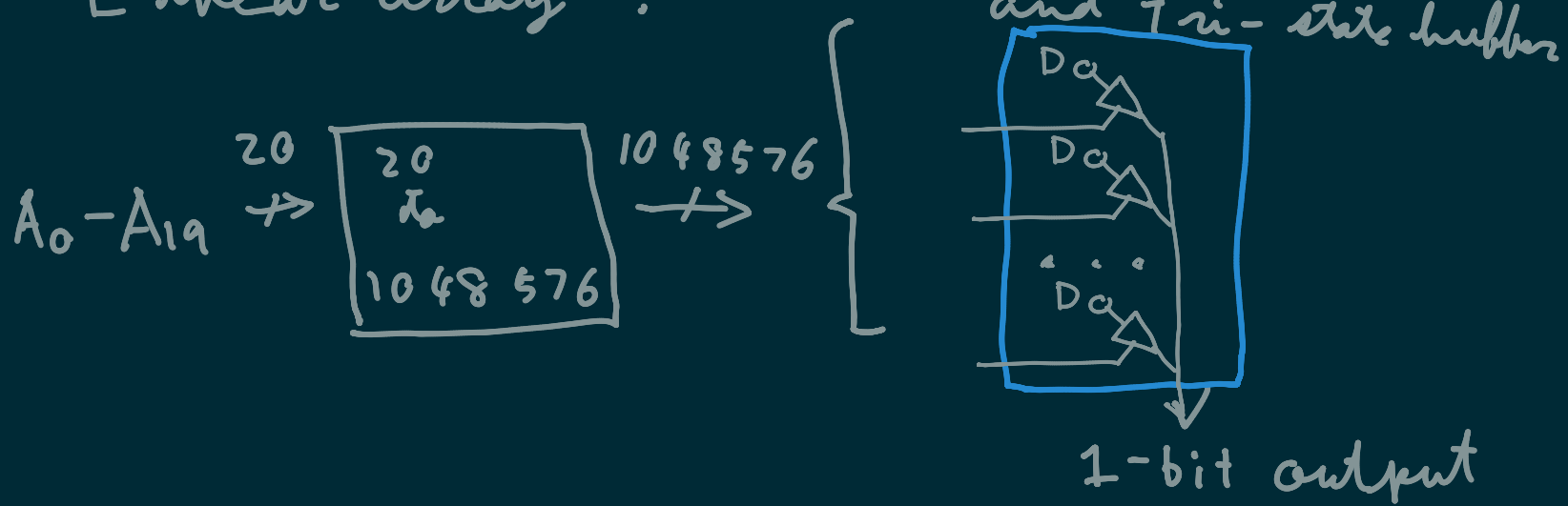


Only one tri-state buffer must be active at a time (otherwise short-circuit)

SRAM Decoder

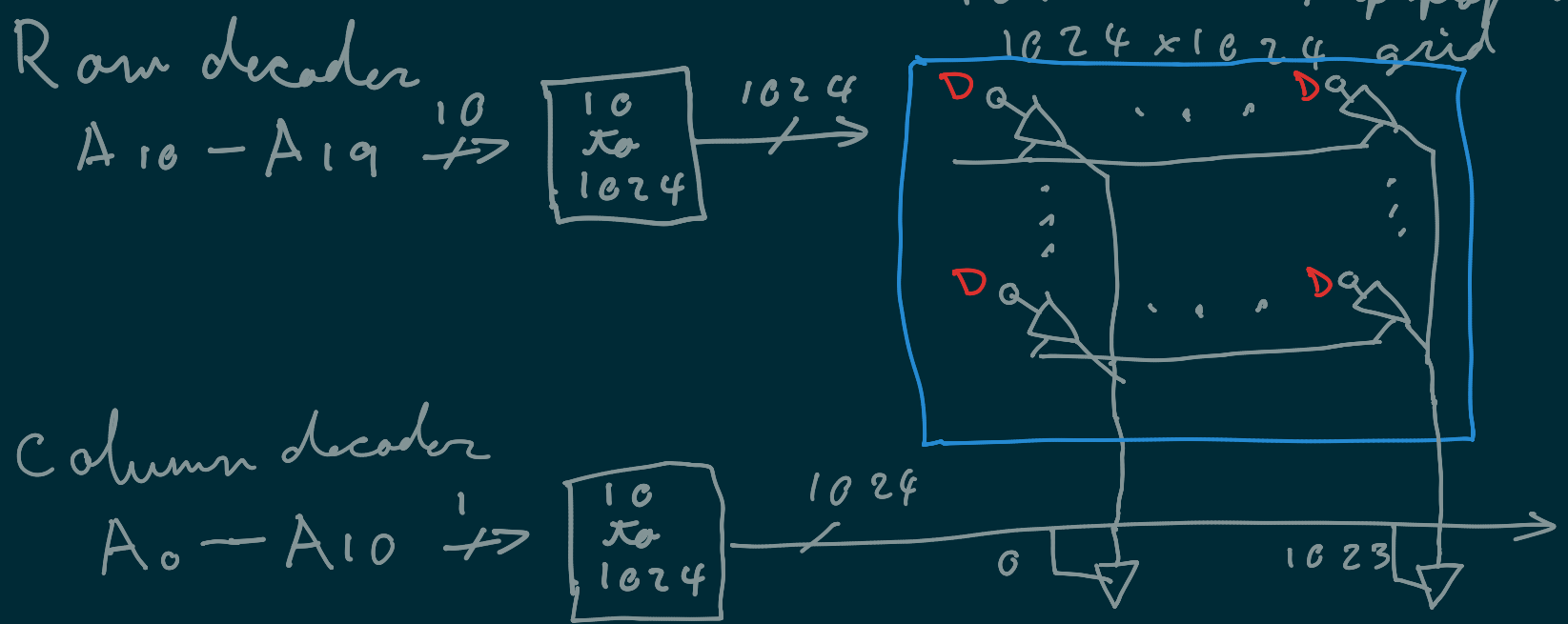
Linear array :

1048576 D flip flop and Tri-state buffer



Rectangle array :

1048576 D flip flop in 1024×1024 grid



SRAM

- Data in D-Latch
- 4 - 6 transistors per bit

DRAM ← better

- Data in capacitor
- 1 transistors per bit