

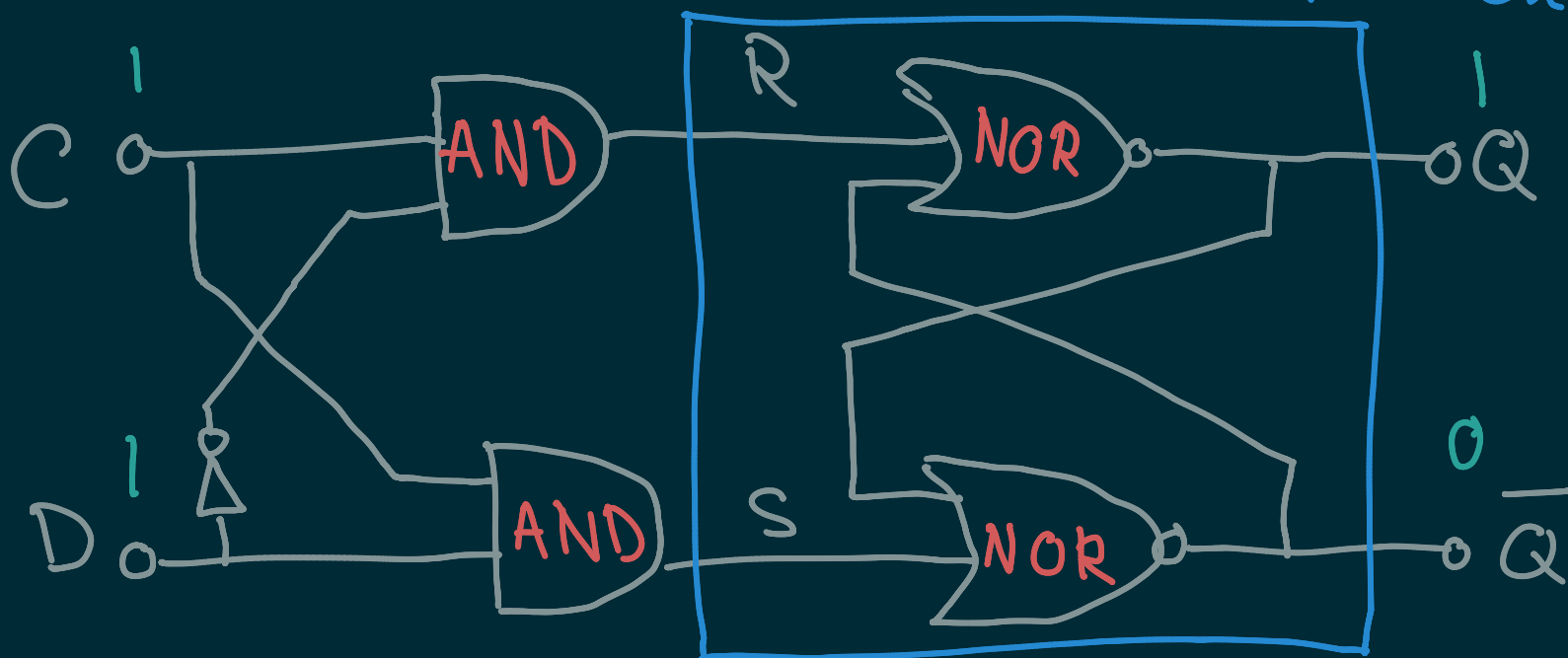
## Set Reset Latch



| S | R | Output      |
|---|---|-------------|
| 0 | 0 | No change   |
| 1 | 0 | $Q = 1$     |
| 0 | 1 | $Q = 0$     |
| 1 | 1 | Not allowed |

## Data Latch

SR Latch



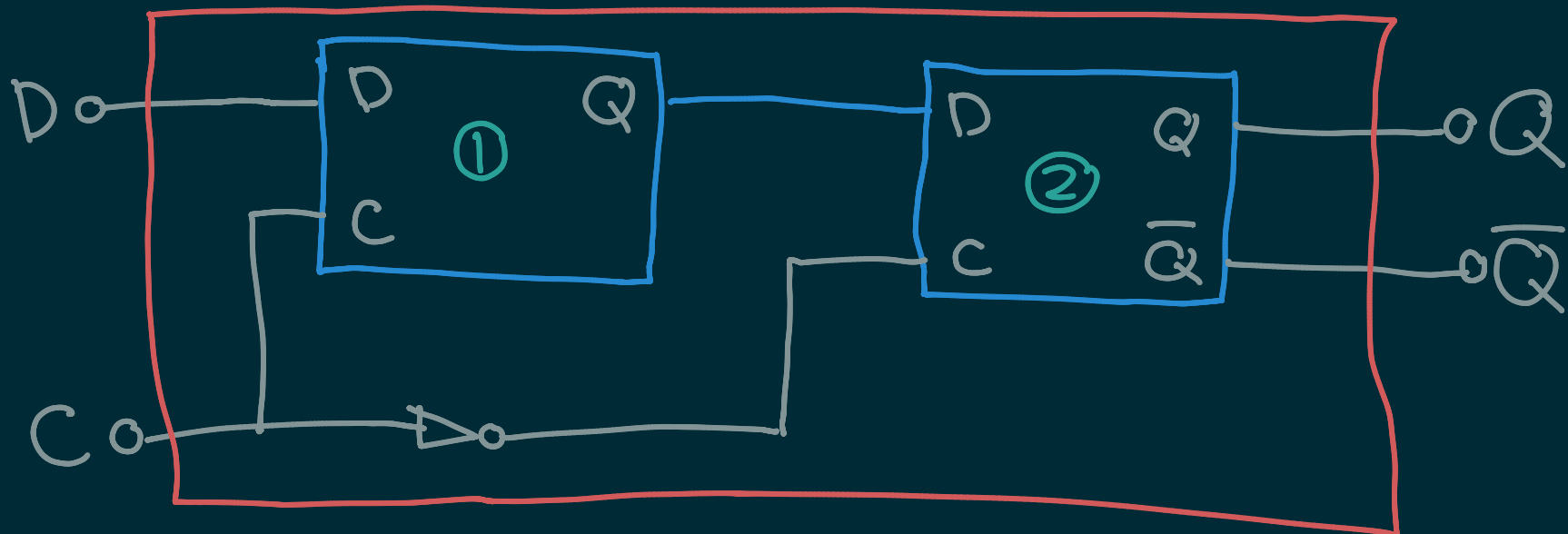
Impossible for R and S to both be 1

| C | D   | Outcome |
|---|-----|---------|
| 0 | Any | Hold    |
| 1 | 1   | $Q = 1$ |
| 1 | 0   | $Q = 0$ |

When C is 1, Q has same value as D

# D flip flop

## 2 D Latch



| C | Outcome      |
|---|--------------|
| 1 | Write D to ① |
| 0 | Write ① to ② |

## Multiplexer

Given  $n$  signals, need  $\log_2 n$  selector input

3-8 Decoder:

