SetResetLatch

R 0 o ⸰

NOR

0 ⸰Q

1

0

0 ⸰ 0

S 0 o⸰

NOR

1 ⸰ $\bar{Q}$

S	R	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Not allowed

Data Latch

SR Latch

1

C o

AND

R

NOR

1 ⸰Q

1

D o

AND

S

NOR

0 ⸰ $\bar{Q}$
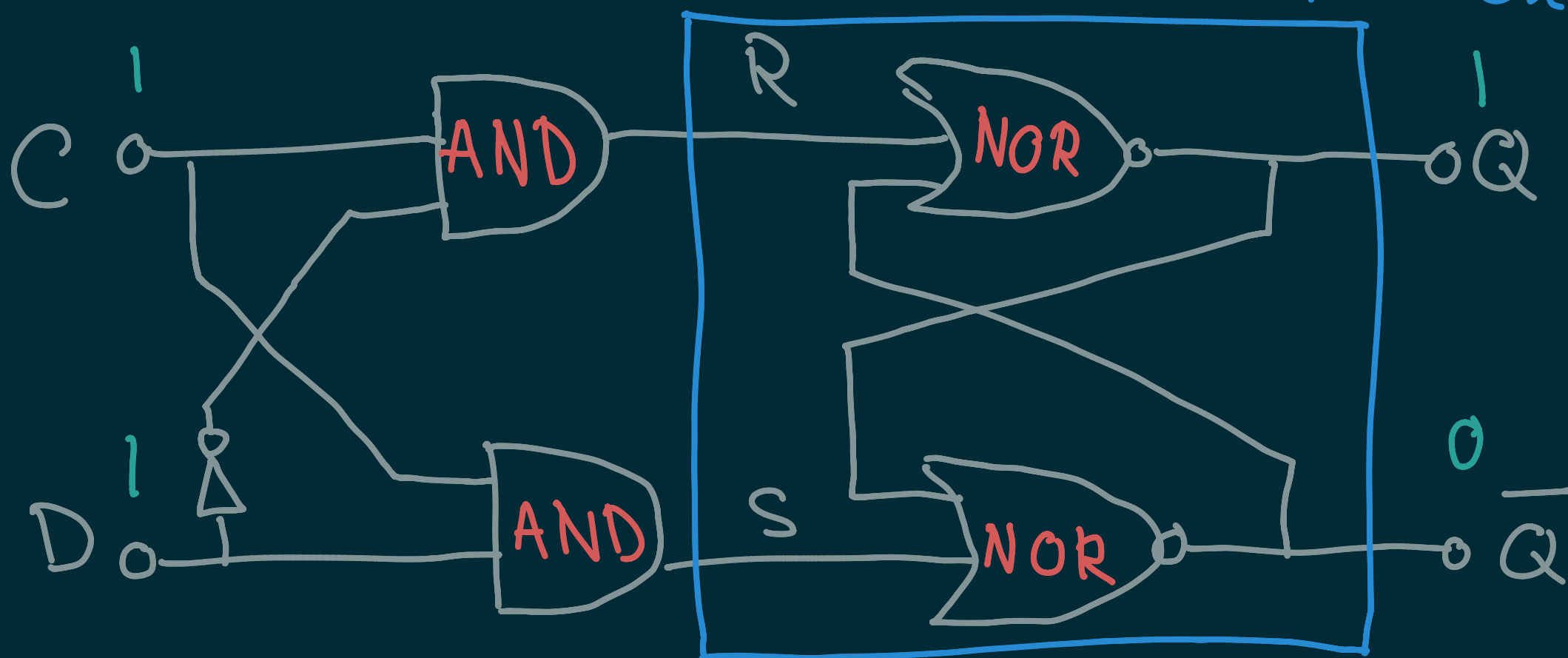
Impossible for R and S to both be 1

C	D	Outcome
0	Any	Hold
1	1	Q = 1
1	0	Q = 0

When C is 1, Q has same value as D

D flip flop

2 D Latch
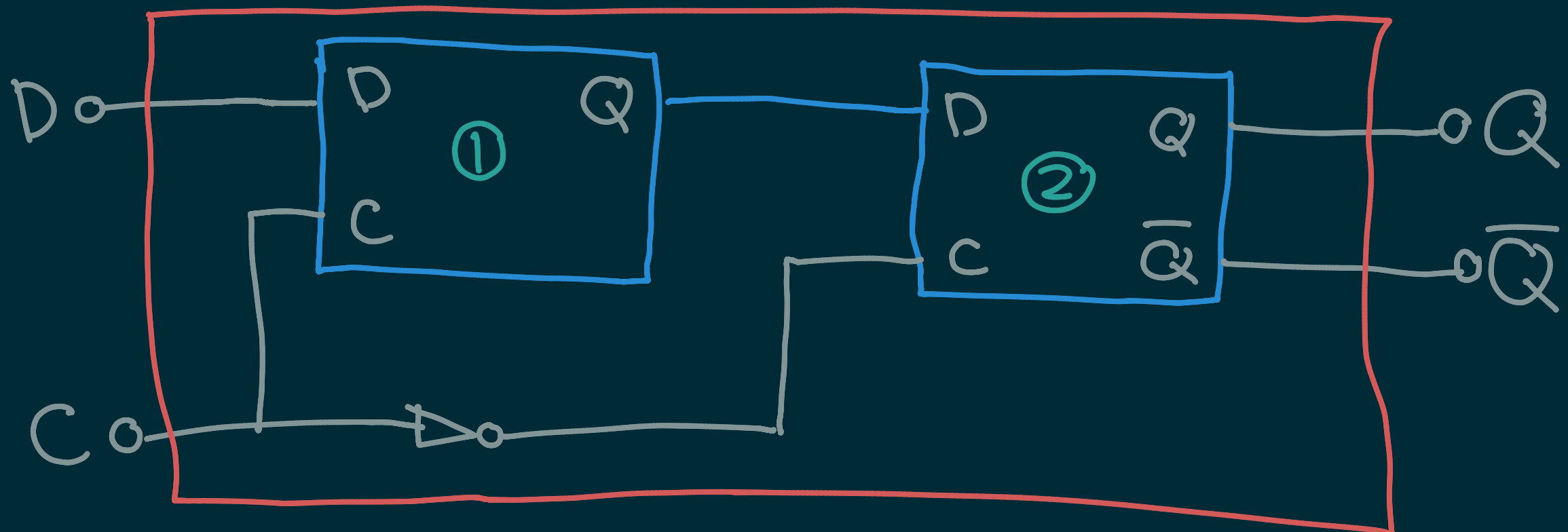
C	Outcome
1	Write D to ①
0	Write ① to ②

Multiplexer

Given n signals, need $\log_2 n$ selector input

3 - 8 Decoder:

Decoder→ generates n signals

← n AND gates to combine signal

← 1 OR gate to compute result