FPGA Ethernet Communication

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Objectives

The primary objective of our final project was to establish basic ethernet communication between a computer and an FPGA. We also wanted to connect the ethernet communication to a basic Arithmetic Logic Unit that we had previously implemented.

Ethernet IPs Explored

Alex Forencich Ethernet IP

The first Ethernet IP we explored was the Alex Forencich Ethernet IP. This IP is a widely used open-source Ethernet MAC implementation for FPGAs. However, Alex Forencich does not have an ethernet IP for the Nexys 4 DDR or the Nexyz A7, and attempts to utilize the IP designed for the Nexys video was unsuccessful as the boards use di□erent ethernet standards.

"FPGAs for Beginners" YouTube tutorial

We were able to find and follow along with a YouTube tutorial series by "FPGAs for Beginners" that walks through the process of using the FPGA's for Beginners Ethernet IP to create a basic ethernet communication with the Nexys A7 board. With this tutorial we were able to implement basic communication between the FPGA and a computer, allowing us to turn on leds and send values from switches to the computer. This seemed very promising, and we thought it would be simple to extend this and connect the ALU. However, we ran into challenges trying to expand on this IP. The IP was not documented and did not follow standard conventions, making it di□cult to understand and modify. We also ran into a learning curve of figuring out how to extend a Vivado block diagram project.

Nexys-4-DDR-Ethernet-MAC

After struggling with the previous IP, we decided to try the Nexys-4-DDR-Ethernet-MAC IP. This IP was better documented, and was easier to understand and modify. It also did not use a Vivado block diagram. Using this IP, we were working on basic ethernet communication allowing the board to echo back and send values to the leds. However due to time constraints we were unable to fully debug this functionality or connect it to the ALU.