Homework 1: UART Arithmetic Logic Unit

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1 Introduction

In this assignment I created an Arithmetic Logic Unit (ALU) that can perform a variety of operations on integers. The ALU supports the following operations:

- Echo back input.
- Addition on a list of 32-bit integers.
- Multiplication on a list of 32-bit signed integers.
- Division on a pair of 32-bit signed integers.

The ALU is designed to be implemented on an iCEBreaker FPGA board and communicates with a host computer via a UART interface. This project is implemented in SystemVerilog.

2 Technical Details

2.1 Hardware

Target: iCEBreaker v1.0 FPGA board.
UART Baud Rate: 115200.
UART Payload Size: 8 bits.
UART Stop Bits: 1.
No UART Parity.

Commands