Politecnico di Torino

From HDL to CMOS

An overview on digital circuit design and implementation

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What is HDL?

Hardware
Description
Language

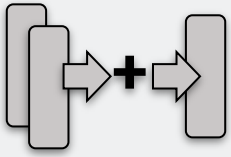
A specialized computer language used to describe the structure and behavior of electronic circuits.

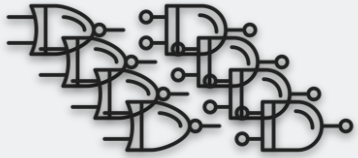
It is primarily used for designing application-specific integrated circuits (ASICs) and programming field-programmable gate arrays (FPGAs).

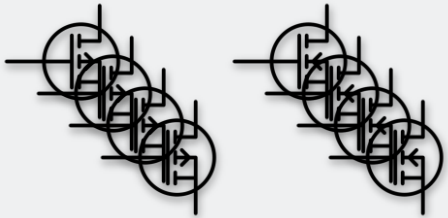
Most used HDL are Verilog, SystemVerilog and VHDL.

An abstraction level perspective

assign c = a + b;





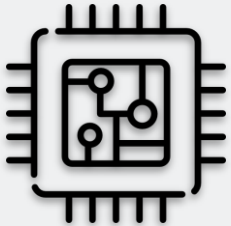


Behavioural description of the design

Intermediate representation

Gate level netlist

Transistor level netlist

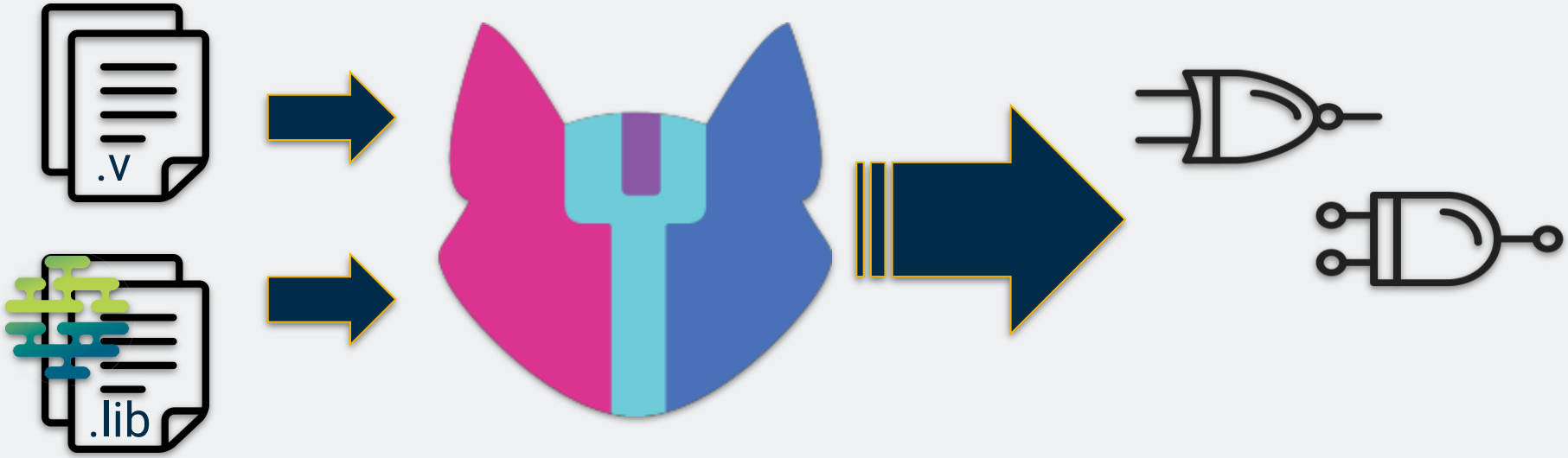


A flow overview - HDL

```
module counter_gen #(
  parameter NBIT = 4
) (
  input                clk,
  input                rstn,
  output reg [NBIT-1:0] out
);

  always @ (posedge clk, negedge rstn) begin
    if (! rstn)
        out <= 0;
    else
        out <= out + 1;
  end

endmodule
```

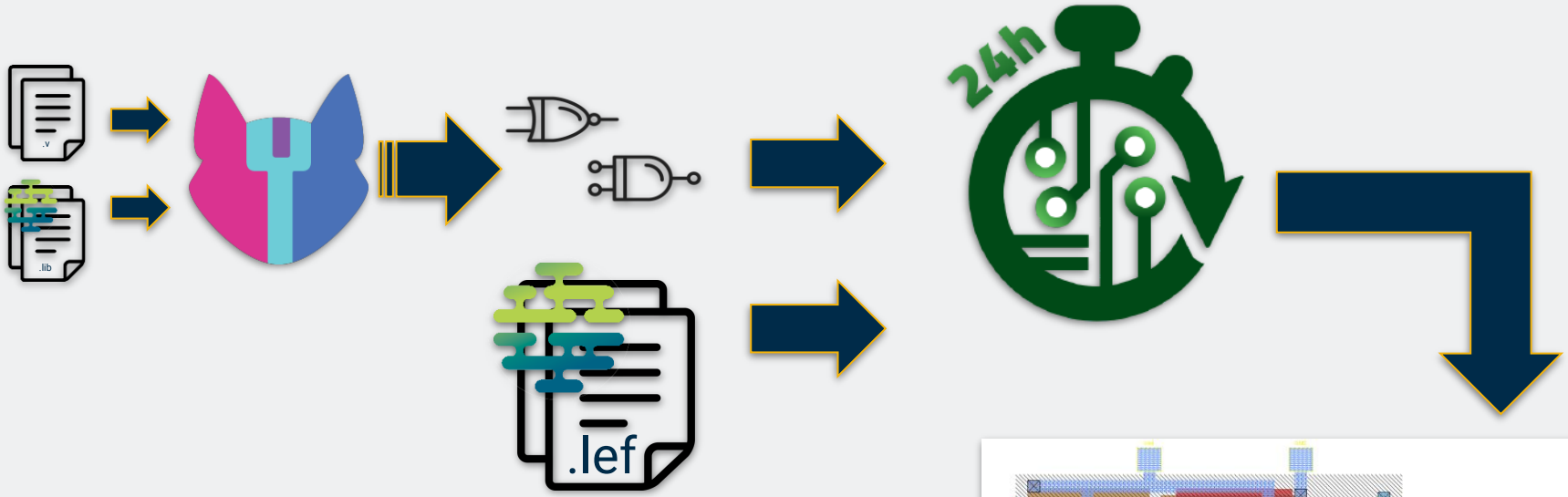
Behavioural description of the circuit

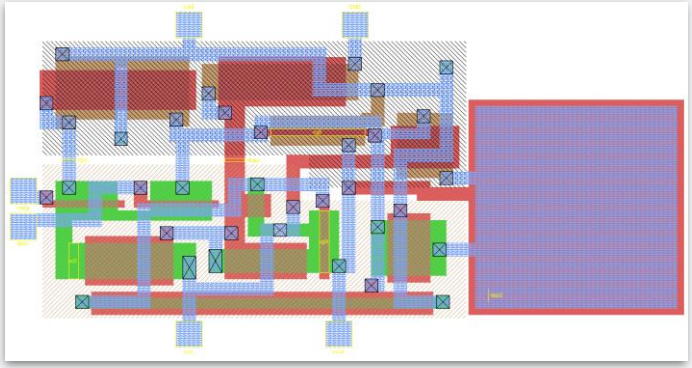
A flow overview - synthesis



Logic synthesis and optimization of the circuit

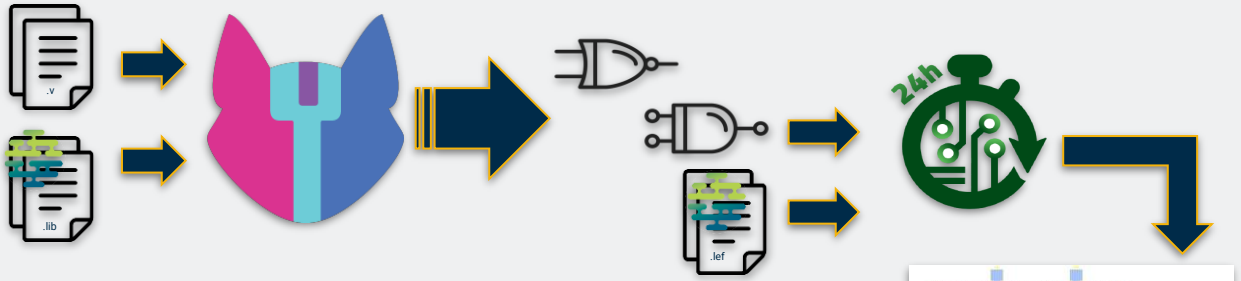
A flow overview - Place and route

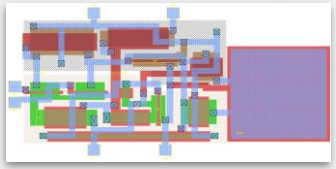


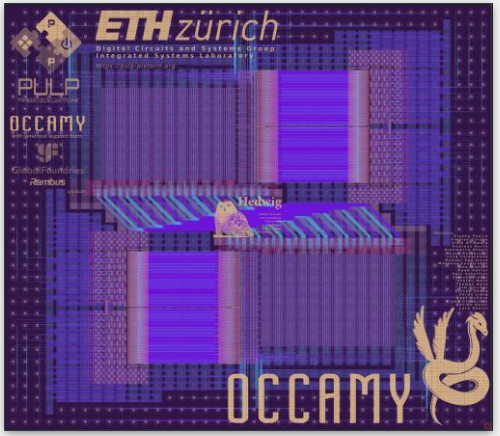


Physical implementation and
electrical optimization of the circuit

A flow overview - Tapeout and production





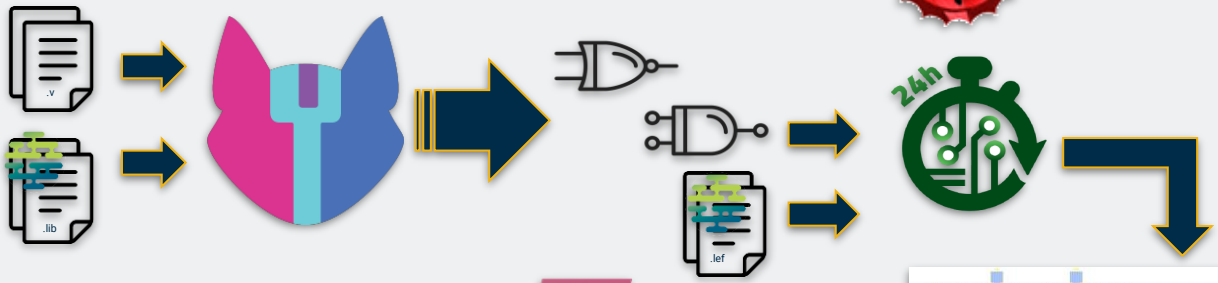


Production file generation and circuit tapeout

skywater

Will my circuit work?

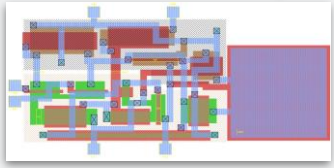
Logical simulation

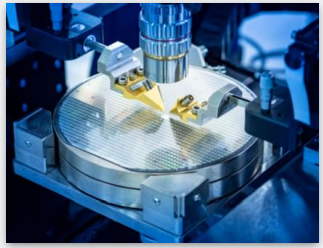


VERILATOR

Functional simulation

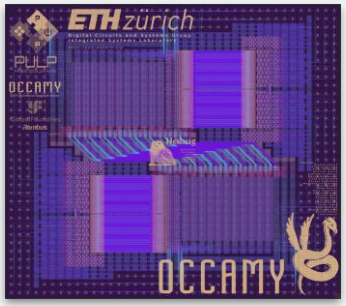
Electrical simulation





Post-silicon testing

skywater



SKY130

Google-Skywater 130 is an open source Process Design Kit (PDK)

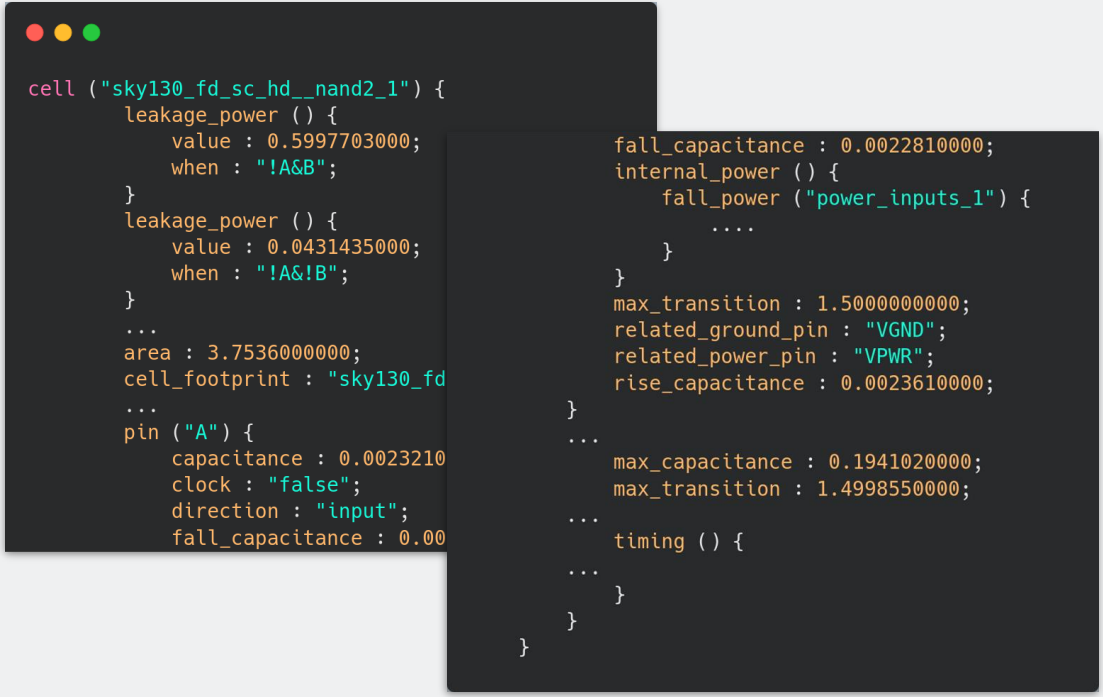
- simulation models

```
module sky130_fd_sc_hd__nand2 (
    Y,
    A,
    B
);

    // Module ports
    output Y;
    input  A;
    input  B;

    // Local signals
    wire nand0_out_Y;

    //   Name   Output       Other arguments
    nand nand0 (nand0_out_Y, B, A           );
    buf  buf0  (Y          , nand0_out_Y    );

endmodule
```

SKY130

Google-Skywater 130 is an open source Process Design Kit (PDK)

- simulation models
- timing and power models



SKY130

Google-Skywater 130 is an open source Process Design Kit (PDK)

- simulation models
- timing and power models
- geometry models

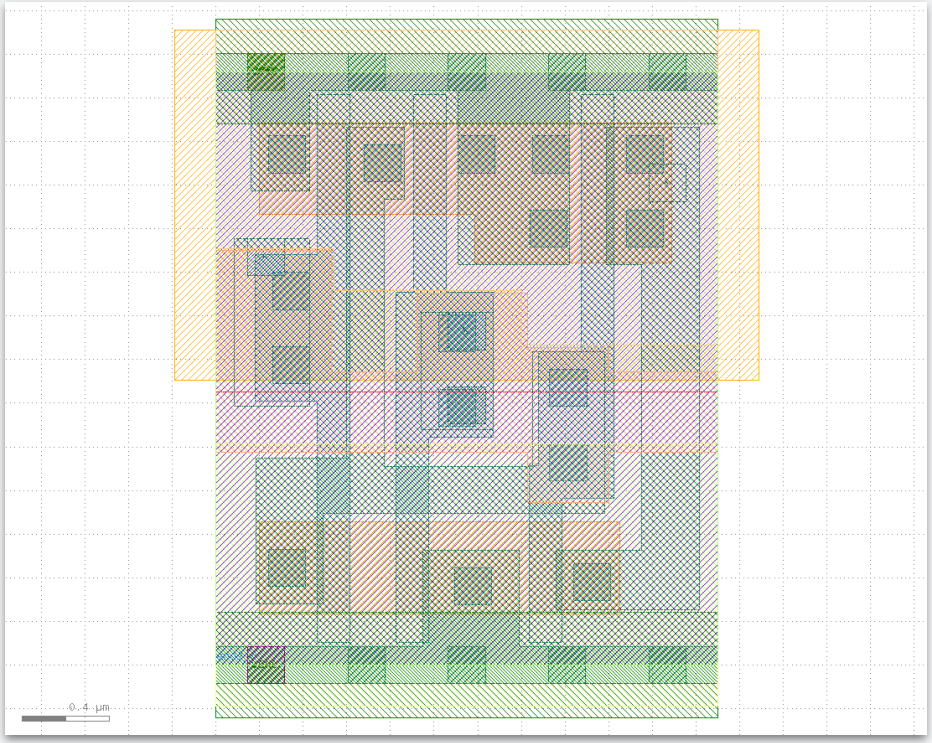
```
MACRO sky130_fd_sc_hd__nand2_1
  CLASS CORE ;
  FOREIGN sky130_fd_sc_hd__nand2_1 ;
  ORIGIN 0.000 0.000 ;
  SIZE 1.380 BY 2.720 ;
  SYMMETRY X Y R90 ;
  SITE unithd ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    ANTENNAGATEAREA 0.247500 ;
    PORT
      LAYER li1 ;
        RECT 0.940 1.075 1.275 1.32
    END
  END A
  ...
```

```
...
OBS
    LAYER li1 ;
      RECT 0.000 2.635 1.380 2.805 ;
      RECT 0.085 1.495 0.365 2.635 ;
      RECT 1.035 1.495 1.295 2.635 ;
      RECT 0.085 0.085 0.395 0.885 ;
      RECT 0.000 -0.085 1.380 0.085 ;
    LAYER mcon ;
      RECT 0.145 2.635 0.315 2.805 ;
      RECT 0.605 2.635 0.775 2.805 ;
      RECT 1.065 2.635 1.235 2.805 ;
      RECT 0.145 -0.085 0.315 0.085 ;
      RECT 0.605 -0.085 0.775 0.085 ;
      RECT 1.065 -0.085 1.235 0.085 ;
  END
END sky130_fd_sc_hd__nand2_1
```

SKY130

Google-Skywater 130 is an open source Process Design Kit (PDK)

- simulation models
- timing and power models
- geometry models
- layout

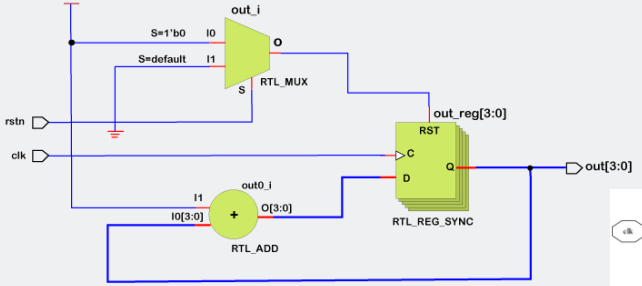


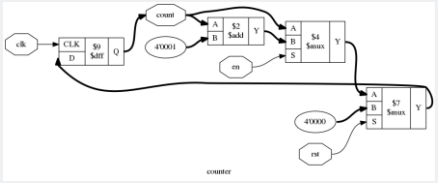
Synthesis

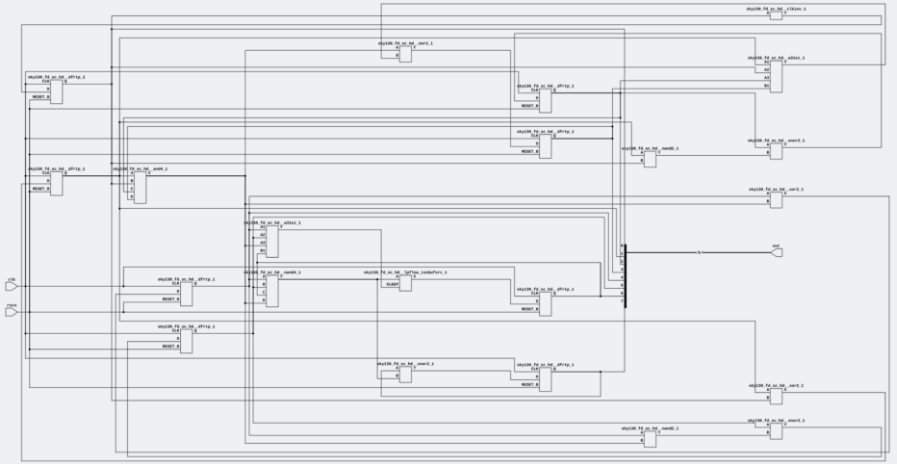
The first step to start the realization of a chip is the logic synthesis and optimization.

The HDL is parsed and converted to an intermediate representation.

The intermediate representation is then mapped to the tech library.

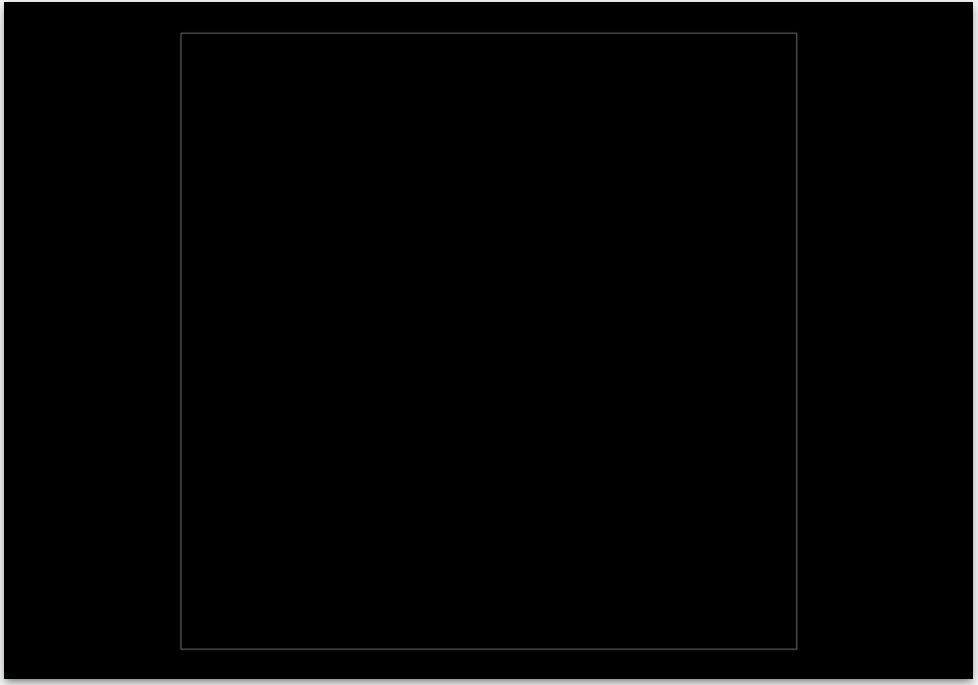






Floorplanning

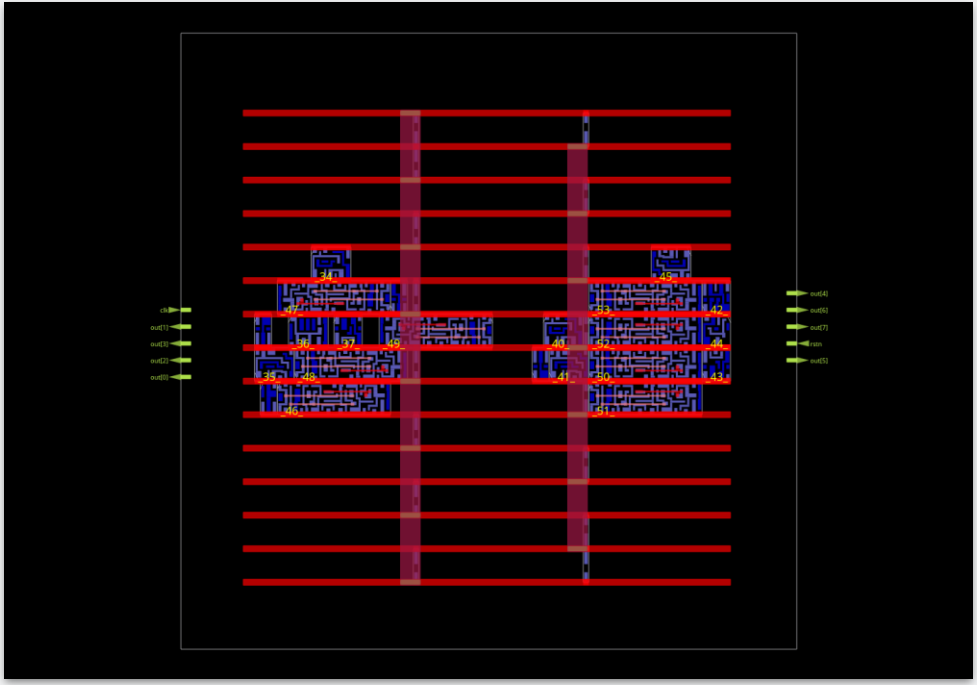
Floorplanning defines the area of IC and where the submodules of the design should be placed.



No explicit floorplanning in the example!

Placement

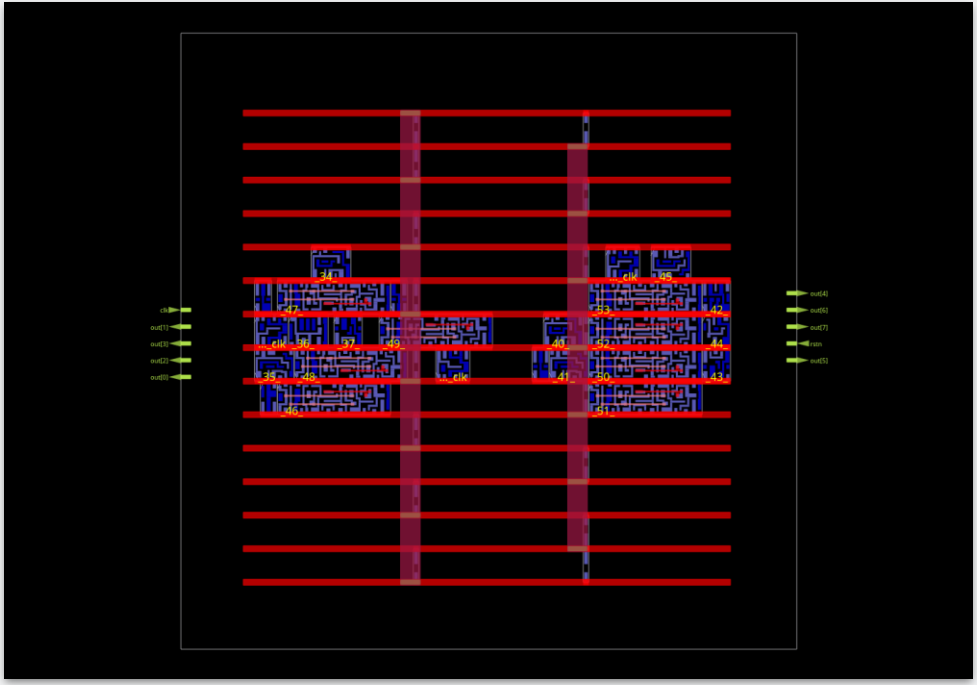
In this step the power grid is defined and the standard cells selected by the synthesizer are placed on the die.



Some of them are overlapping, are too far or too close.

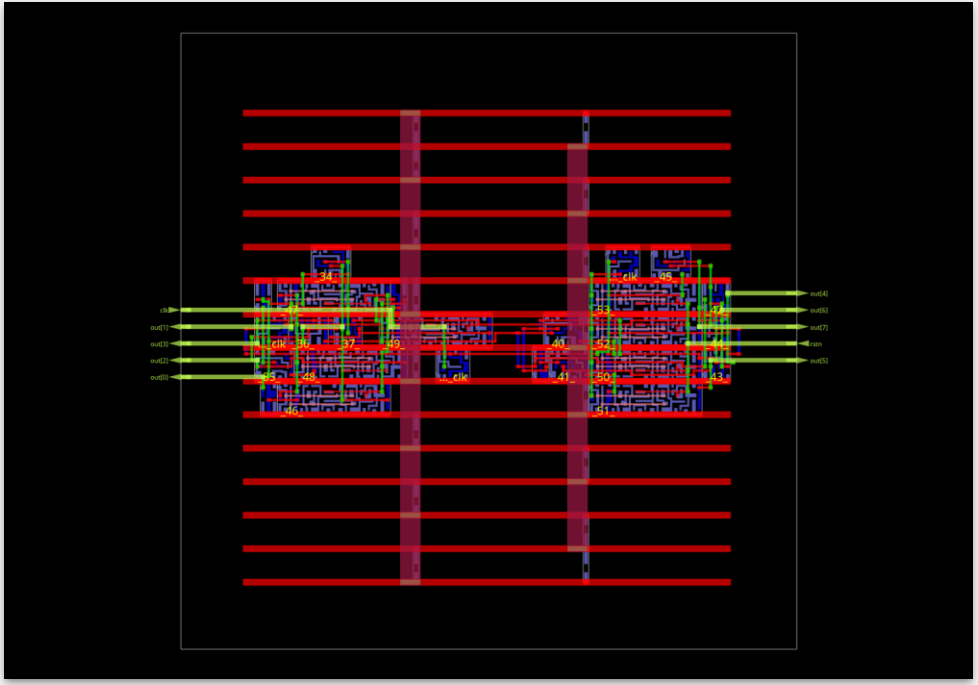
Clock tree synthesis

Clock is identified in the circuit and metal lines for the distribution of this signal are defined.



Routing

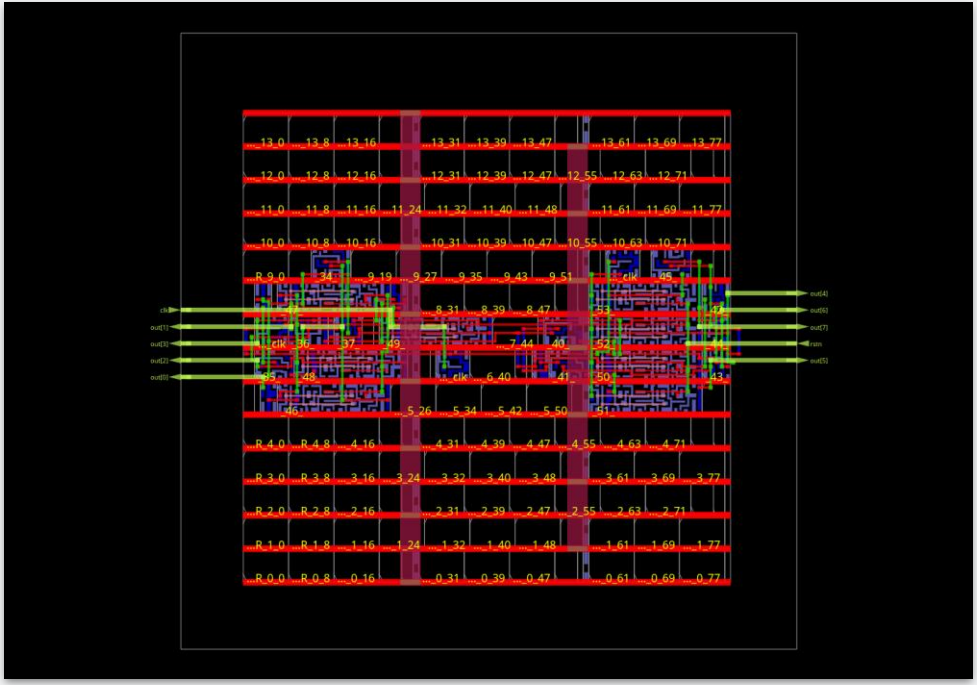
The metal lines to connect the input and the output of the standard cells are placed.



Signoff

To complete the design, filler cells are added and DRC are checked to be sure that the design is valid and ready for production.

After 6 to 8 months, the IC is shipped and ready to be used in your projects.



THANK YOU FOR YOUR ATTENTION!

ANY QUESTION? FEEL FREE TO ASK!

TIME TO EXPERIMENT!

OPEN THE LAB PDF AND FOLLOW THE GUIDE TO TRY IT ON YOUR OWN!