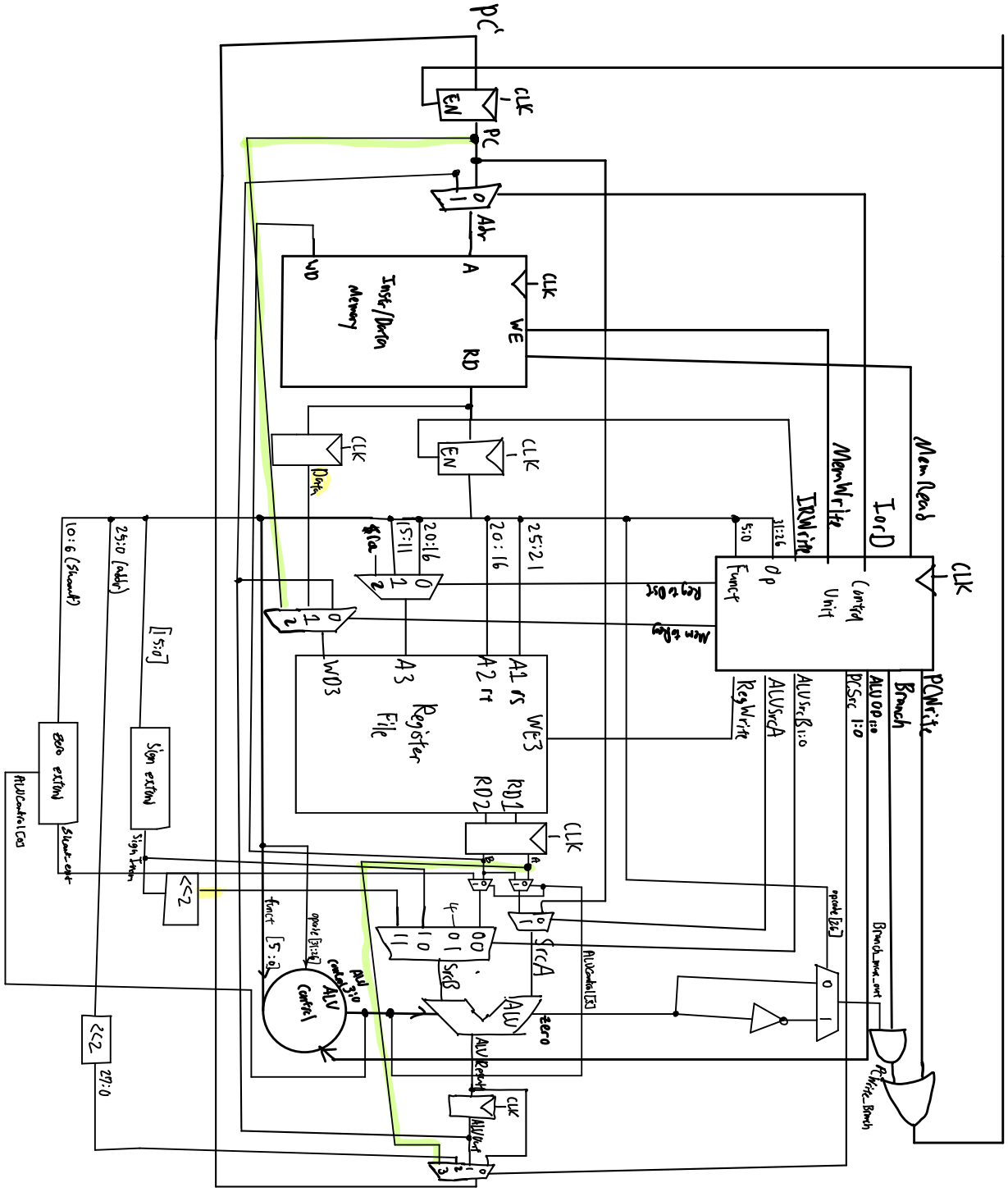
Note: All enables depend also (and) on CLK_en.

Also, the 3 to 1 muxes will be implemented with 4 to 1 muxes where the 4th input will be all zeroes and the select inputs will never be equal 3.



Note: All the control_unit outputs that aren't specified are zeroes since they should be either zeroes or don't cares (so we set them as zeroes).