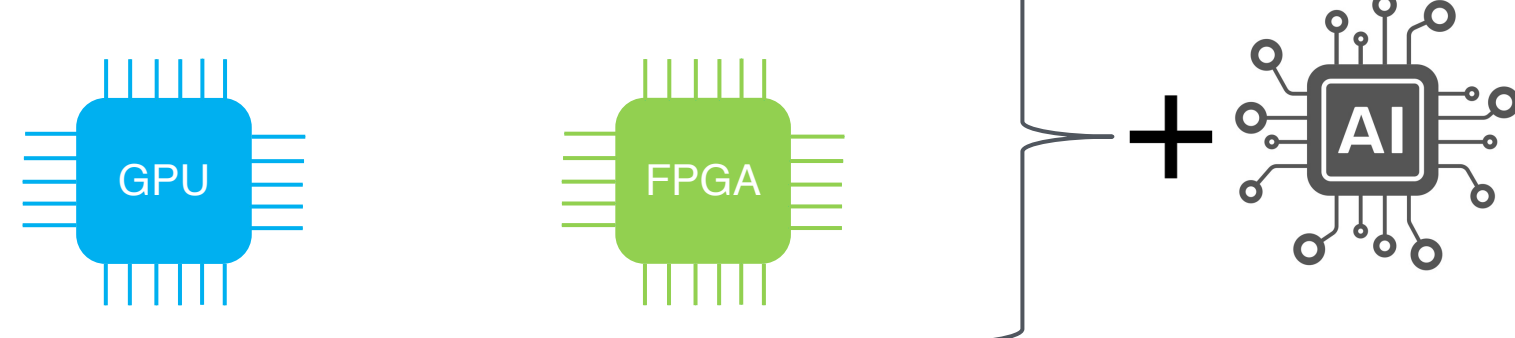


# Identification of Assembly's Patterns for Hardware Acceleration

## Introduction

In today's world, technological applications require more and more computational power to run. CPU speed increase has seen a decline over the past four years, leaving room for ideas to accommodate the increasing need for fast processing power:

### Co-processor configuration



## Aim & Motivation

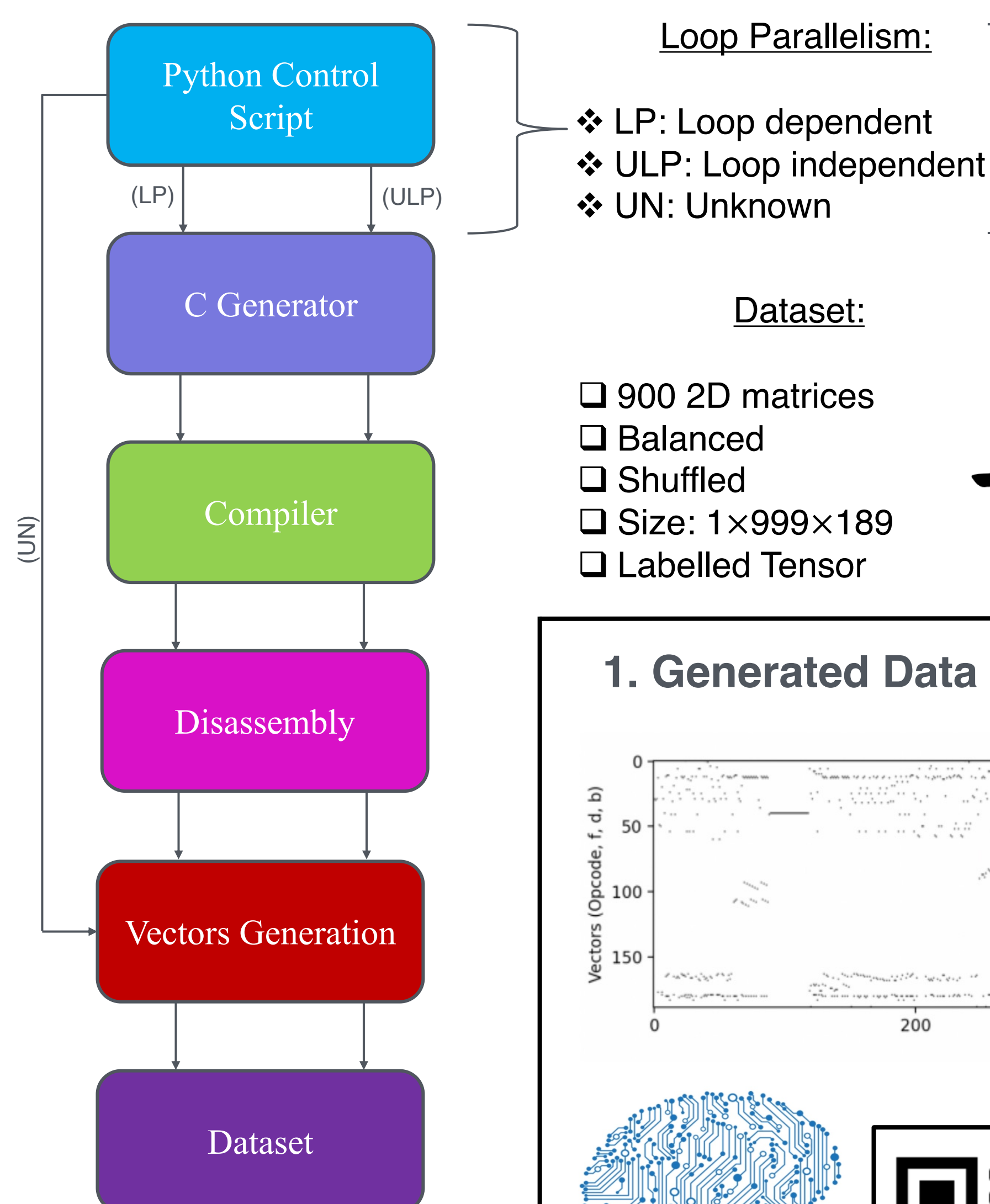
- Discover potential accelerate candidates that can be then used for hardware acceleration
- Explore an analysis technique to analyse assembly machine code.



Automatic Hardware Acceleration using an FPGA co-processor configuration.

## Methods

### 1. Data Generation System



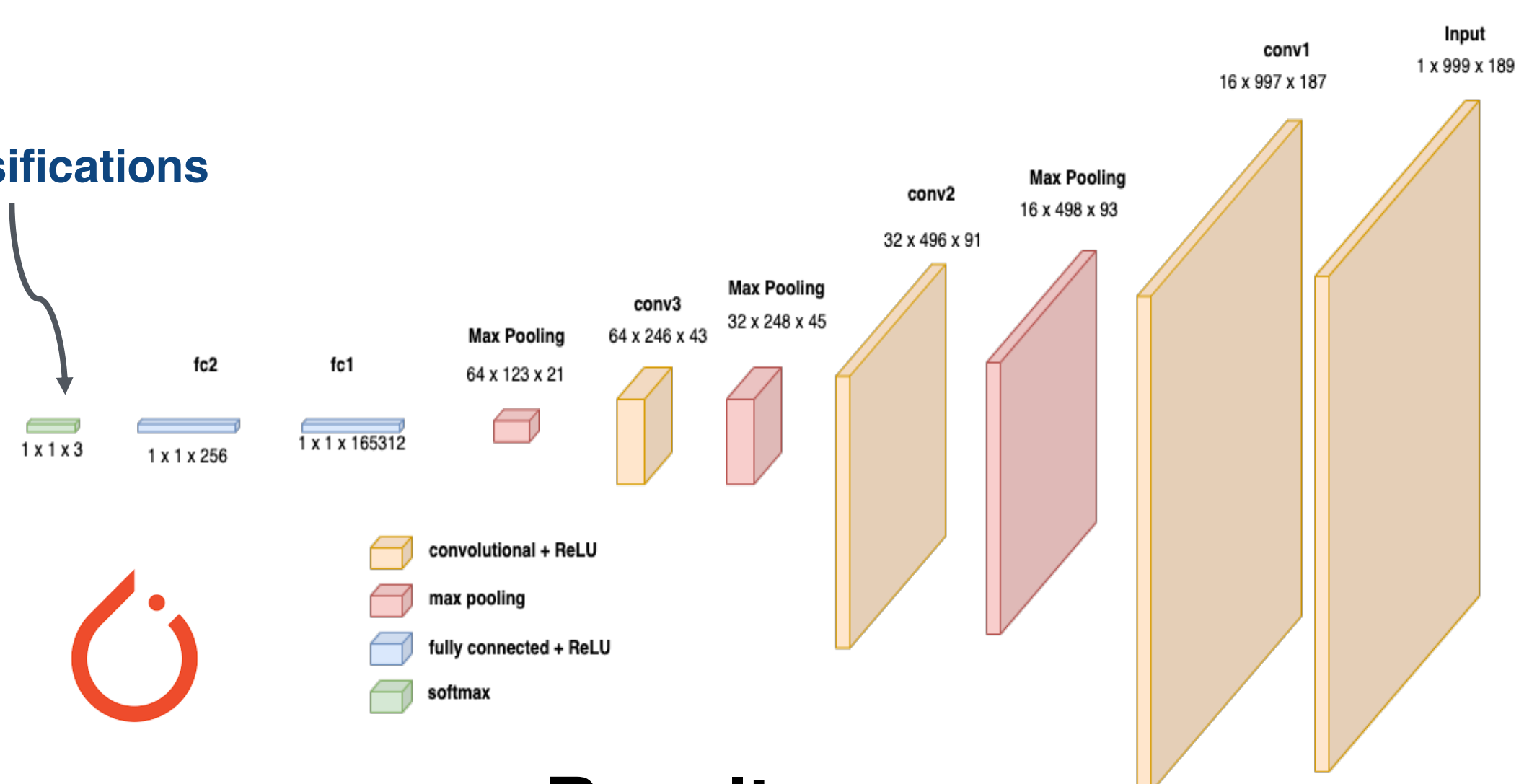
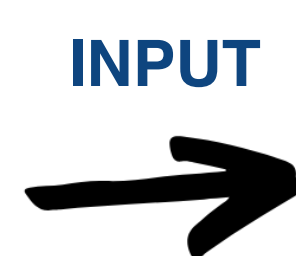
### Loop Parallelism:

- ❖ LP: Loop dependent
- ❖ ULP: Loop independent
- ❖ UN: Unknown

### Dataset:

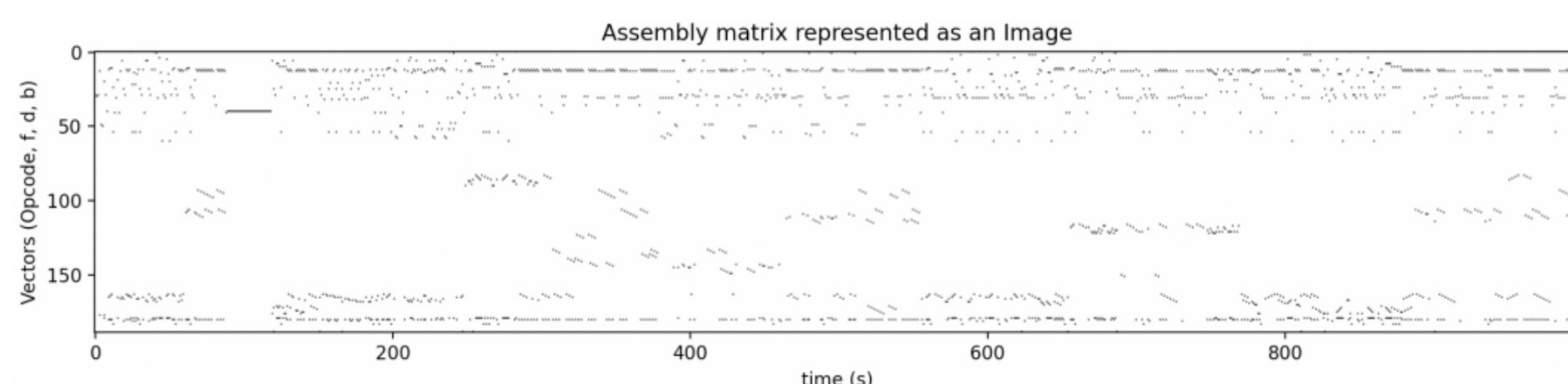
- ❑ 900 2D matrices
- ❑ Balanced
- ❑ Shuffled
- ❑ Size: 1×999×189
- ❑ Labelled Tensor

### Classifications

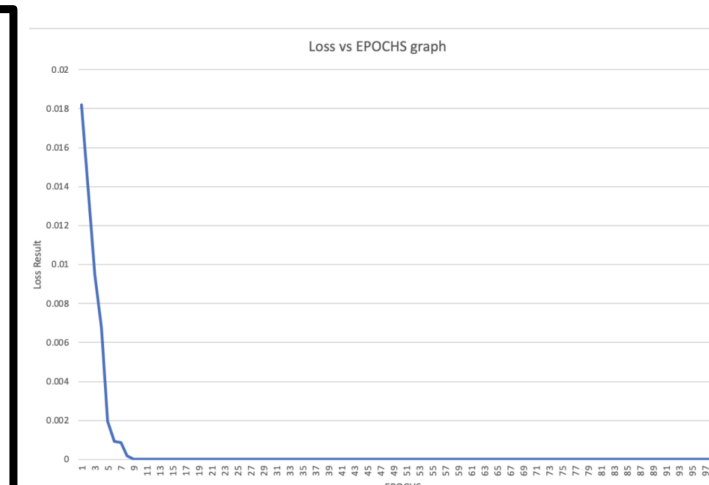


## Results

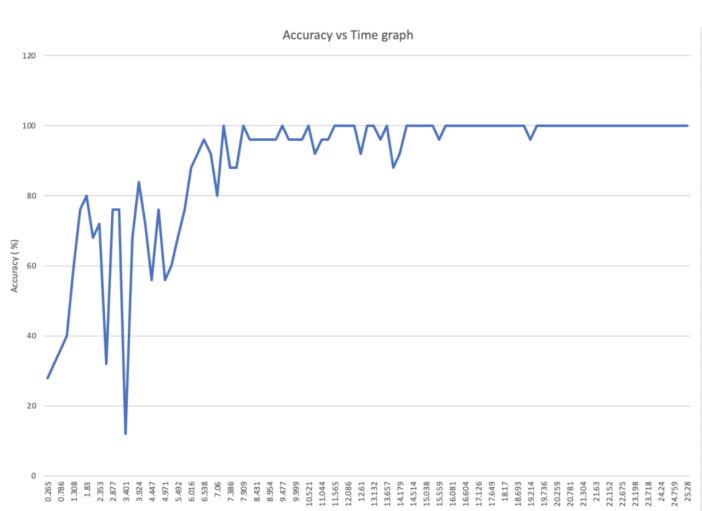
### 1. Generated Data Example:



### 2. Supervised Learning Result:



- ✓ Accuracy: 100%
- ✓ Epochs: 9
- ✓ Batch size: 10
- ✓ MSE Loss Function
- ✓ Adam optimizer



Graphical representation of a loop dependent assembly machine code. Each Vector is derived from the instruction's **opcode** and **operands** using a **one-hot encoder**.

In testing heavy applications like **convolution** and **sigmoid**, the model predicted a **UN** label or unknown pattern.

**Overfitting:**  
Lack of generalisations to new data

## Conclusion

CNN training with **high accuracy**

Lack of generalisations to new data

Data Generation system capable of producing labelled datasets

A **promising** area of research, but the need for more work and data.

### Future Work

- **Data augmentation:** task parallelism
- **“Early stopping”** algorithm
- **Analysis** of compilers

## References

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