DEBRE BERHAN UNIVERSITY
COLLAGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COMPUTER STREAM

[0.75cm] Course Name: VLSI Design

Course Code: ECEg 4201

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VLSI individual assignment

Quotation and Answers

1 What is signal validity?

Signal validity is the process of making sure that the input signal is appropriate for the purpose we need it for.

2 Compare and contrast IOT and Embedded system

well, frist let us define what these two things meant

embedded system is a computer with a dedicated function. It is placed within a larger mechanical or electrical system and often performs pre-defined tasks with very specific requirements.

where as an **IOT** is an integration that can have many connectivity options and devices; however, IoT has nothing to do with technical specifications.

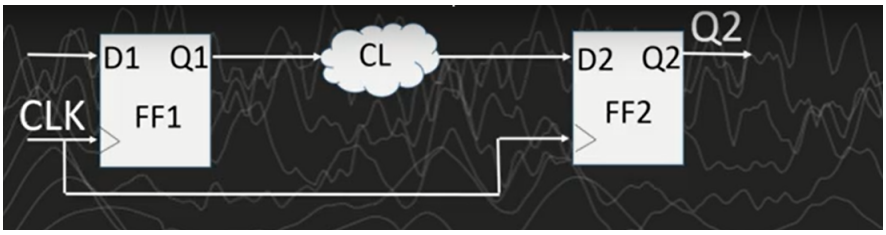
IoT vs Embedded system

IOT	Embedded System
IoT is a network of objects that are connected to the internet	Embedded systems are a combination of customized hardware and software that performs one specific task.
Can be updated using network capabilities	Have a dedicated function that cannot be updated once programmed
IoT has access to the internet and cloud resources, big data and so much more, making it more complex than Embedded systems.	Embedded systems are limited in terms of resources

Embedded system and IoT – how they complement each other

With the growing popularity of IoT, the tasks that can be achieved using embedded systems have become limitless. IoT has created the possibility of using embedded systems however we want and whenever we want. But, how do these two work together? Let's look at some common examples.

3 $tcdregister + tcdlogic \geq thold$ why?



at first both the flip flops are going to pass there input value to the output and we know all the flip flops are have hold time requirement which means that,

Input to the flip flop must be stable of the positive edge of the clock for some minimum time called **Hold time** so its functionalists would be as expected.
when we come to the hold time requirement of flip flop 2,

at its positive edge, when it just started passing its input value D2 to Q2, at the same time flip flop 1 start passing its input value D1 to Q1. which takes equal time as Tcq to give its output to computational logic. and combination logic will take time equal to Tcl to give its output to the input of flip flop 2.

So now in this case, if Tcq + Tcl is less than the hold time requirement, the Hold time requirement of flip flop 2, than its clearly the violating the hold time constraint.

so for our design to work with out hold time violations, Hold time requirement of a capturing flip flop must be less than or equal o the sum of propagation delay of the flip flop and combination logic delay between the two flip flops.

$$tcdregister + tcdlogic \geq thold$$

Hold time violations are independent of clock frequency. they depend on path architectures and corresponding delays in the path.

4 Discus the types of capacitance in a typical MOS device or transistor

So when we discuses about the capacitance in in typical MOS devices we mainly talk about 2 capacitance they are Parasitic capacitance and Internal capacitance.
but in this explanation i will talk about the internal capacitance.

so What are internal capacitance?

internal capacitance are nothing but the wired capacitance within two different MOSFETs when the connections are made.

there are two types of internal capacitance named as The Gate capacitance and The junction capacitance.

the Gate capacitance: is obtained because the gate electrode forms a a parallel plate capacitor with the channel and the oxide layer serving as a capacitor dielectric.

Gate capacitor depends on the capacitor region which are the Triode region, the saturation region and the cutoff region.

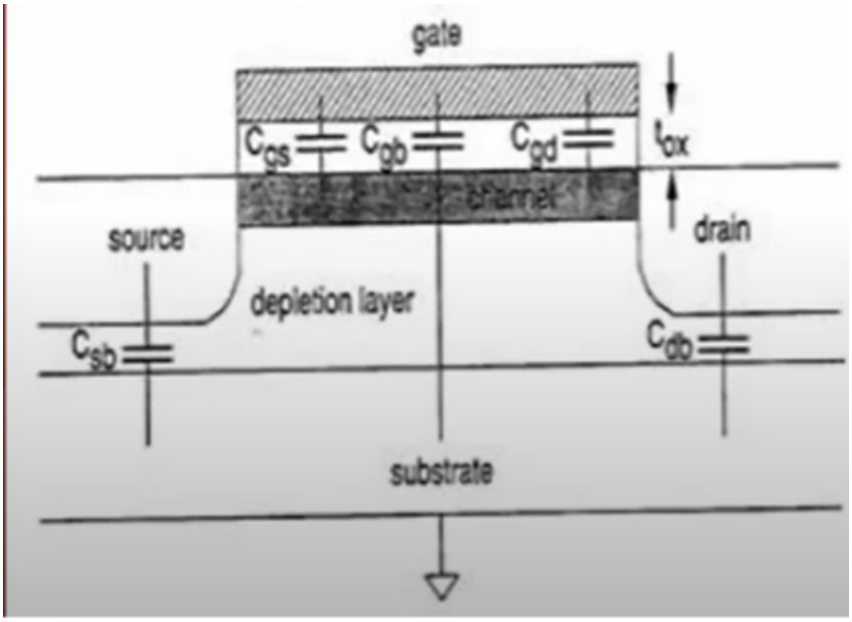


Figure 1: image B

the Junction capacitance: is also called the source body and drain body depletion layer capacitance.

junction capacitance are capacitance of the reviser biased PN junction which are formed by the source region and the p-Substrate, which is called as the source diffusion and also between the positive drain region and the substrate, which is called as the drain diffusion.

So Both the internal capacitance can be modeled by including the capacitance in the MOSFET model between it four terminals which are the gate,drain,source and the substrate.

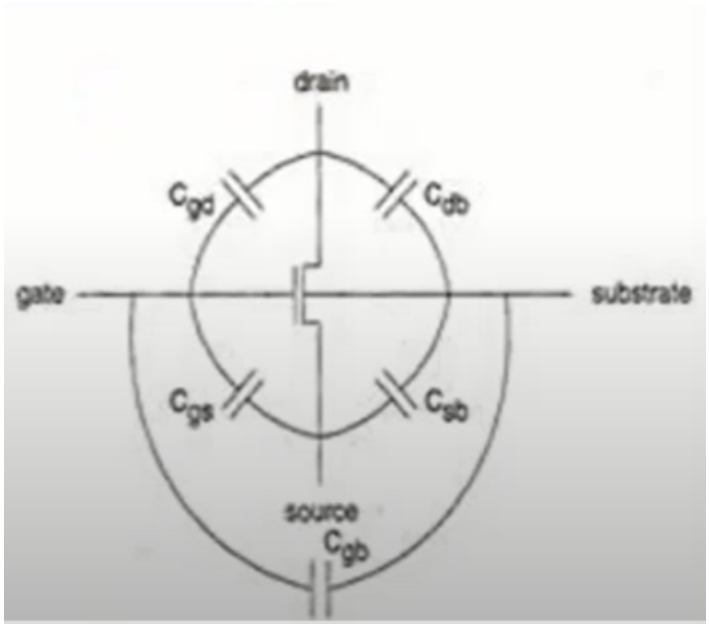


Figure 2: image B

We have 5 interconnection capacitance's in total which are Cgs, Cgb, Cgd which belongs to gate capacitance, and Csb an Cdb, which belongs to Junction capacitance.