In the TB module, we aim to test our code in different states and cases.
We start by declaring our input variables as reg type because they will be subject to modifications within the initial procedural block. We also mention the integer that is used for upcoming for loop.
Having called an instance of the module we are testing as well as necessary commands for the testbench to run, we start by setting SB, NB, clk = 0 and reset =1 to test them. Then, after 10 time units, we toggle them to de-assert reset and assert other signals and start with different tests.
We use a for loop to iterate within 37.5 lock cycles within which we go through all possible combinations of the signals.
The Verilog code works perfectly and is stable.