Elias Kountouris

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Experience

Microchip Technology - FPGA Engineering Intern January 2023 - August 2023

- Researched impacts on performance of high global routing usage for new FPGA fabrics
- Developed **python** and **bash** scripts to generate **structural verilog** designs to validate new hardware
- Expanded proprietary simulation tools to preform automatic verification of generated verilog designs
- Resolved issues during test verification of new SoCs to help team meet tapeout deadline

Level Home - Electrical Engineering Intern May 2022 - August 2022

- Researched range detection with **UWB** using multiple antennas through different materials
- Designed a PCB to evaluate serial cable signal integrity to reduce debug and development time
- Resolved critical issues in product resulting in a lower quiescent current and better battery life
- Designed dev-boards with **nRF52840 SoC** to drive **BLE** antennas and battery monitors
- Co-operated with overseas manufacturers to analyze EVT stage data to increase product yield

Zappos - Software Engineering Intern May 2020 - August 2020

- Utilized **PyTorch** for sentiment analysis to analyze product reviews to improve recommendations
- Implemented web scrappers to gather data for sentiment analysis algorithms

Waterloo Rocketry - Electrical Team Member, Former Lead September 2021 - Present

- Managed and led team to develop **18 custom PCBs** for a single-stage hybrid rocket
- Designed sensor boards which used **CAN bus**, **I2C** and **SPI** to gather telemetry data
- Created 250W power system with polarity protection for ground side control

Projects

PLA Based ALU - Verilog, C++, Verilator, Python, Vivado

- Designed RISC ISA that used programmable logic to implement infrequently used instructions
- Created **python** scripts to synthesize config bits from high level description
- Used **C++** and **verilator** for testing simulations to verify PLA fabric and interface
- Currently working on implementing the ALU into a pipelined CPU

Simple CPU - Verilog, Vivado

- Designed a small ISA inspired by **RISC-V** to create an 8-bit Harvard CPU
- Created custom ALU, memory, register file, and control path modules to implement the ISA
- Used verilog testbenches to verify ALU and control path functionality

Smart Floor Vent - KiCad, LTspice, C

- Smart floor vent that can open and close based on room temperature
- Designed controller PCB to interface with sensors, control servos, and enable fan motors
- Created secondary PCB to add polarity protection and battery life monitoring

Education

University of Waterloo 2021 - 2026

Candidate for Bachelor of Applied Science in Electrical Engineering GPA: 3.97

Technical Skills

RISC-V, Verilog, SystemVerilog, C++, C, Python, Bash, Vivado, Verilator, OrCAD, Allegro, Altium, KiCad