EE 130 Integrated Circuit Devices

Elias Lehman

GSI: Adi Jung

Instructor: Prof. Sayeef Salahuddin

Spring 2023

Abstract

This project describes an introductory approach to MOSFET optimization using the Synopsys Sentaurus simulation program. We were given an n-channel silicon MOSFET with gate length $L_G = 25$ nm (relevant for the "20 nm generation" of CMOS technology) with the following constraints:

- Gate length $L_G = 25$ nm
- Effective oxide thickness $T_{oxe} = 0.9$ nm
- Gate work function = 4.5 eV (corresponding to titanium-nitride)
- Deep source/drain regions:
  - Dopant concentration vs. depth profile is Gaussian
  - Peak dopant concentration = 2×10^{20} cm^{-3}
  - Junction depth (defined as the distance from the Si surface to the depth where the deep source/drain dopant concentration is equal to the body dopant concentration) = 25 nm
- Source/drain extension regions:
  - Dopant concentration vs. depth profile is Gaussian
  - Peak dopant concentration = 9×10^{19} cm^{-3}
- $I_{OFF} \leq 1$ nA per micron channel width.
- $I_{ON} \geq 400\mu$A per micron channel width. The power supply voltage VDD = 0.8V. The body bias voltage VB = 0 V.

1 Experiments

1.1 Controls

To experiment with how certain variables will affect the performance of our MOSFET, in addition to checking that the simulated device is operational, we varied the following parameters and measured the results:

- 5×10^{17} cm$^{-3} \leq N_A \leq 4 \times 10^{18}$ cm^{-3}
- 10 nm $\leq L_{SP} \leq$ 35 nm
- 4 nm $\leq X_J \leq$ 20 nm

1.1.1 Channel Doping

As we increase the channel doping, we expect the threshold voltage to decrease, but carrier mobility to decrease as well. The question that arises, is how will this variable ultimately affect our operation values I_{ON} and I_{OFF}? We held spacer length, $L_{SP} = 20$ nm, and source/drain height, $X_J = 13$ nm, constant while fluctuating carrier concentration in the channel/body.

Our measurement gave the following result:

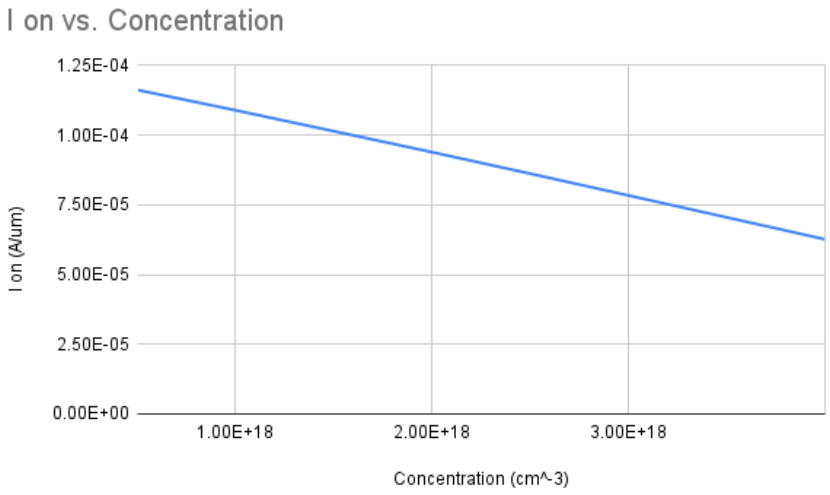

Figure 1: Graph visualizing the change in I_{ON} as a function of channel doping.

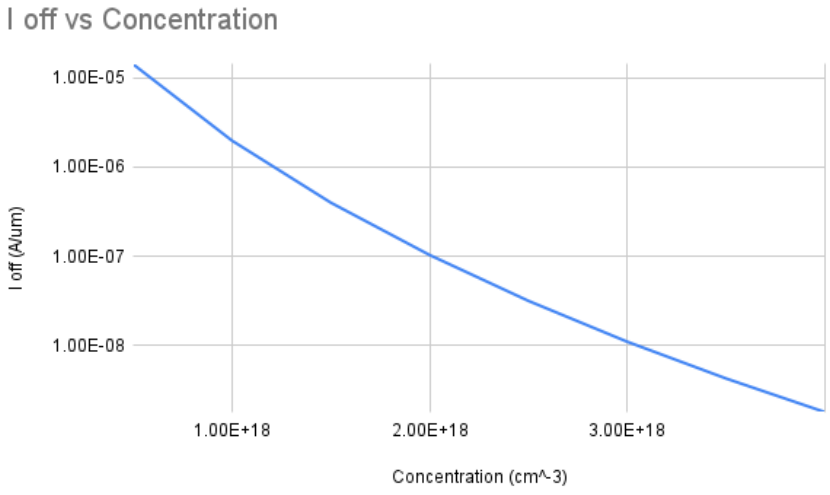

Figure 2: Graph visualizing the change in I_{OFF} as a function of channel doping.

1.1.2 Space Width

The spacers line the sidewalls of the gate and serve as a mask during ion implantation of the deep n+ drain and source regions. Increasing the spaces, increases channel length, but decrease parasitic capacitance between the drain and source. We held carrier concentration, $N_A = 10^{16}$ /cm, and source/drain height, $X_J = 13$ nm, constant while fluctuating spacer length.

Our measurement gave the following result:

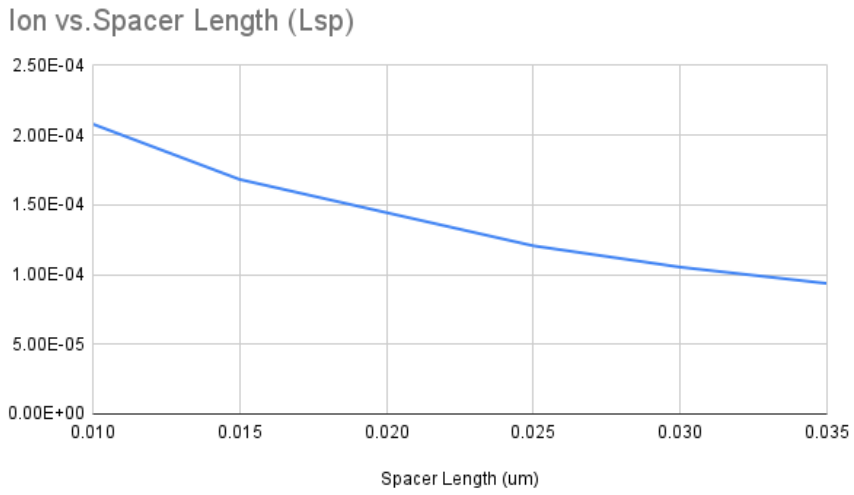

Figure 3: Graph visualizing the change in I_{ON} as a function of spacer length.

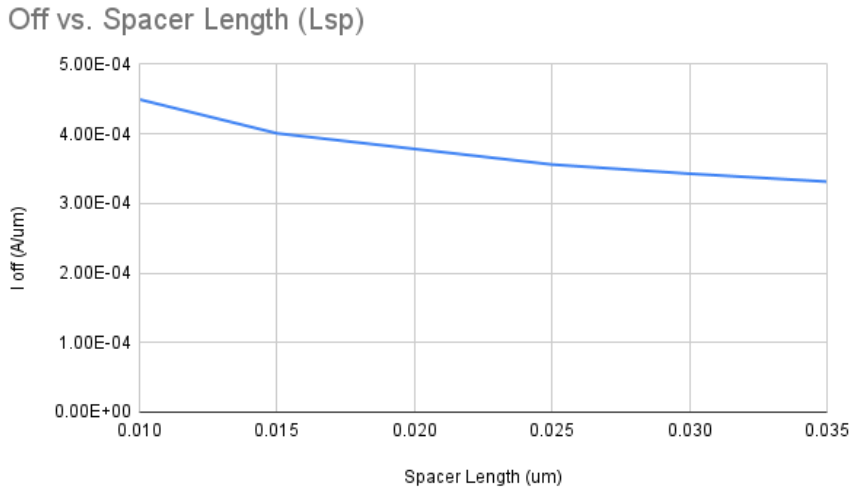

Figure 4: Graph visualizing the change in I_{OFF} as a function of spacer length.

1.1.3 Source and Drain Depth

Parasitic capacitance occurs across the channel, between the source and the drain. This capacitance depends on the height of these regions, which gives the area of the capacitive 'plates.' We held carrier concentration, $N_A = 10^{16}$ /cm, and spacer length, $L_{SP} = 20$ nm, constant while fluctuating the drain depth.

Our measurement gave the following result:

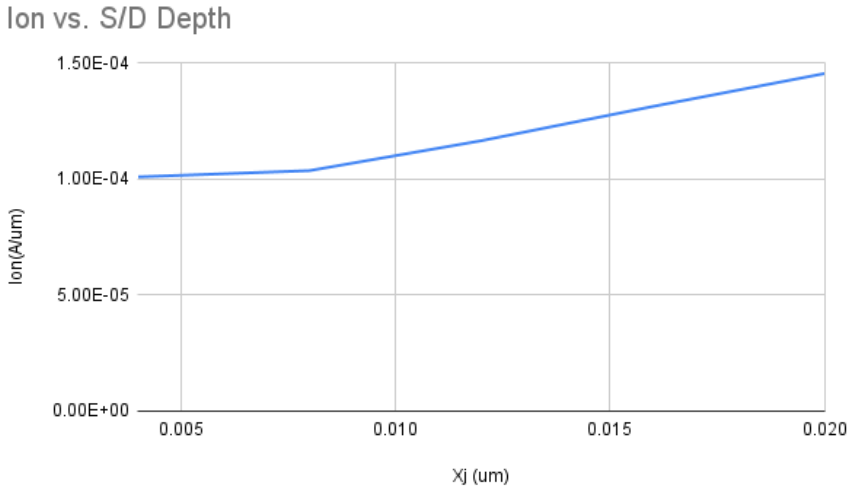

Figure 5: Graph visualizing the change in I_{ON} as a function of S/D depth.

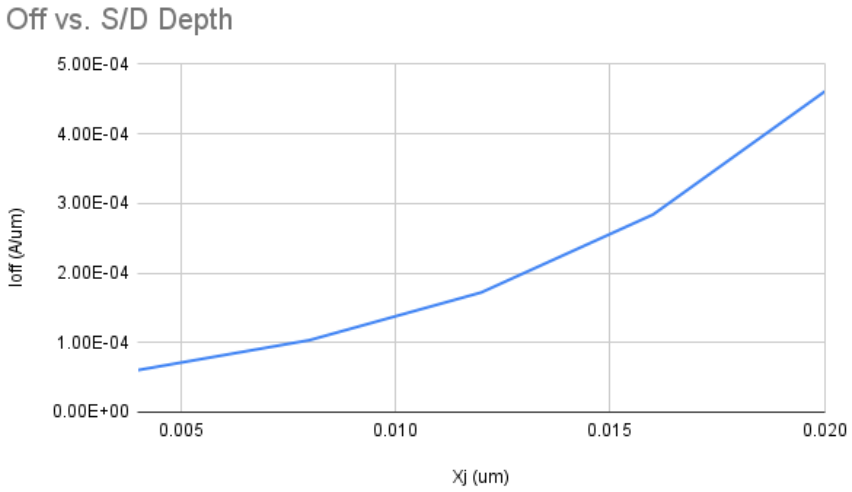

Figure 6: Graph visualizing the change in I_{OFF} as a function of S/D depth.

1.2 Measurements and Calculations

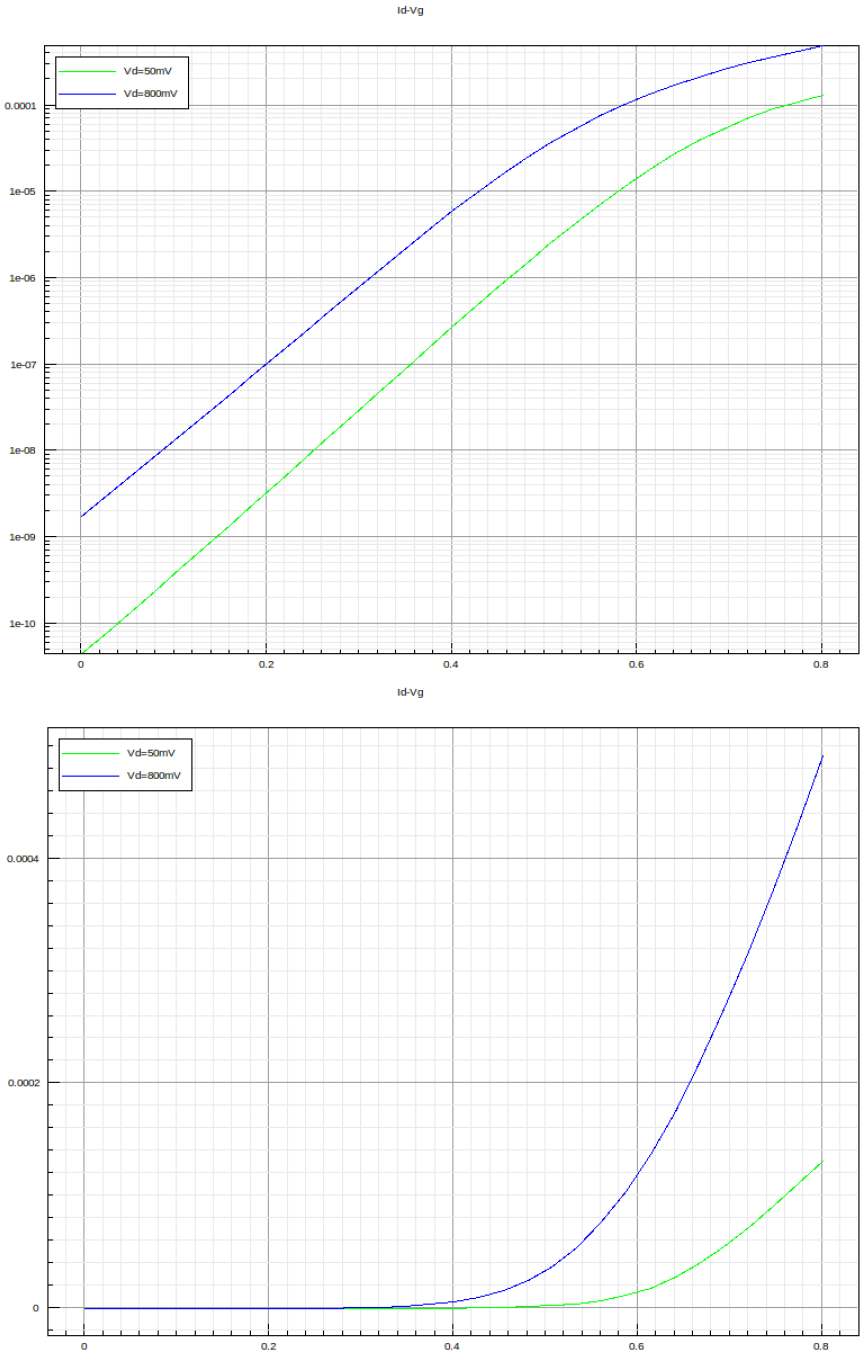

Figure 7: Id [A/um] (y-axis) versus Vg [V] (x-axis) curve for two different Vd values in log scale (top) and linear scale (bottom).

1.2.1 Subthreshold Swing

From the simulated Id-Vg plot, we can extract the minimum subthreshold swing:

$$\begin{aligned} SS &= (\frac{\partial \log(I_{DS})}{\partial V_{GS}})^{-1} \\ &= \frac{1}{1\ dec/0.1\ V} \\ &= 0.1\ V/dec \\ &= \boxed{100\ mV/dec} \end{aligned}$$

1.2.2 Saturation

We know $V_{DS} = V_G = 0.8\ V$ implying the device is in saturation mode, $V_{DS} > V_G - V_T$. When in saturation mode, the current steadily plateaus, and combined with the reasonable size of this MOSFET, leads us to conclude that velocity saturation is the primarily mechanism by which current implying the NMOS is working in **pinch-off regime**.

1.2.3 Threshold Voltage

If we define the ON current to be 300nA/μm, and we set the drain voltage to V_{dd}, we can measure the threshold voltage to be $\boxed{V_t = 0.03\ V}$.

1.2.4 Peak Transductance and Early Voltage

The peak transductance for this MOSFET is measured by

$$gm = \frac{\partial I_{DS}}{\partial V_{GS}} = 0.02\ s = \boxed{20\ ms} \tag{1}$$

Similarly, the early voltage can be found by

$$V = \frac{\partial I_{DS}}{\partial V_{DS}} = \square \tag{2}$$

1.2.5 Oxide Thickness

We changed the EOT to 30A, and measured the Id-Vg curve.

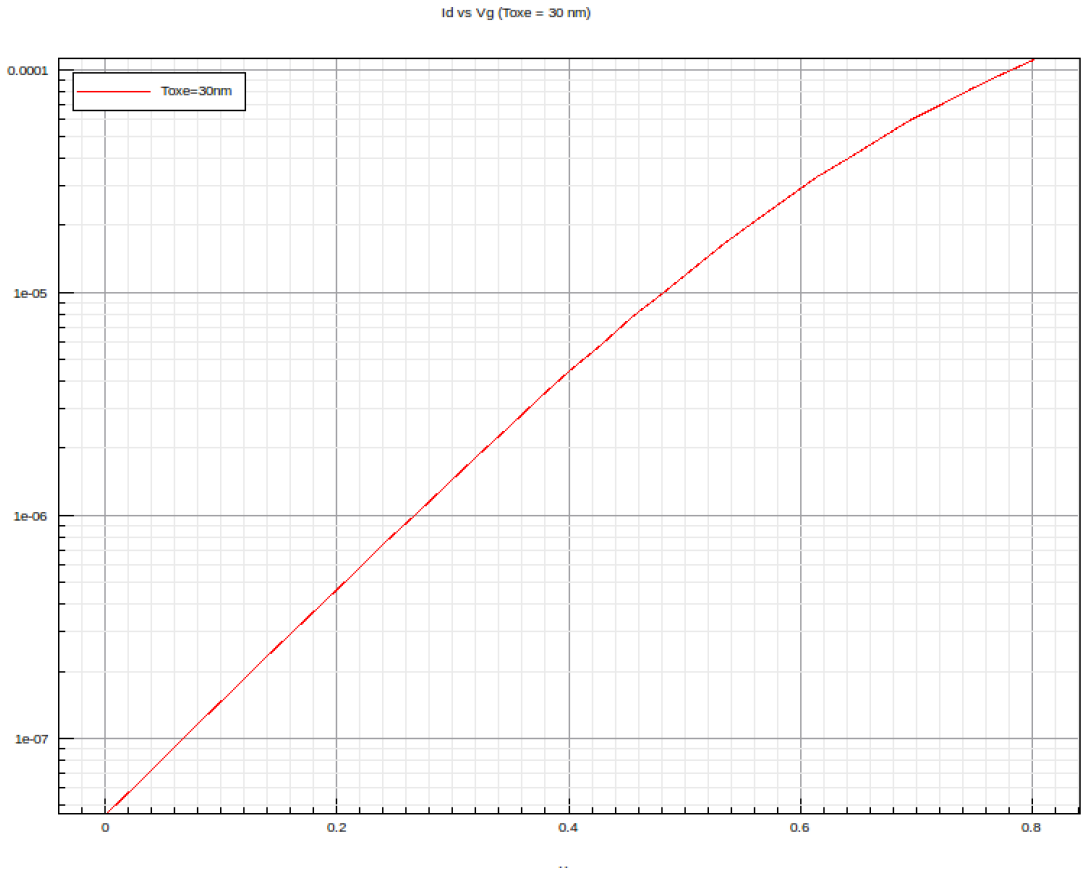

Figure 8: Id vs Vg for 30A effective oxide thickness. Note the voltage is roughly 10 times higher for all V_g.

As we increased EOT, the capacitance decreases so γ increases

$$\gamma = \frac{1}{C_{ox}}\sqrt{2\varepsilon_{si} q N_A} \tag{3}$$

. Therefore, V_T should be less

$$V_T = V_{FB} + 2|\phi_p| + \gamma\sqrt{2|\phi_p|}, \tag{4}$$

Or equivalently, the plot shifts to the left, as we see in Figure (8).

1.2.6 Further Modifications and Trade offs

Say we wanted to increase V_t by 100meV, but only at the cost of 20 percent ON current, I_{DS} for $V_{GS} = V_{DS} = V_{DD}$. Note that the MOSFET device is in the triode region, $V_{DS} <$

$V_{GS} - V_T$, so the current can be modeled as

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \tag{5}$$

or

$$I_{ON} = \frac{W}{L}\mu_n C_{ox}(\frac{V_{DD}^2}{2} - V_T \times V_{DD}) \tag{6}$$

where

$$V_T = V_{FB} + 2|\phi_p| + \gamma\sqrt{2|\phi_p|}, \tag{7}$$

$$\phi_p = -\frac{kT}{q}\ln(\frac{N_A}{n_i}) \tag{8}$$

$$V_{FB} = (\phi_m - (\chi + kT\ln(\frac{N_A}{n_i}) + \frac{E_g}{2}))/q \tag{9}$$

$$\gamma = \frac{1}{C_{ox}}\sqrt{2\varepsilon_{si}qN_A} \tag{10}$$

If we want to increase the threshold voltage while conserving current, we should decrease the oxide capacitance C_{ox} by **increasing the effective oxide thickness by 15 percent**. This would reduce I_{ON} by a controllable and minute amount, while increasing γ by 20 percent, which offers 100mV if $\gamma\sqrt{2|\phi_p|} \geq 500mV$.